Third Party Submission for Application USSN 14/259,011

Document 1

Patent No.:	US Patent 8,238,116
Inventor:	Eggerding et al.
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Concise Description:

Document 1 was published as an application and as a patent prior to the earliest possible priority date of June 14, 2013 for the subject Application USSN 14/259,011.

The subject Application USSN 14/259,011 is entitled "Multilayer Ceramic Capacitor and Board Having the Same Mounted Thereon." It relates in pertinent part to a particular capacitor arrangement which results in a reverse geometry capacitor having relatively low inductance.

Fig. 4 of subject application USSN 14/259,011 is exemplary (reproduced below):

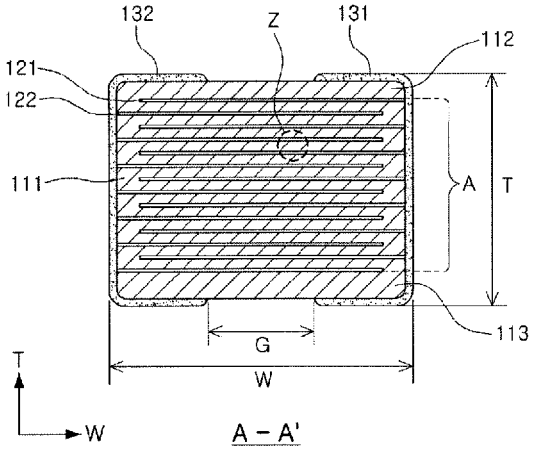


FIG. 4

Exhibit 2001
PGR2017-00010
SEM

Examples from the specification of the subject Application USSN 14/259,011 regarding such reverse geometry feature arrangement and resulting relatively low inductance are recited below re application Paragraphs [0050], and [0056] through [0061] (emphasis added):

> [0050] Referring to FIG. 1, in the multilayer ceramic capacitor according to an exemplary embodiment of the present disclosure, a 'length direction' refers to an 'L' direction, a 'width direction' refers to a 'W' direction, and a 'thickness direction' refers to a 'T' direction. Here, the 'thickness direction' may be the same as a stacking direction in which dielectric layers are stacked.
>
> ...
>
> [0056] The first and second internal electrodes 121 and 122 may be disposed to face each other, having at least one of the dielectric layers 111 interposed therebetween, and may be alternately exposed to the first or second side surface S5 or S6.
>
> [0057] The first and second internal electrodes 121 and 122 are alternately exposed to the first or second side surface S5 or S6, such that **a reverse geometry capacitor (RGC) or low inductance chip capacitor (LICC) may be obtained** as described below.
>
> [0058] In a general multilayer ceramic electronic component, external electrodes may be disposed on opposing end surfaces of the ceramic body in a length direction thereof.
>
> [0059] In this case, when an alternative current (AC) voltage is applied to the external electrodes, a current path is relatively long, whereby an intensity of an induced magnetic field may be increased, resulting in an increase in inductance.
>
> [0060] **In order to solve this problem**, the first and second external electrodes 131 and 132 in the exemplary embodiment of the present disclosure may be disposed on the first and second side surfaces S5 and S6 of the ceramic body 110 opposing each other in the width direction **so as to reduce the current path**.

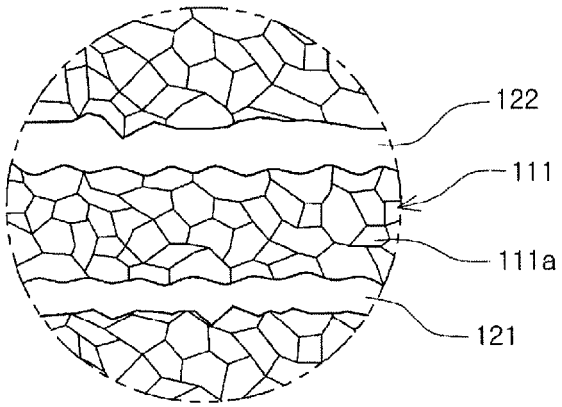
[0061] In this case, **since a distance between the first and second external electrodes 131 and 132 is relatively short, the current path may be reduced, ... resulting in a reduction in inductance**.

Further exemplary information from the specification of the subject Application USSN 14/259,011 relates to dielectric grain subject matter, as recited below re application Paragraphs [0087] and [0088] (emphasis added):

[0087] FIG. 5 is an enlarged view of part Z of FIG. 4.

[0088] Referring to FIG. 5, the average number of dielectric grains 111a present in a single dielectric layer 111 in a thickness direction thereof may be 2 or greater.

Such Fig.5 of the USSN 14/259,011 is reproduced below:



Z

FIG. 5

Claim 1 of the subject Application USSN 14/259,011 relates to multilayered ceramic capacitor subject matter, and recites in pertinent part (bracketed comments added):

1. A multilayer ceramic capacitor, comprising:
a ceramic body [110] including dielectric layers [111] and having first and second main surfaces [S1, S2] opposing each other, first and second

side surfaces [S5, S6] opposing each other, and first and second end surfaces [S3, S4] opposing each other;

an active layer including a plurality of first and second internal electrodes [121, 122] disposed to face each other with at least one of the dielectric layers interposed therebetween and alternately exposed to the first or second side surface;

upper and lower cover layers [112, 113] disposed on and below the active layer, respectively; and

a first external electrode [131] disposed on the first side surface [S3] of the ceramic body and electrically connected to the first internal electrodes [121] and a second external electrode [132] disposed on the second side surface [S4] and electrically connected to the second internal electrodes [122],

wherein when a thickness of the ceramic body is defined as T and a width thereof is defined as W, 0.75W.ltoreq.T.ltoreq.1.25W is satisfied,

when a gap between the first and second external electrodes is defined as G, 30 .mu.m.ltoreq.G.ltoreq.0.9W is satisfied {Fig. 4], and

an average number of dielectric grains in a single dielectric layer in a thickness direction thereof is 2 or greater [Fig. 5].

Independent claim 8 relates to a printed circuit board having at least two electrode pads, and such a multilayer ceramic capacitor mounted and soldered thereon.

Document 1 (D1) is entitled "Land Grid Feedthrough Low ESL Technology," and discloses subject matter pertinent to the subject Application USSN 14/259,011. See, for example, D1, Fig. 4a reproduced below and showing a reverse geometry multi-layer capacitor 400 mounted via traces 442 and 444 on printed circuit board 420:

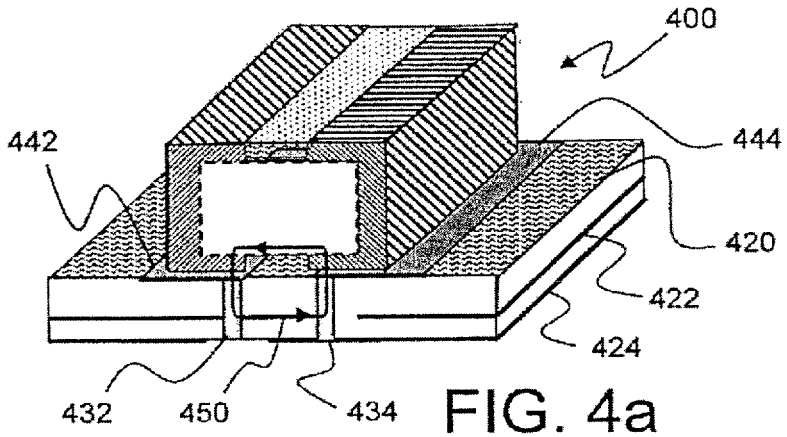


FIG. 4a

Further, the D1 specification refers to reducing inductance in the context of both reverse geometry capacitors and low aspect ratio (length to width ratio). Both such features are pertinent to the subject Application USSN 14/259,011. See, for example, D1, specification Col. 1, lines 33-67 (emphasis added):

> There may be several strategies for reducing equivalent series inductance, or ESL, of chip capacitors compared to standard multilayer chip capacitors. … **A first exemplary strategy for reducing ESL involves reverse geometry termination, such as employed in low inductance chip capacitor (LICC) designs**. In such LICCs, **electrodes are terminated on the long side of a chip instead of the short side. Since the total inductance of a chip capacitor is determined in part by its length to width ratio, LICC reverse geometry termination results in a reduction in inductance** by as much as a factor of six from conventional MLC chips.
>
> Interdigitated capacitors (IDCs) incorporate another strategy for reducing capacitor inductance [by] having a main portion and multiple tab portions that connect to respective terminations formed on the capacitor periphery. …
>
> A still further technology utilized for reduction in capacitor inductance involves [a] low inductance chip array (LICA) product, [which] **achieves low inductance values by low aspect ratio** of the electrodes….

Another aspect of D1 discloses the relationship between the gap between a pair of external electrodes (which creates a current path or loop) and the resulting inductance of such arrangement. See, D1, Fig. 2, per below and its related description:

"FIG. 2 provides a graphical comparison of general inductance trends for low inductance MLCC components especially depicting lumped ESL values versus cancellation loop width for multiple exemplary LGA capacitor embodiments of differing sizes;…"

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