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Rutt

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[54] **VARISTOR OR CAPACITOR AND METHOD OF MAKING SAME**

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Related U.S. Application Data

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[51] **Int. Cl.**[5] **H01G 4/10**; H01G 7/00; C04B 33/34

[52] **U.S. Cl.** **361/321**; 29/25.42; 264/61

[58] **Field of Search** 361/320, 321; 29/25.42; 264/61, 63, 56

[56] **References Cited**

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[57] **ABSTRACT**

A method of manufacturing an improved varistor or capacitor, and the resultant improved varistor or capacitor is described. In accordance with the method the ceramic layers of the varistor are formed by providing at least two strata separated by a boundary layer which resists grain growth thereacross. The ceramic body is sintered under temperature conditions sufficiently low that grain growth within the strata defining the ceramic layers is restricted to the strata such that grain growth across the boundary material is minimized. By this method the ceramic layers have a predictable number of grain boundaries between adjacent electrodes.

4 Claims, 2 Drawing Sheets

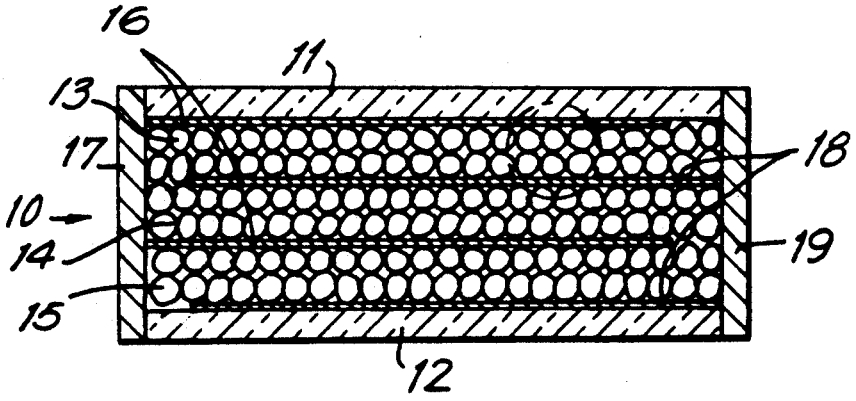


FIG. 1

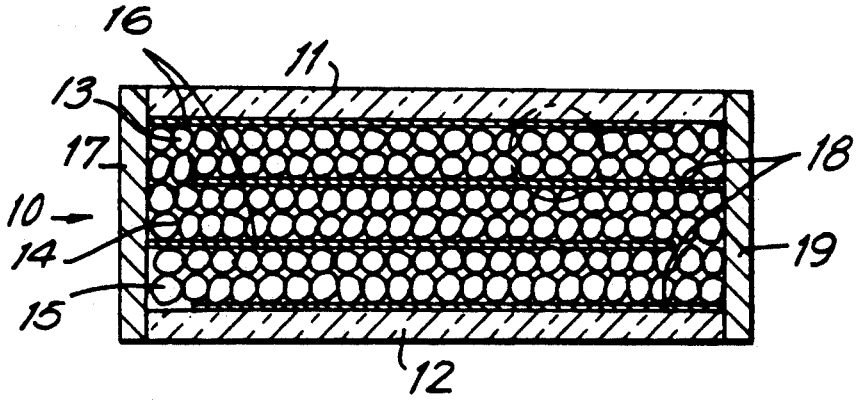
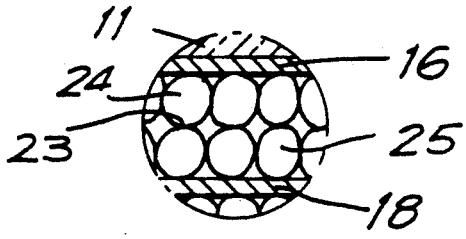


FIG. 1A



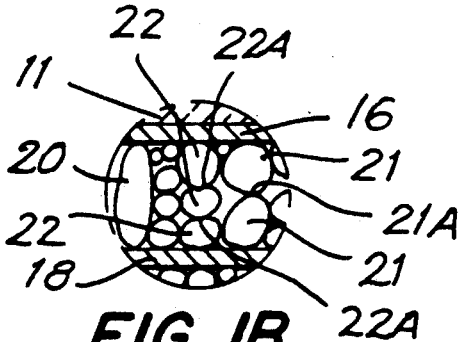


FIG. 1B
PRIOR ART

FIG. 2

FIG. 3

VARISTOR OR CAPACITOR AND METHOD OF MAKING SAME

This application is a division of application Ser. No. 07/191,123 filed May 6, 1988.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is directed to a varistor or capacitor, and more particularly to a monolithic ceramic device of the type described.

2. General Discussion

A ceramic varistor comprises essentially an intergranular barrier layer capacitor including a monolithic ceramic body having a multiplicity of electrode layers separated by ceramic layers. The odd numbered electrode layers, i.e. the first, third, fifth, etc., are electrically connected as are the even numbered electrode layers. The varistor is typically employed in shunting relation of an electronic circuit to be protected. It is the function of a varistor to provide a high resistance (and a degree of capacitance) when voltages impressed on the electronic circuit are maintained below a predetermined threshold voltage, and to provide a low resistance shunt when voltages exceed the threshold.

Heretofore, it has been exceedingly difficult to manufacture varistors having a predictable breakdown voltage, and particularly varistors which are rendered conductive at low voltages, i.e. 15 volts or less. The practical solution heretofore adopted by the industry has been to manufacture the varistor in a conventional manner, i.e. in the same manner as capacitors are conventionally manufactured utilizing known formulations compounded to function as varistors. Thereafter, the varistors produced are individually tested as to break down voltage and classified. It will be readily recognized that the individual testing or batch testing of varistors constitutes a complicating and costly step in the manufacture of varistors. A further desirable characteristic of a varistor is that when the same becomes conductive as a result of exposure to voltages beyond a threshold voltage, that the current carrying capacity of the varistor be as great as is possible. This characteristic is best realized where substantially the entirety of the ceramic components become simultaneously conductive thus providing the greatest current path between the various electrodes of opposite polarity. In conventional varistors, and even those varistors which have been classified to break down at a particular voltage, the break down does not occur uniformly, especially where the impressed voltage only slightly exceeds the threshold voltage. As a result, the ability of such varistors to function as an effective shunt is greatly reduced since conduction between opposed electrodes is focused at limited areas with remaining areas of ceramic continuing to be highly resistive.

It has been experimentally determined that the breakdown voltage of a varistor-ceramic formulation is a function of the number of grain boundaries of the ceramic grains intervening between adjacent electrode layers. The greater the number of boundaries between adjacent layers, the higher the break down voltage necessary to provide a conductive path. Conversely, in the event of a grain size such that grains of ceramic directly span the distance between adjacent electrodes, the device will exhibit break down or pass current at extremely low voltages. From the foregoing experimental findings, it will be evident that a highly undesirable condition results where the number of grain boundaries between adjacent electrodes varies greatly across the expanse of the ceramic layers. In such case, the break down voltage will be a function of and will occur at that area or those areas where there are concentrations of a limited number of grain boundaries. Where the break down is concentrated in a limited number of areas, it will be readily recognized that the current carrying capacity is substantially lower than would be the case if the break down occurred more or less uniformly throughout the entire area of the ceramic.

Efforts have been made to provide a ceramic having uniform grain boundary concentrations across the thickness of the ceramic. These efforts have heretofore been relatively unsuccessful on a commercial scale. Such efforts have included close control of the ceramic particle size embodied in the "green" ceramic layers; processing the ceramic under carefully controlled heating conditions during the sintering procedure; modifying sintering times, etc. As noted, none of the above methods have proven satisfactory.

A particularly acute problem arises when it is desired to provide a varistor having a relatively low break down voltage, i.e. in the order of 15 volts or less. The manufacture of such varistors to provide for break down at low threshold voltages and yet provide high current carrying capacity when the threshold voltage is exceeded has heretofore been very difficult.

SUMMARY OF THE INVENTION

The present invention may be summarized as directed to an improved method for manufacturing varistors and capacitors having predictable and readily repeatable break down or operating voltage characteristics. While it is considered that the principle utility of the instant invention lies in the production of varistors, it would be understood from the ensuing description that capacitors of the intergranular barrier layer type having improved characteristics will likewise benefit from the disclosed technology.

The invention is predicated in large measure on the discovery that ceramic grain growth is inhibited by the higher binder concentrations present at the upper surface of a green ceramic tape or stratum, such that when the tape or stratum is processed within controlled heating parameters, ceramic grains will not grow across the high-binder concentration boundary. By thus constructing a green ceramic layer which is comprised of two or more strata each of which strata incorporates a high-binder concentration at its upper extremity, and by processing such multi-stratum layer in such manner that the grain size does not extend across the boundary between adjacent strata, it is now possible to create a ceramic layer within the varistor wherein the number of grain boundaries within the layer is a function of the number of strata, and is thus controllable in accordance with the number of strata of which the layer is comprised.

The layer which is comprised of a number of strata may be fabricated by any of a number of different techniques. Specifically in addition to the tape stacking process briefly described above, a binder and ceramic formulation may be deposited as by screening or doctoring on a surface and the thus formed stratum may be overcoated with an organic ink as by swabbing. After drying of the organic ink layer, a further thickness of resin bonded ceramic may be overcoated atop the or-

ganic layer, dried, and the process repeated. In this instance, the thin layers of organic ink define the grain growth barriers which provide a predictable grain structure. Numerous other techniques for forming the layers comprising the various strata are known. These techniques include silk-screening, dipping, doctor-blading, spraying, etc.

It is accordingly an object of the invention to provide a varistor or capacitor comprised of one or more layers of ceramic, such layers being characterized by being formed of essentially discreet strata, the said strata having a predictable grain growth characteristic whereby the grain or grains of a given stratum cannot project across the boundary between the next adjacent stratum. In this manner, there may be formed a ceramic layer wherein the number of grains taken in a depth-wise direction may be accurately controlled. A further object of the invention is the provision of a method of forming a varistor or capacitor of the type described and the resultant product.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is now made to the accompanying drawings wherein.

FIG. **1**. is a schematic sectional view through a capacitor or varistor in accordance with the invention.

FIG. **1A** is a magnified section of the circled component portion of FIG. **1**.

FIG. **1B** is a view similar to FIG. **1A** depicting the grain size distribution which is typical of prior art capacitors and or varistors.

FIG. **2** is reproduction through a ceramic section taken by a scanning electron microscope (SEM).

FIG. **3** is a further reproduction of an SEM photograph through a ceramic section magnified 2400 times.

DETAILED DESCRIPTION OF DRAWINGS

Referring now to FIG. **1**, there is disclosed a schematic representation of a varistor **10** formed of a monolithic block of ceramic having internal electrodes separated by ceramic material. More particularly, the ceramic block or monolith includes upper and lower sealing or encapsulating layers **11**, **12** respectively integrally formed with a series of ceramic layers, (three being shown in the illustrated embodiment) the ceramic layers being numbered **13**, **14**, and **15** respectively.

The varistor includes a pair of electrodes **16**, **16** of a first polarity which are joined by a termination area **17**. Electrodes **18**, **18** of opposite polarity are joined by termination **19**. The electrodes **16** are separated from electrodes **18** by the intervening dielectric layers **13**, **14** and **15**.

As thus far described, the construction of the varistor or capacitor is entirely conventional, the invention hereof relating to the nature of the dielectric layers **13**, **14**, and **15**.

As is schematically shown in FIG. **1B** representing a typical prior art dielectric ceramic layer, the layer is comprised of a multiplicity of ceramic grains. The grains intervening between the electrode layers **16**, **18** are randomly distributed in size in such manner that larger grains such as grain **20** may span the entire distance between the electrodes **16**, **18** there thus being no inter-granular boundaries between the electrodes in the area occupied by grain **20**. In a second area a pair of grains **21** may span the electrodes thus defining a single inter-granular boundary **21A** in the area between electrodes **16** and **18** in registry with grains **21**. In similar fashion, grains **22** are dimensioned such that three grains span the distance between the electrodes resulting in a structure in which there are two grain boundaries intervening between the electrodes.

A dielectric ceramic matrix in accordance with that illustrated in FIG. **1B** is highly disadvantageous since as previously noted, the break down resistance of the layer will vary as a function of the number of intervening grain boundaries between the electrodes. Thus in the example of FIG. **1B** a break down will occur first in the area of grain **20** before a break down would occur between grains **21**, and in turn the area between grains **21** will become conductive before the area between grains **22**, etc. It will thus be readily recognized that a varistor wherein the ceramic dielectric layer is of the consistency of the prior art type shown in FIG. **1B** is undesirable in that the threshold voltage for break down will first occur in the areas of no grain boundaries or limited grain boundaries. Accordingly, the desired conductive nature of the varistor will be limited to those electrical current paths which register with grains such as grains **20**, and perhaps **21** and accordingly, even when the varistor becomes conductive, the conductive carrying paths will be limited to the areas of fewest intervening grain boundaries.

In FIGS. **1** and **1A** there is disclosed an idealized grain structure for the dielectric layers wherein the number of grain boundaries intervening between electrodes **16** and **18** are essentially equal throughout the entire area of the dielectric material. For purposes of simplicity of illustration, the dielectric components of FIGS. **1** and **1A** are disclosed as providing a single grain boundary **23** between the strata defined by grains **24** and grains **25**. As will be more fully explained hereinafter, as a practical matter a varistor will be formed with a predictable number of strata and hence a predictable number of grain boundaries, the number of boundaries sometimes being substantially greater than the single grain boundary structure illustrated.

By way of illustration, FIG. **2** comprises a photo micrograph through a section of ceramic formed in accordance with the invention. In the illustrated photograph, the layer **30** is comprised of five distinct strata **30A**, **30B**, **30C**, **30D**, and **30E** whereby the layer **30** exhibits four grain boundary areas **31A**, **31B**, **31C**, and **31D**. In the photo micrograph of FIG. **2** there are illustrated void areas **32**, **33** intervening between layer **30** and adjacent layers **34** and **35**. These intervening areas can be subsequently be filled with electroding material, typically molten lead, in a known manner in accordance with one or more of the following U.S. Pat. Nos. 3,965,522; 3,679,950. Alternatively, the areas **32**, **33** between layers **34** and **30** and **35** and **30** may, prior to conversion of the green ceramic to a sintered ceramic monolith be provided, as by screening or the like, with an electrode forming ink in the manner set forth, by way of example, in U.S. Pat. Nos. Re 26,421 of Jul. 2, 1968 and 4,347,650 of Sep. 7, 1982.

It is to be understood that the manner of forming a varistor or capacitor from the once formed green ceramic layers **30** is conventional and well known to the art, the present invention being directed to the concept of and manner of formation of layers **30** which will, following sintering, provide a predictable and regular number of grain boundaries between intervening electrode layers.

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