US 20110141655A1

(19) United States
(12) Patent Application Publication
Jeong et al.

(10) Pub. No.: US 2011/0141655 A1
(43) Pub. Date: Jun. 16, 2011

(54) **MULTILAYER CERAMIC CAPACITOR**

(75) Inventors: **Ji Hun Jeong**, Suwon (KR); **Hyo Jung Kim**, Suwon (KR); **Hyo Jung Kim**, Seoul (KR); **Dong Ik Chang**, Suwon (KR); **Doo Young Kim**, Yongin (KR)

(73) Assignee: **SAMSUNG ELECTRO-MECHANICS CO., LTD.**

(21) Appl. No.: **12/768,993**

(22) Filed: **Apr. 28, 2010**

(30) **Foreign Application Priority Data**

Dec. 10, 2009 (KR) 10-2009-0122195

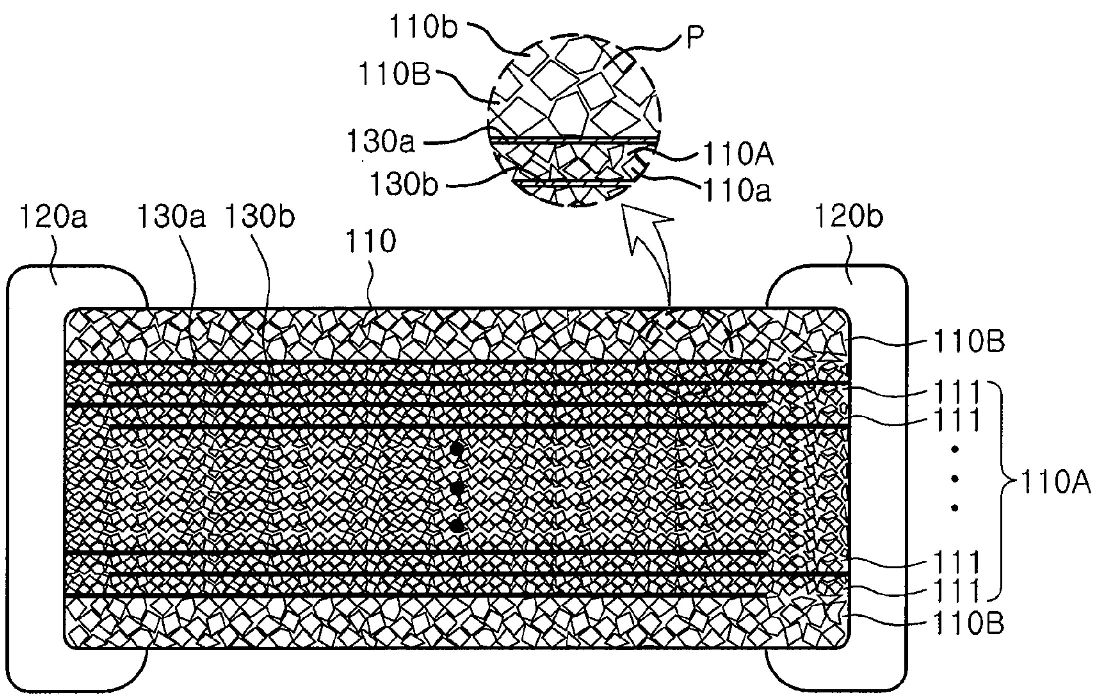
Publication Classification

(51) **Int. Cl.**
H01G 4/12 (2006.01)
H01G 4/005 (2006.01)

(52) **U.S. Cl.** **361/303**; 361/306.3; 361/313

(57) **ABSTRACT**

Disclosed is multilayer ceramic capacitor. The multilayer ceramic capacitor includes a capacitive part including dielectric layers and first and second internal electrodes alternately laminated therein, wherein the dielectric layers include first ceramic particles having an average particle size of 0.1 μm to 0.3 μm, and one set of ends of the first internal electrodes and one set of ends of the second internal electrodes are exposed in a lamination direction of the dielectric layers, a protective layer formed on at least one of top and bottom surfaces of the capacitive part, including second ceramic particles and having a porosity of 2% to 4%, wherein an average particle size ratio of the second ceramic particles to the first ceramic particles ranges from 1.1 to 1.3; and first and second external electrodes electrically connected to the first and second internal electrodes exposed in the lamination direction of the dielectric layers.



I–I'

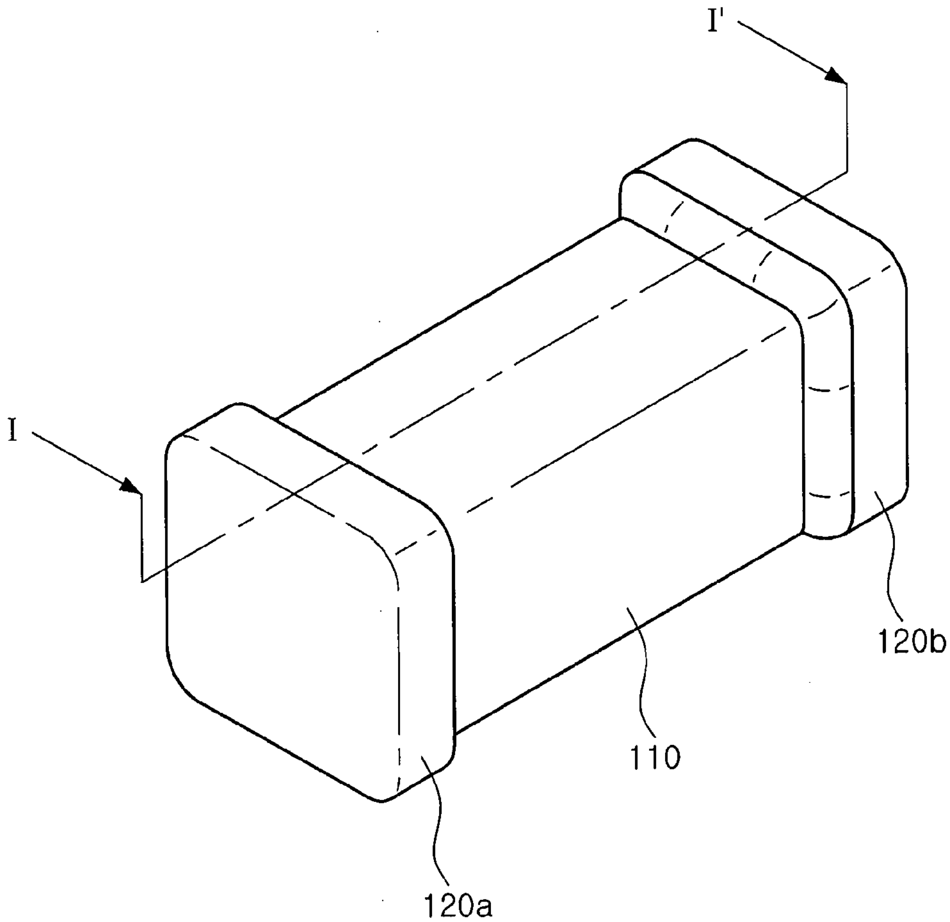


FIG. 1

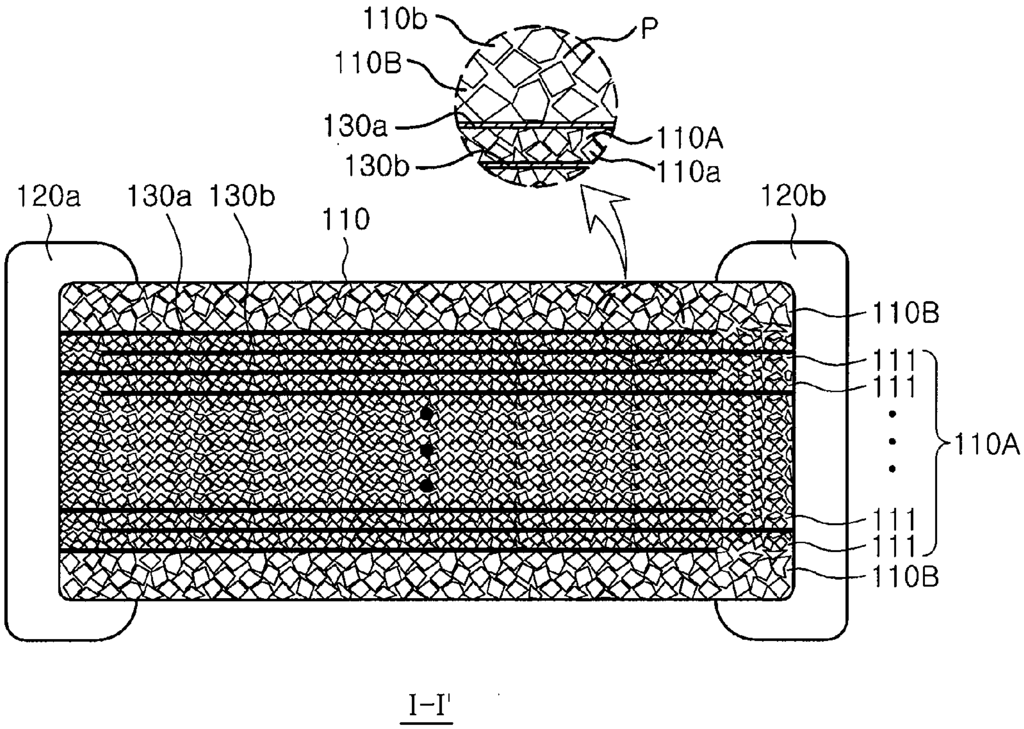

110b
P
110B
130a
110A
130b
110a
120a
130a 130b
110
120b
110B
111
111
110A
111
111
110B
I-I'

FIG. 2

MULTILAYER CERAMIC CAPACITOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority of Korean Patent Application No. 10-2009-0122195 filed on Dec. 10, 2009, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a multilayer ceramic capacitor, and more particularly, to a multilayer ceramic capacitor having a high level of reliability and a low crack occurrence rate by reducing stress acting on the multilayer ceramic capacitor.

[0004] 2. Description of the Related Art

[0005] In general, electronic components using a ceramic material, such as capacitors, inductors, piezoelectric devices, varistors or thermistors, include a ceramic body formed of a ceramic material, internal electrodes provided inside the ceramic body, and external electrodes installed on the surface of the ceramic body.

[0006] Multilayer ceramic capacitors among such ceramic electronic components include a plurality of laminated dielectric layers, internal electrodes interleaved with the dielectric layers, and external electrodes electrically connected to the internal electrodes.

[0007] Multilayer ceramic capacitors are being widely used as a part of mobile communications devices, such as computers, personal digital assistants (PDA) and mobile phones, due to their small size, high capacity and ease of mounting.

[0008] Recently, as electronic products have become compact and multi-functional, chip components have also tended to become compact and highly functional. Following this trend, a multilayer ceramic capacitor is required to be smaller than ever before, but to have a high capacity.

[0009] As for a general method of manufacturing a multilayer ceramic capacitor, ceramic green sheets are manufactured and a conductive paste is printed on the ceramic green sheets to thereby form internal electrode layers. Tens to hundreds of such ceramic green sheets, provided with the internal electrode layers, are then laminated to thereby produce a green ceramic laminate. Thereafter, the green ceramic laminate is pressed at high pressure and high temperature and subsequently cut into green chips. Thereafter, the green chip is subjected to plasticizing, firing and polishing processes, and external electrodes are then formed thereon, thereby completing a multilayer ceramic capacitor.

[0010] Typically, the internal electrodes, formed of metal, shrink and expand easily as compared to ceramic materials. Thus, stress caused by this difference in thermal expansion coefficient may act on the ceramic laminate, thereby causing cracks.

[0011] The multilayer ceramic capacitor is used while mounted on a wiring board. In this case, the external electrodes of the multilayer ceramic capacitor are electrically connected to the wiring board by soldering and a conductive land on the wiring board. When the multilayer ceramic capacitor is mounted on the wiring board by using soldering, or when the wiring board mounted with the multilayer

capacitor. Such thermal impact and shear stress may cause cracks in the multilayer ceramic capacitor.

[0012] As the multilayer ceramic capacitor has recently become smaller in size and higher in capacitance, many attempts have been made to manufacture a thinner and multilayer ceramic body. However, as the ceramic body has become thinner and multilayered, a crack occurrence rate has increased. Therefore, there is an increasing need for preventing this increase in the crack occurrence rate therein.

SUMMARY OF THE INVENTION

[0013] An aspect of the present invention provides a multilayer ceramic capacitor capable of achieving a high level of reliability and a low crack occurrence rate by reducing stress acting on the multilayer ceramic capacitor.

[0014] According to an aspect of the present invention, there is provided a multilayer ceramic capacitor including: a capacitive part including dielectric layers and first and second internal electrodes alternately laminated therein, wherein the dielectric layers include first ceramic particles having an average particle size of 0.1 μm to 0.3 μm, and one set of ends of the first internal electrodes and one set of ends of the second internal electrodes are exposed in a lamination direction of the dielectric layers; a protective layer formed on at least one of top and bottom surfaces of the capacitive part, including second ceramic particles and having a porosity of 2% to 4%, wherein an average particle size ratio of the second ceramic particles to the first ceramic particles ranges from 1.1 to 1.3; and first and second external electrodes electrically connected to the first and second internal electrodes exposed in the lamination direction of the dielectric layers.

[0015] The first ceramic particles may include barium titanate ($BaTiO_3$)-based ceramics, lead complex perovskite-based ceramics, or strontium titanate ($SrTiO_3$)-based ceramics. The second ceramic particles may include barium titanate ($BaTiO_3$)-based ceramics, lead complex perovskite-based ceramics, or strontium titanate ($SrTiO_3$)-based ceramics.

[0016] The dielectric layers of the capacitive part may have a porosity of 1% or less.

[0017] The capacitive part may have a thickness of 50 μm to 2000 μm, and the protective layer may have a thickness of 10 μm to 100 μm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The above and other aspects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0019] FIG. **1** is a schematic perspective view illustrating a multilayer ceramic capacitor according to an exemplary embodiment of the present invention; and

[0020] FIG. **2** is a schematic cross-sectional view taken along line I-I' of FIG. **1**, illustrating the multilayer ceramic capacitor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0021] Exemplary embodiments of the present invention will now be described in detail with reference to the accompanying drawings.

[0022] The invention may, however, be embodied in many ments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. Like reference numerals in the drawings denote like elements.

[0023] FIG. **1** is a schematic perspective view illustrating a multilayer ceramic capacitor according to an exemplary embodiment of the present invention. FIG. **2** is a schematic cross-sectional view taken along line I-I' of FIG. **1**, illustrating the multilayer ceramic capacitor.

[0024] Referring to FIGS. **1** and **2**, a multilayer ceramic capacitor, according to this exemplary embodiment, includes a sintered ceramic body **110**, first and second internal electrodes **130***a* and **130***b* formed inside the sintered ceramic body **110**, and first and second external electrodes **120***a* and **120***b* electrically connected to the first and second internal electrodes **130***a* and **130***b*.

[0025] In FIG. **2**, the sintered ceramic body **110** includes a capacitive part **110**A, and protective layers **110**B formed on the top and bottom surfaces of the capacitive part **110**A.

[0026] The protective layer **110**B may be formed on at least one of the top and bottom surfaces of the capacitive part **110**A. The protective layers **110**B, when formed on both the top and bottom surfaces of the capacitive part **110**A, have excellent influence in lowering a crack occurrence rate.

[0027] The capacitive part **110**A is obtained by laminating a plurality of ceramic dielectric layers **111** and the first and second internal electrodes **130***a* and **130***b* in an alternating manner. The first and second internal electrodes **130***a* and **130***b* are paired as having opposite polarities. These first and second internal electrodes **130***a* and **130***b* oppose each other in a lamination direction of the ceramic dielectric layers **111**, and are electrically insulated from each other by the ceramic dielectric layers **111**. One set of ends of the first internal electrodes **130***a* and the other set of ends of the second internal electrodes **130***b* are exposed in the lamination direction of the ceramic dielectric layers **111**. The exposed ends of the first and second internal electrodes **130***a* and **130***b* are electrically connected to the first and second external electrodes **120***a* and **120***b*, respectively.

[0028] When a predetermined voltage is applied to the first and second external electrodes **120***a* and **120***b*, electric charges are accumulated between the opposing first and second internal electrodes **130***a* and **130***b*. Here, the capacitance of the multilayer ceramic capacitor is in proportion to the area of the opposing first and second internal electrodes **130***a* and **130***b*.

[0029] The ceramic dielectric layers **111** of the capacitive part **110**A contain first ceramic particles having an average particle size D**1** of 0.1 μm to 0.3 μm. The first ceramic particles **110***a* are not specifically limited, provided that they have a high dielectric constant. For example, the first ceramic particles **110***a* may utilize barium titanate ($BaTiO_3$)-based ceramics, lead complex perovskite-based ceramics, strontium titanate ($SrTiO_3$)-based ceramics or the like.

[0030] The first and second internal electrodes **130***a* and **130***b* are formed of a conductive metal, which may utilize, for example, Ni or a Ni alloy. The Ni alloy may contain Mn, Cr, Co or Al as well as Ni.

[0031] The first and second external electrodes **120***a* and **120***b* are formed of a conductive metal, and may contain, for example, copper.

The protective layer **110**B is formed of a ceramic material, and contains second ceramic particles whose average particle size ratio to the first ceramic particles **110***a* ranges from 1.1 to 1.3.

[0033] The second ceramic particles **110***b* are not specifically limited, provided that they have a high dielectric constant. For example, the first ceramic particles **110***a* may utilize barium titanate ($BaTiO_3$)-based ceramics, lead complex perovskite-based ceramics, strontium titanate ($SrTiO_3$)-based ceramics or the like.

[0034] Typically, a thermal expansion coefficient of a ceramic material reaches approximately 8 to 9×10^{-6}/° C., and internal electrodes, formed of nickel, have a thermal expansion coefficient of approximately 13×10^{-6}/° C. Thus, tensile and compressive stress acts on dielectric layers having a relatively small thermal expansion coefficient. Since the thermal expansion stress due to the thermal impact has its greatest influence on the interface between the protective layer **110**B and the capacitive part **110**A, a ceramic laminate having high brittleness may be cracked.

[0035] According to this exemplary embodiment of the present invention, the protective layer **110**B includes the second ceramic particles **110**B having a greater particle size than the first ceramic particles **110***a*. The second ceramic particles **110***b*, having a greater particle size than the first ceramic particles **110***a*, are slow in shrinkage behavior as compared to the first ceramic particles **110***a*. This alleviates a stress difference occurring at the time of the thermal expansion of internal electrodes.

[0036] An average particle size ratio (D**2**/D**1**, where D**1** denotes the average particle size of the first ceramic particles **110***a* and D**2** denotes the average particle size of the second ceramic particles **110***b*) of the second ceramic particles **110***b* to the first ceramic particles **110***a* ranges from 1.1 to 1.3. An average particle size ratio (D**2**/D**1**) of less than 1.1 fails to alleviate thermal impact occurring during the thermal expansion of internal electrode layers. This results in a high crack occurrence rate. An average particle size ratio exceeding 1.3 may cause non-firing or increase a crack occurrence rate.

[0037] Furthermore, the protective layer **110**B includes a plurality of pores P, and the porosity thereof ranges from 2% to 4%. The protective layer **110**B is formed by sintering a slurry which is a mixture of the second ceramic particles **110***b*, an organic binder and a solvent. The porosity of the protective layer **110**B can be controlled by controlling the content of the second ceramic particles **110***b*, and the kind and amount of organic binder. The content of the second ceramic particles **110***b* may range from 15% to 40%.

[0038] The above-mentioned porosity range may enable the absorption of stress generated during the thermal expansion, thereby reducing a crack occurrence rate at the interface between the capacitive part **110**A and the protective layer **110**B.

[0039] A plurality of pores also exist in the capacitive part **110**A, and the porosity of the capacitive part **110**A may be 1% or less.

[0040] The protective layer **110**B may be thicker than a single dielectric layer within the capacitive part **110**A. For example, the single dielectric layer **111** of the capacitive part **110**A may have a thickness of 2 μm or less. As 25 or more of such dielectric layers **111** are laminated, the thickness of the capacitive part **110**A may range from 50 μm to 2000 μm. The

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

WHAT WILL YOU BUILD? | **sales@docketalarm.com** | **1-866-77-FASTCASE**

fastcase®
Smarter legal research.