

Jan. 22, 1963

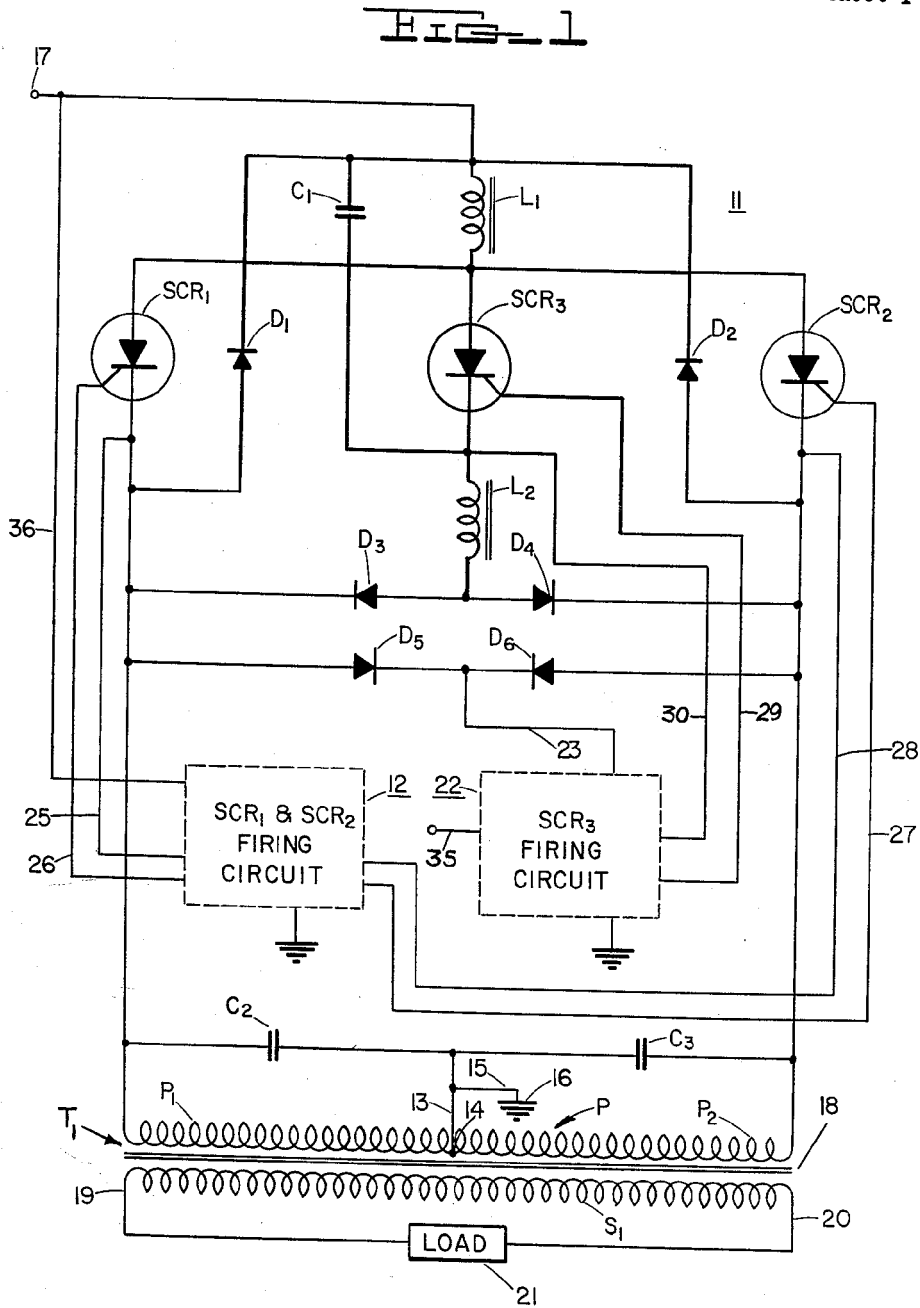
D. V. JONES

3,075,136

VARIABLE PULSE WIDTH PARALLEL INVERTERS

Filed Aug. 31, 1961

2 Sheets-Sheet 1



INVENTOR.
Dwight V. Jones,
BY *Henry J. Marinich*
Attorney.

Jan. 22, 1963

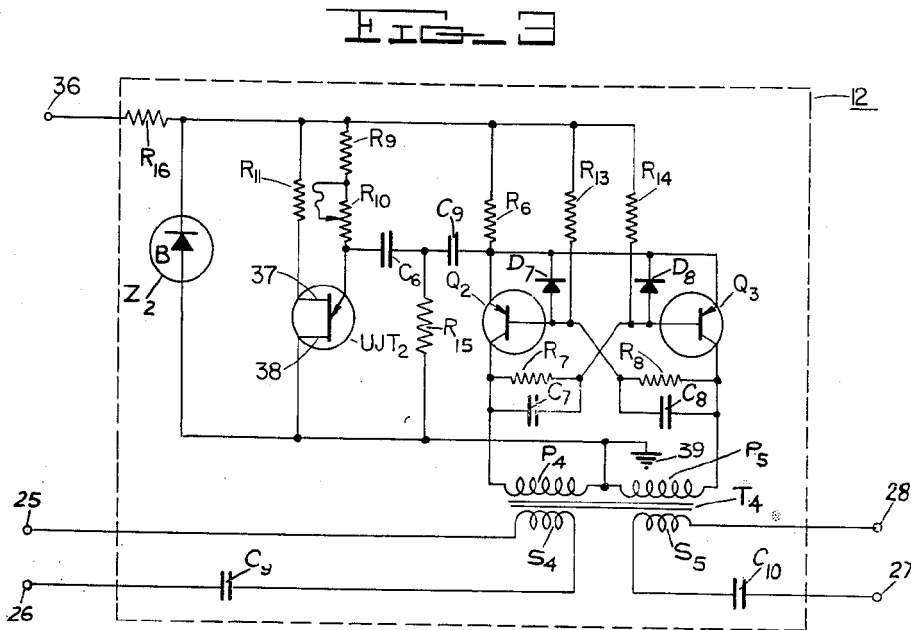
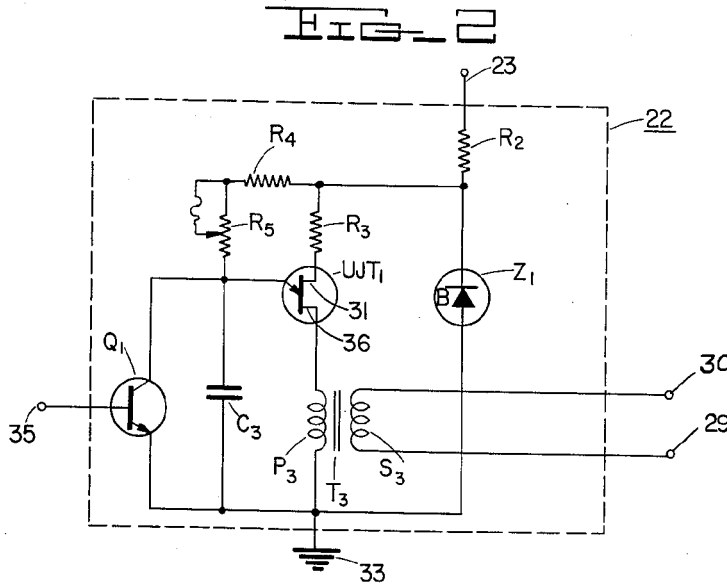
D. V. JONES

3,075,136

VARIABLE PULSE WIDTH PARALLEL INVERTERS

Filed Aug. 31, 1961

2 Sheets-Sheet 2



INVENTOR.
Dwight V. Jones,
BY *Henry J. Muenich*
Attorney.

1

3,075,136

VARIABLE PULSE WIDTH PARALLEL INVERTERS

Dwight V. Jones, Baldwinsville, N.Y., assignor to General Electric Company, a corporation of New York

Filed Aug. 31, 1961, Ser. No. 135,334

11 Claims. (Cl. 321-45)

This invention relates to parallel inverters and more particularly to an improved arrangement of a parallel inverter wherein the pulse width of the inverter output can be readily controlled.

Parallel inverters employing such switching devices as thyratrons, ignitrons and silicon controlled rectifiers, have been generally used for higher power applications as compared with the series type of inverters. At low operating frequencies, the parallel inverter can be used to provide a substantially square-wave alternating output from a direct current source. By rectifying the output voltage of the parallel inverter, the inverter can be used as a D.C. to D.C. converter or by employing a rectified alternating voltage input, the inverter can be readily adapted for use as a frequency changer.

In many applications of the parallel inverter, it is desirable that the power output of the inverter be effectively regulated. For example, in a lamp dimming system, a wide range of regulation is required to effectively operate the lamps at various levels of luminous intensity. Similarly, in a power supply system for the operation of motors at various speeds, it is desirable, if not necessary, to regulate the power supplied to the motors. Heretofore, the arrangements used to achieve power regulation in a parallel inverter have not been entirely satisfactory. In prior art parallel inverter circuits employing thyratrons, regulation was achieved at the expense of increased commutating capacity, and the circuits were inefficient. There is a need, therefore, for a parallel circuit inverter wherein a high degree of regulation can be achieved readily and efficiently.

Accordingly, an object of this invention is to provide an improved variable pulse width parallel inverter.

Another object of the present invention is to provide an improved parallel inverter wherein regulation of the power supplied by the inverter is efficiently achieved.

It is still another object of the invention to provide an improved parallel circuit inverter wherein the pulse width of the inverter output can be readily varied to achieve regulation by feedback control arrangements.

The foregoing and other objects and advantages of the invention are realized by a parallel inverter circuit having a pair of parallel connected controlled rectifiers which are alternately triggered at a predetermined frequency to cause a reversal of current flow through a first and a second primary winding portion of an output transformer. The conduction time of the pair of controlled rectifiers is controlled by firing a cut-off controlled rectifier at a predetermined point at each half cycle to connect a charged capacitor in parallel with an inductor in the circuit and thus provide a pulse that turns off the conducting one of the pair of controlled rectifiers. In this manner the pulse width of the inverter output is regulated. The firing of the cut-off controlled rectifier is synchronized with the start of the conduction of the controlled rectifiers so that the controlled rectifier is fired after a predetermined interval in each half cycle after one of the pair of controlled rectifiers is fired.

The subject matter which I regard as my invention is set forth in the appended claims. The invention itself, however, together with further objects and advantages thereof may be understood by referring to the following

2

FIG. 1 is a schematic circuit diagram of a parallel inverter circuit illustrating one embodiment of the invention.

FIG. 2 is a schematic circuit diagram of the firing circuit for triggering controlled rectifier SCR₃ of the parallel inverter illustrated in FIG. 1; and

FIG. 3 is a schematic circuit diagram of the firing circuit used to alternately trigger controlled rectifiers SCR₁ and SCR₂ of the parallel inverter illustrated in FIG. 1.

Having more specific reference now to the parallel inverter identified generally by reference numeral 11 and shown in FIG. 1, it will be seen that the parallel inverter 11 includes a pair of controlled rectifiers SCR₁ and SCR₂ connected in circuit with a first winding portion P₁ and a second winding portion P₂ of output transformer T₁. As the controlled rectifiers SCR₁ and SCR₂ are alternately triggered by firing circuit 12, a voltage of one polarity is induced across secondary windings S₁ during one half of each cycle of the inverter output and a voltage of opposite polarity is induced across the secondary winding S₁ in the other half of each cycle.

It will be noted that controlled rectifier SCR₁ and primary winding portion P₁ are connected in a parallel circuit with controlled rectifier SCR₂ and primary winding portion P₂ across a direct current supply means which includes a lead 13 connected to a center-tap 14 on primary winding P₁, lead 15 connected to a ground 16, and input terminal lead 17 provided for connection to the positive side of a direct current source.

The output transformer T₁ has a magnetic core 18 and a secondary winding S₁ inductively coupled with the primary winding P which is divided by tap 14 into primary winding portions P₁ and P₂. As shown in FIG. 1, the secondary winding S₁ is connected in circuit by output leads 19, 20 with a load 21. Since transformer T₁ is subjected to rapidly changing currents during the commutation interval of the parallel inverter 11, the leakage reactance of the transformer T₁ was preferably kept down to a minimum. Thus, the transformer T₁ was designed so that it operates below saturation. The leakage inductance between the primary winding portions P₁ and P₂, and the source impedance is preferably kept relatively small so that it will have no significant effect on the commutation of the controlled rectifiers SCR₁ and SCR₂.

It will be seen that in the illustrative embodiment of the invention shown in FIG. 1, the input terminal lead 17 is connected in circuit with a pair of feedback diodes D₁, D₂ and with controlled rectifiers SCR₁, SCR₂ through an inductor L₁. Input terminal lead 17 is provided for connection to a suitable direct current voltage source, which should be capable of accepting power as well as supplying power. Inductor L₁ is connected in series circuit with a cut-off controlled rectifier SCR₃. A commutating capacitor C₁ is connected in parallel circuit across inductor L₁ and controlled rectifier SCR₃ so that when the controlled rectifier SCR₃ is triggered into a conducting state, inductor L₁ is connected in electrical circuit and in parallel with the commutating capacitor C₁. Thus, when connected in parallel, inductor L₁ and the commutating capacitor C₁ comprise an oscillatory circuit.

Feedback diode D₁ is connected in circuit with one end of primary winding portion P₁ and in inverse relation with controlled rectifier SCR₁. Similarly, feedback diode D₂ is connected in circuit with primary winding portion P₂ of the primary winding P and in inverse relation with controlled rectifier SCR₂.

Connected in such an arrangement, the feedback diodes D₁, D₂ serve to limit the voltage across primary winding portions P₁, P₂ of transformer T₁ to the magnitude of the D.C. voltage supply and make it possible to

3

in connection with the description of the operation of the parallel inverter 11, the diodes D_1 , D_2 feed back reactive power into the supply and thereby reduce voltage variations across the secondary winding S_1 .

Continuing with the description of the circuit shown schematically in FIG. 1, it will be seen that one end of the inductor L_2 is connected in circuit with commutating capacitor C_1 and controlled rectifier SCR_3 . The other end of the inductor L_2 is connected in circuit with the anodes of diodes D_3 , D_4 . They are so poled that when either controlled rectifier SCR_1 or SCR_2 is in a conducting state, the lower plate of capacitor C_1 , as seen in the view of FIG. 1, will be negatively charged to a voltage considerably greater than the source of voltage. This increased voltage is due to the transformer action in charging the commutating capacitor C_1 through the diodes D_3 and D_4 and also the circuit time constants. Preferably, the inductor L_2 provides an inductance sufficient to keep the current flow through it to a low value until the controlled rectifier SCR_3 is turned off by the reversal of the current in the oscillatory circuit comprised of the capacitor C_1 and the inductor L_1 .

The controlled rectifiers SCR_1 , SCR_2 and SCR_3 used in the illustrative embodiment of the invention were PNP semiconductor devices each having three terminals, an anode represented by the arrow symbol, a cathode represented by a line drawn through the apex of the arrow symbol and a gate represented by a diagonal line extending from the cathode. Silicon controlled rectifiers are desirable power switching devices since relatively large amounts of power can be switched into a load using an insignificant amount of power to trigger the switching device. The operating characteristics of a silicon controlled rectifier are such that it conducts in a forward direction with a forward characteristic very similar to that of an ordinary rectifier when a gate signal is applied. Thus, when a positive voltage is applied to the outside P layer and a negative voltage is applied to the outside N layer, the two outside junctions are biased in a forward direction while the inner junction is reversely biased. Current does not flow through the controlled rectifier under these conditions, except for a small leakage current. When the voltage is increased to a breakover voltage, the current gain of the device increases to unity at which time the current through the controlled rectifier will increase suddenly and become a function of the applied voltage and the load impedance. The controlled rectifier will remain in a conductive state provided the current through the device exceeds a minimum holding value.

A small amount of current supplied to the gate lead can be used for controlling the firing of the controlled rectifier since the current supplied to the gate lowers the breakover voltage. The controlled rectifier is normally operated well below the forward breakover voltage and is triggered by supplying current to the gate lead.

A capacitor C_2 is connected in circuit with the cathode of controlled rectifier SCR_1 and across the primary winding portion P_1 so that the cathode is clamped to ground when a negative turn-off pulse is applied to the anode of controlled rectifiers SCR_1 . It also serves to minimize switching transients from the load. Similarly, capacitor C_3 is connected in circuit with controlled rectifier SCR_2 and across primary winding portion P_2 of the output transformer T_1 so that the cathode of controlled rectifier SCR_2 is clamped to ground when a negative turn-off pulse is applied to its anode. Capacitors C_2 and C_3 enhance the performance of the circuit, but they are not absolutely necessary since the circuit will operate without them.

In order to provide a unidirectional supply voltage for firing circuit 22, diodes D_5 and D_6 are connected across the primary winding P . A lead 23 is connected in cir-

4

controlled rectifiers SCR_1 , SCR_2 . Thus, firing circuit 22 is energized when either controlled rectifier SCR_1 or SCR_2 is conducting. It will be seen that the diode D_5 is poled so that when controlled rectifier SCR_1 starts conducting, a current is supplied to firing circuit 22. Also, diode D_6 is poled so that current will be supplied to firing circuit 22 the instant controlled rectifier SCR_2 is triggered. In this manner the firing circuit 22 is synchronized with the start of each half cycle of the inverter output which begins with the triggering of one of the controlled rectifiers SCR_1 , SCR_2 .

In FIGS. 2 and 3, I have illustrated the schematic circuit diagrams which are represented in the schematic diagram of FIG. 1 in block form. Firing circuit 12 is connected in circuit with the gates and cathodes of controlled rectifiers SCR_1 , SCR_2 by electrical leads 25, 26 and 27, 28, respectively. The gate and cathode of cut-off controlled rectifiers SCR_3 are connected in circuit with firing circuit 22 by means of electrical leads 29, 30. The type of firing circuits 12 and 22 which were employed in the exemplification of the invention shown in FIG. 1 are well known in the art and are described in the General Electric Controlled Rectifier Manual, first edition, 1960, at pages 50-58.

In accordance with the invention, the firing circuit 22 provides a current pulse to fire controlled rectifier SCR_3 which turns off the conducting controlled rectifier SCR_1 or SCR_2 at a predetermined point in each half cycle. It will be seen that input lead 23 connects firing circuit 22 in circuit with the controlled rectifiers so that a current is supplied only when one of the controlled rectifiers is conducting. A resistor R_2 and the zener diode Z_1 limit the maximum interbase voltage of unijunction transistor UJT_1 . The zener diode Z_1 is a semiconductor diode, preferably a silicon diode, having a predetermined reverse breakdown voltage. For voltages below the breakdown value, the zener diode Z_1 acts as a rectifier and only a negligibly small current can flow in the reverse direction. When the reverse voltage exceeds the breakdown value, the zener diode Z_1 presents a very low resistance and permits current to flow freely in the reverse direction with no substantial increase in voltage.

A resistor R_3 is connected in circuit with the base-two electrode 31 in order to compensate for temperature variations of the interbase resistance of the unijunction transistor UJT_1 . Capacitor C_3 is charged through resistor R_4 and the variable resistor R_5 . The rate at which the capacitor C_3 is charged to the peak emitter voltage of unijunction transistor UJT_1 determines the point in each half cycle at which unijunction transistor UJT_1 is fired. When unijunction transistor UJT_1 is fired, a pulse of current flows through primary winding P_3 of the pulse transformer T_3 and a current pulse is induced in the secondary winding S_3 , electrical leads 29, 30 applying this pulse across the gate and cathode of cut-off controlled rectifier SCR_3 . It will be seen that the primary winding P_3 is connected at one end with base-one electrode 32 and at the other end with a ground 33.

Transistor Q_1 acts as a shunt to divert charging current flowing through the resistor R_4 and R_5 . The amount of charging current diverted is proportional to the amount of current supplied to the base electrode of the transistor through lead 35. Thus, as base current is increased, additional current is diverted and the firing angle of the unijunction transistors UJT_1 is retarded. Accordingly, the firing of controlled rectifier SCR_3 is also retarded and the cut-off of the conducting controlled rectifier SCR_1 or SCR_2 is delayed.

In FIG. 3, I have illustrated a transistor multi-vibrator firing circuit 12 that was used in the illustrative embodiment of the invention to alternately apply firing pulses to controlled rectifiers SCR_1 and SCR_2 . Two pairs of output leads 25, 26 and 27, 28 which are connected in circuit

5

cathode of controlled rectifiers SCR₁, SCR₂, respectively, as shown in FIG. 1. The primary winding portions P₄, P₅ are connected in circuit with the collector of transistors Q₂, Q₃. Input terminal lead 36 is provided for connection to the positive side of the direct current source used to energize the parallel inverter in FIG. 1.

Although in the exemplification of the invention a multi-vibrator circuit configuration was used to provide alternating trigger pulses with good symmetry to the controlled rectifiers SCR₁, SCR₂, it will be appreciated that other firing circuits can be used to generate and provide alternate triggering pulses at a predetermined frequency to a pair of controlled rectifiers. As an example, a pair of unijunction transistor relaxation oscillators coupled together by means of a capacitor connected between the emitters may be employed to provide the alternating pulses. Also, firing circuits utilizing saturating reactors may be used as a pulse source.

The unijunction relaxation oscillator portion of the multi-vibrator circuit provides good symmetry and frequency control to the multi-vibrator. Although in exemplification of the invention the inverter circuit 11 shown in FIG. 1 was supplied with short duration trigger pulses to fire controlled rectifiers SCR₁ and SCR₂, for highly reactive loads the trigger pulse width must be extended in time for the duration of reactive current flow. The maximum pulse width at the gate cannot exceed the inverter pulse width, therefore for large reactive loads the trigger pulse width must follow the changing inverter pulse width. This varying trigger pulse width can be obtained by varying the symmetry of a multivibrator as a function of the inverter pulse width.

Continuing now with the description of the firing circuit 12 shown schematically in FIG. 3, it will be seen that the firing circuit 12 employs two PNP transistors Q₂, Q₃ in a saturating flip-flop arrangement. A unijunction transistor UJT₂ serves to trigger the flip-flop from one state to the other by providing a negative trigger pulse. This negative pulse is developed across resistor R₁₅ and is coupled to the resistor R₈ by means of the capacitor C₉. Capacitor C₆ serves as a timing capacitor. Cross coupling capacitors C₇ and C₈ are relatively small in size and are connected in parallel with the cross-coupling resistors R₇, R₈ and in circuit with the base electrodes of transistors Q₂, Q₃. Diodes D₇ and D₈ clamp the base electrode of transistors Q₂, Q₃ to the emitter electrode.

Resistor R₉ and the variable resistor or potentiometer R₁₀ control the charging rate of the timing capacitor C₆ and thereby serve as the frequency control for the inverter circuit. Resistor R₁₁ is connected to the base-two electrode 37 of the unijunction transistor UJT₂. Base-one electrode 38 is connected in circuit with a ground 39 by means of leads 40, 41. Resistors R₆, R₁₃, R₁₄ serve as temperature stabilizing resistors. Resistor R₁₀ provides the frequency control for the output of the inverter since it controls the rate at which the flip-flop is triggered. Capacitors C₉ and C₁₀ in conjunction with the gate to cathode impedance of the controlled rectifier differentiate the square wave across secondary windings S₄ and S₅ to provide a pulse output. Pulse triggering can be used unless the load has a low and lagging power factor. Through the action of the zener diode Z₂ and resistor R₁₆ a regulated D.C. voltage is applied to the unijunction transistor UJT₂.

Having reference now to the circuit shown in FIGS. 1, 2 and 3, the operation of the parallel inverter circuit 11 will now be more fully described. When the positive terminal of a direct current source is connected in circuit with input terminal lead 17 and the inverter circuit 11 is effectively grounded as shown in FIG. 1, inverter circuit 11 is energized. Let us assume arbitrarily that a firing pulse is supplied initially to the gate of the controlled rectifier SCR₁. When controlled rectifier SCR₁ is trig-

6

ged due to the transformed action that charges the capacitor C₁ through the diode D₄. Also, when controlled rectifier SCR₁ is triggered, current flows through diode D₅ to firing circuit 22 and capacitor C₃ begins its charging period.

Depending upon the setting of the variable resistor or potentiometer R₅ and the feed-back current being supplied to the transistor Q₁, the unijunction transistor UJT₁ will trigger the control rectifier SCR₃ at a predetermined point in the half cycle of the alternating inverter output. When controlled rectifier SCR₃ is triggered, it will be seen that the lower plate of the commutating capacitor C₁ is negatively charged. Also, when controlled rectifier SCR₃ is triggered, commutating capacitor C₁ is connected in parallel circuit relation with the inductor L₁. An oscillatory pulse is developed across the inductor L₁ which reverse biases controlled rectifier SCR₁ and thereby turns it off.

The commutating capacitor C₁ will maintain a reverse bias across controlled rectifier SCR₁ long enough for the controlled rectifier SCR₁ to return to a blocking state. Capacitor C₂ clamps the cathode of controlled rectifier SCR₁ to ground 16 while the negative turn-off pulse is applied to the anode. It will be seen that controlled rectifier SCR₃ conducts for a very short interval since it is reverse biased when the current reverses in the oscillatory circuit comprised of capacitor C₁ and the inductor L₁.

During the commutating interval an inductive load connected at the output of the inverter circuit 11 would prevent the main load current from reversing instantaneously. Diodes D₁, D₂ are therefore provided to feed-back this current to the direct current supply until the load current reverses. In the first half of each cycle it will be appreciated that during the interval that current flows through diode D₂, controlled rectifier SCR₂ will be back-biased, and if conducting, would be turned off. For highly reactive loads, the triggering pulse width provided by firing circuit 22 was extended in time for the duration of the reactive current flow but did not exceed the inverter pulse width.

Continuing with the description of the operation of the inverter circuit, the second half of the cycle commences when a pulse is supplied to the gate of controlled rectifier SCR₂. With controlled rectifier SCR₂ conducting, the commutating capacitor C₁ is charged through diode D₃, the lower plate of capacitor C₁ as seen in FIG. 1, again being negatively charged. The turn-off of controlled rectifier SCR₂ is accomplished in the same manner as the turn-off of controlled rectifier SCR₁. Firing circuit 22 triggers controlled rectifier SCR₃ which connects the negatively charged plate of the commutating capacitor C₁ in circuit with the anode of controlled rectifier SCR₂ and also connects the capacitor C₁ in parallel circuit with inductor L₁. Thus, a negative pulse is developed across the inductor L₁ which results in a reverse bias being applied across controlled rectifier SCR₂ and it is turned off. Similarly, diode D₁ feeds back to the direct current source reactive power during the commutating interval, the amount of the feed-back being proportional to the inductive components of the load.

It will be seen that as the firing circuit 12 applies positive trigger pulses alternately to the gates of the controlled rectifiers SCR₁, SCR₂, the current from the direct current supply will flow alternately through the opposite ends of the primary winding P of the transformer T₁ and generate an alternating current voltage across secondary winding S₁. According to the invention, regulation of the output across the secondary winding S₁ is achieved by turning off the conducting controlled rectifier in each half cycle to vary the pulse width of the inverter output.

From the foregoing description of the inverter circuit and its operation, it will be seen that the conduction time

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.