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(12) **United States Patent**  
**Aono**

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(54) **ADDRESS RESOLUTION UNIT AND  
ADDRESS RESOLUTION METHOD FOR A  
MULTIPROCESSOR SYSTEM**

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(73) Assignee: **NEC Corporation**, Tokyo (JP)

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(51) Int. Cl.<sup>7</sup> ..... **G06F 15/16**; G06F 15/173;  
G06F 12/10

(52) U.S. Cl. .... **712/11**; 712/14; 712/17;  
712/18; 712/30; 712/244; 711/210; 711/206;  
709/248; 709/249

(58) Field of Search ..... 709/251.7, 252,  
709/314, 313, 215, 219, 230, 213, 249,  
238, 216; 711/145, 144, 214, 163, 221,  
216, 210, 206; 714/12, 27; 712/10, 12,  
13, 14, 15, 16, 17, 23, 28, 29, 36, 11, 20,  
18, 30, 31; 710/40, 39, 129, 200, 240, 220,  
244, 23

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Japanese Office Action dated Oct. 31, 2000 with partial translation.

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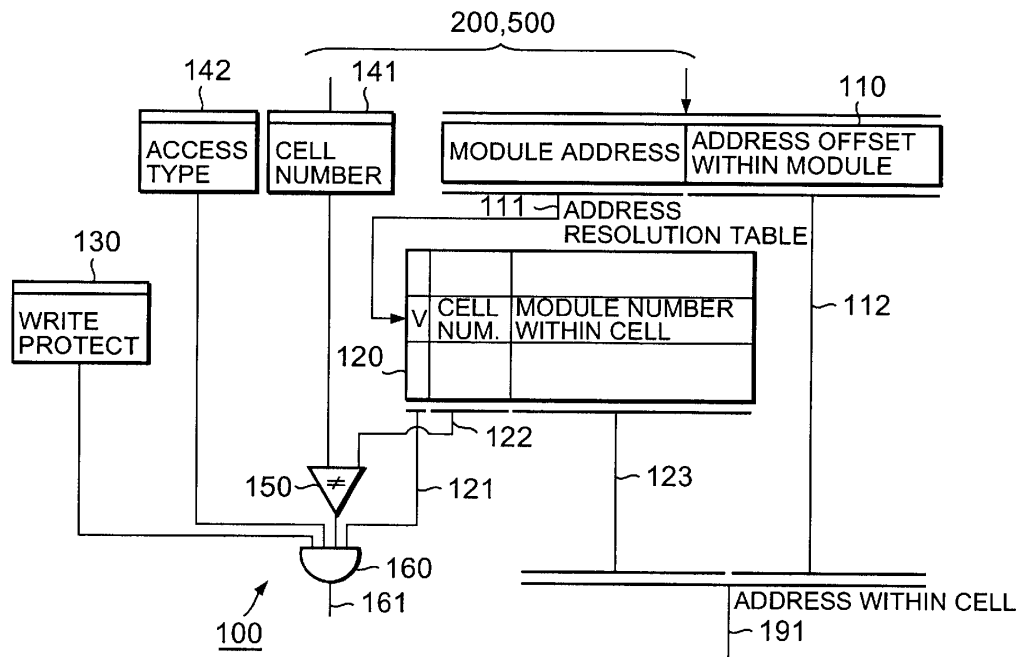
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(57) **ABSTRACT**

The present invention provides an address resolution method for use in a multiprocessor system with distributed shared memory. The method allows users to change a memory configuration and a system configuration to increase system operation flexibility and to isolate errors. A cell controller indexes into an address resolution table using the high-order part of a processor-specified address. A write protection flag specifies whether to permit write access from other cells. An attempt to write-access a cell inhibited for write access causes a logical circuit to output an access exception signal.

**9 Claims, 11 Drawing Sheets**



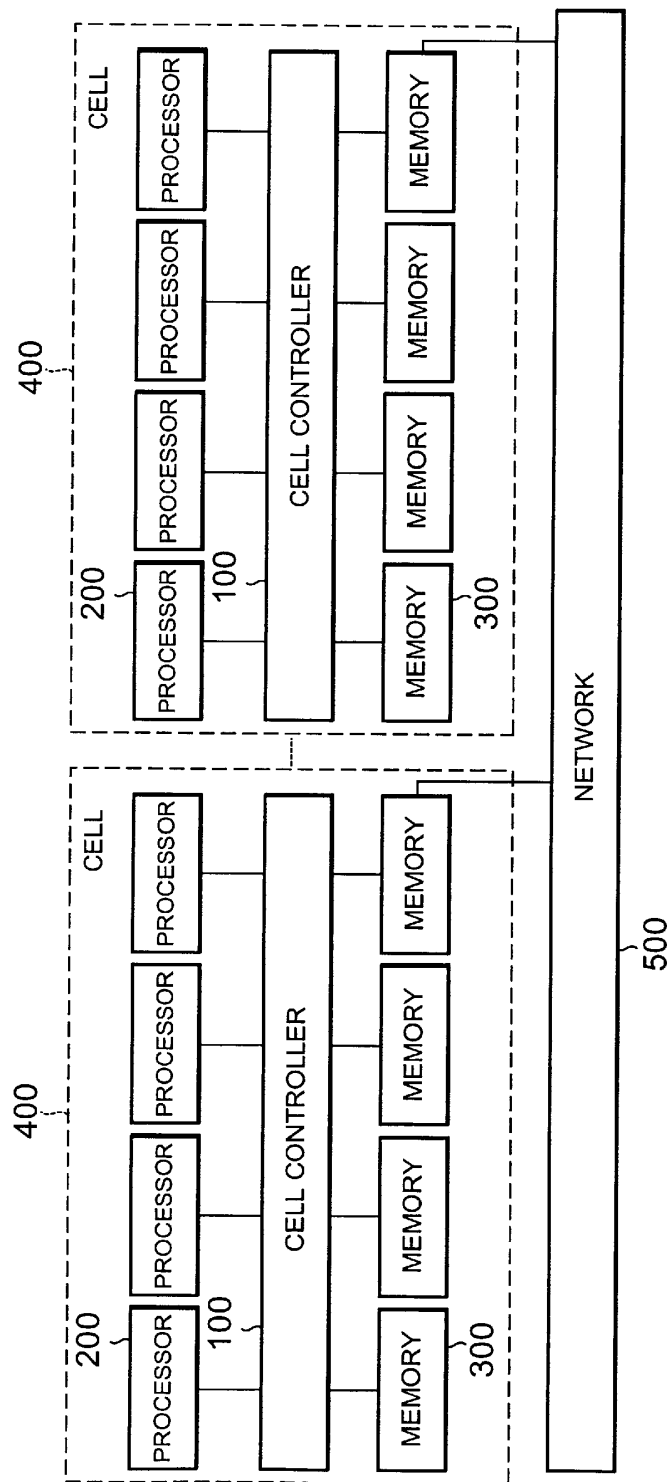


FIG. 1

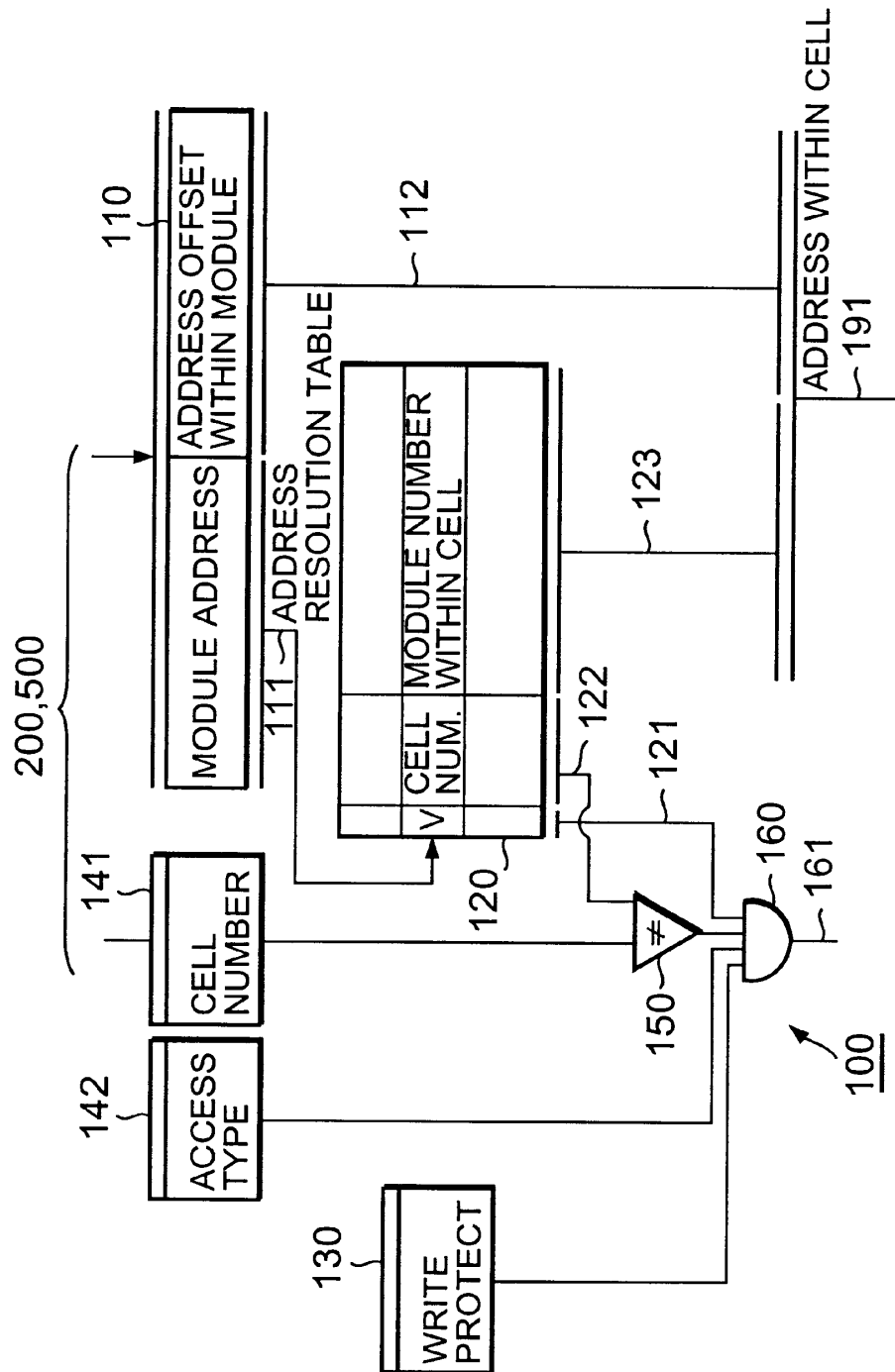


FIG. 2

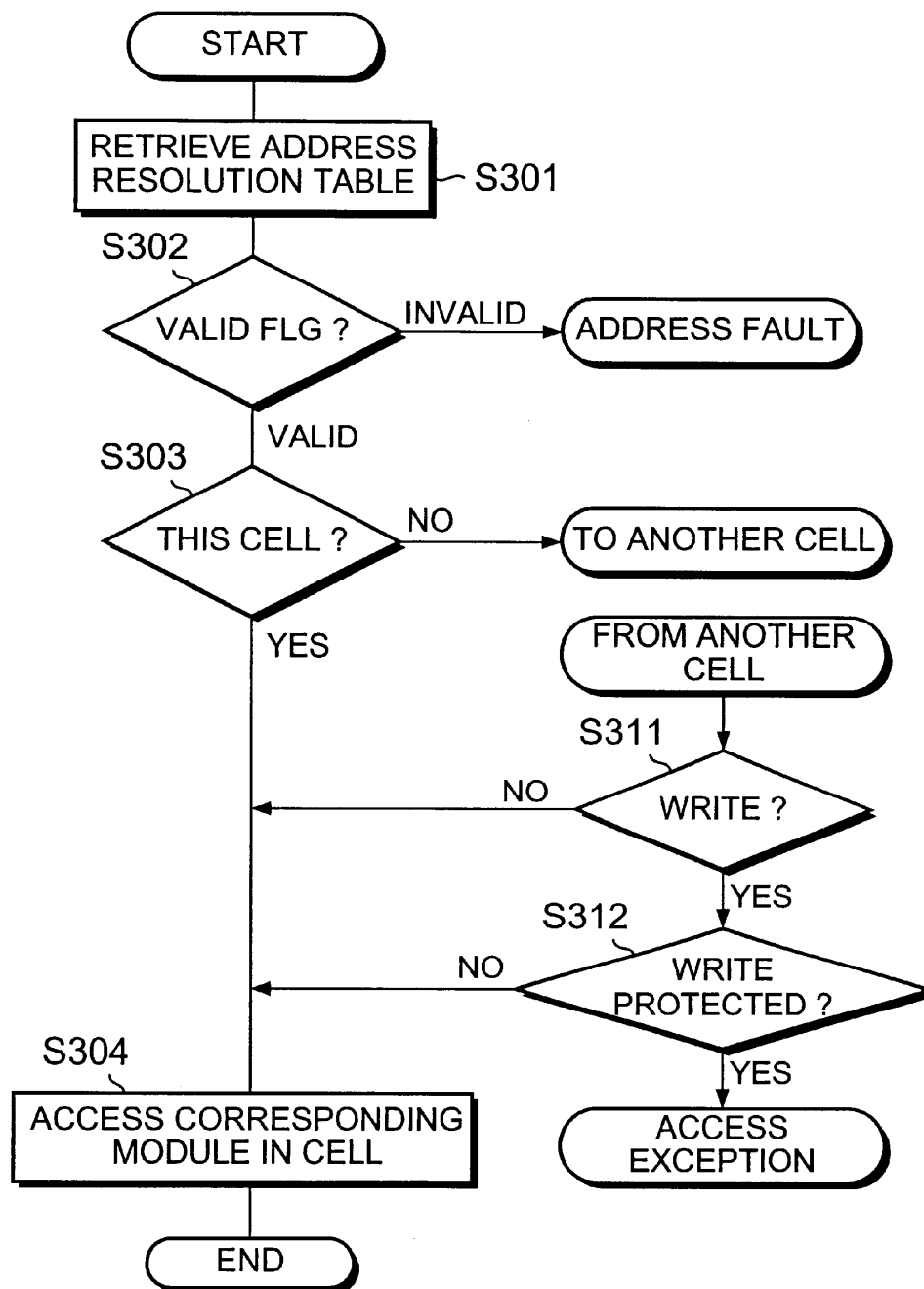


FIG. 3

0	1	0	0
1	1	0	1
2	1	0	2
3	1	0	3
4	1	1	3
5	1	2	3
6	1	3	3
7	0	-	-
8	0	-	-
9	0	-	-
A	0	-	-
B	0	-	-
C	0	-	-
D	0	-	-
E	0	-	-
F	0	-	-

NODE#0

0	1	1	0
1	1	1	1
2	1	1	2
3	1	0	3
4	1	1	3
5	1	2	3
6	1	3	3
7	0	-	-
8	0	-	-
9	0	-	-
A	0	-	-
B	0	-	-
C	0	-	-
D	0	-	-
E	0	-	-
F	0	-	-

NODE#1

0	1	2	0
1	1	2	1
2	1	2	2
3	1	0	3
4	1	1	3
5	1	2	3
6	1	3	3
7	0	-	-
8	0	-	-
9	0	-	-
A	0	-	-
B	0	-	-
C	0	-	-
D	0	-	-
E	0	-	-
F	0	-	-

NODE#2

0	1	3	0
1	1	3	1
2	1	3	2
3	1	0	3
4	1	1	3
5	1	2	3
6	1	3	3
7	0	-	-
8	0	-	-
9	0	-	-
A	0	-	-
B	0	-	-
C	0	-	-
D	0	-	-
E	0	-	-
F	0	-	-

NODE#3

FIG. 4

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