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Ma

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(54) **PREVENTION OF METASTABILITY IN BISTABLE CIRCUITS**

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(58) **Field of Search** 326/94; 327/155, 327/218; 370/298; 710/58; 375/354, 355, 357

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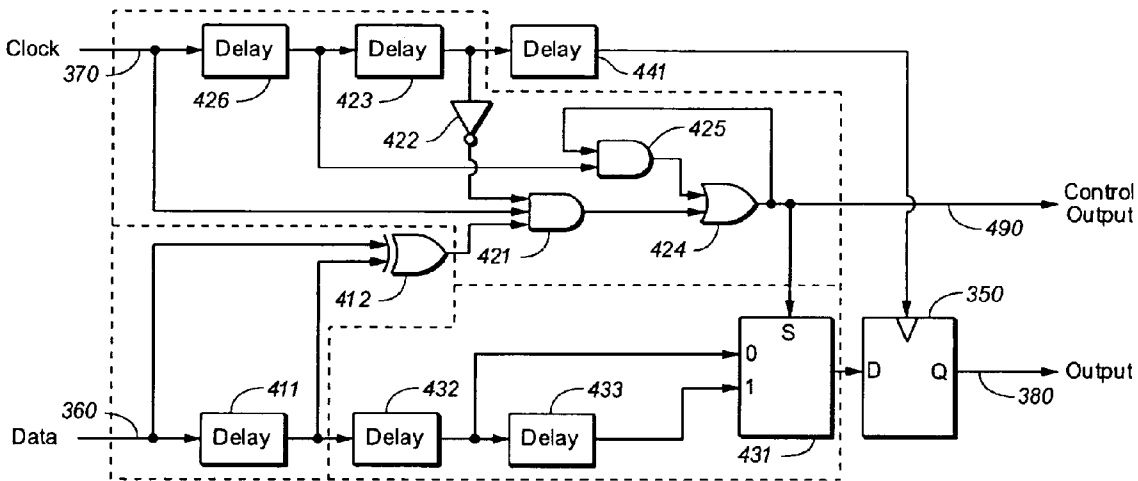
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(57) **ABSTRACT**

Methods and apparatus implementing techniques for prevention of metastability in a bistable circuit. The techniques include detecting a change in a data signal, sampling the detected change in reference to a sampling window of a clock signal input of a bistable circuit to determine if the detected change occurs within the sampling window, and selecting a stable data input to present to an input of the bistable circuit based on whether the detected change occurs within the sampling window. The sampling window represents a time period during which a change in the data signal can cause metastability in a bistable circuit.
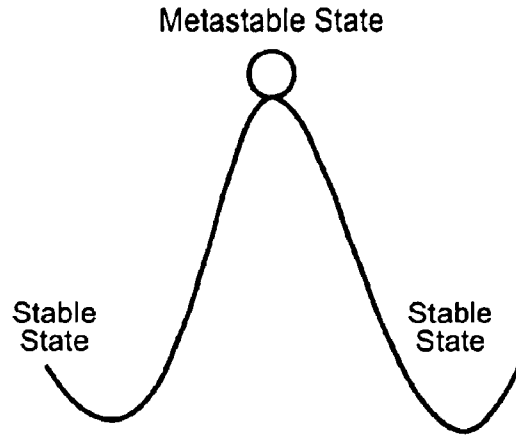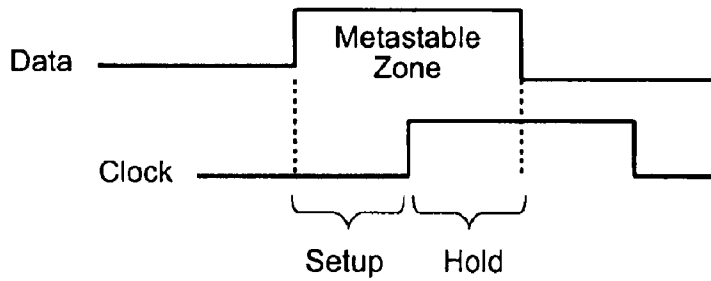
24 Claims, 5 Drawing Sheets

Metastable State

Stable State   Stable State

FIG._1

Data

Metastable Zone

Clock

Setup   Hold

Metastable Zone for positive clock edge Flip Flop

FIG._2

Clock ——— 370

Data Input

360

Transition Detect — 310

Sample & Hold

320

Clock Delay

340

Data Selection

330

D Flip Flop Q

350

Output

380

FIG._3

Clock

370

Delay
426

Delay
423

Delay
441

422

425

490

Control
Output

424

421

412

411

432

433

350

431

Data

360

Delay

Delay

Delay

S

0

1

D   Q

Output

380

FIG._4

Name	59.199ns	60.319ns	61.439ns	62.559ns	63.679ns
Input					
Input_Delay					
Change_Detected					
Clock					
Clock_Invert					
Bad_News					
Select_Alternate					
Sample_Clock					
Hold_News					

FIG._5

Name	70.159ns	72.399ns	74.639ns	76.879ns	79.119ns
Select_Alternate					
Input_Delay1					
Input_Delay2					
FF_Input					
Output					
FF_Clock					

FIG._6

Clock

370

Delay

723

Delay

741

Control
Output

490

421

424

412

S

0

1

350

D   Q

380

Output

Qn

431
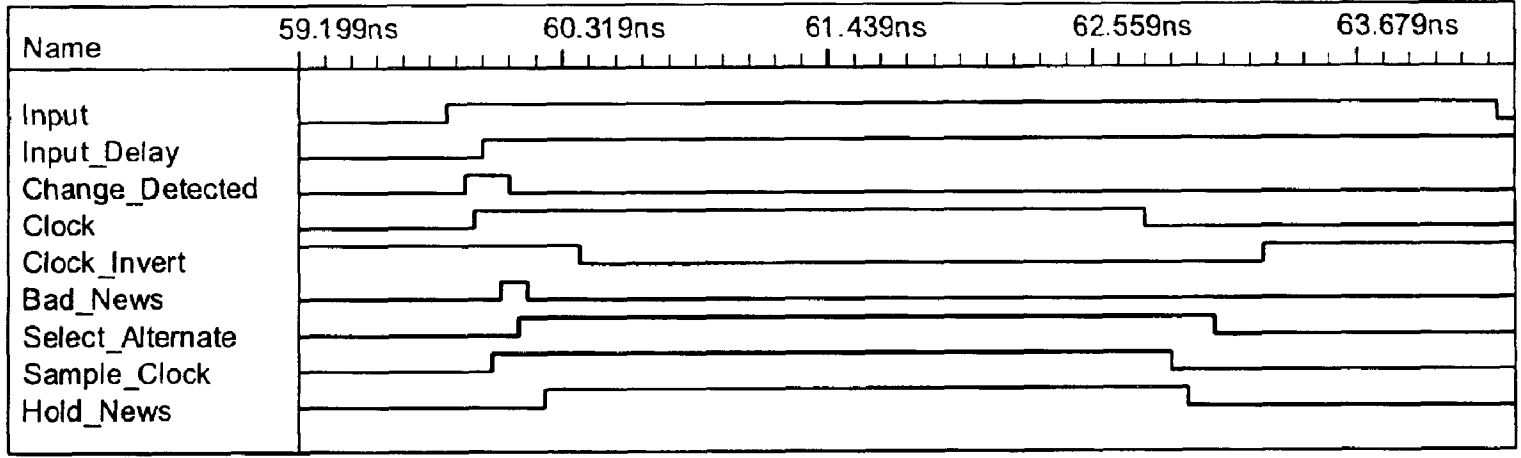
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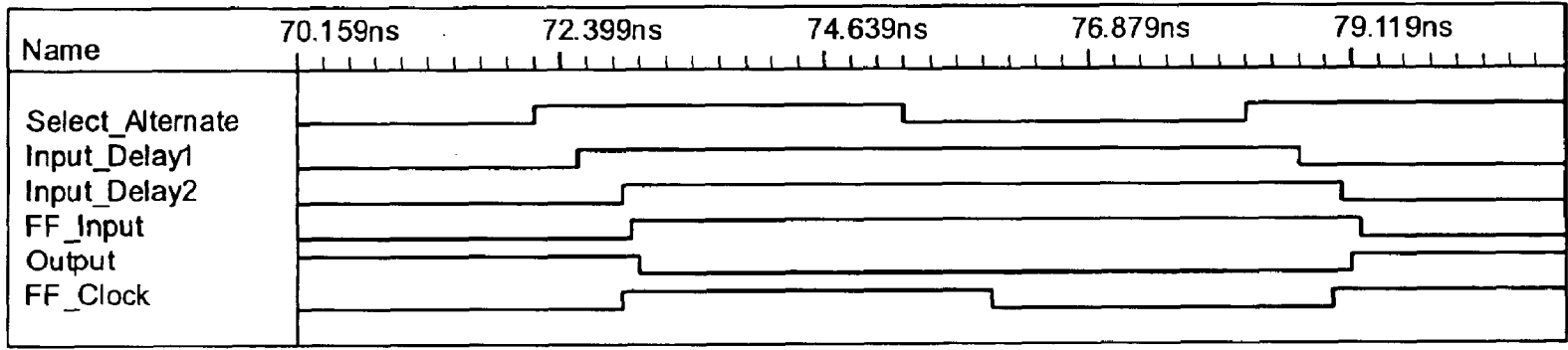Data

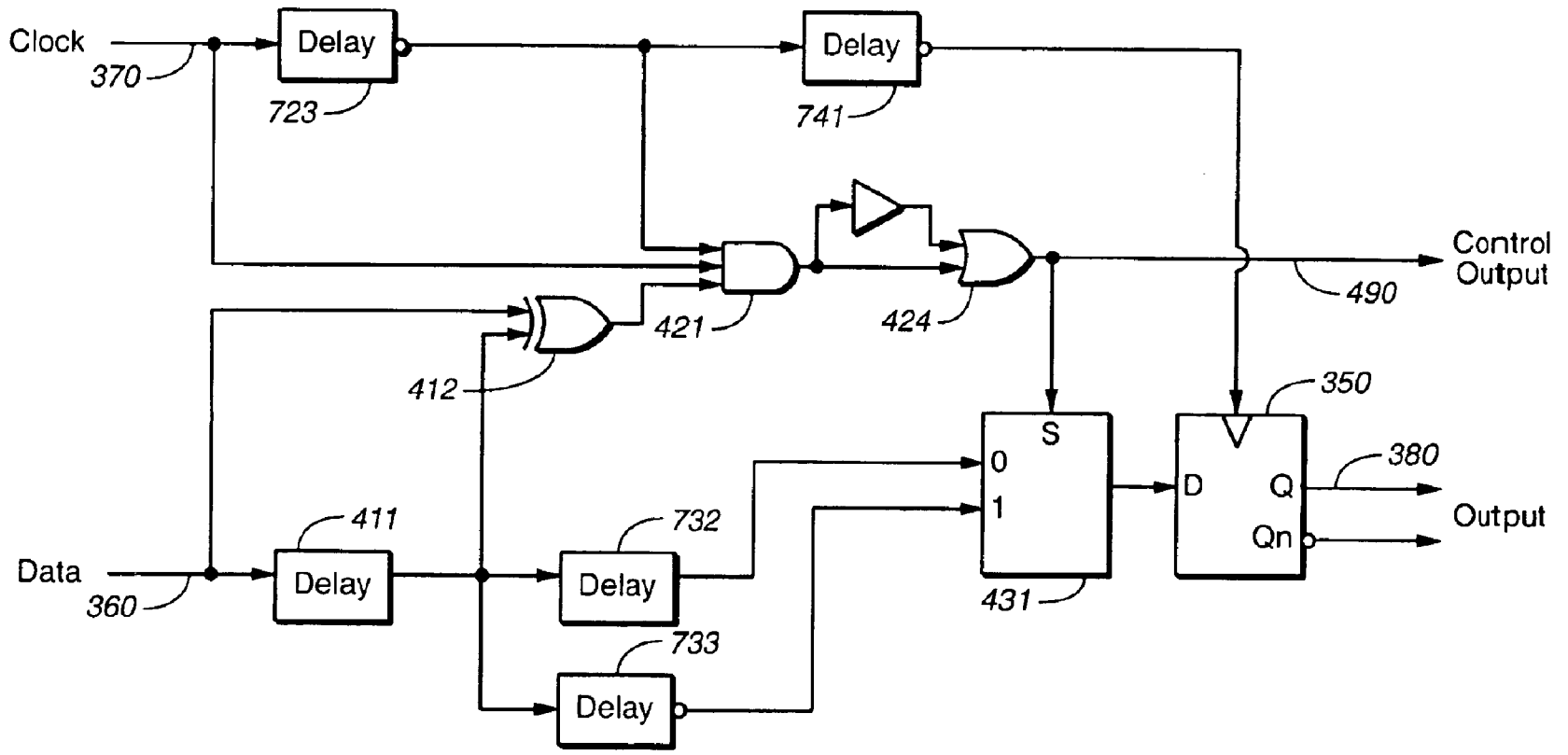360

Delay

732

Delay

733

Delay

FIG._7

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