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(54) **LOAD REDUCED MEMORY MODULE**

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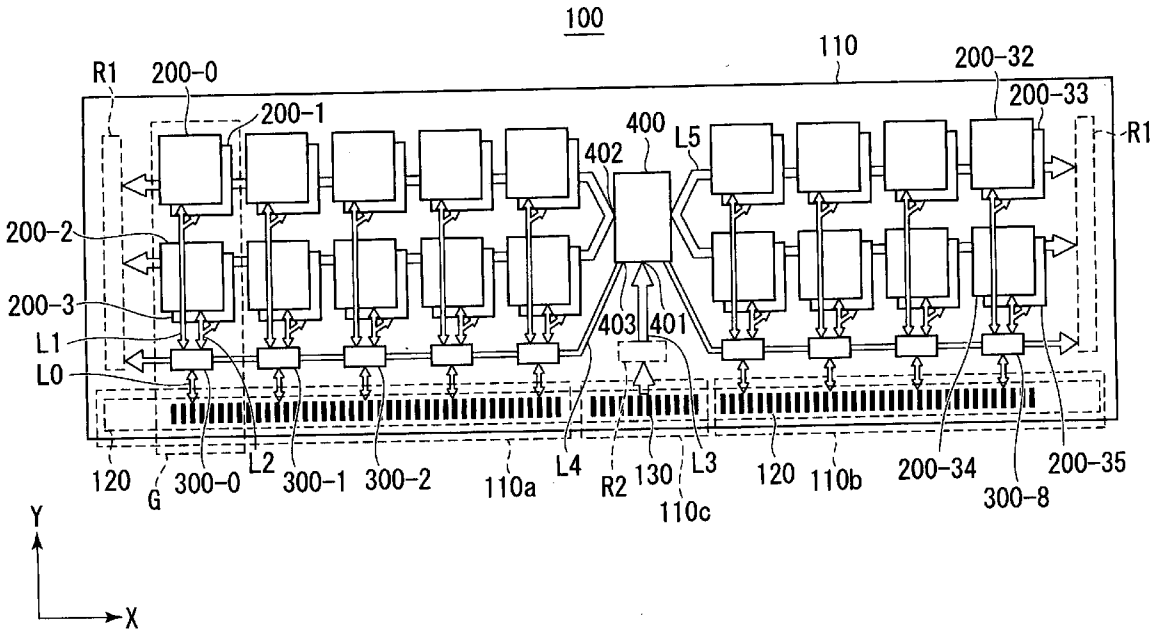
(57) **ABSTRACT**

A memory module includes a plurality of memory chips and a plurality of data register buffers mounted on the module substrate. At least two memory chips are allocated to each of the data register buffers. Each of the data register buffers includes M input/output terminals (M is a positive integer equal to or larger than 1) that are connected to the data connectors via a first data line and N input/output terminals (N is a positive integer equal to or larger than 2M) that are connected to corresponding memory chips via second and third data lines, so that the number of the second and third data lines is N/M times the number of the first data lines. According to the present invention, because the load capacities of the second and third data lines are reduced by a considerable amount, it is possible to realize a considerably high data transfer rate.



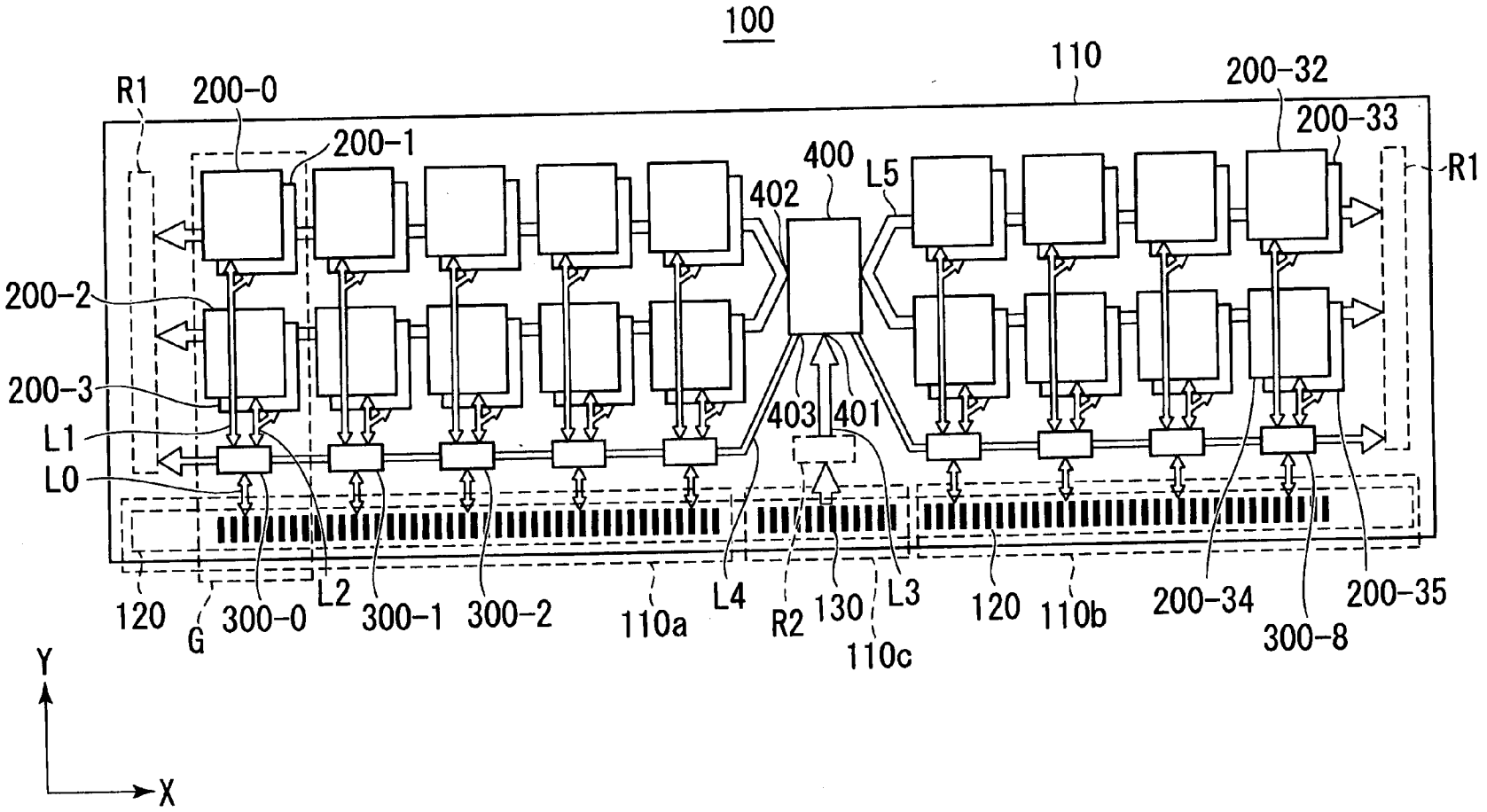


FIG.1

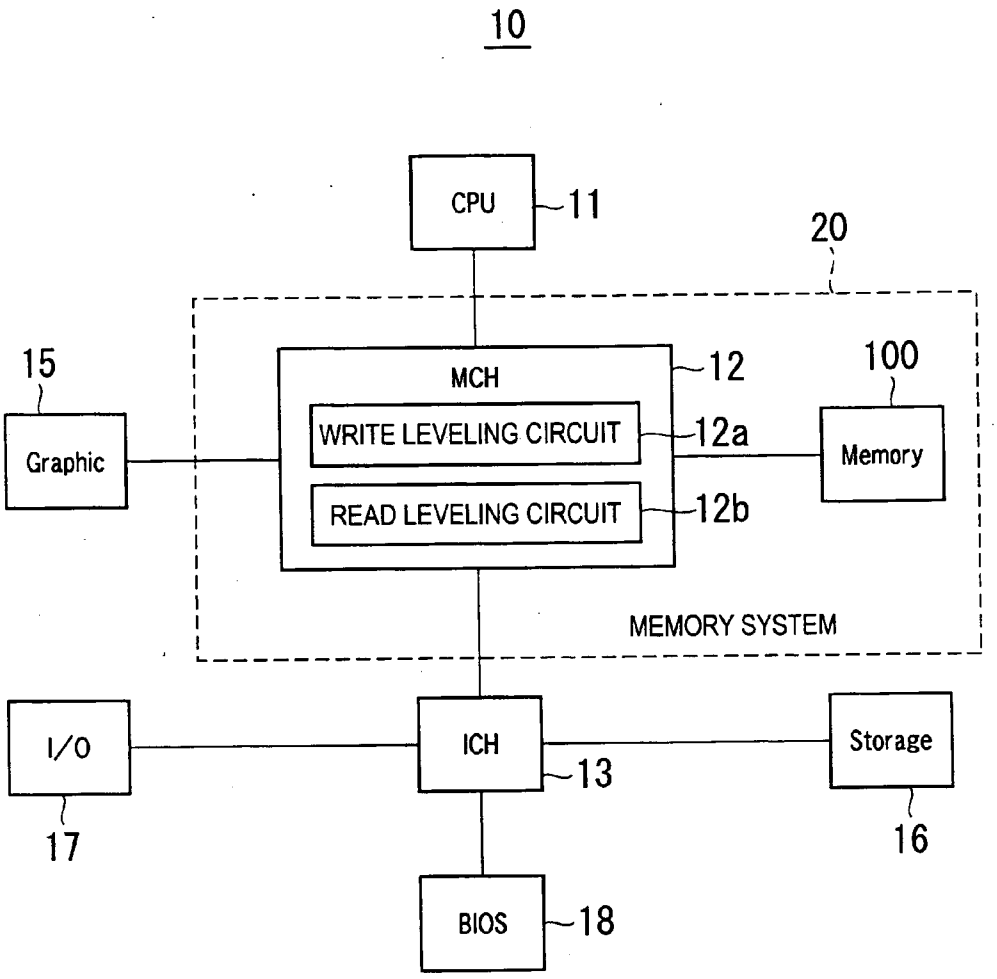


FIG.2

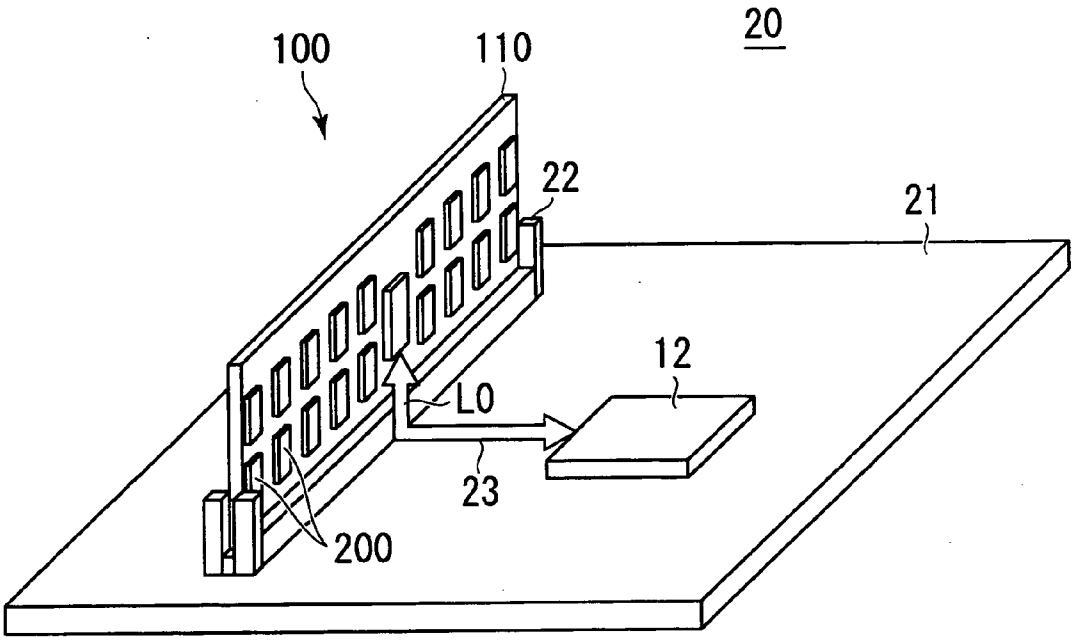


FIG.3

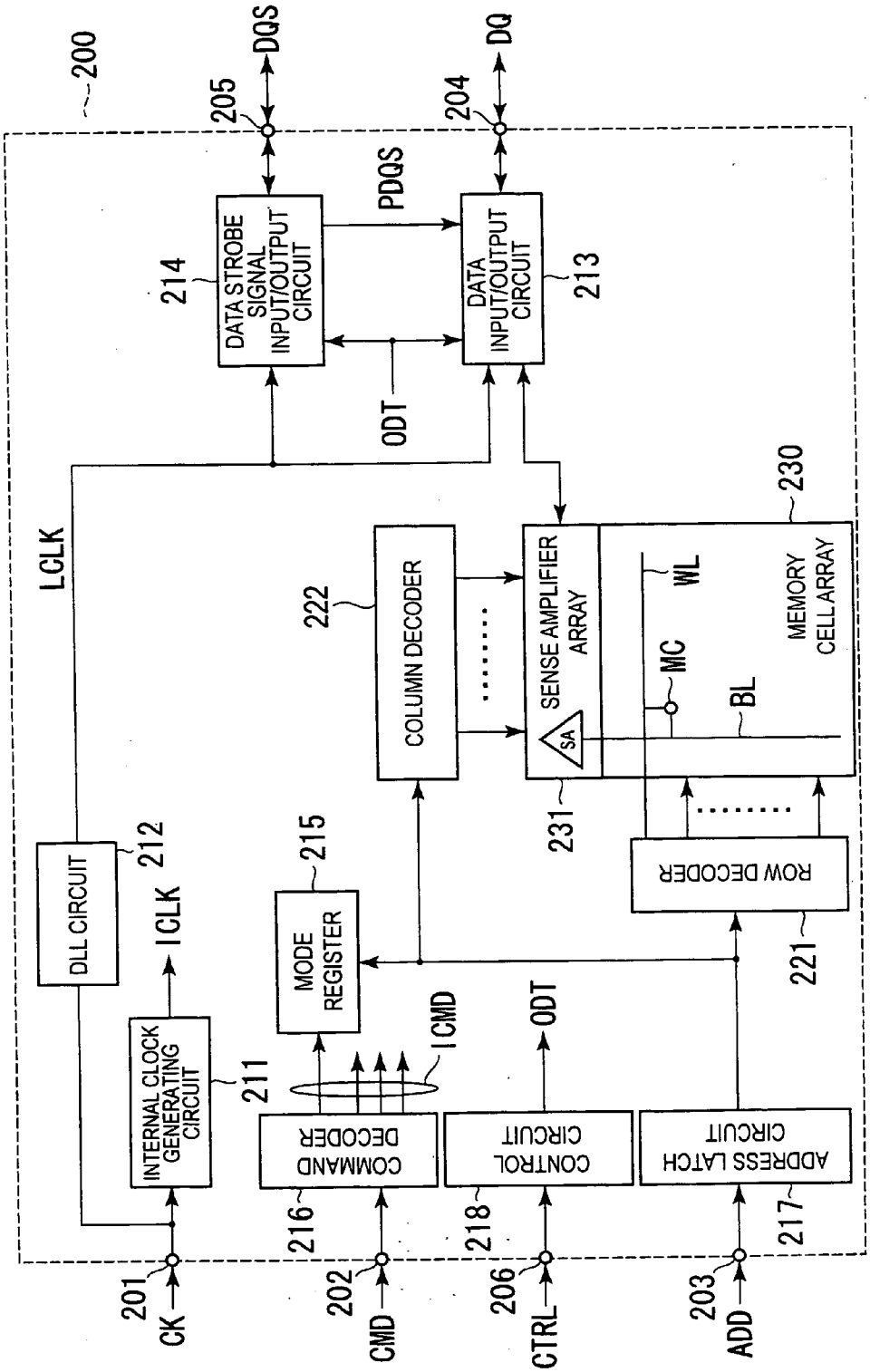


FIG.4

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