Robert G. Wedig, Ph.D.

April 2023

Education

B.E.E.   Electrical Engineering, University of Dayton, 1977.

M. S.   Electrical Engineering, University of Southern California, 1979.

Ph.D.   Electrical Engineering, Stanford University, 1982.

Professional Experience

1/86 - present Independent Consultant. Wedig Consulting, Inc. Sunnyvale, Ca.

8/82 - 12/85   Assistant Professor of Electrical and Computer Engineering. Carnegie-Mellon University, Pittsburgh, PA.

9/79 - 6/82   Research Assistant, Instructor, and Teaching Assistant. Computer Systems Laboratory, Stanford University, Stanford, Ca.

4/77 - 9/79   Processor Design Engineer. Hughes Aircraft Company, Fullerton, Ca.

9/74 - 4/77   Application Programmer. University of Dayton, Dayton, Ohio.

Awards

1983 - 1985   IBM Faculty Development Award.

1980 - 1982   IBM Predoctoral Fellowship.

1977 -1979   Hughes Aircraft Masters Fellowship.

Professional Societies
Tau Beta Pi, IEEE, ACM

Invited Presentations

"The Directly Interfaceable Parallel I/O Chip", Professional Seminar, Xerox Palo Alto Research Center, April 1981.

"Advances in Computer Architecture", Program for Technical Managers, Carnegie-Mellon University, April 1983.

"The GaAs Realization of a Production System Machine", Hawaii International Conference on System Sciences, January 1986.

"GaAs Computer Architectures", NCR Corporation, April 1986.

"Software and Hardware Techniques for Stack Management", Hawaii International Conference on System Sciences, January 1987.

"A Performance Analysis of Automatically Managed Top of Stack Buffers", NCR Corporation, June 1987.

"Concurrency in Single Chip Processors", NCR Corporation, September 1987.

Professional Activities

• Session Leader of GaAs Processor Session, Hawaii International Conference on System Sciences, January 1986.

• Minitrack Chairman of Hardware Track, Hawaii International Conference on System Sciences, January 1988.

• Committee Member, Asilomar Microcomputer Workshop, 1986 – 2012.

• Program Chairman, Asilomar Microcomputer Workshop, 1998.

• Committee Member, HOT Interconnects Symposium, 2000 – 2001.

Publications

1. Wedig, R. G., "Dynamic Detection of Concurrency in DO-Loops Using Ordering Matrices", Technical Report 209, Stanford University, May 1981.

2. Wedig, R. G., A "Phenomenal" Chip for Toy Design, *VLSI Design*, Vol. 2, No. 3, 1981, pp. 51-52

3. Wedig, R. G., "Dynamic Detection of Concurrency in DEL Instruction Streams", Technical Report 231, Stanford University, February 1982.

4. *Detection of Concurrency in Directly Executed Language Instruction Streams*, Ph.D. dissertation, Stanford University, June 1982.

5. Wedig, R. G. and Flynn, M. J., "Concurrency Detection in Language-Oriented Processing Systems", *Proceedings of the 3rd International Conference on Distributed Computing Systems*, IEEE, October 1982, pp. 805-810.

6. With Flynn, M. J., Huck, J. C. and Wakefield, S. P., "Performance Evaluation of Execution Aspects of Computer Architectures", *Proceedings of the International Workshop on High Level Language Computer Architectures,* University of Maryland and the Office of Naval Research, December 1982.

7. Wedig, R. G., "The Detection of Concurrency Using Structured Control Flow", *Proceedings of the International Workshop on Computer Systems Organization*, IEEE Computer Society, March 1983, pp. 28-35.

8. Wedig, R. G., "A Language-Oriented Approach for Implementing Branches: Structured Control Flow", *Proceedings of the International Workshop on High-Level Computer Architecture,* University of Maryland, May 1984, pp. 3.1-3.7.

9. Wedig, R. G. and Rose, M. A., "The Reduction of Branch Instruction Execution Overhead Using Structured Control Flow", *Proceedings of the 11th Annual International Symposium on Computer Architecture,* IEEE Computer Society, June 1984, pp. 119-125

10. Wedig, R. G., "Using ISPS to Teach Computer Architecture", Proceedings of the National Educational Computing Conference, ACM, June 1984.

11. With Forgy, C., Gupta, A. and Newell, A., "Initial Assessment of Architectures for Production Systems", *Proceedings of the National Conference on Artificial Intelligence*, AAAI, August 1984.

12. Wedig, Robert G. and Lehr, Theodore F., "The GaAs Implementation of a Production System Machine", *The Proceedings of the 19th Annual Hawaii International Conference on System Sciences*, IEEE Computer Society, January 1986.

13. With Anoop Gupta and Charles Forgy, "Parallel Algorithms and Architectures for Rule-Based Systems", *Proceedings of the 13th Annual International Conference on Computer Architecture*, IEEE, June 1986.

14. With Augustus K. Uht, "Hardware Extraction of Low-Level Concurrency from Serial Instruction Streams", *Proceedings of the 15th Annual International Conference on Parallel Processing,* ACM, August 1986.

15. Wedig, Robert G., Software and Hardware Techniques for Stack Management, *The Proceedings of the 20th Annual Hawaii International Conference on System Sciences,* IEEE Computer Society, January 1987.

16. With Theodore F. Lehr, "The GaAs Implementation of a Production System Machine, *IEEE Computer*, April 1987.

17. With Timothy Stanley, "A Performance Analysis of Automatically Managed Top of Stack Buffers", *Proceedings of the 14th Annual International Conference on Computer Architecture*, IEEE, June 1987.

18. Wedig, R. G., *High Level Language Computer Architectures*, Elsevier Science, New York, NY, 1988, chapter 6.

Prior Expert Witness Work

Neutral Expert

1. Expert for Judge John Flaherty, Ret., Systems America, Inc. v. Rockwell Software, Inc., Judicial Arbitration and Mediation Services (JAMS), December, 2005.

2. Source Code Auditor, Niku Coporation v. Ameripay Payroll, Ltd., United States District Court, Northern District of California, December 2004.

3. Neutral Expert, ISS v. Blade Software, United States District Court, Northern District of Georgia, March 2003.

4. Expert for the Mediator, OneBox v. iHello.com Mediation, July 1999.

5. Expert to the Supreme Court of Singapore, Aztech Systems Ltd. v. Creative Laboratories Ltd., June, 1995.

6. Auditor for the Chips and Technologies v. Elite Microelectronics Settlement Agreement, June, 1990.

Courtroom Testimony

1. In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same, Expert for SK hynix Inc., International Trade Commission, Inv. No. 337-TA-1089, July 17, 2019.

2. In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same, Expert for SK hynix Inc., International Trade Commission, Inv. No. 337-TA-1023, May 10, 2017.

3. Mondis Technology, LTD. v. Hon Hai Precision Industry Co., LTD., Chimei Innolux Corp., and Innolux Corp., Expert for the Plaintiff, United States District Court, Eastern District of Texas, June 23, 2011.

4. Phillip M. Adams & Associates, LLC v. Dell, Inc., et. al., Expert for the Defendants, United States District Court, District of Utah, September, 2010

5. In the matter of Certain Electronic Devices Including Handheld, Wireless Communication Devices, Expert for Palm and Samsung Electronics Co., Ltd., International Trade Commission, October 28, 2009.

6. Renesas Technology Corp. and Renesas Technology America, Inc. v. the International Trade Commission, Expert for Samsung Electronics Co., Ltd., March, 2008.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.

fastcase
Smarter legal research.