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**PATENT NUMBER: 7,038,685**

**ISSUE DATE: May 2, 2006**

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**Miguel Tarver**  
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(12) **United States Patent**  
**Lindholm**

(10) **Patent No.:** **US 7,038,685 B1**  
(45) **Date of Patent:** **May 2, 2006**

(54) **PROGRAMMABLE GRAPHICS PROCESSOR FOR MULTITHREADED EXECUTION OF PROGRAMS**

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(73) Assignee: **NVIDIA Corporation**, Santa Clara, CA (US)

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 134 days.

(21) Appl. No.: **10/609,967**

(22) Filed: **Jun. 30, 2003**

(51) **Int. Cl.**  
**G06F 15/00** (2006.01)  
**G06F 13/00** (2006.01)  
**G06F 12/02** (2006.01)  
**G06F 9/46** (2006.01)  
**G06T 1/00** (2006.01)

(52) **U.S. Cl.** ..... **345/501**; 345/543; 345/536; 718/104

(58) **Field of Classification Search** ..... 345/501, 345/502, 530, 531, 522, 418, 419, 426, 427, 345/543, 505, 536; 718/100, 104, 103  
See application file for complete search history.

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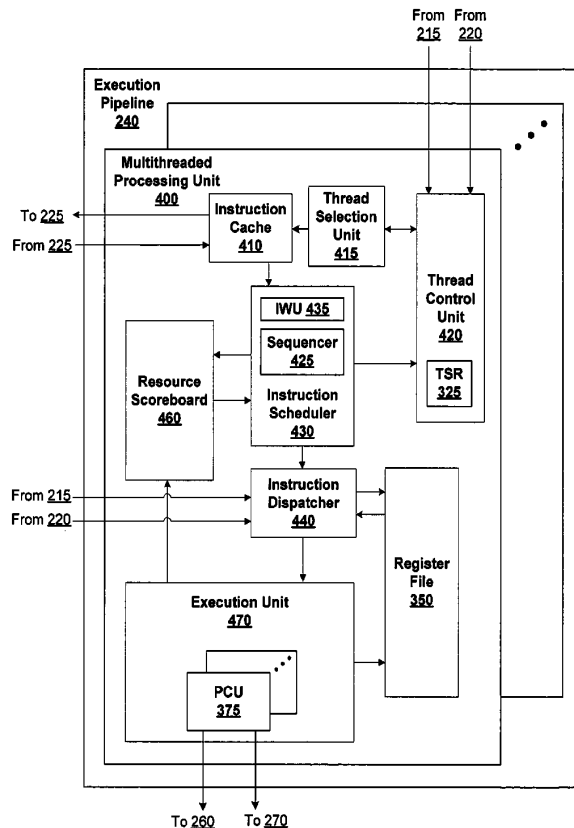
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(57) **ABSTRACT**

A programmable graphics processor for multithreaded execution of program instructions including a thread control unit. The programmable graphics processor is programmed with program instructions for processing primitive, pixel and vertex data. The thread control unit has a thread storage resource including locations allocated to store thread state data associated with samples of two or more types. Sample types include primitive, pixel and vertex. A number of threads allocated to processing a sample type may be dynamically modified.

**45 Claims, 9 Drawing Sheets**



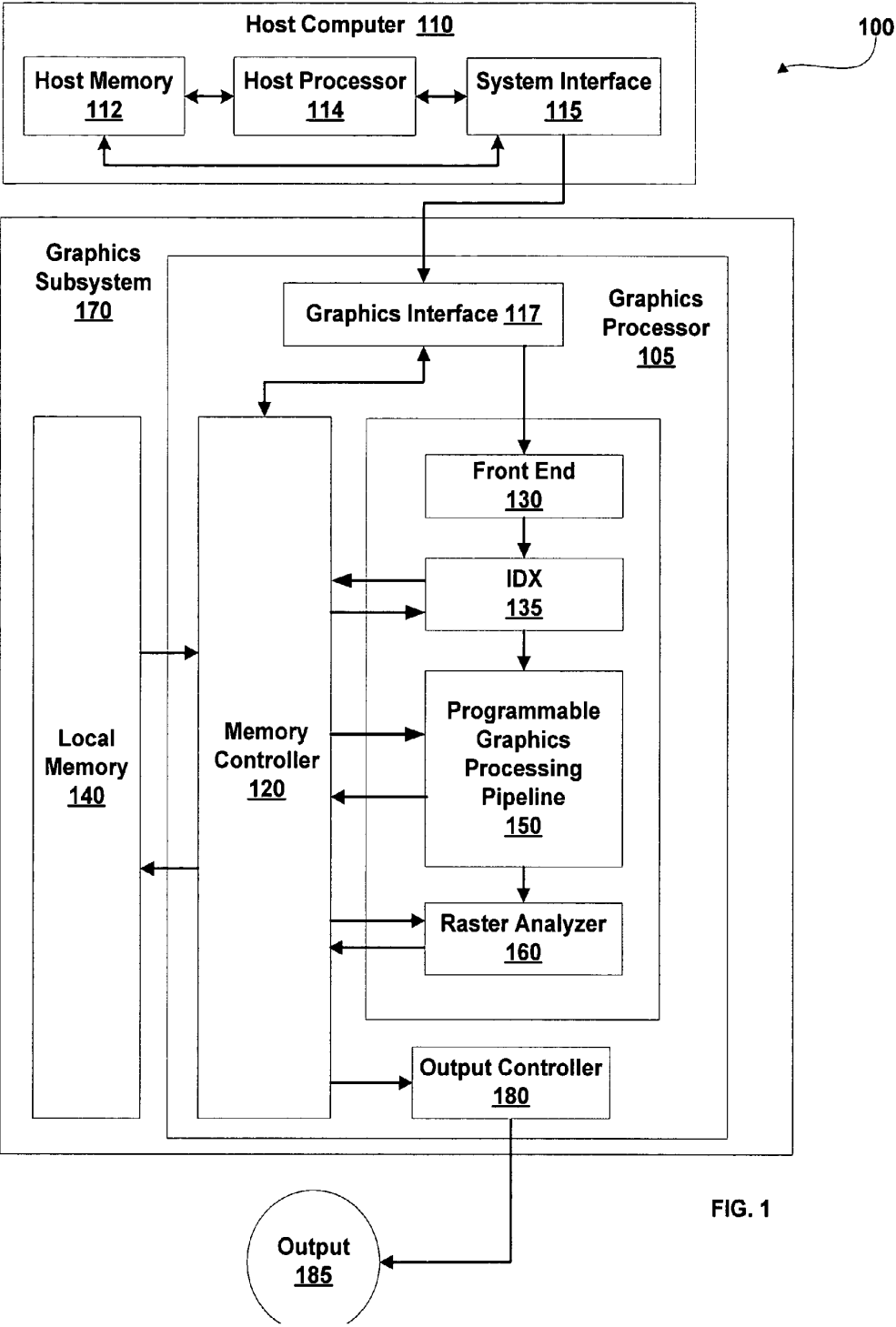


FIG. 1

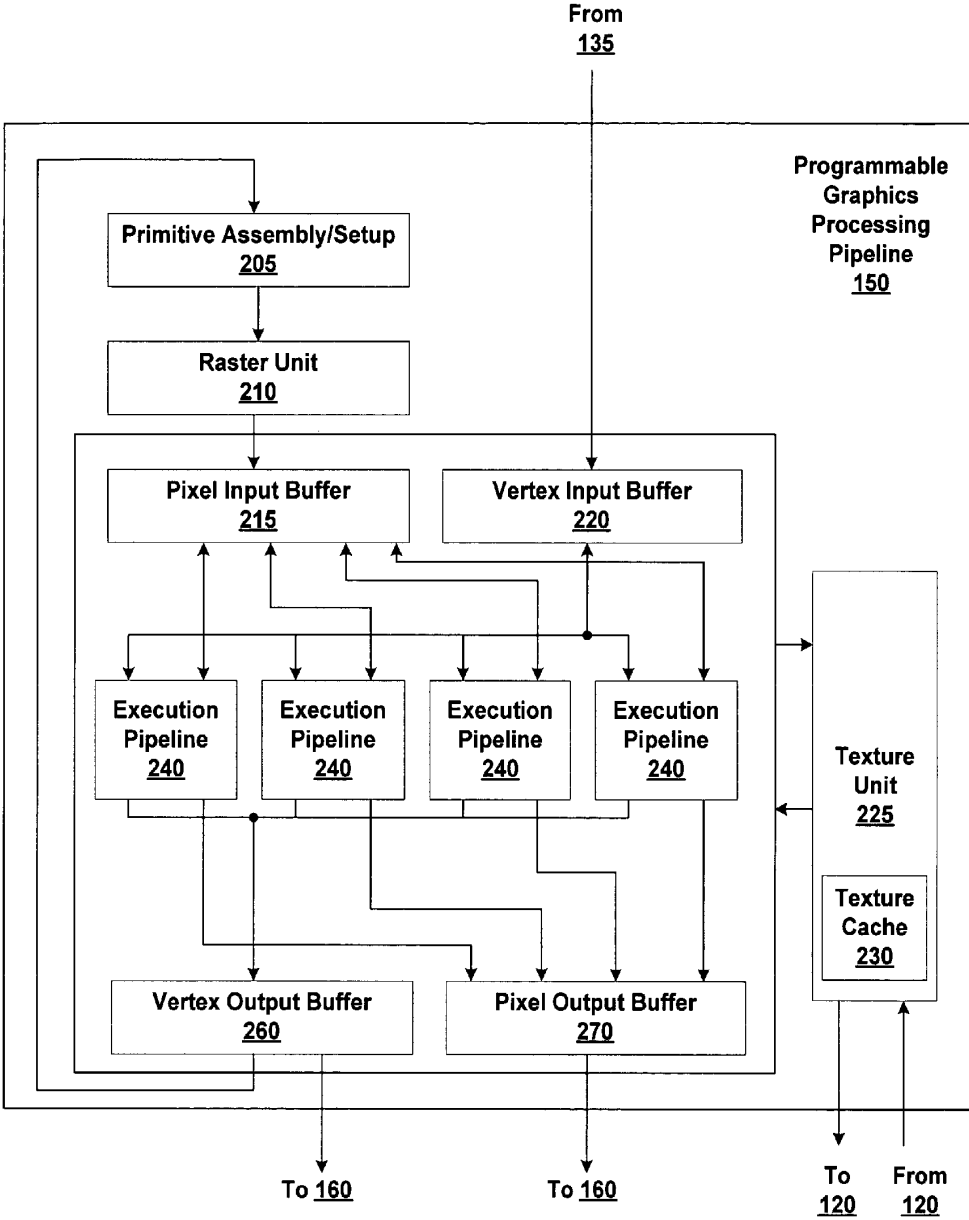


FIG. 2

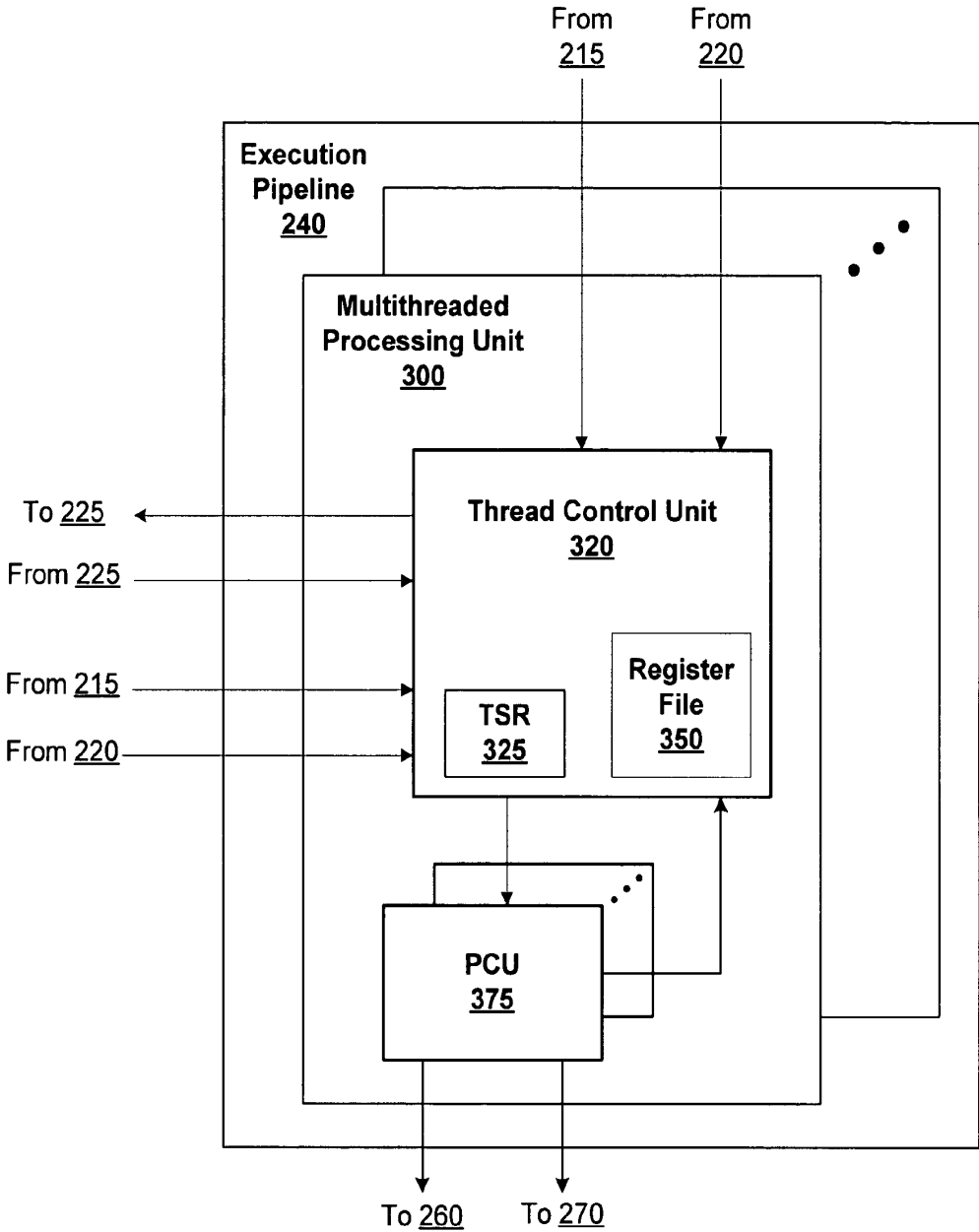


FIG. 3

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