US008892931B2

(12) **United States Patent**
Kruglick

(10) **Patent No.: US 8,892,931 B2**
(45) **Date of Patent: Nov. 18, 2014**

(54) **POWER CHANNEL MONITOR FOR A MULTICORE PROCESSOR**

(75) Inventor: **Ezekiel John Joseph Kruglick**, Poway, CA (US)

(73) Assignee: **Empire Technology Development LLC**, Wilmington, DE (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 260 days.

(21) Appl. No.: **12/582,301**

(22) Filed: **Oct. 20, 2009**

(65) **Prior Publication Data**

US 2011/0093733 A1 Apr. 21, 2011

(51) **Int. Cl.**
G06F 1/26 (2006.01)
G06F 1/32 (2006.01)

(52) **U.S. Cl.**
CPC ***G06F 1/3203*** (2013.01); ***G06F 1/3243*** (2013.01); *Y02B 60/1239* (2013.01)
USPC **713/340**; 713/300; 713/320; 714/22; 711/211; 711/E12.033

(58) **Field of Classification Search**
USPC 713/300, 320, 322, 323, 324, 340; 714/22; 711/211, E12.033
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,210,962	A	7/1980	Marsh et al.
4,916,659	A	4/1990	Persoon et al.
5,745,778	A	4/1998	Alfieri
5,806,059	A	9/1998	Tsuchida et al.
5,826,079	A	10/1998	Boland et al.
6,289,369	B1	9/2001	Sundaresan
6,567,806	B1	5/2003	Tsuchida et al.
6,658,448	B1	12/2003	Stefaniak et al.
6,745,336	B1	6/2004	Martonosi et al.
6,769,017	B1	7/2004	Bhat et al.
6,782,410	B1	8/2004	Bhagat et al.
7,143,412	B2	11/2006	Koenen
7,146,607	B2	12/2006	Nair et al.
7,363,523	B2	4/2008	Kurts et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	1 736 851	A2	12/2006
JP	H08315598	A	11/1996

(Continued)

OTHER PUBLICATIONS

Brooks et al., "Dynamic Thermal Management for High-Performance Microprocessors" Jan. 2001, Proceedings of the 7th International Symposium on High Performance Computer Architecture, 12 pages.

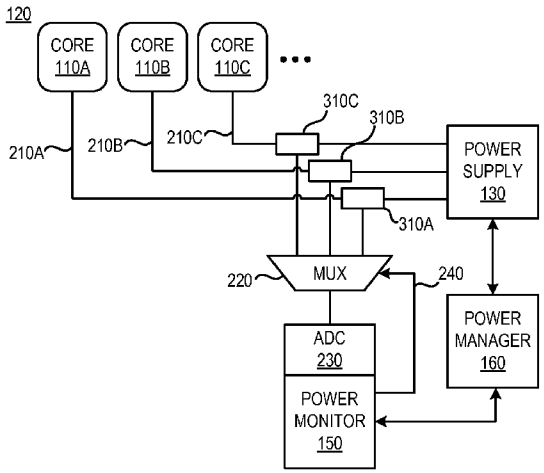
(Continued)

Primary Examiner — Michael J Brown
(74) *Attorney, Agent, or Firm* — Hope Baldauff, LLC

(57) **ABSTRACT**

Technologies are generally described for power channel monitoring in multicore processors. A power management system can be configured to monitor the power channels supplying individual cores within a multicore processor. A power channel monitor can provide a direct measurement of power consumption for each core. The power consumption of individual cores can indicate which cores are encountering higher or lower usage. The usage determination can be made without sending any data messages to, or from, the cores being measured. The determined usage load being serviced by each processor core may be used to adjust power and/or clock signals supplied to the cores.

19 Claims, 6 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

7,383,396	B2	6/2008	Wyman	
7,437,581	B2	10/2008	Grochowski et al.	
7,574,567	B2	8/2009	Wyman	
8,051,418	B1	11/2011	Dice	
8,078,832	B1	12/2011	Agarwal et al.	
8,108,843	B2	1/2012	Nair et al.	
8,181,169	B2	5/2012	Nakaike et al.	
8,214,817	B2	7/2012	Mendelson et al.	
8,443,341	B2	5/2013	Berg et al.	
2003/0171907	A1	9/2003	Gal-On et al.	
2003/0236919	A1	12/2003	Johnson et al.	
2004/0181730	A1*	9/2004	Monfared et al.	714/745
2005/0154861	A1	7/2005	Arimilli et al.	
2005/0210472	A1	9/2005	Accapadi et al.	
2005/0246461	A1	11/2005	Accapadi et al.	
2006/0041599	A1	2/2006	Tsuchida et al.	
2006/0225074	A1	10/2006	Vaid et al.	
2006/0259800	A1	11/2006	Maejima	
2007/0027972	A1	2/2007	Agrawal et al.	
2007/0044084	A1	2/2007	Wang et al.	
2007/0079308	A1	4/2007	Chiaramonte et al.	
2007/0124457	A1	5/2007	May et al.	
2008/0046895	A1	2/2008	Dillenberger et al.	
2008/0126751	A1	5/2008	Mizrachi et al.	
2008/0178183	A1	7/2008	Accapadi et al.	
2008/0181283	A1*	7/2008	Elhanati et al.	375/130
2008/0229127	A1*	9/2008	Felter et al.	713/320
2009/0031317	A1	1/2009	Gopalan et al.	
2009/0031318	A1	1/2009	Gopalan et al.	
2009/0070553	A1	3/2009	Wallach et al.	
2009/0077562	A1	3/2009	Sen et al.	
2009/0125894	A1	5/2009	Nair et al.	
2009/0126006	A1	5/2009	Zhang et al.	
2009/0187915	A1	7/2009	Chew et al.	
2010/0017804	A1	1/2010	Gupta et al.	
2010/0122101	A1*	5/2010	Naffziger et al.	713/340
2010/0191854	A1	7/2010	Isci et al.	
2010/0225496	A1*	9/2010	Hou et al.	340/636.1
2011/0004692	A1	1/2011	Occhino et al.	
2011/0088021	A1	4/2011	Kruglick	
2011/0088022	A1	4/2011	Kruglick	
2011/0088038	A1	4/2011	Kruglick	
2011/0088041	A1	4/2011	Alameldeen et al.	
2011/0302585	A1	12/2011	Dice	

FOREIGN PATENT DOCUMENTS

JP	2005085164	A	3/2005
JP	2006318380	A	11/2006
JP	2008513912	A	5/2008
JP	2008306522		12/2008

OTHER PUBLICATIONS

Donald et al., "Techniques for Multicore Thermal Management: Classification and New Exploration". Jun. 2006, Proceedings of the 33rd Annual International Symposium on Computer Architecture, pp. 78-88.

Kang et al., "Preliminary Study toward Intelligent Run-time Resource Management Techniques for Large Multi-Core Architectures," Apr. 15, 2008, University of Southern California—Information Sciences Institute, 2 pages.

Shirako et al., "Compiler Control Power Saving Scheme for Multi Core Processors" In *Lecture Notes in Computer Science: Languages and Compilers for Parallel Computing*. vol. 4339/2006. Springer-Verlag, Berlin, pp. 362-376, 2007.

International Search Report dated Feb. 3, 2011 in International Application No. PCT/US2010/053110.

"P6T New Era for Ultimate Performance! Intel® Core™ i7 Platform," accessed at http://www.asus.com/Motherboards/Intel_Socket_1366/P6T/, accessed on Mar. 5, 2012, pp. 4.

U.S. Office Action dated Jan. 31, 2012 in U.S. Appl. No. 12/578,321.

U.S. Office Action dated Jul. 5, 2012 in U.S. Appl. No. 12/578,321.

U.S. Office Action dated Jun. 6, 2012 in U.S. Appl. No. 12/578,295.

U.S. Office Action dated Jun. 21, 2012 in U.S. Appl. No. 12/578,336.

Albonesi, D., "Selective Cache Ways: On-Demand Cache Resource Allocation," Nov. 1999, Proceedings of the International Symposium on Microarchitecture, 12 pages.

Bala, et al., "Dynamo: A Transparent Dynamic Optimization System," Jun. 2000, Proceedings of Programming Language Design and Implementation, 12 pages.

Baraz, et al., "IA_32 Execution Layer: A Two-Phase Dynamic Translator Designed to Support IA-32 Application on Itanium®-based Systems," Dec. 2003, Proceedings of the 36th International Symposium on Microarchitecture, 11 pages.

Dehnert, et al., "The Transmeta Code Morphing™ Software: Using Speculation, Recovery, and Adaptive Retranslation to Address Real-Life Challenges," 2003, ACM International Conference Proceedings Series, vol. 37, Proceedings of the International Symposium on Code Generation and Optimization: Feedback-directed and Runtime Optimization, Abstract, 9 pages.

Ebcioglu, et al., "DAISY: Dynamic Compilation for 100% Architectural Compatibility," 1997, Proceedings of the 24th International Symposium on Computer Architecture, 13 pages.

Song, et al., "Feedback-Directed Thread Scheduling with Memory Considerations," ACM, Jun. 2007, pp. 1-10.

Microsoft .NET Framework, http://www.microsoft.com/net/, accessed Oct. 13, 2009, 1 page.

Song, et al., "Analytical Modeling and Optimization for Affinity Based Tread Scheduling on Multicore Systems", Jul. 14, 2009, IEEE Cluster 2009, New Orleans, Louisiana, 10 pages.

Japanese Office Action dated Sep. 3, 2013.

U.S. Office Action dated Nov. 21, 2012 in U.S. Appl. No. 12/578,295.

U.S. Office Action dated Nov. 21, 2012 in U.S. Appl. No. 12/578,336.

U.S. Official Action dated Sep. 5, 2013 in U.S. Appl. No. 12/578,321.

U.S. Notice of Allowance dated Sep. 17, 2013 in U.S. Appl. No. 12/578,336.

Simon, CS 267: Applications of Parallel Computers Lecture 17: Parallel Sparse Matrix-Vector Multiplication; pp. 66; Oct. 22, 2002. http://www.cs.berkeley.edu/~strive/cs267.

Filch et al., On the Potential of NOC Virtualization for Multicore Chips; Scalable Computing: Practice and Experience; vol. 9, No. 3, pp. 165-177 http://www.scpe.org; 2008.

U.S. Official Action dated Jan. 28, 2014 in U.S. Appl. No. 12/578,321.

* cited by examiner

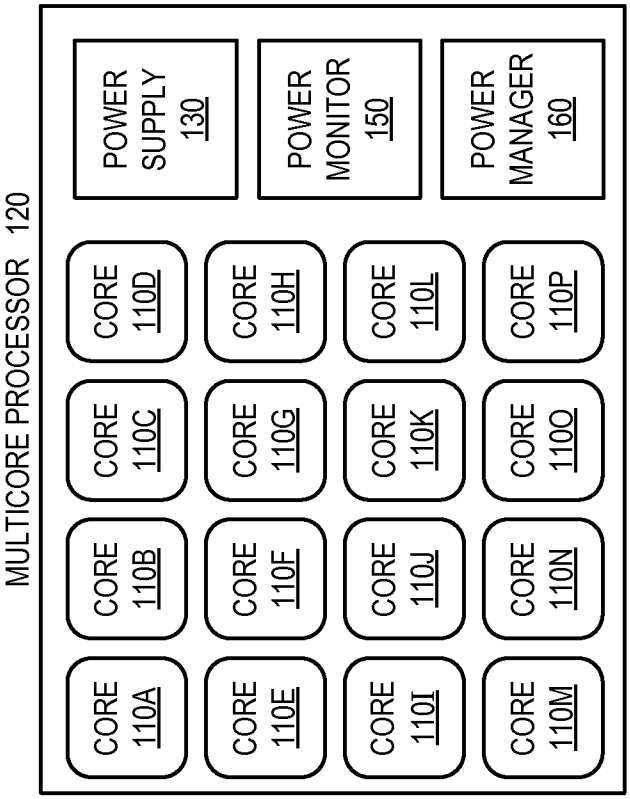


FIG. 1

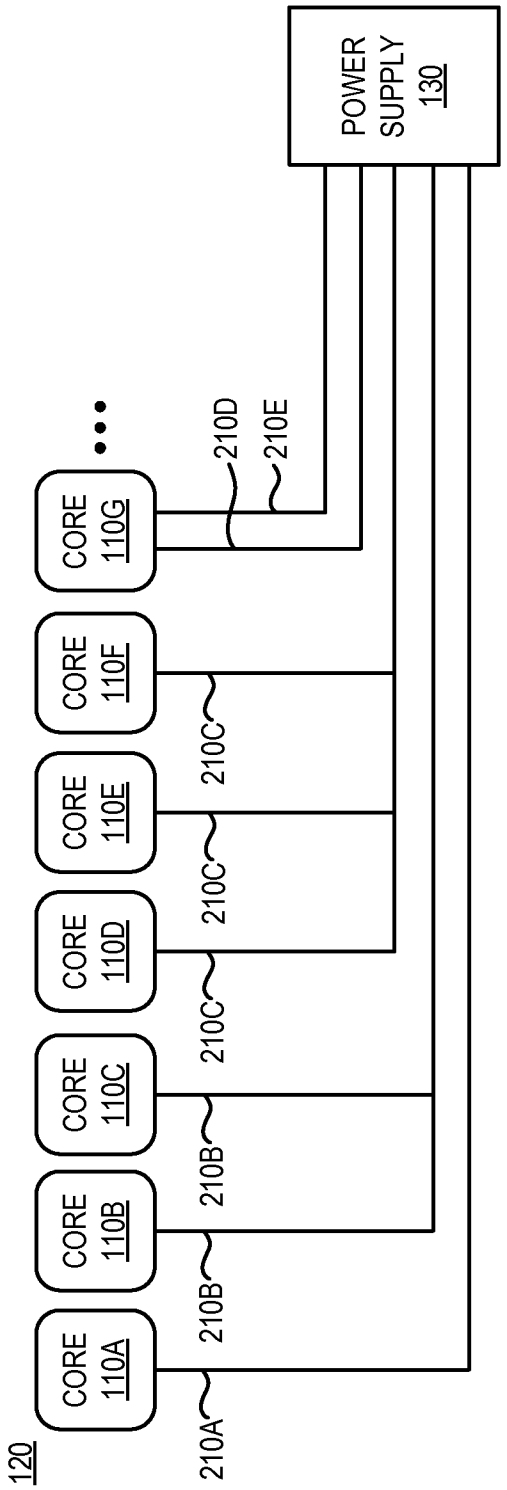


FIG. 2

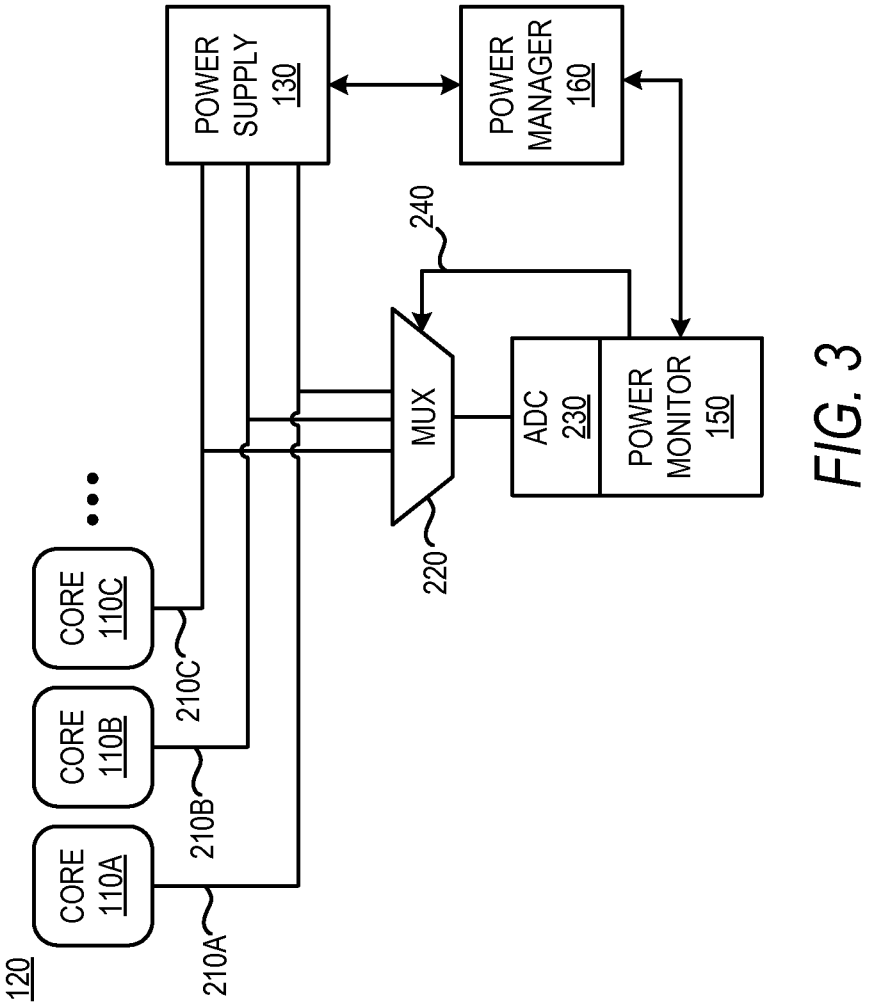


FIG. 3

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.