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Paper 10
Entered: February 13, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-01333
Patent 10,049,080 B2

Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and GREGG I. ANDERSON, *Administrative Patent Judges*.

GIANNETTI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314
Dismissing Contingent Motion for Joinder
35 U.S.C. § 315(c); 37 C.F.R. § 42.122

I. INTRODUCTION

A. Background

Mercedes-Benz USA, LLC ("Mercedes-Benz") filed a Petition requesting *inter partes* review of claims 1–24 (the "challenged claims") of U.S. Patent No. 10,049,080 B2 (Ex. 1001, the "'080 patent"). Paper 1 ("Pet."). The Petition was accompanied by a "Contingent Motion for Joinder" seeking joinder with IPR2023-00567 (the "'567 IPR"), a proceeding originally filed by Samsung and Qualcomm, involving a challenge to the same claims of the '080 patent as this proceeding. Paper 2. That proceeding has now been terminated. '567 IPR, Paper 22 (Termination Decision).

Daedalus Prime ("Patent Owner") has waived filing of a preliminary response. Paper 9. For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. *See* 35 U.S.C. § 314(a) (*inter partes* review may not be instituted unless "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.") We therefore institute *inter partes* review as to all of the challenged claims of the '080 patent and all of the asserted grounds of unpatentability. *See SAS Inst. Inc. v Iancu*, 138 S.Ct. 1348, 1356 (2018); 37 C.F.R. § 42.108 (a) ("When instituting inter partes review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.").

B. Related Proceedings

The parties identify the following district court and ITC proceedings involving the '080 patent: (1) *Daedalus Prime LLC v. Arrow Electronics, Inc.*, 1:22-cv-01107 (D. Del.); (2) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01109 (D. Del.); (3) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01108 (D. Del.); (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd.*, 2:22-cv-00352 (E.D. Tex.); (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (USITC); and (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC). Pet. 1–2; Paper 5, 2.

As noted *supra*, the '080 patent was also the subject of the '567 IPR, now terminated.

C. Real Parties-in-Interest

Petitioner identifies the following real parties-in-interest: Mercedes-Benz USA, LLC; Mercedes-Benz Intellectual Property GmbH & Co. KG; Mercedes-Benz Group AG; and Mercedes-Benz AG. Pet. 1. Patent Owner identifies Daedalus Prime LLC as the real party-in-interest. Paper 5, 2

At this stage, neither party challenges those identifications.

D. The '080 Patent

The '080 patent is titled "Asymmetric Performance Multicore Architecture with Same Instruction Set Architecture." Ex. 1001, (54). The '080 patent relates to multi-core processors in computing systems and

methods of managing power in multi-core processors. *Id.* at 1:16–1:20; 2:1–2:42; 3:50–4:19.

According to the '080 patent, typically, power management schemes scale up processing performance as the system's workload increases and scale down processing performance as the system's workload decreases. *Id.* at 2:22–26. Scaling process performance with workload is usually accomplished by enabling or disabling entire cores and raising or lowering core supply voltages and operating frequencies in response to workload. *Id.* at 2:30–33. For example, all cores are enabled under a maximum performance/power consumption state, and only one core is enabled under a minimum performance/power consumption state. *Id.* at 2:33–41; *see also id.* Fig. 2.

The '080 patent explains that some prior art multi-core processor power management schemes have been implemented on processors whose constituent cores are identical, while others have been implemented on processors in which the cores are radically different from each other (i.e., asymmetric). Ex. 1001, 3:34–39. For example, a processor with cores that are different from each other may have a low power core that lacks sizeable "chunks" of logic circuitry responsible for executing the program code instructions compared to the other cores in the processor and supports a reduced instruction set. *Id.* at 3:39–46. However, processors with cores that are different from each other can suffer from drawbacks because it is difficult for system software to adjust switch operation between processor cores having different instruction sets. *Id.* at 3:46–49.

The '080 patent purports to address this issue by disclosing multi-core processors in which at least one of the cores is designed to be lower

performance and therefore consumes less power than other cores in the processor. *Id.* at 3:50–4:9. According to the '080 patent, the lower power cores have the same logic design as the higher power cores and support the same instruction set, but consume less power by having narrower drive transistor widths than the higher power cores or other power consumption-related design features. *Id.* at 3:50–62.

The '080 patent explains that the lower power core allows the multi-processor "to entertain a power management strategy that is the same/similar to already existing power management strategies, yet, still achieve an even lower power consumption in the lower/lowest performance/power states." *Id.* at 4:20–46; *see also id.* Fig. 5. The process begins with a multi-core processor in which multiple high power cores and at least one low power core are operating. *Id.* Fig. 6 (610), 4:54–59. When the demand on the processor drops below a threshold, a high power core is disabled. *Id.* at 4:54–59. This process is repeated with the enabled high power cores each time demand reaches a lower threshold. *Id.* at 4:54–5:6. When all of the high power cores are disabled and the demand on the processor continues to drop, the low power cores are disabled one by one in the same manner until only one low power core is enabled and the lower power state is reached. *Id.* at 5:25–35.

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