U.S. Patent No. 10,049,080		
1[pre]. A multi-core processor comprising:	9[pre]. A method comprising:	17[pre]. A non-transi\... readable medium con\... code that when proce\... causes a method to be\... method comprising:
1[a][i]. a first plurality of cores and a second plurality of cores that support a same instruction set,	9[a][i]. operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set,	17[a][i]. operating a \... such that a first plural\... second plurality of co\... instruction set,
1[a][ii]. wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and	9[a][ii]. wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and	17[a][ii]. wherein the \... cores consume less p\... applied operating fre\... voltage, than the first \... and
1[b][i]. power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,	9[b][i]. disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,	17[b][i]. disabling wi\... management hardwar\... the first plurality of c\... plurality of cores are \... first plurality of cores\... demand below a thres\... disabling any of the s\... cores,
1[b][ii]. wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.	9[b][ii]. wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.	17[b][ii]. wherein an \... executing on the mult\... monitors a demand fo\... processor and control\... management hardwar\... demand.
2. The multi-core processor of claim 1, wherein the second plurality of cores	10. The method of claim 9, wherein the operating of the second plurality of cores	18. The non-transitor\... medium of claim 17, \...

comprise logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.	comprises driving logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.	operating of the secon comprises driving log narrower logic gate d corresponding logic g plurality of cores.
3. The multi-core processor of claim 1, wherein the second plurality of cores comprise logic gates that consume less power than corresponding logic gates of the first plurality of cores.	11. The method of claim 9, wherein the operating of the second plurality of cores comprises driving logic gates that consume less power than corresponding logic gates of the first plurality of cores.	19. The non-transitory medium of claim 17, operating of the secon comprises driving log consume less power t logic gates of the firs
4. The multi-core processor of claim 1, wherein the second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.	12. The method of claim 9, wherein the operating comprises operating the second plurality of cores at a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.	20. The non-transitory medium of claim 17, operating comprises o plurality of cores at a frequency that is less operating frequency o of cores.
5[a]. The multi-core processor of claim 1, wherein the power management hardware is to disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and	13[a]. The method of claim 9, further comprising disabling, with the power management hardware, an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and	21[a]. The non-transit readable medium of c comprising disabling, management hardwar of the second plurality continued drop in der lower threshold until second plurality of co and
5[b]. lower and operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.	13[b]. lowering an operating frequency or a supply voltage of the one core of the second plurality of cores as demand crops below a next lower threshold.	21[b]. lowering an op a supply voltage of th second plurality of co below a next lower th

6. The multi-core processor of claim 5, wherein the power management hardware is to raise a supply voltage or an operating frequency of said one core in response to higher demand.	14. The method of claim 13, further comprising raising, with the power management hardware, a supply voltage or an operating frequency of said one core in response to higher demand, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.	22. The non-transitory medium of claim 21, raising, with the powe hardware, a supply vc frequency of said one higher demand, where system executing on t processor monitors a multi-core processor power management h demand.
7. The multi-core processor of claim 1, wherein the first plurality of cores are at a maximum operating frequency in the state.	15. The method of claim 9, wherein the operating comprises operating the first plurality of cores at a maximum operating frequency in the state.	23. The non-transitory medium of claim 17, operating comprises c plurality of cores at a frequency in the state
8[pre]. The multi-core processor of claim 1, wherein	16[pre]. The method of claim 9, further comprising	24[pre]. The non-tran readable medium of c comprising
8[a]. the power management hardware is to enable all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores,	16[a]. enabling, with the power management hardware, all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores,	24[a]. enabling, with management hardwar plurality of cores for demand above the thr disabling any of the s cores,
8[b]. wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.	16[b]. wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.	24[b]. wherein an ope monitor a demand for processor and control management hardwar demand.