



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	02/14/2017	9569278	42P38886	6542

131413 7590 01/25/2017
NDWE LLP/ Intel
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1172 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Varghese George, Folsom, CA;
Sanjeev S. Jahagirdar, Folsom, CA;
Deborah T. Marr, Portland, OR;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

“FEE ADDRESS” INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the “Fee Address” under the provisions of 37 CFR 1.363 the address associated with:

Customer Number: 00197

OR

The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	13/335,257

Completed by (check one):

- Applicant/Inventor /Scott A. Simmons/
Signature
- Attorney or Agent of record Scott A. Simmons
Typed or printed name
- Assignee of record of the entire interest. See 37 CFR 3.71. 408-675-0441
Statement under 37 CFR 3.73(b) is enclosed. Requester's telephone number
(Form PTO/SB/96)
- Assignee recorded at Reel _____ Frame _____ 12/27/2016
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

* Total of One forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13335257				
Filing Date:	22-Dec-2011				
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE				
First Named Inventor/Applicant Name:	Varghese George				
Filer:	Scott Alan Simmons/Allison Madsen				
Attorney Docket Number:	42P38886				
Filed as Large Entity					
Filing Fees for Utility under 35 USC 111(a)					
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)	
Basic Filing:					
Pages:					
Claims:					
Miscellaneous-Filing:					
Petition:					
Patent-Appeals-and-Interference:					
Post-Allowance-and-Post-Issuance:					
UTILITY APPL ISSUE FEE	1501	1	960	960	

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	27910789
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	131413
Filer:	Scott Alan Simmons/Allison Madsen
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	27-DEC-2016
Filing Date:	22-DEC-2011
Time Stamp:	19:56:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$960
RAM confirmation Number	122816INTEFSW00005378504238
Deposit Account	504238
Authorized User	Allison Madsen

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)
 37 CFR 1.20 (Post Issuance fees)
 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P38886_IF_12_27_16.pdf	255482 078c9e531cc1a92b9746d55d150a133fa856997c	no	1

Warnings:

Information:

2	Change of Address	P38886_Fee_Address_Change_12_27_16.pdf	311836 b969415ac6e4245620b8104e5f070694536b080a	no	2
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Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	30595 4bdbe9ec41a859ca8ad8c6cade34543ea42a07c4	no	2
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Warnings:

Information:

Total Files Size (in bytes): 597913

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



NOTICE OF ALLOWANCE AND FEE(S) DUE

131413 7590 09/27/2016
NDWE LLP/ Intel
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

EXAMINER

COLEMAN, ERIC

ART UNIT PAPER NUMBER

2183

DATE MAILED: 09/27/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	Varghese George	42P38886	6542

TITLE OF INVENTION: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/27/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

131413 7590 09/27/2016
 NDWE LLP/ Intel
 c/o CPA Global
 900 2nd Avenue South, Suite 600
 Minneapolis, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

_____ (Depositor's name)
_____ (Signature)
_____ (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	Varghese George	42P38886	6542

TITLE OF INVENTION: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/27/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
COLEMAN, ERIC	2183	712-032000

<p>1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).</p> <p><input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.</p> <p><input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.</p>	<p>2. For printing on the patent front page, list</p> <p>(1) The names of up to 3 registered patent attorneys or agents OR, alternatively, _____ 1</p> <p>(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. _____ 2</p> <p>_____ 3</p>
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

<p>4a. The following fee(s) are submitted:</p> <p><input type="checkbox"/> Issue Fee</p> <p><input type="checkbox"/> Publication Fee (No small entity discount permitted)</p> <p><input type="checkbox"/> Advance Order - # of Copies _____</p>	<p>4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)</p> <p><input type="checkbox"/> A check is enclosed.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input type="checkbox"/> The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).</p>
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5. **Change in Entity Status** (from status indicated above)

Applicant certifying micro entity status. See 37 CFR 1.29

Applicant asserting small entity status. See 37 CFR 1.27

Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.

131413 7590 09/27/2016
NDWE LLP/ Intel
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

EXAMINER

COLEMAN, ERIC

ART UNIT PAPER NUMBER

2183

DATE MAILED: 09/27/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/335,257	Applicant(s) GEORGE ET AL.	
	Examiner ERIC COLEMAN	Art Unit 2183	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to amendment filed 08/26/2016.
 A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. The allowed claim(s) is/are 1-6,10-14,17-19 and 21-26. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) All b) Some *c) None of the:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|
| 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Examiner's Amendment/Comment |
| 2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. <input type="checkbox"/> Other _____. |
| 4. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/ERIC COLEMAN/ Primary Examiner, Art Unit 2183	
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Notice of References Cited	Application/Control No. 13/335,257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.	
	Examiner ERIC COLEMAN	Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0328055 A1	12-2009	Bose; Pradip	G06F1/3203	718/105
*	B	US-2008/0127192 A1	05-2008	Capps; Louis B.	G06F1/3203	718/103
*	C	US-2009/0271646 A1	10-2009	Talwar; Vanish	G06F1/3203	713/322
*	D	US-2009/0307512 A1	12-2009	Munjal; Ashish	G06F1/30	713/324
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.




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BIB DATA SHEET

CONFIRMATION NO. 6542

SERIAL NUMBER 13/335,257	FILING or 371(c) DATE 12/22/2011 RULE	CLASS 712	GROUP ART UNIT 2183	ATTORNEY DOCKET NO. 42P38886	
APPLICANTS INVENTORS Varghese George, Folsom, CA; Sanjeev S. Jahagirdar, Folsom, CA; Deborah T. Marr, Portland, OR; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 01/09/2012					
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged <u>/ERIC COLEMAN/</u> Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials _____	STATE OR COUNTRY CA	SHEETS DRAWINGS 8	TOTAL CLAIMS 19	INDEPENDENT CLAIMS 3
ADDRESS NDWE LLP/ Intel c/o CPA Global 900 2nd Avenue South, Suite 600 Minneapolis, MN 55402 UNITED STATES					
TITLE ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE					
FILING FEE RECEIVED 1680	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

Search Notes 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.
	Examiner ERIC COLEMAN	Art Unit 2183

CPC- SEARCHED		
Symbol	Date	Examiner
G06F1/3293,3296	12/26/2014	KN
G06F1/3293,3296 (updated)	4/29/2015	KN
G06f1/3293,3296 (updated)	5/17/2016	KN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
712	32,43	12/26/2014	KN
712	32,43 (updated)	4/29/2015	KN


SEARCH NOTES		
Search Notes	Date	Examiner
East text search	12/26/2014	KN
Inventor name search	12/26/2014	KN
Updated east text search (see search history printout)	4/29/2015	KN
Updated east text search (see search history printout)	5/17/2016	KN
Assignee search	5/17/2016	KN
updated above	09/22/2016	EC
712/32	09/22/2016	EC
G06F9/5094 1/3293 9/3296 1/3206	09/22/2016	EC
Y0B60/121 60/142	09/22/2016	EC
Searched Google scholar search terms multiple plural core power down gate stop clock priority asymmetric chip multiprocessor group cluster cores processors	09/22/2016	EC

INTERFERENCE SEARCH

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US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
712	32	09/22/2016	EC
G06F	9/5094 1/3293 9/3296 1/3206	09/22/2016	EC

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Index of Claims 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.
	Examiner ERIC COLEMAN	Art Unit 2183

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE									
Final	Original	09/22/2016									
1	1	=									
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3	3	=									
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	20	-									
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16	22	=									
17	23	=									
18	24	=									
19	25	=									
20	26	=									

EAST Search History

EAST Search History (Prior Art)

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L1	845	712/32.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:00
L2	20256	(G06F1/3296 OR G06F1/3293 OR G06F9/5094)".CPC"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:00
L3	46134	(disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down) near6 (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:00
L4	27638	(high or higher or low or lower) near2 (power or performance) near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:01
L5	3425	3 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:01
L6	124	(power near2 hungry or high\$3 near2 power) near6 first with (off or down or disabl\$3 or deactivat\$3 or sleep\$3) same (processor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:01
L7	1712	(cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more or more near2 power) near6 (power\$3 near down or power\$3 near off or disabl\$3 or deactiva\$3) same (threshold or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:02
L8	15034	(cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more or more near2 power) near6 (power\$3 near down or power\$3 or turn\$3 near off or disabl\$3 or deactiva\$3) same (threshold or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:02
L9	24	highest near4 lowest near4 (power or performance) near6 (cpu or processor or core) same (sequence or disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:02
L10	228	(sequential or sequnc\$3) near4 power with (cpu or processor or core)	US-PGPUB; USPAT;	OR	ON	2016/09/22 12:03

			EPO; JPO; DERWENT; IBM_TDB			
L11	3678	(sequential or sequenc\$3) near4 power with (cpu or processor or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:03
L12	85	1 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:03
L13	16	1 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:04
L14	2	1 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:04
L15	0	1 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 12:04

9/ 22/ 2016 12:04:49 PM

EAST Search History

EAST Search History (Prior Art)

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L1	192	varghese near2 george.in.inv.inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/09/22 09:18
L2	192	varghese near2 george.in.inv.inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:18
L3	0	sanjeev near2 george.in,inv,inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:19
L4	2	sanjeev near2 george.in.inv.inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:20
L5	100	sanjeev near2 jahagirdar.in,inv,inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:20
L6	29	deborah near2 marr.in,inv,inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:21
L7	7079	(G06F1/3296 OR G06F1/3293 OR G06F9/5094).CPC.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:23
L8	1852	7 and @pd> "20150908"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:24
L9	78249	intel.aaat,aanm,as,asn,aszz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:25
L10	46134	(disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down) near6 (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:27

L11	27638	(high or higher or low or lower) near2 (power or performance) near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:29
L12	3425	10 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:29
L13	372	9 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:30
L14	21776	713/300,322,323,324.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:30
L15	4546	713/324.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:30
L17	2207	power near2 hungry or high\$3 near2 power) near6 first with (off or down or disabl\$3 or deactivat\$3 or sleep\$3 same (processor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:32
L18	11	15 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:34
L19	8	18 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:37
L20	1544	17 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:37
L21	124	(power near2 hungry or high\$3 near2 power) near6 first with (off or down or disabl\$3 or deactivat\$3 or sleep\$3) same (processor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:39
L22	3	21 and 19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:40
L23	3	22 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:40

L24	1712	(cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more or more near2 power) near6 (power\$3 near down or power\$3 near off or disabl\$3 or deactiva\$3) same (threshold or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:45
L25	15034	(cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more or more near2 power) near6 (power\$3 near down or power\$3 or turn\$3 near off or disabl\$3 or deactiva\$3) same (threshold or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:48
L26	21776	713/300,322,323,324.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:49
L27	1943	25 and 26	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:49
L28	1456	27 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:51
L29	64	28 and (asymmetric or heterogeneous) near5 (process\$3 or core or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:52
L30	0	highest adj to adj lowest near4 (power or performance) near6 (cpu or processor or core)same (sequence or disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:55
L31	13	highest near2 lowest near4 (power or performance) near6 (cpu or processor or core)same (sequence or disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:56
L32	24	highest near4 lowest near4 (power or performance) near6 (cpu or processor or core)same (sequence or disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:57
L33	21995	(asymmetric or heterogeneous) near5 (processor or core or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:57
L34	329	14 and 33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:58

EAST Search History


L35	191	34 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 09:59
L36	12	35 and (cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more near2 power) near6 (power\$3 near down or power\$3 near off or turn\$3 near off or disabl\$3 or deactivat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:03
L37	228	(sequential or sequnc\$3) near4 power with (cpu or processor or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:05
L38	7	(sequential or sequnc\$3) near4 power with (cpu or processor or core) with (high\$3 or low\$3) near2 (performance or power)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:12
L39	3	38 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:15
L40	2	39 and (heterogeneous or asymmetric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:16
L41	21995	(heterogeneous or asymmetric) near5 (core or cpu or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:16
L42	1881	41 and (threshold or level) same power same (core or cpu or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:17
L43	834	42 and (high\$3 or low\$3) near3 (power or performance) near3 (core or cpu or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:18
L44	3286	(G06F9/5094 OR G06F1/3293 OR G06F9/3296).CPC.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:20
L45	187	43 and 44	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:20
L46	84	45 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2016/09/22 10:21

			IBM_TDB			
L47	1027	42 and ((high\$3 or low\$3) near3 (power or performance) near3 (core or cpu or processor) or (big\$3 or small\$3) near3 (core or cpu or processor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:25
L48	23887	26 or 44	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:27
L49	315	47 and 48	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:27
L50	139	49 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:28
L51	45	high\$3 near3 (power or performance) with (all or every) near3 (cpu or processor core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:29
L52	22	51 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:30
L53	2	"20100131781".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:31
L54	2	"20090055826".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:32
L55	1094	(asymmetric or heterogeneous) near5 (process\$3 or core or cpu) same (high\$3 near2 (power or performance) or low\$3 near2 (power or performance) or (big or large or small) near2 core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:34
L56	385	55 and ("same" or similar) near3 (instruction set or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:35
L57	196	55 and ("same" or similar) near3 (instruction adj set or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:35
L58	168	55 and ("same" or similar) near3 (instruction adj set or isa) with (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2016/09/22 10:36

EAST Search History

			IBM_TDB			
L59	24	58 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:36
L60	6369	(G06F9/5094 OR G06F1/3293 OR G06F9/3296 or G06F1/3206 OR Y02B60/121 OR Y06B60/142).CPC.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:43
L61	116	34 and 60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:44
L62	52	55 and 61	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/22 10:44


9/ 22/ 2016 10:47:04 AM

Issue Classification 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.	
	Examiner ERIC COLEMAN	Art Unit 2183	

CPC					
Symbol				Type	Version
G06F	9		5094	F	2013-01-01
G06F	1		3206	I	2013-01-01
G06F	1		3293	I	2013-01-01
Y02B	60		142	A	2013-01-01
Y02B	60		121	A	2013-01-01


CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/ERIC COLEMAN/ Primary Examiner. Art Unit 2183	09/22/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.
	Examiner ERIC COLEMAN	Art Unit 2183

US ORIGINAL CLASSIFICATION					INTERNATIONAL CLASSIFICATION											
CLASS		SUBCLASS			CLAIMED				NON-CLAIMED							
712		32			G	0	6	F	9 / 50 (2006.01.01)							
CROSS REFERENCE(S)					G	0	6	F	1 / 32 (2006.01.01)							
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/ERIC COLEMAN/ Primary Examiner. Art Unit 2183	09/22/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.
	Examiner ERIC COLEMAN	Art Unit 2183

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/ERIC COLEMAN/ Primary Examiner. Art Unit 2183	09/22/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	Varghese George	42P38886	6542
131413	7590	08/29/2016	EXAMINER	
NDWE LLP/ Intel c/o CPA Global 900 2nd Avenue South, Suite 600 Minneapolis, MN 55402			COLEMAN, ERIC	
			ART UNIT	PAPER NUMBER
			2183	
			NOTIFICATION DATE	DELIVERY MODE
			08/29/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patent@nicholsondevos.com
ndwe_docketing@cardinal-ip.com
inteldocs_docketing@cpaglobal.com

<i>Applicant-Initiated Interview Summary</i>	Application No. 13/335,257	Applicant(s) GEORGE ET AL.	
	Examiner ERIC COLEMAN	Art Unit 2183	

All participants (applicant, applicant's representative, PTO personnel):

- (1) ERIC COLEMAN. (3) _____.
(2) Scott A. Simmons (Reg.No. 60,206). (4) _____.

Date of Interview: 23 August 2016.

Type: Telephonic Video Conference
 Personal [copy given to: applicant applicant's representative]

Exhibit shown or demonstration conducted: Yes No.
If Yes, brief description: _____.

Issues Discussed 101 112 102 103 Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1-6,10-14,17-19 and 21-26.

Identification of prior art discussed: Memon (patent application publication No. 2010/0131781) and Sutardja (patent application publication No. 2008/0288748).

Substance of Interview

(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Counsel and Examiner discussed the claims and disclosed invention in the specification, and cited prior art and possible claim changes. No agreement was reached.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Attachment

/ERIC COLEMAN/
Primary Examiner, Art Unit 2183

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/335,257	Filing Date 12/22/2011	<input type="checkbox"/> To be Mailed
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ENTITY: LARGE SMALL MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	08/26/2016	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total (37 CFR 1.16(i))	* 20	Minus ** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus *** 3	= 0	X \$420 =	0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))					
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	0

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total (37 CFR 1.16(i))	*	Minus **	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X \$ =	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))					
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/MOLIKI MAY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
 If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Attorney's Docket No.: 42P38886

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Varghese George

Examiner: Eric Coleman

Application No.: 13/335,257

Art Unit: 2183

Filed: December 22, 2011

Confirmation No.: 6542

For: ASYMMETRIC PERFORMANCE
MULTICORE ARCHITECTURE WITH
SAME INSTRUCTION SET
ARCHITECTURE

Mail Stop Amendment
Commissioner for Patents
e-Filed via EFS-WEB

RESPONSE AND AMENDMENT

Sir:

In response to the Office action transmitted on May 26, 2016, Applicant respectfully requests the Examiner enter the following amendments and consider the following remarks.

CERTIFICATE OF EFS-Web

I hereby certify that this correspondence is being submitted electronically via EFS-Web on the date shown below to the United States Patent and Trademark Office.

Date of Deposit: 08/26/2016

Name of Person Mailing Correspondence: Allison Madsen

Signature: /Allison Madsen/

Appl. No.: 13/335,257

Amdt. Dated 08/26/16

Reply to Office action of 05/26/16

1

Atty. Docket No.: 42P38886

Petitioner Mercedes Ex-1010, 0034

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

What is claimed is:

1. (Currently amended) A multi-core processor comprising:
a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and
power management hardware to, from an initial state where the first plurality of cores and the second plurality of cores are enabled, disable an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, ~~[[and]]~~disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the ~~first-second~~ plurality of cores remains enabled, and lower at least one of an operating frequency and a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.
2. (Previously presented) The multi-core processor of claim 1 wherein the second plurality of cores include logic gates that have narrower logic gate driver transistors than a corresponding logic gate of the first plurality of cores.
3. (Previously presented) The multi-core processor of claim 1 wherein the second plurality of cores comprise logic gates that consume less power than a corresponding logic gate of the first plurality of cores.
4. (Previously presented) The multi-core processor of claim 1 wherein the second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.

5. (Previously presented) The multi-core processor of claim 1 further comprising a switch fabric between the first plurality of cores, the second plurality of cores, and a system memory interface.

6. (Currently amended) A method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, the first plurality of cores being higher performance and consuming more power than the second plurality of cores under a same applied supply voltage and operating frequency; and

disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, ~~and then~~ disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the ~~first~~ second plurality of cores remains enabled, and lowering at least one of an operating frequency and a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

7-9. (Canceled)

10. (Previously presented) The method of claim 6 wherein the operating of the first plurality of cores includes driving load lines with wider transistor widths than corresponding transistor widths in said second plurality of cores.

11. (Previously presented) The method of claim 6 further comprising lowering at least one of a supply voltage and an operating frequency of said one core in response to lower demand being offered to said multi-core processor.

12. (Previously presented) The method of claim 11 further comprising raising at least one of a supply voltage and an operating frequency of said one core in response to higher demand being offered to said multi-core processor.

13. (Previously presented) The method of claim 6 further comprising:

raising at least one of a supply voltage and an operating frequency of said one core in response to higher demand being offered to said multi-core processor.

14. (Currently amended) A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, the first plurality of cores being higher performance and consuming more power than a second plurality of cores under a same applied supply voltage and operating frequency; and

disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, ~~and then~~ disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled, and lowering at least one of an operating frequency and a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

15-16. (Canceled)

17. (Previously presented) The non-transitory machine readable medium of claim 14 wherein said method further comprises lowering at least one of a supply voltage and an operating frequency of said one core in response to lower demand being offered to said multi-core processor.

18. (Previously presented) The non-transitory machine readable medium of claim 17 wherein said method further comprises raising at least one of a supply voltage and an operating frequency of said one core in response to higher demand being offered to said multi-core processor.

19. (Previously presented) The non-transitory machine readable medium of claim 14 wherein said method further comprises raising at least one of a supply voltage and an operating frequency of said one core in response to higher demand being offered to said multi-core processor.

20. (Canceled)

21. (Previously presented) The multi-core processor of claim 1 wherein the power management hardware is to lower at least one of a supply voltage and an operating frequency of each additional core to a lower operating level before disablement.

22. (Previously presented) The multi-core processor of claim 1 wherein the power management hardware is to enable an additional core of the second plurality of cores for each continued increase in demand above a next higher threshold without enabling any of the first plurality of cores until the second plurality of cores is enabled, and enable an additional core of the first plurality of cores for each continued increase in demand above a next higher threshold until the first plurality of cores is also enabled.

23. (Previously presented) The multi-core processor of claim 1 wherein the power management hardware is to lower at least one of a supply voltage and an operating frequency of said one core in response to lower demand.

24. (Previously presented) The multi-core processor of claim 1 wherein the power management hardware is to raise at least one of a supply voltage and an operating frequency of said one core in response to higher demand.

25. (Previously presented) The method of claim 6 further comprising lowering at least one of a supply voltage and an operating frequency of each additional core to a lower operating level before disablement.

26. (Previously presented) The non-transitory machine readable medium of claim 14 wherein said method further comprises lowering at least one of a supply voltage and an operating frequency of each additional core to a lower operating level before disablement.

REMARKS

The Applicant sincerely thanks Examiner Coleman for the phone interview on August 23, 2016.

(1) Interview Summary:

In the call, the Examiner and Applicant's representative discussed the claim rejections and potential claim amendments.

(2) Response to the Office Action

The enclosed is responsive to the Examiner's Office action transmitted on May 26, 2016. Claims 1-6, 10-14, 17-19, and 21-26 are pending, with claims 1, 6, and 14 being independent. Claims 7-9, 15, 16, and 20 have been cancelled. Claims 1, 6, and 14 have been amended. No new subject matter has been added. Applicant respectfully requests reconsideration of the present application and the allowance of all claims now presented.

Objections

Applicant submits that the amendments in this response overcome the objections in the Office action.

35 U.S.C. § 103 Rejections

Claims 1-6, 10-14, 17-19, and 21-26 were rejected under pre-AIA 35 U.S.C. 103(a) as being allegedly unpatentable over Memon et al., U.S. Publication No. 2010/0131781 (hereinafter "Memon"), in view of Sutardja et al., U.S. Publication No. 2008/0288748 (hereinafter "Sutardja").

The cited portions of the references do not appear to teach or suggest the Applicant's claims. For example, the cited portions of the references do not appear to teach or suggest:

1. A multi-core processor comprising:

a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and power management hardware to, from an initial state where the first plurality of cores and the second plurality of cores are enabled, disable an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lower at least one of an operating frequency and a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold. (Emphasis added.)

as in Applicant's independent claim 1, or:

6. (Currently amended) A method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, the first plurality of cores being higher performance and consuming more power than the second plurality of cores under a same applied supply voltage and operating frequency; and

disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lowering at least one of an operating frequency and a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold. (Emphasis added.)

as in Applicant's independent claim 6, or:

14. (Currently amended) A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, the first plurality of cores being higher performance and consuming more power than a second plurality of cores under a same applied supply voltage and operating frequency; and

disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold

without disabling any of the second plurality of cores until the first plurality of cores is disabled, disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled, and lowering at least one of an operating frequency and a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold. (Emphasis added.)

as in Applicant's independent claim 14.

Because the Applicant has demonstrated the patentability of all pending independent claims, the Applicant respectfully submits that all pending claims are allowable. The Applicant's silence with respect to the dependent claims should not be construed as an admission by the Applicant that the Applicant is complicit with the Examiner's rejection of these claims. Because the Applicant has demonstrated the patentability of the independent claims, the Applicant need not substantively address the theories of rejection applied to the dependent claims.

In light of the comments above, Applicant respectfully requests the allowance of all claims.

CONCLUSION

Applicant respectfully submits that all objections and rejections have been overcome and that all pending claims are in condition for allowance. If the Examiner believes an additional telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Scott A. Simmons at (408) 675-0441. Authorization is hereby given to charge our Deposit Account No. 504238 for any charges that may be due.

Respectfully submitted,
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP

Date: 8/26/2016

/Scott A. Simmons/
Scott A. Simmons
Reg. No.: 60,206

217 High Street
Palo Alto, CA 94301
(408) 675-0441

Electronic Acknowledgement Receipt

EFS ID:	26764817
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	131413
Filer:	Scott Alan Simmons/Allison Madsen
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	26-AUG-2016
Filing Date:	22-DEC-2011
Time Stamp:	17:19:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38886_ROA_08_26_16.pdf	49317 cadd974e9ccf618f099479e0cfe93f392643c00d	yes	10

Multipart Description/PDF files in .zip description		
Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	6
Applicant Arguments/Remarks Made in an Amendment	7	10

Warnings:

Information:

Total Files Size (in bytes):	49317
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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Table with columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
13/335,257 12/22/2011 Varghese George 42P38886 6542
131413 7590 05/26/2016 NDWE LLP/ Intel c/o CPA Global 900 2nd Avenue South, Suite 600 Minneapolis, MN 55402
EXAMINER NIELSEN, KEITH A
ART UNIT 2183 PAPER NUMBER
NOTIFICATION DATE 05/26/2016 DELIVERY MODE ELECTRONIC

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Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patent@nicholsondevos.com
ndwe_docketing@cardinal-ip.com
inteldocs_docketing@cpaglobal.com

Office Action Summary	Application No. 13/335,257	Applicant(s) GEORGE ET AL.	
	Examiner KEITH NIELSEN	Art Unit 2183	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 9/8/2015.
 A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) Claim(s) 1-6,10-14,17-19 and 21-26 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) Claim(s) _____ is/are allowed.
- 7) Claim(s) 1-6,10-14,17-19 and 21-26 is/are rejected.
- 8) Claim(s) _____ is/are objected to.
- 9) Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) The specification is objected to by the Examiner.
- 11) The drawing(s) filed on 9/8/2015 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) All b) Some** c) None of the:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____.
- 3) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 4) Other: _____.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Claims 21-26 have been added.

Claims 7-9, 15-16, and 20 have been cancelled.

Claims 1-6, 10-14, 17-19, and 21-26 are presented for examination.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/18/2015 has been entered.

Claim Objections

Claims 1, 6, and 14 are objected to because of the following informalities:

- Claims 1, 6, and 14, last line - "one core of the first plurality" should be --one core of the second plurality--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6, 10-14, 17-19, and 21-26 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Memon et al. (US Patent Publication No. 2010/0131781) in view of Sutardja et al (US Patent Publication No. 2008/0288748).

As per claim 1, Memon teaches a multi-core processor (Fig. 2), comprising:

a first plurality of cores (Fig. 2 - cores 212) and a second plurality of cores (Fig. 2 - cores 214) [that support a same instruction set], wherein the second plurality of cores consume less power [at a same applied operating frequency and supply voltage] than the first plurality of cores ([0019] - low power core); and

power management hardware (Fig. 2 - power management unit 220), from an initial state where the first plurality of cores and the second plurality of cores are enabled (Fig. 1, [0016] - high level of traffic can use all cores), disable an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled (Fig. 1, [0016], [0022] - for each threshold, power down cores starting with the higher power cores), and disable an additional core of the second plurality of

cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled (Fig. 1, [0016], [0022] - at the lowest threshold, leave one low power core enabled).

Memon is silent as to the instruction set that the processor cores use, as well as the lower power core operating at a same frequency and voltage as the high power core.

However, Sutardja teaches that a high power core and a low power core use the same instruction set ([0214], [0225]), and that a low power core uses less power than a high power core since the transistors are smaller ([0230]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the high and low power cores of Sutardja for the high and low power cores of Memon. A substitution of similar high and low power cores would have yielded the predictable result of efficiently executing tasks across heterogeneous cores. Claims 6 and 14 are method and medium claims corresponding to claim 1 and are rejected for the same reason as set forth in the rejection of claim 1.

As per claim 2, Memon and Sutardja teach the multi-core processor of claim 1 wherein the second plurality of cores include logic gates that have narrower logic gate driver transistors than a corresponding logic gate of the first plurality of cores (Sutardja, [0230]).

Claim 10 is a method claim corresponding to claim 2 and is rejected for the same reason as set forth in the rejection of claim 2.

As per claim 3, Memon and Sutardja teach the multi-core processor of claim 1 wherein the second plurality of cores comprise logic gates that consume less power than a corresponding logic gate of the first plurality of cores (Sutardja, [0230]).

As per claim 4, Memon and Sutardja teach the multi-core processor of claim 1 wherein the second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores (Sutardja, [0234] - HP core operates at more than 1GHz while the LP core operates at less than or equal to 500 MHz).

As per claim 5, Memon and Sutardja teach the multi-core processor of claim 1 further comprising a switch fabric between the first plurality of cores, the second plurality of cores, and a system memory interface (Fig. 2 - busses between memory and cores).

As per claim 21, Memon and Sutardja teach the multi-core processor of claim 1 wherein the power management hardware is to lower at least one of a supply voltage and an operating frequency of each additional core to a lower operating level before disablement (Sutardja, [0304] - voltage/frequency can be raised and lowered according to the performance demanded by the application).

Claims 25 and 26 are method and medium claims corresponding to claim 21 and are rejected for the same reason as set forth in the rejection of claim 21.

As per claim 22, Memon and Sutardja teach the multi-core processor of claim 1, wherein the power management hardware is to enable an additional core of the second plurality of cores for each continued increase in demand above a next higher threshold without enabling any of the first plurality of cores until the second plurality of cores is enabled (Fig. 1, [0016], [0022] - cores are enabled according to the traffic thresholds), and enable an additional core of the first plurality of cores for each continued increase in demand above a next higher threshold until the first plurality of cores is also enabled (Fig. 1, [0016] - high level of traffic can use all cores).

As per claim 23, Memon and Sutardja teach the multi-core processor of claim 1 further comprising lowering at least one of a supply voltage and an operating frequency of said one core in response to lower demand (Sutardja, [0304] - voltage/frequency can be raised and lowered according to the performance demanded by the application).

Claims 11 and 17 are method and medium claims corresponding to claim 23 and are rejected for the same reason as set forth in the rejection of claim 23.

As per claim 24, Memon and Sutardja teach the multi-core processor of claim 1 further comprising raising at least one of a supply voltage and an operating frequency of said one core in response to higher demand (Sutardja, [0304] - voltage/frequency can be raised and lowered according to the performance demanded by the application).

Claims 12, 13, 18 and 19 are method and medium claims corresponding to claim 24 and are rejected for the same reason as set forth in the rejection of claim 24.

Response to Arguments

Applicant's arguments, see pages 7-8 of the remarks, filed 9/8/2015, with respect to the rejection(s) of claim(s) 1-20 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Memon et al. and Sutardja et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH NIELSEN whose telephone number is (571)270-3584. The examiner can normally be reached on Monday-Friday, 9:00am - 6:00pm, Alt. Friday, EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on 571-272-3702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. N./
Examiner, Art Unit 2183

/ANDREW CALDWELL/
Supervisory Patent Examiner, Art Unit 2183

Notice of References Cited	Application/Control No. 13/335,257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.	
	Examiner KEITH NIELSEN	Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0055826 A1	02-2009	Bernstein; Kerry	G06F9/3891	718/102
*	B	US-2010/0131781 A1	05-2010	Memon; Mazhar I.	G06F1/3209	713/310
*	C	US-2011/0239015 A1	09-2011	Boyd; William T.	G06F1/3203	713/320
*	D	US-2011/0252260 A1	10-2011	Flachs; Brian K.	G06F1/3287	713/324
*	E	US-2012/0117403 A1	05-2012	Bieswanger; Andreas	G06F1/3206	713/322
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	varghese near2 george.in.inv.inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:11
L2	188	varghese near2 george.in,inv,inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:11
L3	97	sanjeev near2 jahagirdar.in,inv,inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:11
L4	29	deborah near2 marr.in,inv,inzz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:12
L13	3623	g06f1/3296.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:24
L16	1762	G06f9/5094.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:25
L19	1321	G06f1/3293.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:26
L20	608	13 and @pd> "20150908"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:26
L21	265	16 and @pd> "20150908"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:26
L22	267	19 and @pd> "20150908"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:26

EAST Search History

L23	73625	intel.aaat,aanm,as,asn,aszz.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:27
L26	44424	(disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down) near6 (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:30
L29	26262	(high or higher or low or lower) near2 (power or performance) near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:31
L30	3223	26 and 29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:31
L31	319	23 and 30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/17 22:31
S24	15931	713/300,322,323,324.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2016/05/16 05:31
S25	3263	713/324.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2016/05/16 05:31
S26	4523	713/324.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 05:32
S27	2159	(power near2 hungry or high\$3 near2 power) near6 first with (off or down or disabl\$3 or deactivat\$3 or sleep\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 05:33
S28	12	S26 and S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 05:33
S29	110	(power near2 hungry or high\$3 near2 power) near6 first with (off or down or disabl\$3 or deactivat\$3 or sleep\$3) same (processor or cpu or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 05:33
S30	9	S28 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 05:34
S31	48	S29 and @ad<"20111222"	US-PGPUB;	ADJ	ON	2016/05/16

			USPAT; EPO; JPO; DERWENT; IBM_TDB			05:34
S32	997	(cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more near2 power) near6 (power\$3 near down or power\$3 near off or disabl\$3 or deactivat\$3) same (threshold or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 05:51
S33	3075	(cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more near2 power) near6 (power\$3 near down or power\$3 near off or turn\$3 near off or disabl\$3 or deactivat\$3) same (threshold or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 05:51
S34	21490	713/300,322,323,324.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 05:52
S35	148	S33 and S34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 05:52
S36	111	S35 and @ad< "20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 05:52
S37	5	S36 and (asymmetric or heterogeneous) near5 (process\$3 or core or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 05:55
S38	0	highest adj to adj lowest near4 (power or performance) near6 (cpu or processor or core) same (sequence or disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 06:23
S39	12	highest near2 lowest near4 (power or performance) near6 (cpu or processor or core) same (sequence or disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 06:23
S40	23	highest near4 lowest near4 (power or performance) near6 (cpu or processor or core) same (sequence or disabl\$3 or deactivat\$3 or power\$3 near2 off or turn\$3 near2 off or power\$3 near2 down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 06:25
S41	46439	(asymmetric or heterogeneous) near5 (process\$3 or core or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 06:29
S42	365	S24 and S41	US-PGPUB;	ADJ	ON	2016/05/16:

			USPAT; EPO; JPO; DERWENT; IBM_TDB			06:29
S43	224	S42 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 06:29
S44	16	S43 and (cpu or processor or node or server or rack or computer or core) near4 (high\$3 or most or more near2 power) near6 (power\$3 near down or power\$3 near off or turn\$3 near off or disabl\$3 or deactivat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:28
S45	3516	(sequential or sequenc\$3) near4 power with (cpu or processor or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:39
S46	162	(sequential or sequenc\$3) near4 power with (cpu or processor or core) with (high\$3 or low\$3) near2 (performance or power)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:40
S47	95	S46 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:40
S48	4	S47 and (heterogeneous or asymmetric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:44
S49	20565	(heterogeneous or asymmetric) near5 (core or cpu or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:45
S50	1691	S49 and (threshold or level) same power same (core or cpu or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:46
S51	721	S50 and (high\$3 or low\$3) near3 (power or performance) near3 (core or cpu or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:47
S52	1758	g06f9/5094.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:48
S53	4845	g06f1/3293,3296.cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16: 07:48

EAST Search History

S54	20322	S24 or S52 or S53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 07:48
S55	310	S51 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 07:48
S56	131	S55 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 07:48
S57	904	S50 and ((high\$3 or low\$3) near3 (power or performance) near3 (core or cpu or processor) or (big\$3 or small\$3) near3 (core or cpu or processor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 07:54
S58	345	S54 and S57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 07:54
S59	150	S58 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 07:54
S61	40	high\$3 near3 (power or performance) with (all or every) near3 (cpu or processor or core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 10:35
S63	21	S61 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 10:35
S64	2	"20100131781".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 12:01
S65	2	"20090055826".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 12:02
S66	1757	(asymmetric or heterogeneous) near5 (process\$3 or core or cpu) same1 (high\$3 near2 (power or performance) or low\$3 near2 (power or performance) or (big or large or small) near2 core)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 12:30
S67	222	S66 and ("same" or similar) near3 (instruction set or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 12:33

EAST Search History


S68	160	S66 and ("same" or similar) near3 (instruction set or isa) with (core or processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 12:33
S69	30	S68 and @ad<"20111222"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2016/05/16 12:34

EAST Search History (Interference)

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5/ 17/ 2016 10:32:48 PM

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Search Notes 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.
	Examiner KEITH NIELSEN	Art Unit 2183

CPC- SEARCHED		
Symbol	Date	Examiner
G06F1/3293,3296	12/26/2014	KN
G06F1/3293,3296 (updated)	4/29/2015	KN
G06f1/3293,3296 (updated)	5/17/2016	KN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
712	32,43	12/26/2014	KN
712	32,43 (updated)	4/29/2015	KN

SEARCH NOTES		
Search Notes	Date	Examiner
East text search	12/26/2014	KN
Inventor name search	12/26/2014	KN
Updated east text search (see search history printout)	4/29/2015	KN
Updated east text search (see search history printout)	5/17/2016	KN
Assignee search	5/17/2016	KN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/335,257	12/22/2011	Varghese George	42P38886

CONFIRMATION NO. 6542

POA ACCEPTANCE LETTER

131413
NDWE LLP/ Intel
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402



Date Mailed: 09/10/2015

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2015.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dtdinh/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/335,257	12/22/2011	Varghese George	42P38886

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

CONFIRMATION NO. 6542
POWER OF ATTORNEY NOTICE



Date Mailed: 09/10/2015

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2015.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervenered as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dt Dinh/

Electronic Patent Application Fee Transmittal

Application Number:	13335257				
Filing Date:	22-Dec-2011				
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE				
First Named Inventor/Applicant Name:	Varghese George				
Filer:	Scott Alan Simmons/allison madsen				
Attorney Docket Number:	42P38886				
Filed as Large Entity					
Filing Fees for Utility under 35 USC 111(a)					
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)	
Basic Filing:					
Pages:					
Claims:					
Miscellaneous-Filing:					
Petition:					
Patent-Appeals-and-Interference:					
Post-Allowance-and-Post-Issuance:					
Extension-of-Time:					

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	1251	1	200	200
Miscellaneous:				
Total in USD (\$)				200

Electronic Acknowledgement Receipt

EFS ID:	23426160
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	45209
Filer:	Scott Alan Simmons/allison madsen
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	08-SEP-2015
Filing Date:	22-DEC-2011
Time Stamp:	15:01:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$200
RAM confirmation Number	1546
Deposit Account	506674
Authorized User	SIMMONS, SCOTT

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	30769 <small>df5a86ed4c6417317abd31a8fc2935cd30df665f</small>	no	2

Warnings:

Information:

Total Files Size (in bytes):	30769
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

**REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)**

Application Number	13335257	Filing Date	2011-12-22	Docket Number (if applicable)	42P38886	Art Unit	2183
First Named Inventor	Varghese George			Examiner Name	NIELSEN, KEITH A		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

Other _____

Enclosed

Amendment/Reply

Information Disclosure Statement (IDS)

Affidavit(s)/ Declaration(s)

Other _____

MISCELLANEOUS

Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 504238

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Patent Practitioner Signature

Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Scott A. Simmons/	Date (YYYY-MM-DD)	2015-09-08
Name	Scott A. Simmons	Registration Number	60206

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

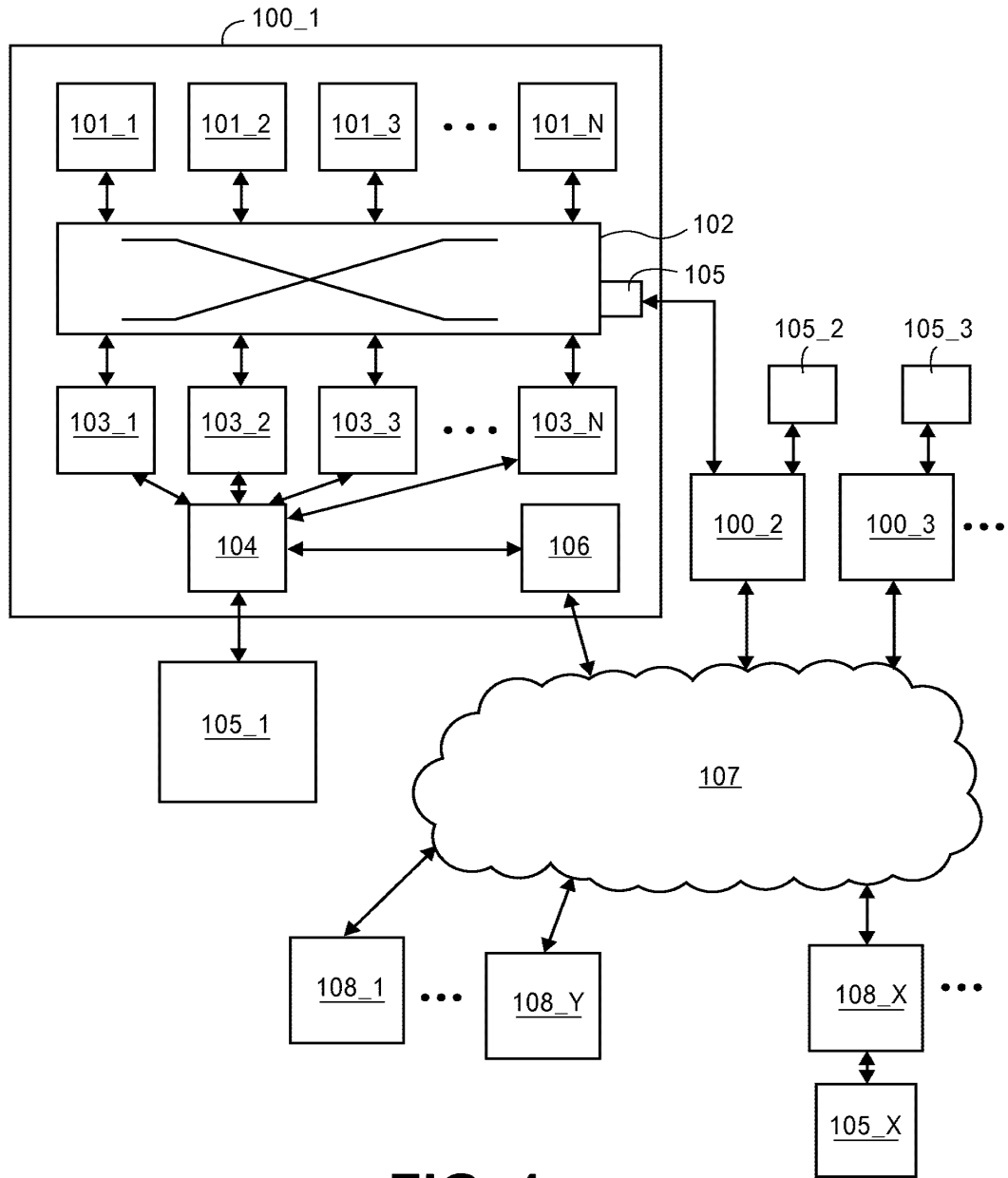


FIG. 1

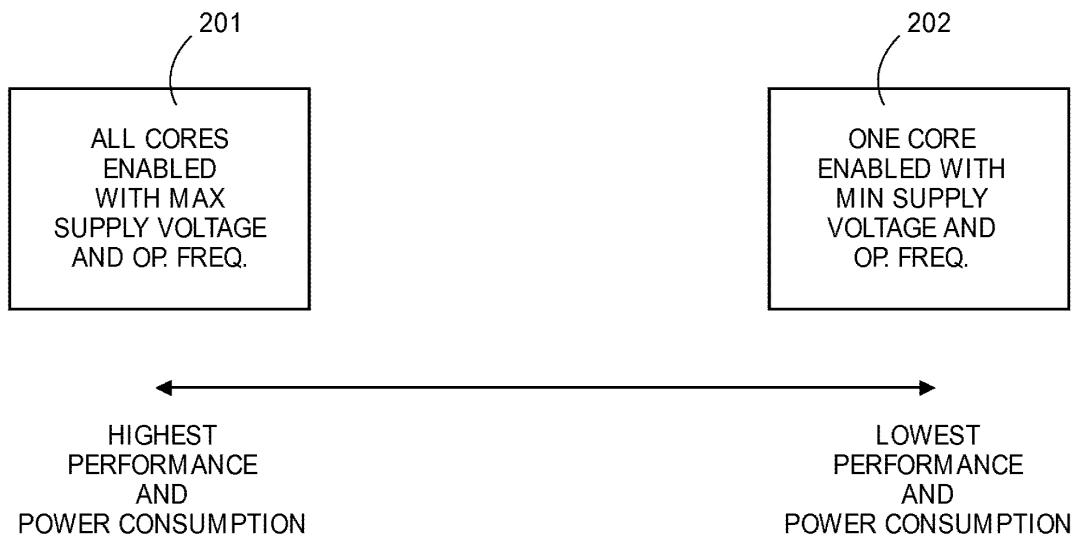


FIG. 2

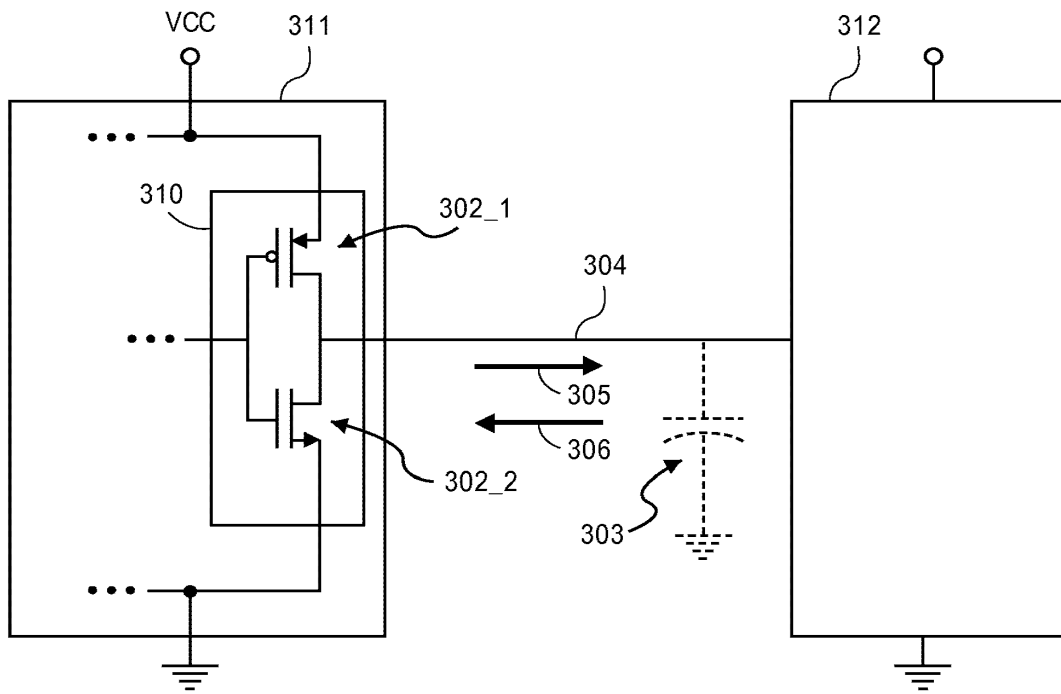


FIG. 3

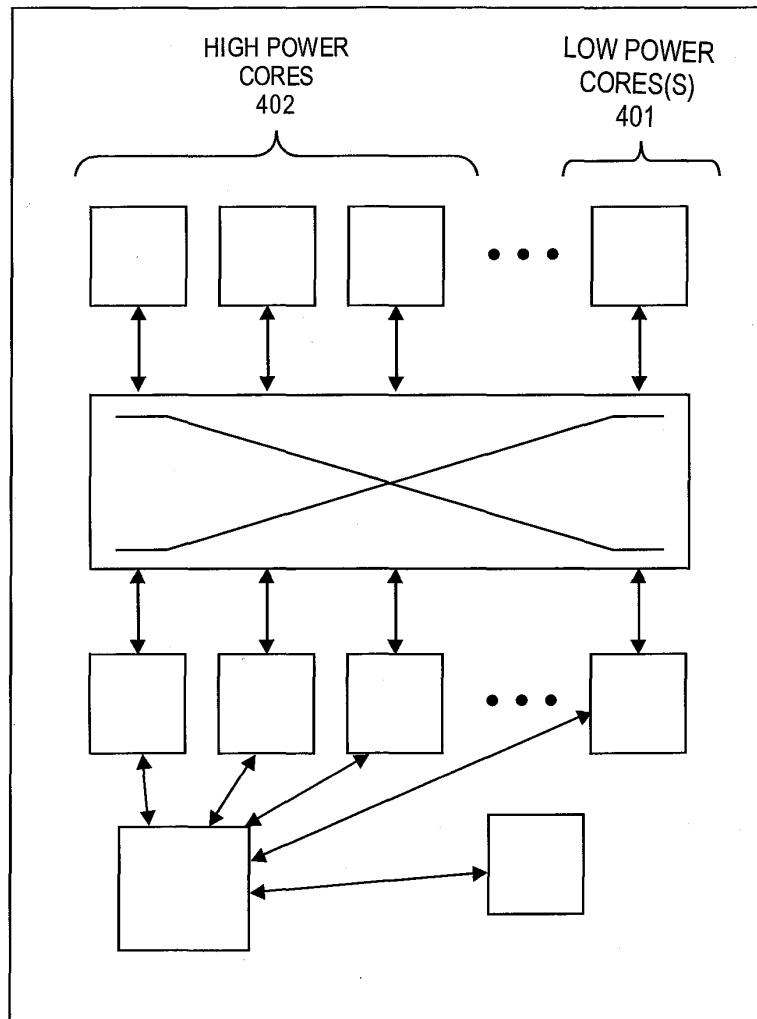


FIG. 4

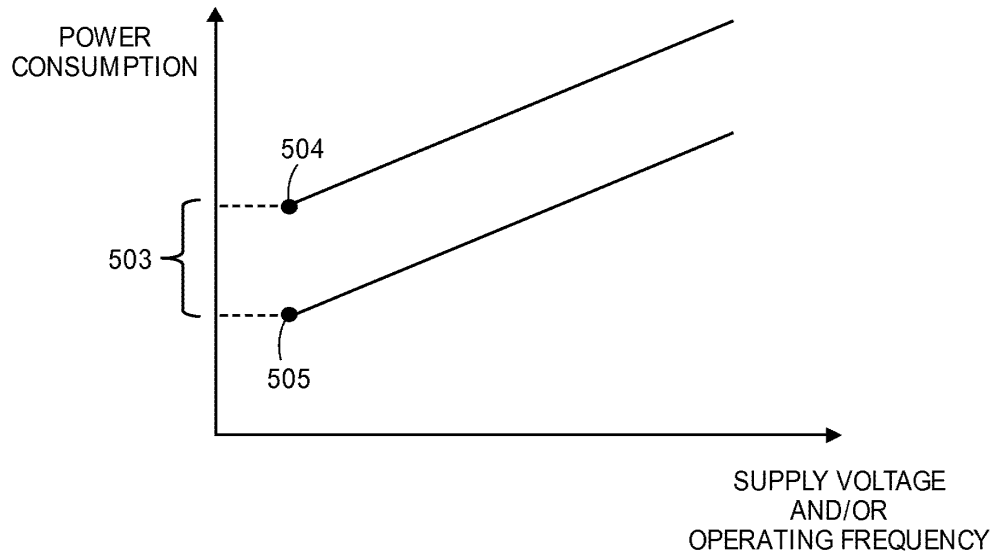


FIG. 5

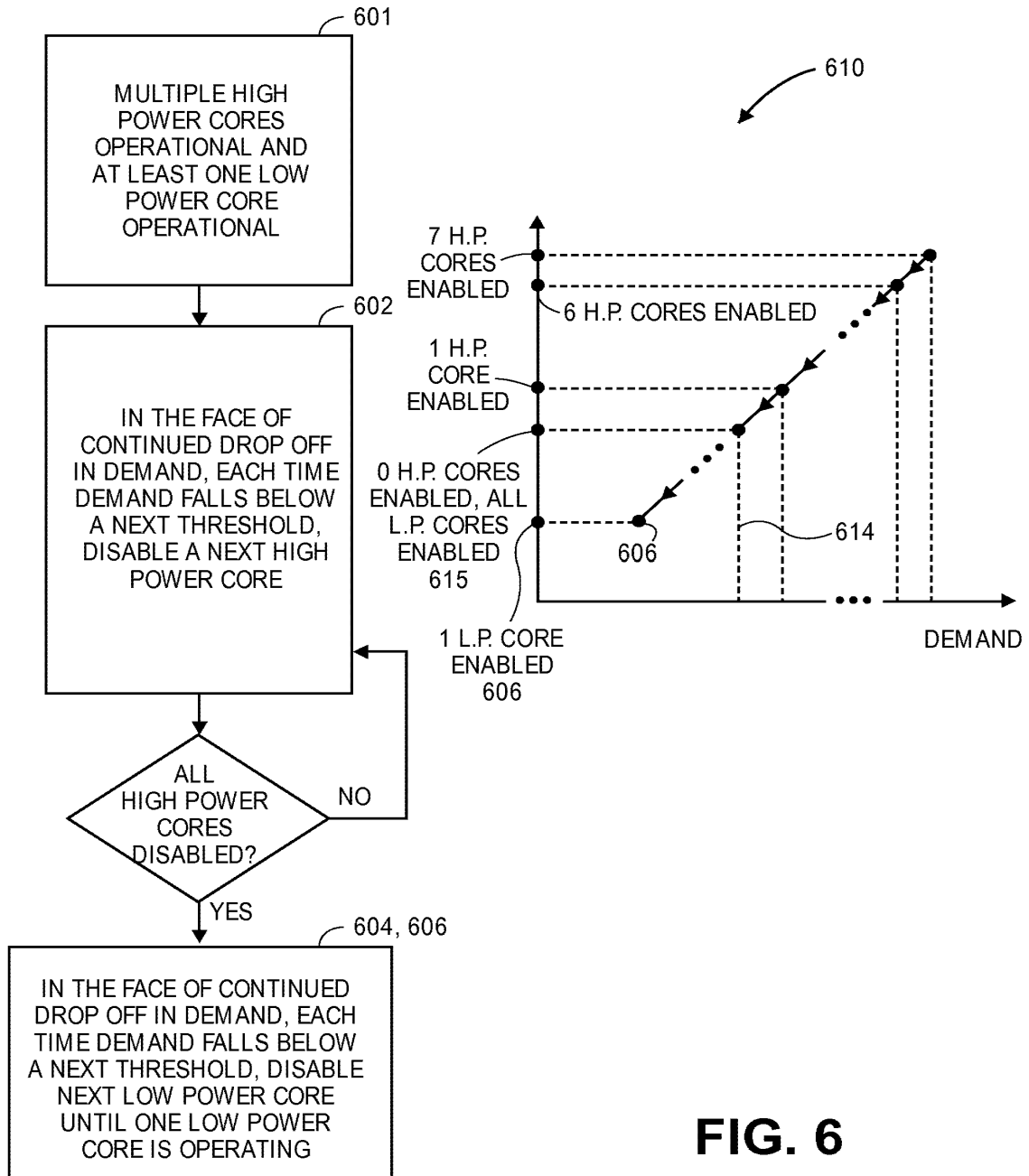
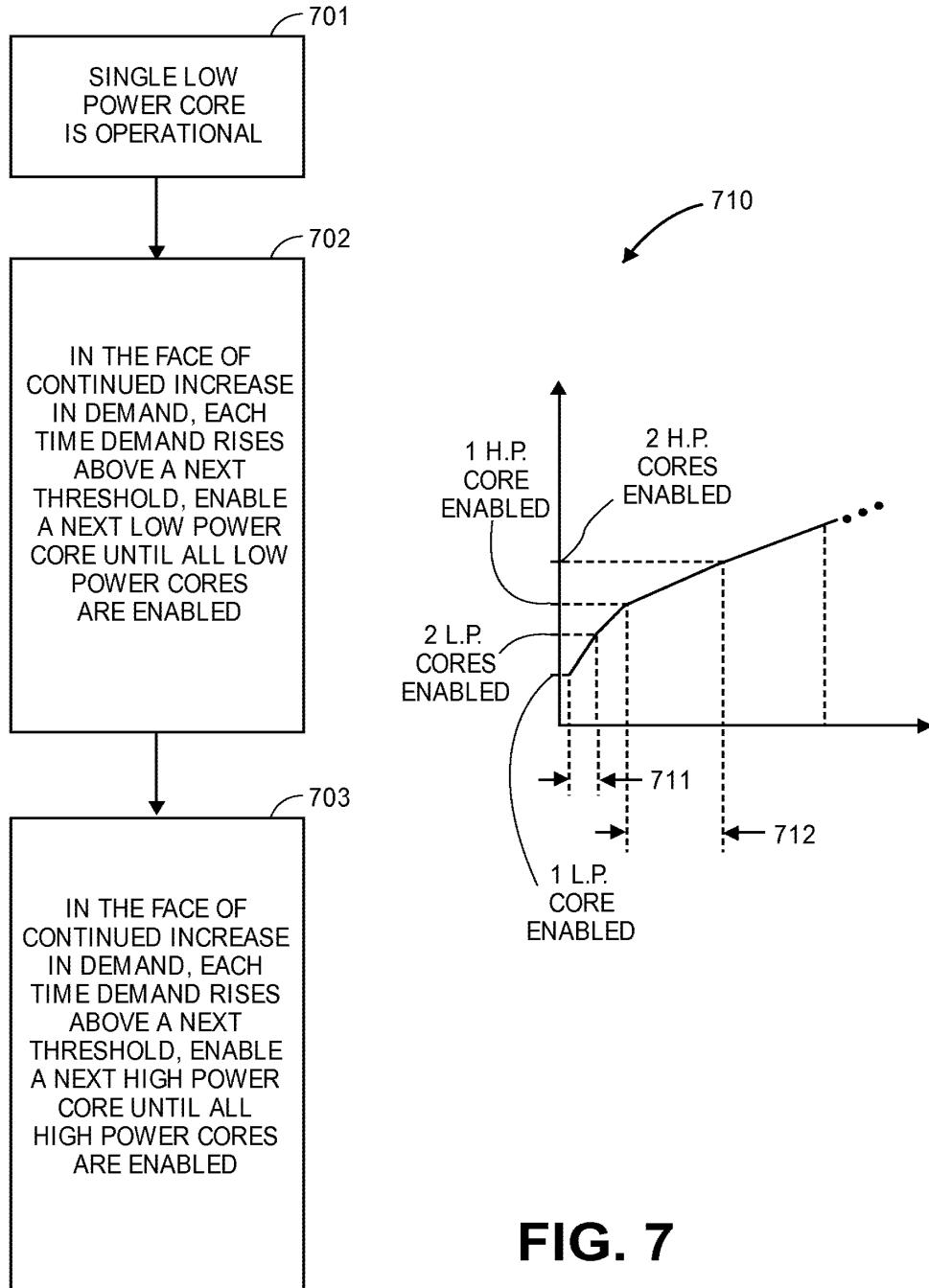


FIG. 6



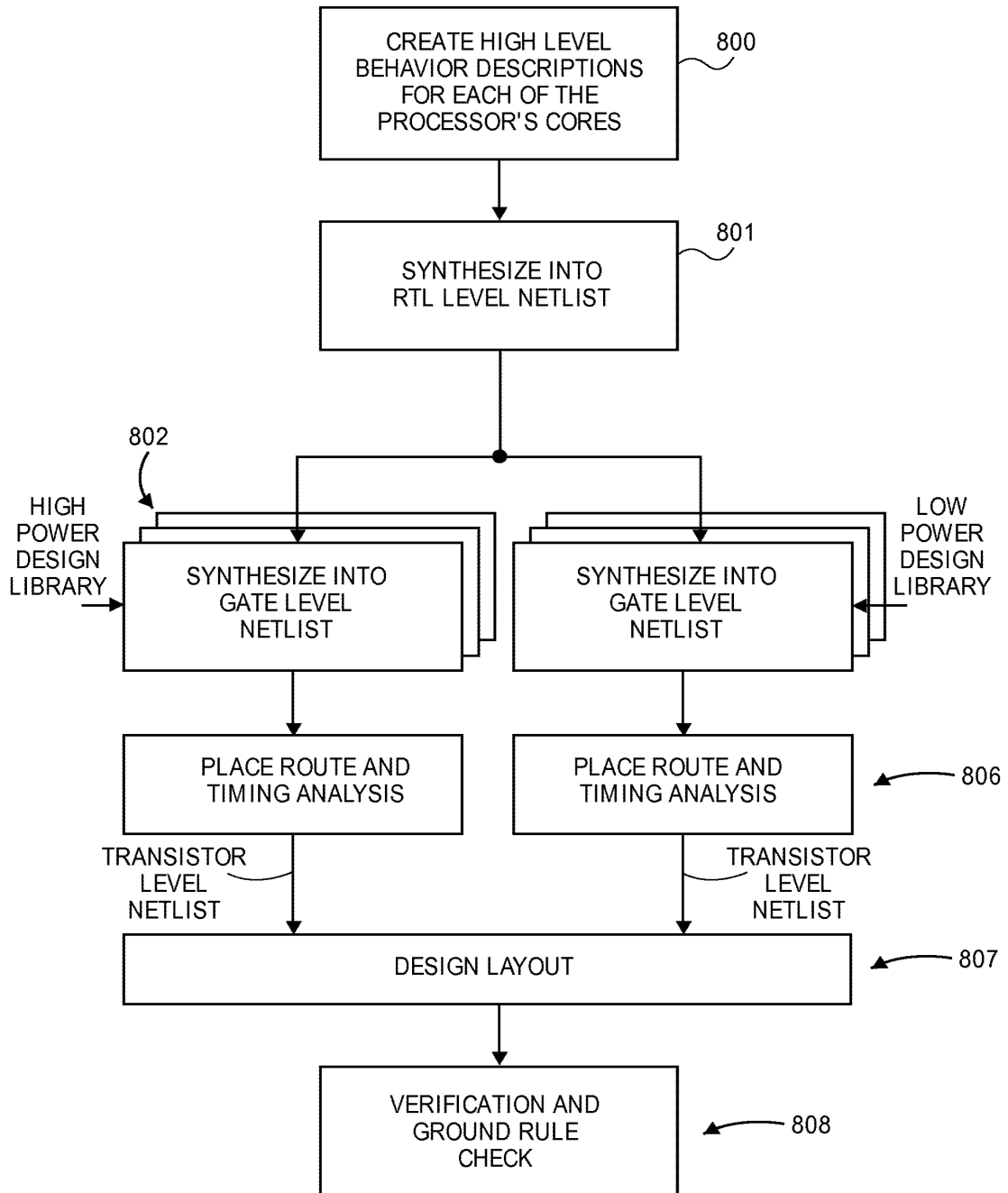


FIG. 8

Electronic Patent Application Fee Transmittal

Application Number:	13335257			
Filing Date:	22-Dec-2011			
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE			
First Named Inventor/Applicant Name:	Varghese George			
Filer:	Scott Alan Simmons/allison madsen			
Attorney Docket Number:	42P38886			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	23427091
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	45209
Filer:	Scott Alan Simmons/allison madsen
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	08-SEP-2015
Filing Date:	22-DEC-2011
Time Stamp:	15:28:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1200
RAM confirmation Number	2196
Deposit Account	504238
Authorized User	SIMMONS, SCOTT

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)
 Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)
 Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38886_RFOA_09_08_15.pdf	54220 fd4ef8583ae4d2c36da38a7f5148f9cbedac bec2	yes	10
Multipart Description/PDF files in .zip description					
	Document Description		Start		End
	Amendment Submitted/Entered with Filing of CPA/RCE		1		1
	Claims		2		5
	Drawings-only black and white line drawings		6		6
	Applicant Arguments/Remarks Made in an Amendment		7		10
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	P38886_RCE_09_08_15.pdf	697609 930083fcd7e89fa417c13b1c2213c5c39294 c222	no	3
Warnings:					
Information:					
3	Drawings-only black and white line drawings	P38886_Replacement_figs_v2.pdf	314427 92e9b58fca33e97766fc1b79cfab3ad6aa46 9bde	no	8
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30619 f7a3118659e5e9dfabe8c18f15a7e8ddb35 9c6f	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1096875		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney's Docket No.: 42P38886

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Varghese George

Examiner: Nielsen, Keith A.

Application No.: 13/335,257

Art Unit: 2183

Filed: December 22, 2011

Confirmation No.: 6542

For: ASYMMETRIC PERFORMANCE
MULTICORE ARCHITECTURE WITH
SAME INSTRUCTION SET
ARCHITECTURE

Mail Stop Amendment
Commissioner for Patents
e-Filed via EFS-WEB

AMENDMENT AND RESPONSE WITH REQUEST FOR CONTINUED

EXAMINATION (RCE) UNDER 37 C.F.R. §1.114

Sir:

In response to the Final Office action transmitted on May 5, 2015, the Applicant respectfully requests continued examination of the application and that the Examiner enter the following amendments and consider the following remarks.

CERTIFICATE OF EFS-Web

I hereby certify that this correspondence is being submitted electronically via EFS-Web on the date shown below to the United States Patent and Trademark Office.

Date of Deposit: 09-08-2015

Name of Person Mailing Correspondence: Allison Madsen

Signature: /Allison Madsen/

Appl. No.: 13/335,257
Amdt. dated 09/08/15
Reply to the Final Office action of 05/05/15

1

Atty. Docket No.: 42P38886

Petitioner Mercedes Ex-1010, 0085

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please amend the claims as follows:

1. (Currently amended) A multi-core processor comprising:

a first plurality of cores and a second plurality of cores that support a same instruction set, wherein ~~at least two of the~~ second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than ~~at least one other of the~~ first plurality of cores; and

power management hardware to, from an initial state where the first plurality of cores and the second plurality of cores are enabled, disable an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, and disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled.

2. (Currently amended) The multi-core processor of claim 1 wherein the ~~at least two of the~~ second plurality of cores include logic gates that have narrower logic gate driver transistors than a corresponding logic gate of the ~~at least one other of the~~ first plurality of cores.

3. (Currently amended) The multi-core processor of claim 1 wherein the ~~at least two of the~~ second plurality of cores comprise logic gates that consume less power than a corresponding logic gate of the ~~at least one other of the~~ first plurality of cores.

4. (Currently amended) The multi-core processor of claim 1 wherein the ~~at least two of the~~ second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the ~~at least one other of the~~ first plurality of cores.

5. (Currently amended) The multi-core processor of claim 1 further comprising a switch fabric between the first plurality of cores, the second plurality of cores, and a system memory interface.

6. (Currently amended) A method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, ~~[[a]]the first core of the plurality of cores being higher performance and consuming more power than [[a]]the second set of cores of the plurality of cores~~ under a same applied supply voltage and operating frequency; and

disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, and then disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled.

7-9. (Canceled)

10. (Currently amended) The method of claim 6 wherein the operating of the first plurality of cores includes driving load lines with wider transistor widths than corresponding transistor widths in said second~~[[set]]~~ plurality of cores.

11. (Currently amended) The method of claim 6 further comprising lowering at least one of a supply voltage and an operating frequency of said ~~first one~~ core in response to lower demand being offered to said multi-core processor.

12. (Currently amended) The method of claim ~~[[6]]~~11 further comprising raising at least one of a supply voltage and an operating frequency of said ~~first one~~ core in response to higher demand being offered to said multi-core processor.

13. (Currently amended) The method of claim 6 further comprising:

raising at least one of a supply voltage and an operating frequency of said one core in response to higher demand being offered to said multi-core processor ~~disabling said first core in response to a drop in demand applied to said multi-core processor; and lowering at least~~

~~one of a supply voltage and an operating frequency of said second set of cores in response to an additional drop in demand applied to said multi-core processor.~~

14. (Currently amended) A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, ~~[[a]]~~the first core of the plurality of cores being higher performance and consuming more power than a second set of cores of the plurality of cores under a same applied supply voltage and operating frequency; and

disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, and then disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled.

15-16. (Canceled)

17. (Currently amended) The non-transitory machine readable medium of claim 14 wherein said method further comprises lowering at least one of a supply voltage and an operating frequency of said ~~first one~~ core in response to lower demand being offered to said multi-core processor.

18. (Currently amended) The non-transitory machine readable medium of claim ~~[[14]]~~ 17 wherein said method further comprises raising at least one of a supply voltage and an operating frequency of said ~~first one~~ core in response to higher demand being offered to said multi-core processor.

19. (Currently amended) The non-transitory machine readable medium of claim 14 wherein said method further comprises raising at least one of a supply voltage and an operating frequency of said one core in response to higher demand being offered to said

~~multi-core processor: disabling said first core in response to a drop in demand applied to said multi-core processor; and~~

~~lowering at least one of a supply voltage and an operating frequency of said second set of cores in response to an additional drop in demand applied to said multi-core processor.~~

20. (Canceled)

21. (New) The multi-core processor of claim 1 wherein the power management hardware is to lower at least one of a supply voltage and an operating frequency of each additional core to a lower operating level before disablement.

22. (New) The multi-core processor of claim 1 wherein the power management hardware is to enable an additional core of the second plurality of cores for each continued increase in demand above a next higher threshold without enabling any of the first plurality of cores until the second plurality of cores is enabled, and enable an additional core of the first plurality of cores for each continued increase in demand above a next higher threshold until the first plurality of cores is also enabled.

23. (New) The multi-core processor of claim 1 wherein the power management hardware is to lower at least one of a supply voltage and an operating frequency of said one core in response to lower demand.

24. (New) The multi-core processor of claim 1 wherein the power management hardware is to raise at least one of a supply voltage and an operating frequency of said one core in response to higher demand.

25. (New) The method of claim 6 further comprising lowering at least one of a supply voltage and an operating frequency of each additional core to a lower operating level before disablement.

26. (New) The non-transitory machine readable medium of claim 14 wherein said method further comprises lowering at least one of a supply voltage and an operating frequency of each additional core to a lower operating level before disablement.

Amendments to the Drawings:

The attached replacement drawings (FIGS. 1-8) replace previous FIGS. 1-8.

Attachment: Replacement Sheets (FIGS. 1-8)

REMARKS

The Applicant sincerely thanks Examiner Nielsen for the phone interview on August 5, 2015.

(1) Interview Summary:

In the call, the Examiner and Applicant's representative discussed the claim rejections and potential claim amendments.

(2) Response to the Office Action

The enclosed is responsive to the Examiner's Final Office action transmitted on May 5, 2015 and is being filed pursuant to a Request for Continued Examination (RCE) as provided under 37 CFR 1.114. Claims 1-6, 10-14, 17-19, and 21-26 are pending, with claims 1, 6, and 14 being independent. Claims 7-9, 15, 16, and 20 have been cancelled. Claims 1-6, 10-14, and 17-19 have been amended. Claims 21-26 have been added. No new subject matter has been added. The Applicant respectfully request reconsideration of the present application and the allowance of all claims now presented.

35 U.S.C. § 103 Rejections

Claims 1-20 were rejected under pre-AIA 35 U.S.C. 103(a) as being allegedly unpatentable over Sutardja et al., U.S. Publication No. 2008/0288748 (hereinafter "Sutardja"), in view of Grochowski et al., U.S. Patent No. 2006/0095807 (hereinafter "Grochowski"). Aruj, "Evolution: 20 years of switching fabric" (hereinafter "Aruj"), was referenced for claim 5 as alleged extrinsic evidence of a system bus being a switch fabric.

Sutardja and the cited portion of Grochowski do not teach or suggest the Applicant's claims. For example, Sutardja and the cited portion of Grochowski do not teach or suggest:

1. A multi-core processor comprising:
a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and
power management hardware to, from an initial state where the first plurality of cores and the second plurality of cores are enabled, disable an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores

is disabled, and disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled. (Emphasis added.)

as in Applicant's independent claim 1, or:

6. A method comprising:
operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, the first plurality of cores being higher performance and consuming more power than the second plurality of cores under a same applied supply voltage and operating frequency; and
disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, and then disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled. (Emphasis added.)

as in Applicant's independent claim 6, or:

14. A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:
operating a multi-core processor such that a first plurality of cores and a second plurality of cores support respective software routines with a same instruction set, the first plurality of cores being higher performance and consuming more power than a second plurality of cores under a same applied supply voltage and operating frequency; and
disabling with power management hardware, from an initial state where the first plurality of cores and the second plurality of cores are enabled, an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, and then disabling an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the first plurality of cores remains enabled. (Emphasis added.)

as in Applicant's independent claim 14.

Because the Applicant has demonstrated the patentability of all pending independent claims, the Applicant respectfully submits that all pending claims are allowable. The Applicant's silence with respect to the dependent claims should not be construed as an admission by the Applicant that the Applicant is complicit with the Examiner's rejection of these claims. Because the Applicant has demonstrated the patentability of the independent

claims, the Applicant need not substantively address the theories of rejection applied to the dependent claims.

In light of the comments above, Applicant respectfully requests the allowance of all claims.

CONCLUSION

Applicant respectfully submits that all rejections have been overcome and that all pending claims are in condition for allowance. If the Examiner believes an additional telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Scott A. Simmons at (408) 675-0441. Authorization is hereby given to charge our Deposit Account No. 504238 for any charges that may be due.

Respectfully submitted,
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP

Date: 09-08-2015

/Scott A. Simmons/
Scott A. Simmons
Reg. No.: 60,206

217 High Street
Palo Alto, CA 94301
(408) 675-0441

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

**REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)**

Application Number	13335257	Filing Date	2011-12-22	Docket Number (if applicable)	42P38886	Art Unit	2183
First Named Inventor	Varghese George			Examiner Name	NIELSEN, KEITH A		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

Other _____

Enclosed

Amendment/Reply

Information Disclosure Statement (IDS)

Affidavit(s)/ Declaration(s)

Other _____

MISCELLANEOUS

Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 504238

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Patent Practitioner Signature

Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Scott A. Simmons/	Date (YYYY-MM-DD)	2015-09-08
Name	Scott A. Simmons	Registration Number	60206

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/335,257	Filing Date 12/22/2011	<input type="checkbox"/> To be Mailed	
ENTITY: <input checked="" type="checkbox"/> LARGE <input type="checkbox"/> SMALL <input type="checkbox"/> MICRO							
APPLICATION AS FILED – PART I							
(Column 1)			(Column 2)				
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A				
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A	N/A				
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A				
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	minus 20 =	*	X \$ =				
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =				
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL				
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT	09/08/2015	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X \$80 = 0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$420 = 0	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))						
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0	
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=		
	Independent (37 CFR 1.16(h))	*	Minus	***	=		
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))						
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE		
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>							

LIE
/TAMIE JARRETT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

Practitioners associated with the Customer Number:

131413

OR

Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:



The address associated with Customer Number:

131413

OR

<input type="checkbox"/> Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

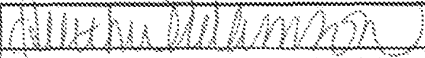
Assignee Name and Address:

Intel Corporation
2200 Mission College Boulevard
Santa Clara, California, 95054

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	6/17/2015
Name	Heather Adamson	Telephone	
Title	Administrator of Patents, Intel Corporation		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. This information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEE OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	23371389
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	45209
Filer:	Scott Alan Simmons/allison madsen
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	01-SEP-2015
Filing Date:	22-DEC-2011
Time Stamp:	15:15:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	P38886_373b_sb0096.pdf	422824 e6d9b56a8005bc6988b90db6factb4359c2a5d40	no	2

Warnings:

Information:

2	Power of Attorney	Pre_AIA_POA.PDF	376185 05cd888c171a0f9d5a4eec633288cd76d99656d	no	1
Warnings:					
Information:					
Total Files Size (in bytes):				799009	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Intel Corporation

Application No./Patent No.: 13/335,257

Filed/Issue Date: December 22, 2011

Titled: **ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE**

Intel Corporation, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

- 1. the assignee of the entire right, title, and interest in;
- 2. an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or
- 3. the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 028046, Frame 0420, or for which a copy therefore is attached.

OR

B. A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet(s).

As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Scott A. Simmons/

September 1, 2015

Signature

Date

Scott A. Simmons, Reg. No. 60,206

Attorney

Printed or Typed Name

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	Varghese George	42P38886	6542

45209 7590 08/14/2015
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER

NIELSEN, KEITH A

ART UNIT	PAPER NUMBER
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2183

NOTIFICATION DATE	DELIVERY MODE
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08/14/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteldocs_docketing@cpaglobal.com
Database_Group@bstz.com

Applicant-Initiated Interview Summary	Application No. 13/335,257	Applicant(s) GEORGE ET AL.	
	Examiner KEITH NIELSEN	Art Unit 2183	

All participants (applicant, applicant's representative, PTO personnel):

(1) KEITH NIELSEN. (3) Scott Simmons, Reg. No. 60,206.
(2) Andrew Caldwell, SPE. (4) _____.

Date of Interview: 05 August 2015.

Type: Telephonic Video Conference
 Personal [copy given to: applicant applicant's representative]

Exhibit shown or demonstration conducted: Yes No.
If Yes, brief description: _____.

Issues Discussed 101 112 102 103 Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: Sutardja, Grochowski.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

On August 5, 2015, the Examiner called the Applicant's representative Scott Simmons to conduct the interview. The issues outlined in the attached agenda were discussed. Specifically, the details of paragraphs 33-37 of the instant application were discussed. In order to advance prosecution, Examiner suggested reciting more specific limitations in the claim such as the steps to achieve the lower power and frequency and the structure used to perform the functions.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Attachment

/K. N./ Examiner, Art Unit 2183	/ANDREW CALDWELL/ Supervisory Patent Examiner, Art Unit 2183
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Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Attachment to Interview Summary

Nielsen, Keith

From: Scott Simmons <scott@nicholsondevos.com>
Sent: Monday, August 03, 2015 11:22 PM
To: Nielsen, Keith
Subject: Agenda for call on Tuesday August 4, 2015 (U.S. Pat. App. No. 13/335,257)

Examiner Nielsen,

Two matters:

(1) Thank you for agreeing to speak with me about U.S. Pat. App. No. 13/335,257 (George et al.) on Tuesday August 4, 2015. I will initiate the call to your work number at 4:30 pm (Eastern time) unless you indicate otherwise.

(2) Proposed Agenda (for discussion purposes only, not for official entry):

- (i) Discussion of the claim rejections of the Office action transmitted on May 5, 2015;
- (ii) Discussion of the Sutardja and Grochowski references; and
- (iii) Discussion of paragraphs [0034]-[0037] and FIGS. 6-7 of the Applicant's published patent application.

Best regards,
Scott

Scott A. Simmons | Attorney at Law (*licensed in Texas and Colorado)
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP
217 High Street | Palo Alto, CA 94301
Main: 408-675-0441

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	Varghese George	42P38886	6542

45209 7590 05/05/2015
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER

NIELSEN, KEITH A

ART UNIT	PAPER NUMBER
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2183

NOTIFICATION DATE	DELIVERY MODE
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05/05/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteldocs_docketing@cpaglobal.com
Database_Group@bstz.com

Office Action Summary	Application No. 13/335,257	Applicant(s) GEORGE ET AL.	
	Examiner KEITH NIELSEN	Art Unit 2183	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 4/13/2015.
 A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) Claim(s) _____ is/are allowed.
- 7) Claim(s) 1-20 is/are rejected.
- 8) Claim(s) _____ is/are objected to.
- 9) Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) The specification is objected to by the Examiner.
- 11) The drawing(s) filed on 4/13/2015 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) All b) Some** c) None of the:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 1/9/2015
- 3) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 4) Other: _____

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. New claim 20 has been added.
3. Claims 1-20 are presented for examination.

Drawings

4. The drawings filed 4/13/2015 are acceptable for examination.

Claim Objections

5. Claim 11 is objected to because of the following informalities:
 - Claim 11, line 3 - insert a hyphen between "multi" and "core"
6. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sutardja et al. (US Patent Publication No. 2008/0288748) in view of Grochowski et

al. (US Patent Publication No. 2006/0095807). Aruj, "Evolution: 20 years of switching fabric" is referenced for claim 5 as extrinsic evidence of a system bus being a switch fabric.

9. As per claim 1, Sutardja teaches **a multi-core processor** (e.g. Figs. 3A, 3B - HP and LP cores) **comprising a plurality of cores that support a same instruction set** ([0214], [0225]), **wherein [a core] of the plurality of cores consume less power, for a same applied operating frequency and supply voltage, than at least one other of the plurality of cores** ([0230] - transistors of the HP core consume more power than the transistors of the LP core. The size of the transistors and gates in the HP core are larger than the size of the transistors and gates of the LP core). Sutardja does not specifically teach that there are at least two lower power cores. Rather, Sutardja teaches a single lower power core and one or a multiple of higher power cores.

However, Grochowski teaches that a plurality of smaller 'B cores' may be enabled to reduce the throughput performance discontinuity gap when switching off a larger 'A core' ([0033]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a plurality of smaller and lower power cores in an asymmetric multiprocessing system such as taught by Grochowski in the invention of Sutardja. One would have been motivated to reduce the performance gap between a single low power core and a single high power core.

10. As per claim 2, Sutardja and Grochowski teach **the multi-core processor of claim 1**. Sutardja further teaches **wherein the at least two of the plurality of cores include logic gates that have narrower logic gate driver transistors than a corresponding logic gate of the at least one other of the plurality of cores** ([0230] - size of the gates of the transistors of the LP core are smaller than the gates of the transistors of the HP core).

11. As per claim 3, Sutardja and Grochowski teach **the multi-core processor of claim 1**. Grochowski further teaches **wherein the at least two of the plurality of cores comprise logic gates that consume less power than a corresponding logic gate of the at least one other of the plurality of cores** ([0230] - transistors of the HP core consume more power than the transistors of the LP core).

12. As per claim 4, Sutardja and Grochowski **teach the multi-core processor of claim 1**. Sutardja further teaches **wherein the at least two of the plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the at least one other of the plurality of cores** ([0234] - HP core may operate greater than 1 GHz while the LP core may operate at less than or equal to 500 MHz).

13. As per claim 5, Sutardja and Grochowski teach **the multi-core processor of claim 1**. Sutardja further teaches **a switch fabric between the plurality of cores and**

a system memory interface (e.g. Fig. 11E, [0327] - system bus. One of ordinary skill in the art would have considered the system bus a switching fabric at the time of the invention as shown by Aruj, "Evolution: 20 years of switching fabric". On page 1, "Shared Bus", Aruj shows a shared bus being a form of switching fabric).

14. As per claim 6, Sutardja teaches **a method comprising: operating a multi core processor such that a plurality of cores support respective software routines with a same instruction set, a first core of the plurality of cores being higher performance and consuming more power than a second [...] core of the plurality of cores under a same applied supply voltage and operating frequency** ([0212], [0213], [0230] - HP core is a high power, high performance core. LP core is low power, lower performance core).

Sutardja does not specifically teach that there are at least two lower power cores. Rather, Sutardja teaches a single lower power core and one or a multiple of higher power cores.

However, Grochowski teaches that a plurality of smaller 'B cores' may be enabled to reduce the throughput performance discontinuity gap when switching off a larger 'A core' ([0033]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a plurality of smaller and lower power cores in an asymmetric multiprocessing system such as taught by Grochowski in the invention of

Sutardja. One would have been motivated to reduce the performance gap between a single low power core and a single high power core.

15. Claim 14 is a machine readable medium corresponding to claim 6 and is rejected for the same reason as set forth in the rejection of claim 6.

16. As per claim 7, Sutardja and Grochowski teach **the method of claim 6**. Sutardja further teaches **disabling the first core but leaving at least one of the second set of cores operable in response to lower demand being offered to the multi-core processor** ([0218], [0305] - deactivate the HP core and process the application on the LP core when performance demanded by the application is not optimal on the HP core).

17. Claim 20 is a machine readable medium corresponding to claim 7 and is rejected for the same reason as set forth in the rejection of claim 7.

18. As per claim 8, Sutardja and Grochowski **teach the method of claim 6**. Sutardja further teaches **enabling the first core after it is disabled in response to a higher demand being offered to the multi-core processor** ([0303] - activate the HP core (Core2) when processing on the LP core is at its maximum).

19. Claim 15 is a machine readable medium corresponding to claim 8 and is rejected for the same reason as set forth in the rejection of claim 8.

20. As per claim 9, Sutardja and Grochowski teach **the method of claim 6**. Sutardja further teaches **wherein the method further comprises: disabling said first core**

after detecting a first drop in demand offered to said multi-core processor ([0305]

- deactivate the HP core when application demand is decreased); **and enabling said**

first core after detecting a first rise in demand offered to said multi-core

processor ([0303] - activate HP core when application demand is more than is efficient

with the LP core. [0294] - core switching may occur based on a threshold, e.g. number

of applications where the HP core is used when the number of applications is 10 or

more, and the LP core is used when the number of applications is less than 10).

21. Claim 16 is a machine readable medium corresponding to claim 9 and is rejected for the same reason as set forth in the rejection of claim 9.

22. As per claim 10, Sutardja and Grochowski teach **the method of claim 6**.

Sutardja further teaches **wherein the operating of the first core includes driving**

load lines with wider transistor widths than corresponding transistor widths in

said second set of cores ([0230] - the size of the transistors and gates in the HP core

are larger than the size of the transistors and gates of the LP core).

23. As per claim 11, Sutardja and Grochowski teach **the method of claim 6**.

Sutardja further teaches **lowering at least one of a supply voltage and an operating**

frequency of said first core in response to lower demand being offered to said

multicore processor ([0304] - voltage/frequency can be raised and lowered according

to the performance demanded by the application).

24. Claim 17 is a machine readable medium corresponding to claim 11 and is rejected for the same reason as set forth in the rejection of claim 11.

25. As per claim 12, Sutardja and Grochowski teach **the method of claim 6**. Sutardja further teaches **raising at least one of a supply voltage and an operating frequency of said first core in response to higher demand being offered to said multi-core processor** ([0304] - voltage/frequency can be raised and lowered according to the performance demanded by the application).

26. Claim 18 is a machine readable medium corresponding to claim 12 and is rejected for the same reason as set forth in the rejection of claim 12.

27. As per claim 13, Sutardja and Grochowski teach **the method of claim 6**. Sutardja further **teaches disabling said first core in response to a drop in demand applied to said multi-core processor** ([0305] - deactivate the HP core when performance demanded by the application is decreased); **and lowering at least one of a supply voltage and an operating frequency of said second set of cores in response to an additional drop in demand applied to said multi-core processor** ([0301]-[0302] - LP frequency and voltage may be lowered when performance demand is low).

28. Claim 19 is a machine readable medium corresponding to claim 13 and is rejected for the same reason as set forth in the rejection of claim 13.

Response to Arguments

29. Applicant's arguments, see page 8 of the Remarks, filed 4/13/2015, with respect to the rejection(s) of claim(s) 1-2 and 4-19 under 35 USC 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sutardja et al. and Grochowski et al. See the rejections of claims 1 and 6 above.

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

31. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH NIELSEN whose telephone number is (571)270-

3584. The examiner can normally be reached on Monday-Friday, 9:00am - 6:00pm, Alt. Friday, EDT.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on 571-272-3702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BORIS GORNEY/
Supervisory Patent Examiner, Art
Unit 2183

/K. N./
Examiner, Art Unit 2183

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	(varghese near2 george.in. or sanjeev near2 jahagirdar.in. or deborah near2 marr.in.) and @pd> "20141226"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:01
L2	10	712/43,32.ccls. and @pd> "20141226"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:01
L3	5	2 and (disabl\$3 or enabl\$3 or activat\$3 or de\$1activat\$3) near4 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:02
L4	1011	g06f9/5094.cpc.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:03
L5	668	g06f1/3293.cpc.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:03
L6	0	go6f1/3296.cpc.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:03
L7	2108	g06f1/3296.cpc.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:04
L8	953	(4 or 5 or 7) and (disabl\$3 or enabl\$3 or activat\$3 or de\$1activat\$3) near4 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:04
L9	560	8 and (less or lower or low) near4 (performance or power) near3 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:04
L10	34	9 and @pd> "20141226"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:04
L11	7	10 and asymmetric	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:10
L12	985	(narrower or wider or larger or smaller) near4 (logic gate or driver) near3 transistor	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:13

EAST Search History

L13	32	12 and (core or processor) near6 (power or frequency) near4 (high\$2 or low\$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:13
L14	0	13 and @pd> "20141226"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:14
L15	9085	(low or lower) near2 (power or performance) near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:14
L16	13706	(high or higher) near2 (power or performance) near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:14
L17	1021	15 same 16	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:15
L18	422	17 and (low or lower) near2 (power or performance) near2 (cores! or processors!)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:15
L19	44	18 and "7"?? clas. and (disabl\$3 or deactivat\$3) near3 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:15
L20	103	(plurality or multiple) adj3 (low or lower) near2 (power or performance) near3 (cores! or processors!)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:16
L21	287	asymmetric near (multi\$1processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:16
L22	4574	(disabl\$3 or deactivat\$3) near3 (core or processor) same1 power	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:17
L23	8	21 and 22	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2015/04/29 13:17

EAST Search History (Interference)

< This search history is empty >

4/ 29/ 2015 1:18:19 PM

C:\Users\knielsen\Documents\EAST\Workspaces\13335257.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application No.	13/335,257
	Filing Date	December 22, 2011
	First Inventor	Varghese George, et al.
	Art Unit	2183
	Examiner Name	NIELSEN, KEITH A
	Attorney Docket No.	42P38886

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The references listed were cited in a communication in a counterpart Taiwanese application on September 29, 2014.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

None

The IDS Filing Fee in the amount of \$180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Scott A. Simmons/	Date (MM-DD-YYYY)	01-09-2015
Name/Print	Scott A. Simmons	Registration Number	60206

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

/Debbie Casias/ _____ Date 01-09-15

The collection of information is required by 37 C.F.R. 1.97 and 1.98. This information is required to obtain or retain a benefit by the public which is in the best of the USPTO to process an application. Certification is governed by 35 U.S.C. 122 and 37 C.F.R. 1.14. The collection is necessary to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete the form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22315-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22315-1480.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	13/335,257
	Filing Date	12/22/2011
	First Named Inventor	Varghese George
	Group Art Unit	2183
	Examiner Name	NIELSEN, KEITH A
Sheet 1 of 1	Attorney Docket No: 42P38886	


US PATENT DOCUMENTS					
Examiner Initial *	Cite No. ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Page, Column, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Copy of Notice of Allowance from TW counterpart Application No. 101147200, (Atty. Docket No. 42P38886TW), Mailed September 29, 2014, 1 page.	

EXAMINER /KEITH NIELSEN/ DATE CONSIDERED 04/29/2015

Based on FIC51826A(02-04) - Substitute Disclosure Statement Form (PTO-1449) as modified by BPTZ 03/05/07
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). Applicant is to place a check mark here if English language Translation is attached.

Search Notes 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.
	Examiner KEITH NIELSEN	Art Unit 2183

CPC- SEARCHED		
Symbol	Date	Examiner
G06F1/3293,3296	12/26/2014	KN
G06F1/3293,3296 (updated)	4/29/2015	KN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
712	32,43	12/26/2014	KN
712	32,43 (updated)	4/29/2015	KN

SEARCH NOTES		
Search Notes	Date	Examiner
East text search	12/26/2014	KN
Inventor name search	12/26/2014	KN
Updated east text search (see search history printout)	4/29/2015	KN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	Varghese George	42P38886	6542

45209 7590 04/20/2015
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER

NIELSEN, KEITH A

ART UNIT	PAPER NUMBER
----------	--------------

2183

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

04/20/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteldocs_docketing@cpaglobal.com
Database_Group@bstz.com

Applicant-Initiated Interview Summary	Application No. 13/335,257	Applicant(s) GEORGE ET AL.	
	Examiner KEITH NIELSEN	Art Unit 2183	

All participants (applicant, applicant's representative, PTO personnel):

(1) KEITH NIELSEN. (3)_____.

(2) Scott Simmons, Reg. No. 60,206. (4)_____.

Date of Interview: 13 April 2015.

Type: Telephonic Video Conference
 Personal [copy given to: applicant applicant's representative]

Exhibit shown or demonstration conducted: Yes No.
If Yes, brief description: _____.

Issues Discussed 101 112 102 103 Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: Sutardja et al. (US Pub. 2008/0288748).

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

On 4/13/2015, Applicant telephoned Examiner to conduct the interview. The matters outlined in the attached agenda were discussed. Specifically, it was discussed that the instant application has multiple lower power cores, where Sutardja only discloses one. Examiner stated that the proposed amendment to claim 1 would appear to overcome the 102(b) rejection over Sutardja. However, additional search and consideration would be required. Examiner suggested replacing "multiple" with --at least two-- in the proposed amendment to avoid a potential grammatical issue. An agreement was not reached at the time of the interview.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Attachment

/K. N./
Examiner, Art Unit 2183

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Attachment to Interview Summary

Nielsen, Keith

From: Scott Simmons <scott@nicholsondevos.com>
Sent: Monday, April 13, 2015 12:07 AM
To: Nielsen, Keith
Subject: Agenda for call on Monday April 13, 2015 (U.S. Pat. App. No. 13/335,257)

Examiner Nielsen,

Two matters:

(1) Thank you for agreeing to speak with me about U.S. Pat. App. No. 13/335,257 (George et al.) on Monday April 13, 2015. I will initiate the call to your work number at 3:30 pm (Eastern time).

(2) Proposed Agenda (for discussion purposes only, not for official entry):

- (i) Discussion of the claim rejections of the Office action transmitted on January 12, 2015;
- (ii) Discussion of the Sutardja reference; and
- (iii) Discussion of the proposed amendment to claim 1 below (and the corresponding amendments to the other independent claims):

- 1. (Currently amended) A multi-core processor comprising:
a plurality of cores that support a same instruction set, wherein at least one multiple of the cores ~~is constructed of logic gates that~~ consume less power, for a same applied operating frequency and supply voltage, than ~~the same corresponding logic gates of~~ at least one other of the cores.

Best regards,
Scott

Scott A. Simmons | Attorney at Law (*licensed in Texas and Colorado)
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP
217 High Street | Palo Alto, CA 94301
Main: 408-675-0441

The information contained in this message may be privileged and/or confidential. If the reader of this message is not the intended recipient, or an employee or agent responsible for delivering this message to the intended recipient, you are hereby notified that any dissemination, distribution or copying of this communication is strictly prohibited. If you have received this communication in error, please notify us immediately by replying to the message and deleting it from your computer.

Attorney's Docket No.: 42P38886

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Varghese George

Examiner: NIELSEN, KEITH A.

Application No. 13/335,257

Art Unit: 2183

Filed: 12/22/2011

Confirmation No. 6542

For: ASYMMETRIC PERFORMANCE
MULTICORE ARCHITECTURE WITH
SAME INSTRUCTION SET
ARCHITECTURE

Mail Stop Amendment
Commissioner for Patents
e-Filed via EFS-WEB

RESPONSE AND AMENDMENT

Madam:

In response to the Office action mailed January 12, 2015, Applicant respectfully requests the Examiner enter the following amendments and consider the following remarks.

CERTIFICATE OF EFS Web

I hereby certify that this correspondence is being submitted electronically via EFS-Web on the date shown below to the United States Patent and Trademark Office.

Date of Deposit: April 13, 2015

Name of Person Mailing Correspondence: Scott Simmons

Signature: /Scott Simmons/

Appl. No.: 13/335,257
Amdt. Dated April 13, 2015
Reply to Office action of 01/12/2015

1

Atty. Docket No.: 42P38886

Petitioner Mercedes Ex-1010, 0128

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

What is claimed is:

1. (Currently amended) A multi-core processor comprising a plurality of cores that support a same instruction set, wherein ~~in~~ at least two ~~one~~ of the plurality of cores is ~~constructed of logic gates that~~ consume less power, for a same applied operating frequency and supply voltage, than ~~the same corresponding logic gates of~~ at least one other of the plurality of cores.

2. (Currently amended) The multi-core processor of claim 1 wherein the at least two of the plurality of cores include logic gates that ~~consume less power~~ have narrower logic gate driver transistors than ~~a the same~~ corresponding logic gate ~~[[s]]~~ of the at least one other of the plurality of cores.

3. (Currently amended) The multi-core processor of claim 1 wherein ~~there are~~ the at least two of the plurality of cores ~~that are constructed of the~~ comprise logic gates that consume less power than a corresponding logic gate of the at least one other of the plurality of cores.

4. (Currently amended) The multi-core processor of claim 1 wherein the at least two of the plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the at least one other of the plurality of cores ~~only one of the cores is constructed of the logic gates that consume less power.~~

5. (Currently amended) The multi-core processor of claim 1 further comprising a switch fabric between the plurality of cores and a system memory interface.

6. (Currently amended) A method ~~[[,]]~~ comprising:
operating ~~enabled cores of~~ a multi-core processor such that ~~both a plurality of~~ cores support respective software routines with a same instruction set, a first core of the plurality of

cores being higher performance and consuming more power than a second set of cores of the plurality of cores under a same ~~set of~~ applied supply voltage and operating frequency.

7. (Currently amended) The method of claim 6 further comprising:
disabling the first core but leaving at least one of the second set of cores operable in response to lower demand being offered to the multi-core processor.

8. (Currently amended) The method of claim 6 ~~[[7]]~~ further comprising enabling the first core after it is disabled in response to higher demand being offered to the multi-core processor.

9. (Currently amended) The method of claim 6 ~~[[8]]~~ wherein said method further comprises:

disabling said first core after detecting a first drop in demand offered to said multi-core processor; and

enabling said first core after detecting a first rise in demand offered to said multi-core processor; ~~the amount of demand associated with said first drop being greater than the amount of demand associated with said second drop.~~

10. (Currently amended) The method of claim 6 wherein the operating of the first core includes driving load lines with wider transistor widths than corresponding transistor widths in said second set of cores.

11. (Currently amended) The method of claim 6 further comprising lowering at least one of a supply voltage and~~[[/or]]~~ an operating frequency of said first core in response to lower demand being offered to said multicore processor.

12. (Currently amended) The method of claim 6 further comprising raising at least one of a supply voltage and~~[[/or]]~~ an operating frequency of said first core in response to higher demand being offered to said multi-core processor.

13. (Currently amended) The method of claim 6 further comprising:
disabling said first core in response to a drop in demand applied to said multi-core processor; and~~[[,]]~~ lowering at least one of a supply voltage and~~[[/or]]~~ an operating frequency of

said second set of cores in response to an additional drop in demand applied to said multi-core processor.

14. (Currently amended) A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating ~~enabled cores of~~ a multi-core processor such that ~~both a plurality of cores~~ support respective software routines with a same instruction set, a first core of the plurality of cores being higher performance and consuming more power than a second set of cores of the plurality of cores under a same ~~set of~~ applied supply voltage and operating frequency;

~~disabling the first core but leaving the second core operable in response to lower demand being offered to the multi-core processor;~~

15. (Currently amended) The non-transitory machine readable medium of claim 14 wherein said method further comprises enabling the first core after it is disabled in response to higher demand being offered to the multicore processor.

16. (Currently amended) The non-transitory machine readable medium of claim 14 ~~[[15]]~~ wherein said method further comprises:

disabling said first core after detecting a first drop in demand offered to said multi-core processor; and

enabling said first core after detecting a first rise in demand offered to said multi-core processor, ~~the amount of demand associated with said first drop being greater than the amount of demand associated with said second drop.~~

17. (Currently amended) The non-transitory machine readable medium of claim 14 wherein said method further comprises lowering at least one of a supply voltage and~~[[/or]]~~ an operating frequency of said first core in response to lower demand being offered to said multi-core processor.

18. (Currently amended) The non-transitory machine readable medium of claim 14 wherein said method further comprises raising at least one of a supply voltage and~~[[/or]]~~ an

operating frequency of said first core in response to higher demand being offered to said multi-core processor.

19. (Currently amended) The non-transitory machine readable medium of claim 14 wherein said method further comprises: disabling said first core in response to a drop in demand applied to said multi-core processor; and[[[,]]

lowering at least one of a supply voltage and[[[/or]] an operating frequency of said second set of cores in response to an additional drop in demand applied to said multi-core processor.

20. (New) The non-transitory machine readable medium of claim 14 wherein the method further comprises disabling the first core but leaving at least one of the second set of cores operable in response to lower demand being offered to the multi-core processor.

Amendments to the Drawings:

The attached replacement drawings (FIGS. 1-8) include the changes requested by the Examiner. The Applicant and Examiner agreed that FIG. 2 need not be amended.

Attachment: Replacement Sheets (FIGS. 1-8)

REMARKS

The Applicant sincerely thanks Examiner Nielsen for the phone interview on April 13, 2015.

(1) Interview Summary:

In the call, the Examiner and Applicant's representative agreed that Sutardja does not teach or suggest:

1. A multi-core processor comprising:
a plurality of cores that support a same instruction set, wherein at least two of the plurality of cores consume less power, for a same applied operating frequency and supply voltage, than at least one other of the plurality of cores.

Applicant has submitted that claim herein as claim 1 along with similar amendments to the other independent claims.

(2) Response to the Office Action

The enclosed is responsive to the Examiner's Office action mailed on January 12, 2015. Claims 1-19 are pending, with claims 1, 6, and 14 being independent. Claims 1-19 have been amended. No claims have been canceled. Claim 20 has been added. No new subject matter has been added. Applicant respectfully requests reconsideration of the present application and the allowance of all claims now presented.

Objections

Claims 1-2, 4-6 and 14 are objected to because of the following informalities:

- Claim 1, lines 2, 4 - insert --plurality of-- before "cores"
- Claim 2, line 2 - insert --plurality of-- before "cores"
- Claim 4, line 1 - insert --plurality of-- before "cores"
- Claim 5, line 2 - insert --plurality of-- before "cores"
- Claim 6, line 1 - lack of antecedent basis for "both cores"; Examiner suggests rewording to "a first core and a second core".
- Claim 14, line 3 - lack of antecedent basis for "both cores"
- Claim 14 - replace the semicolon at the end of the claim with a period.

Applicant submits that the amendments in this response overcome the objections in the Office action.

Appl. No.: 13/335,257
Amdt. Dated April 13, 2015
Reply to Office action of 01/12/2015

Amendments to the Drawings

Applicant has submitted replacement drawings with the changes as requested by the Examiner. The Applicant and Examiner agreed that FIG. 2 need not be amended.

35 U.S.C. § 101 Rejections

Claims 14-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Applicant thanks the Examiner for his suggestion here and has amended claims 14-19 accordingly.

35 U.S.C. § 102 Rejections

Claims 1-2 and 4-19 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Sutardja et al., US Patent Publication No. 2008/0288748 (hereinafter “Sutardja”). The cited references do not anticipate, teach, or suggest Applicant’s current claims. For example, Sutardja does not anticipate, teach, or suggest:

1. A multi-core processor comprising:
a plurality of cores that support a same instruction set, wherein at least two of the plurality of cores consume less power, for a same applied operating frequency and supply voltage, than at least one other of the plurality of cores.

as in Applicant’s independent claim 1 and similarly in the other independent claims. For example, Sutardja only discusses embodiments having multiple high-power (HP) cores (referred to as a “first asymmetric core” or “Core2” in Sutardja) but a single low-power (LP) core (referred to as a “second asymmetric core” or “Core1” in Sutardja) using the same instruction set architecture (ISA) (emphasis added).

Because the Applicant has demonstrated the patentability of all pending independent claims, the Applicant respectfully submits that all pending claims are allowable. The Applicant’s silence with respect to the dependent claims should not be construed as an admission by the Applicant that the Applicant is complicit with the Examiner’s rejection of these

claims. Because the Applicant has demonstrated the patentability of the independent claims, the Applicant need not substantively address the theories of rejection applied to the dependent claims.

In light of the comments above, Applicant respectfully requests the allowance of all claims.

CONCLUSION

Applicant respectfully submits that all objections and rejections have been overcome and that all pending claims are in condition for allowance. If the Examiner believes an additional telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Scott A. Simmons at 408-675-0441. Authorization is hereby given to charge our Deposit Account No. 504238 for any charges that may be due.

Respectfully submitted,
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP

Date: April 13, 2015 /Scott A. Simmons/
Scott A. Simmons
Reg. No.: 60,206

217 High Street
Palo Alto, CA 94301
408-675-0441

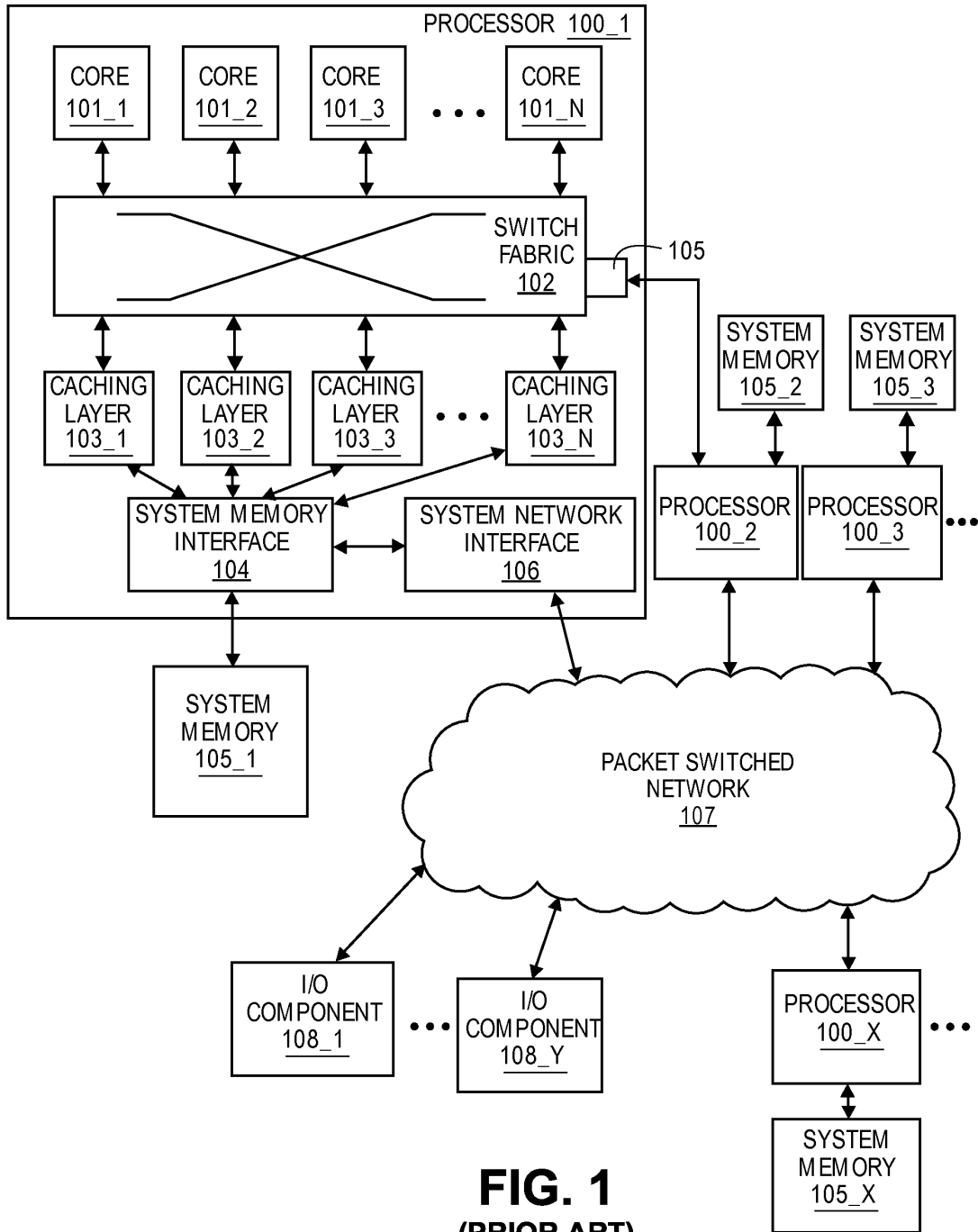


FIG. 1
(PRIOR ART)

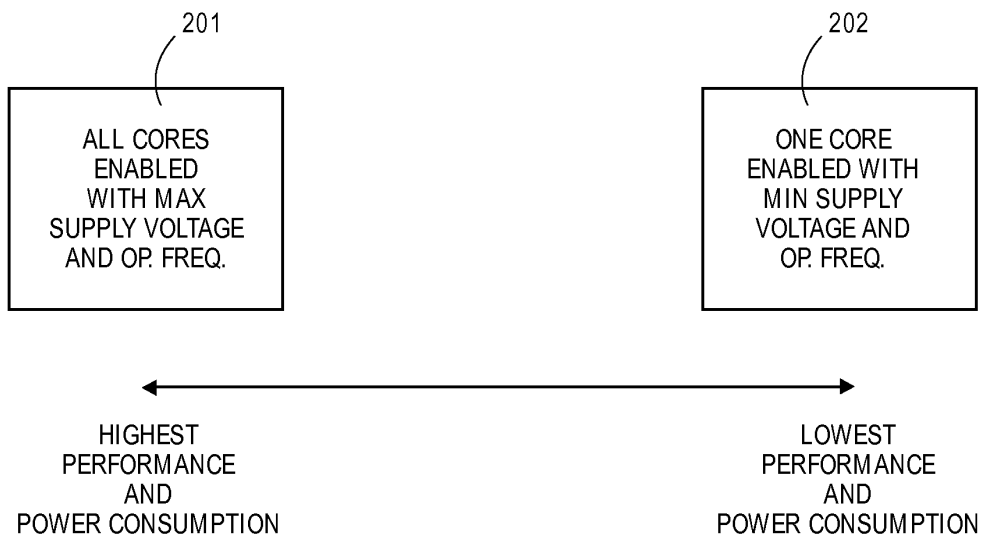


FIG. 2

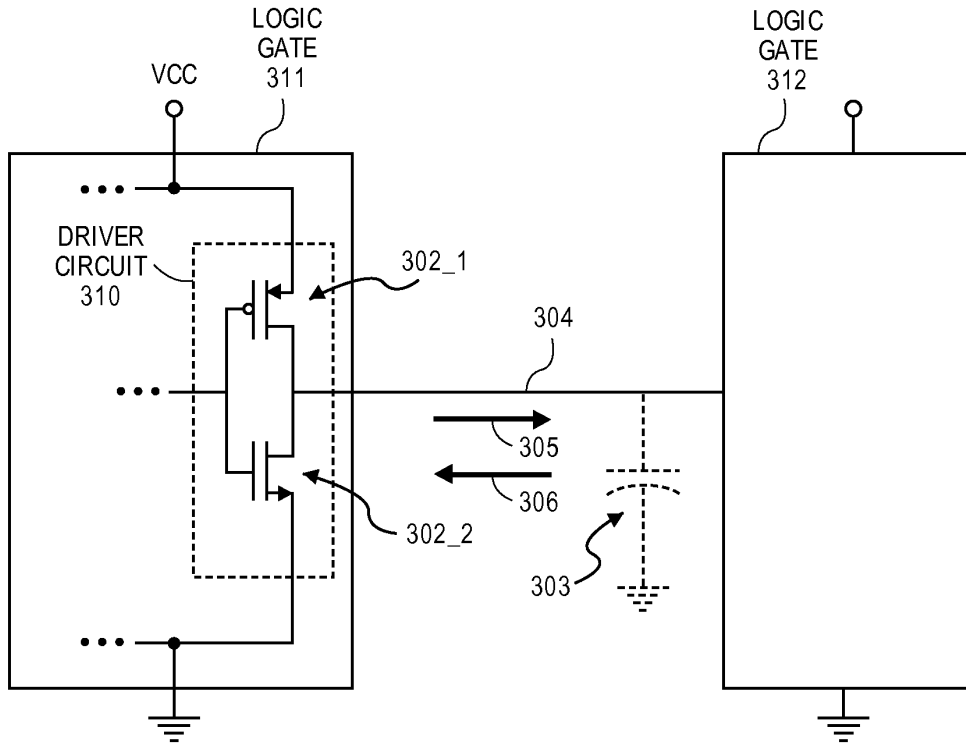


FIG. 3

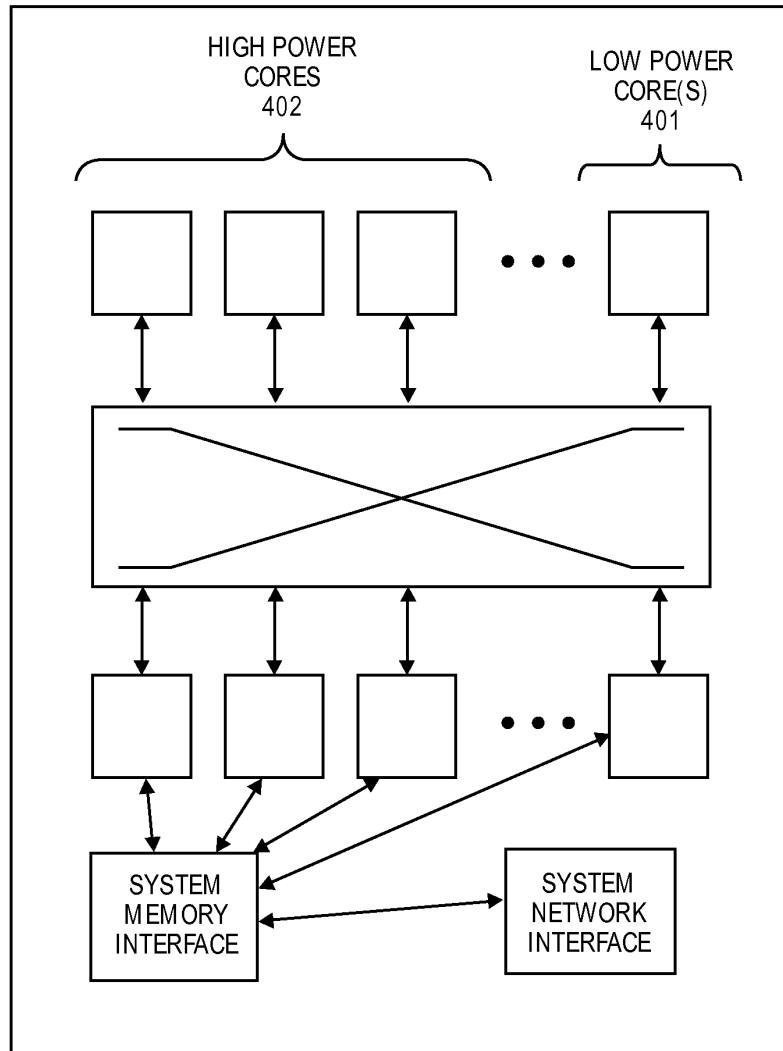


FIG. 4

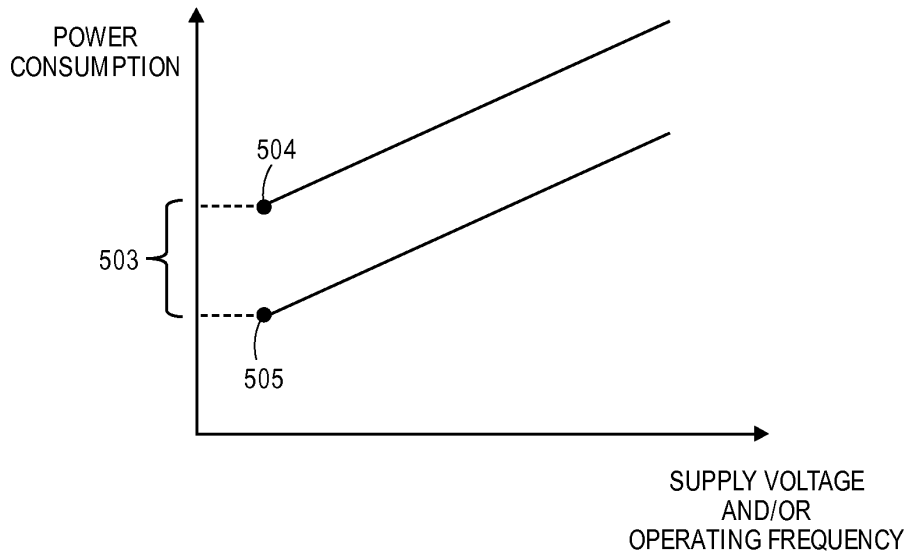


FIG. 5

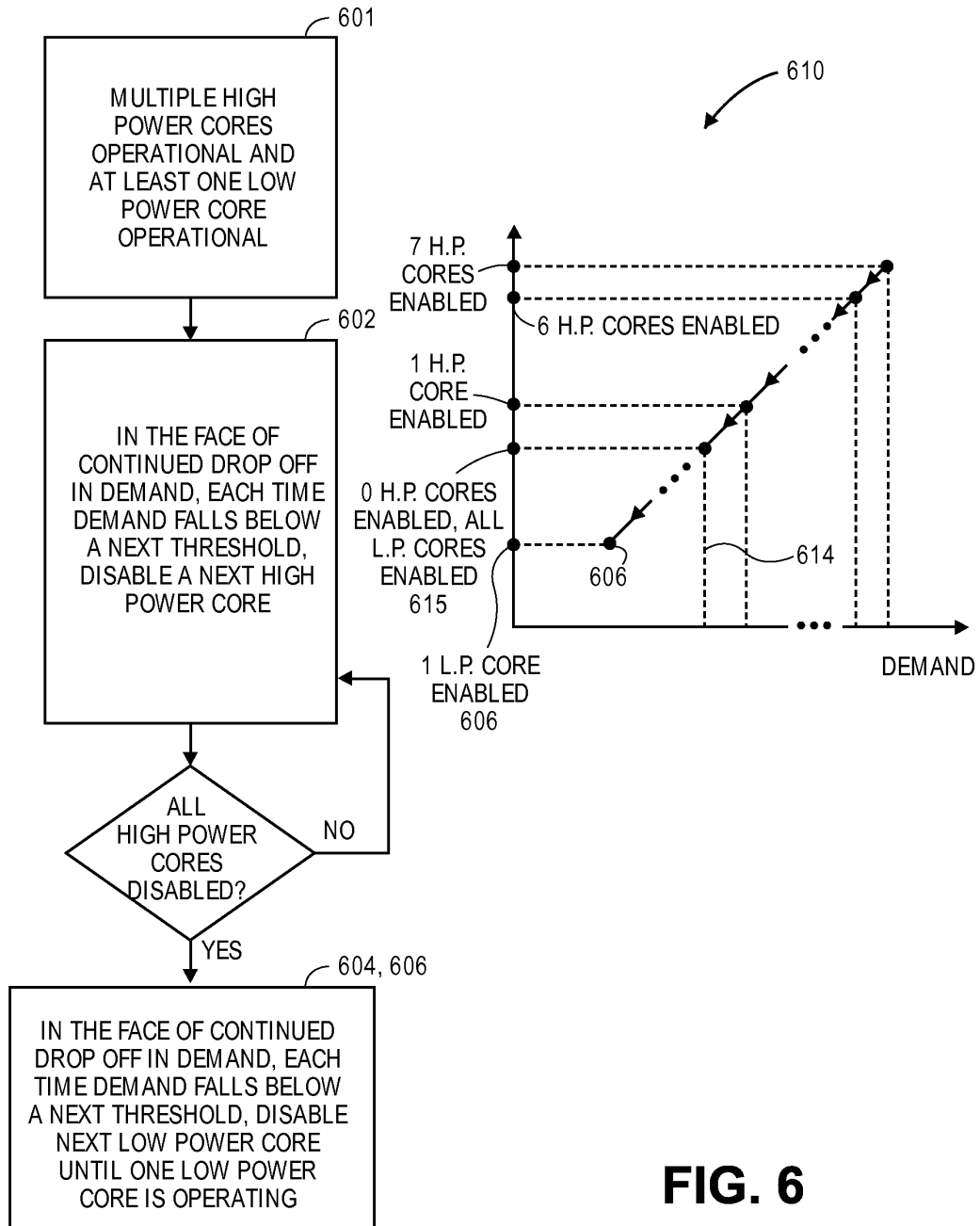
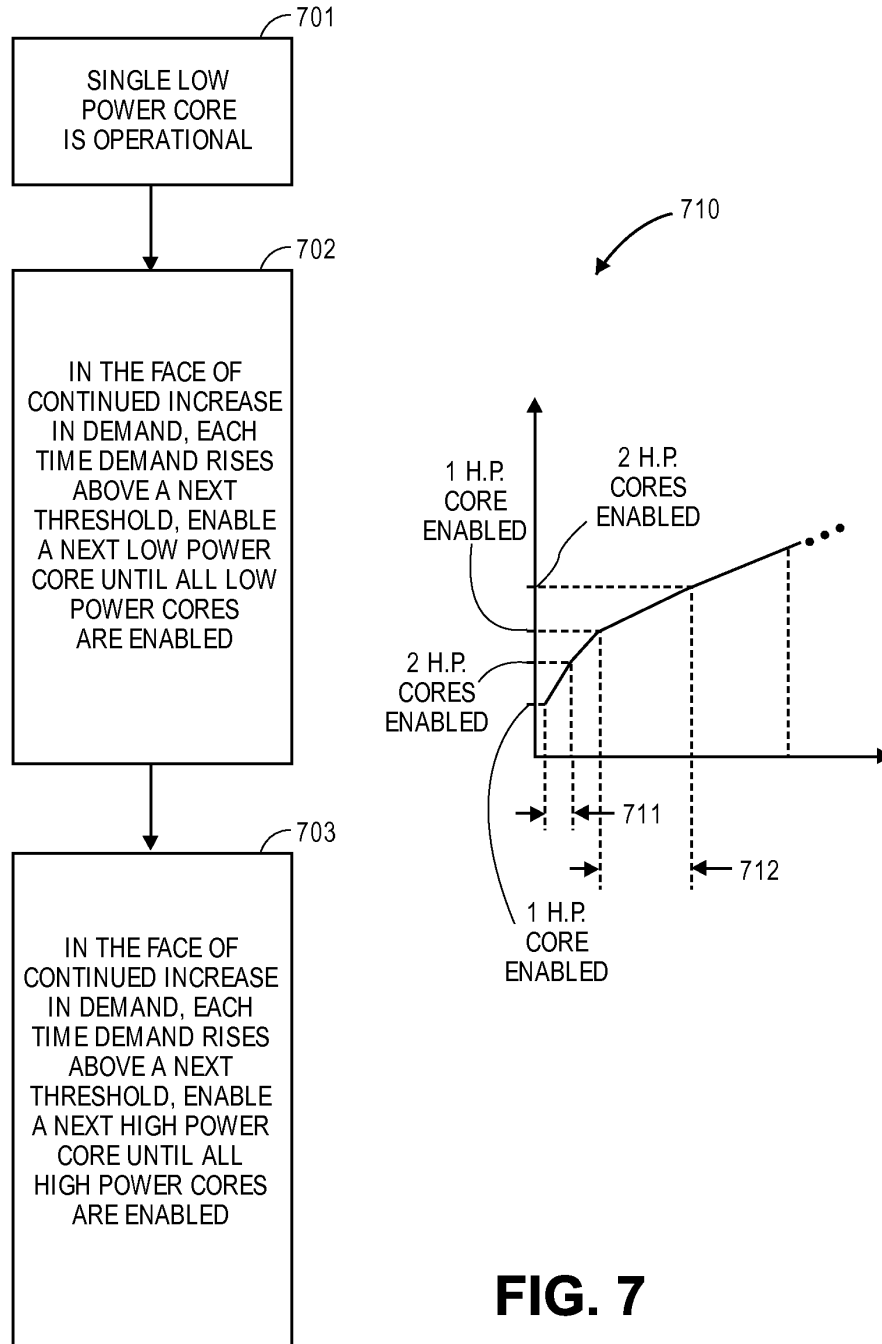


FIG. 6



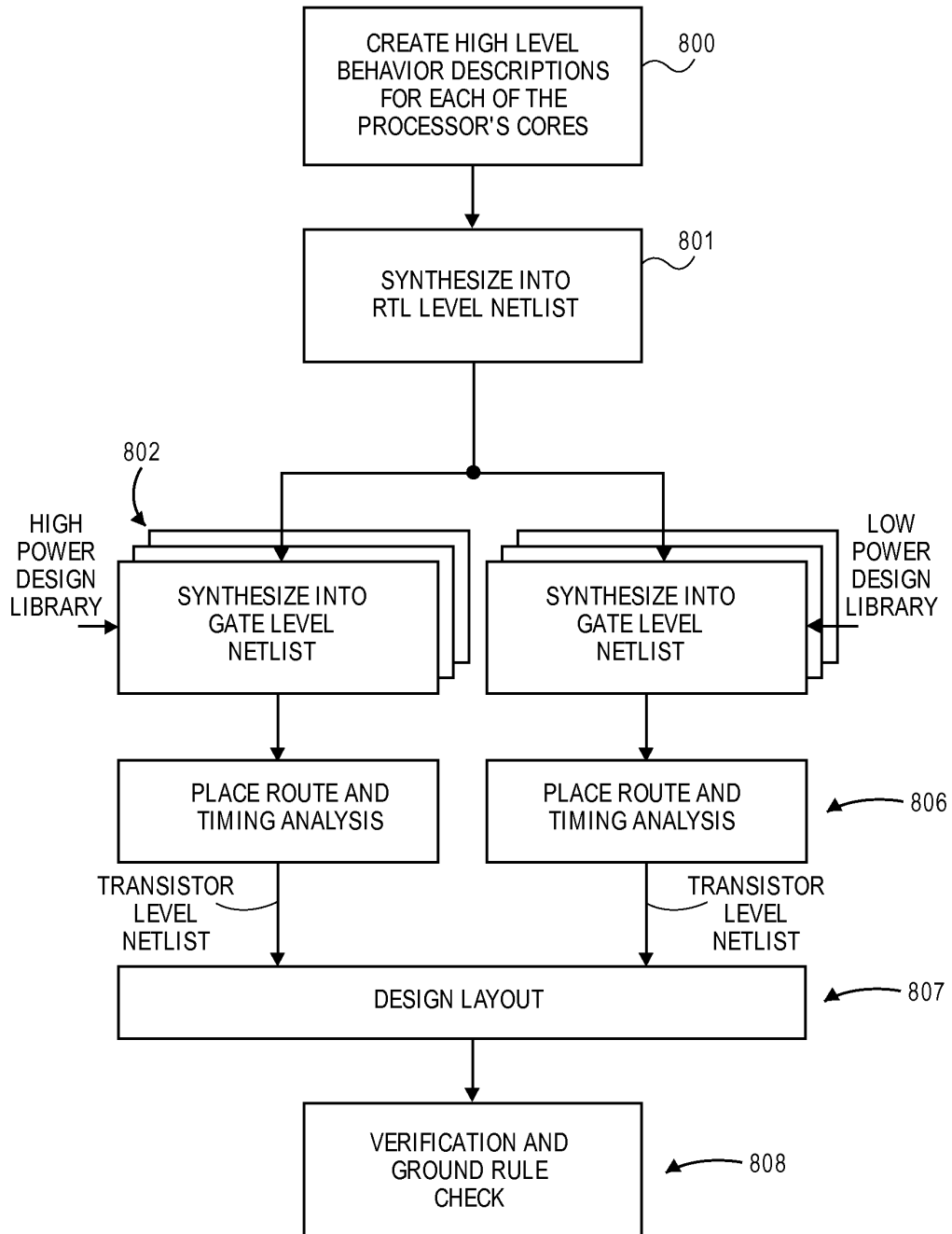


FIG. 8

Electronic Acknowledgement Receipt

EFS ID:	22050194
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	45209
Filer:	Scott Alan Simmons/c v
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	13-APR-2015
Filing Date:	22-DEC-2011
Time Stamp:	22:46:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38886_Response_04_13_15.pdf	46668 <small>d02577362cee431363f5ed84908ab633c5b7c97f</small>	yes	10

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Amendment/Req. Reconsideration-After Non-Final Reject		1	1
Claims		2	5
Drawings-only black and white line drawings		6	6
Applicant Arguments/Remarks Made in an Amendment		7	10

Warnings:

Information:

2	Drawings-only black and white line drawings	P38886_Replacement_Drawings_04_13_15.pdf	71362	no	8
			42dc2402f9bd7553f0115fee5fb056ef86b2ed51		

Warnings:

Information:

Total Files Size (in bytes): 118030

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875			Application or Docket Number 13/335,257	Filing Date 12/22/2011	<input type="checkbox"/> To be Mailed		
ENTITY: <input checked="" type="checkbox"/> LARGE <input type="checkbox"/> SMALL <input type="checkbox"/> MICRO							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)					
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)			
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A				
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A	N/A				
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A				
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	minus 20 =	*	X \$ =				
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =				
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL				
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)	(Column 3)				
AMENDMENT	04/13/2015	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$80 = 0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$420 = 0	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))						
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE	0			
(Column 1)		(Column 2)	(Column 3)				
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=		
	Independent (37 CFR 1.16(h))	*	Minus	***	=		
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))						
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.							
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".							
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".							
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							
LIE /SUSAN HAY/							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	Varghese George	42P38886	6542
45209	7590	01/12/2015	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN c/o CPA Global P.O. Box 52050 Minneapolis, MN 55402			NIELSEN, KEITH A	
			ART UNIT	PAPER NUMBER
			2183	
			NOTIFICATION DATE	DELIVERY MODE
			01/12/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteldocs_docketing@cpaglobal.com
Database_Group@bstz.com

Office Action Summary	Application No. 13/335,257	Applicant(s) GEORGE ET AL.	
	Examiner KEITH NIELSEN	Art Unit 2183	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 4/13/2012.
 A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) Claim(s) 1-19 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) Claim(s) _____ is/are allowed.
- 7) Claim(s) 1-19 is/are rejected.
- 8) Claim(s) _____ is/are objected to.
- 9) Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) The specification is objected to by the Examiner.
- 11) The drawing(s) filed on 4/13/2012 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) All b) Some** c) None of the:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 12/30/2014.
- 3) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 4) Other: _____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Claims 1-19 are presented for examination.

Drawings

3. The drawings filed 4/13/2012 are not acceptable for examination.
4. Figs. 1 and 3 are objected to because they do not comply with 37 CFR 1.84(o) which requires that the drawings contain suitable descriptive legends to understand the drawing. For example, elements 101_1 through 101_N should be labeled --cores-- or --processor cores--.
5. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated as indicated by [0007] and [0008] of the instant specification. See MPEP § 608.02(g).
6. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional

replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claims 1-2, 4-6 and 14 are objected to because of the following informalities:

- Claim 1, lines 2, 4 - insert --plurality of-- before "cores"
- Claim 2, line 2 - insert --plurality of-- before "cores"
- Claim 4, line 1 - insert --plurality of-- before "cores"
- Claim 5, line 2 - insert --plurality of-- before "cores"
- Claim 6, line 1 - lack of antecedent basis for "both cores"; Examiner suggests rewording to "a first core and a second core".
- Claim 14, line 3 - lack of antecedent basis for "both cores"
- Claim 14 - replace the semicolon at the end of the claim with a period.

8. Appropriate correction is required.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 14-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

11. Claims 14-19 refer to “a machine readable medium”. When the broadest reasonable interpretation of a claim covers a signal per se, the claim must be rejected under 35 U.S.C. 101 as covering non-statutory subject matter. See *In re Nuijten*, 500 F.3d 1346, 1356-57 (Fed. Cir. 2007) (transitory embodiments are not directed to statutory subject matter) and Interim Examination Instructions for Evaluating Subject Matter Eligibility Under 35 U.S.C. 101, Aug. 24, 2009; p. 2. Examiner suggests changing the limitation to be “a non-transitory machine readable medium”. (“Subject Matter Eligibility of Computer Readable Media”, 1/26/2010, Kappos)

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-2 and 4-19 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Sutardja et al. (US Patent Publication No. 2008/0288748). Aruj,

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“Evolution: 20 years of switching fabric” is referenced for claim 5 as extrinsic evidence of a system bus being a switch fabric.

14. As per claim 1, Sutardja teaches a multi-core processor comprising a plurality of cores (e.g. Figs. 3A, 3B - HP and LP cores) that support a same instruction set ([0214], [0225]), where, at least one of the cores is constructed of logic gates that consume less power, for a same applied operating frequency and supply voltage, than the same corresponding logic gates of at least one other of the cores ([0225] - HP and LP cores have the same architecture; [0230] - transistors of the HP core consume more power than the transistors of the LP core. The size of the transistors and gates in the HP core are larger than the size of the transistors and gates of the LP core).

15. As per claim 2, Sutardja teaches the multi-core processor of claim 1, wherein the larger gates that consume less power have narrower logic gate driver transistors than the same corresponding logic gates of the at least one other of the cores ([0230] - size of the gates of the transistors of the LP core are smaller than the gates of the transistors of the HP core).

16. As per claim 4, Sutardja teaches the multi-core processor of claim 1, wherein only one of the cores is constructed of the logic gates that consume less power ([0230] - LP core).

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17. As per claim 5, Sutardja teaches the multi-core processor of claim 1 further comprising a switch fabric between the cores and a system memory interface (e.g. Fig. 11E, [0327] - system bus. One of ordinary skill in the art would have considered the system bus a switching fabric at the time of the invention as shown by Aruj, "Evolution: 20 years of switching fabric". On page 1, "Shared Bus", Aruj shows a shared bus being a form of switching fabric).

18. As per claim 6, Sutardja teaches a method comprising: operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set ([0214], [0225]), a first core being a higher performance and consuming more power than a second core ([0212], [0213], [0230] - HP core is a high power, high performance core. LP core is low power, lower performance core).

19. As per claim 7, Sutardja teaches the method of claim 6 further comprising: disabling the first core but leaving the second core operable in response to lower demand being offered to the multi-core processor ([0218], [0305] - deactivate the HP core and process the application on the LP core when performance demanded by the application is not optimal on the HP core).

20. Claim 14 is a machine readable medium corresponding to claim 7 and is rejected for the same reason as set forth in the rejection of claim 7.

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21. As per claim 8, Sutardja teaches the method of claim 7 further comprising: enabling the first core after it is disabled in response to higher demand being offered to the multi-core processor ([0303] - activate the HP core (Core2) when processing on the LP core is at its maximum.

22. Claim 15 is a machine readable medium corresponding to claim 8 and is rejected for the same reason as set forth in the rejection of claim 8.

23. As per claim 9, Sutardja teaches the method of claim 8 wherein said method further comprises: disabling said first core after detecting a first drop in demand offered to said multi-core processor ([0305] - deactivate the HP core when application demand is decreased);

enabling said first core after detecting a first rise in demand offered to said multi-core processor, the amount of demand being greater than the amount of demand associated with the second drop ([0303] - activate HP core when application demand is more than is efficient with the LP core. [0294] - core switching may occur based on a threshold, e.g. number of applications where the HP core is used when the number of applications is 10 or more, and the Lp core is used when the number of applications is less than 10).

24. Claim 16 is a machine readable medium corresponding to claim 9 and is rejected for the same reason as set forth in the rejection of claim 9.

25. As per claim 10, Sutardja teaches the method of claim 6 wherein the operating of the first core includes driving load lines with wider transistor widths

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than corresponding transistor widths in said second core ([0230] - the size of the transistors and gates in the HP core are larger than the size of the transistors and gates of the LP core).

26. As per claim 11, Sutardja teaches the method of claim 6 further comprising lowering a supply voltage and/or operating frequency of said first core in response to lower demand being offered to said multi-core processor ([0304] - voltage/frequency can be raised and lowered according to the performance demanded by the application).

27. Claim 17 is a machine readable medium corresponding to claim 11 and is rejected for the same reason as set forth in the rejection of claim 11.

28. As per claim 12, Sutardja teaches the method of claim 6 further comprising raising a supply voltage and/or operating frequency of said first core in response to higher demand being offered to said multi-core processor ([0304] - voltage/frequency can be raised and lowered according to the performance demanded by the application).

29. Claim 18 is a machine readable medium corresponding to claim 12 and is rejected for the same reason as set forth in the rejection of claim 12.

30. As per claim 13, Sutardja teaches the method of claim 6 further comprising: disabling said first core in response to a drop in demand applied to said multi-core processor ([0305] - deactivate the HP core when performance

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demanded by the application is decreased); and lowering a supply voltage and/or operating frequency of said second core in response to an additional drop in demand applied to said multi-core processor ([0301]-[0302] - LP frequency and voltage may be lowered when performance demand is low).

31. Claim 19 is a machine readable medium corresponding to claim 13 and is rejected for the same reason as set forth in the rejection of claim 13.

Claim Rejections - 35 USC § 103

32. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

33. Claim 3 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sutardja et al. as applied to claim 1 above, and further in view of Grochowski et al. (US Patent Publication No. 2006/0095807).

34. As per claim 3, Sutardja teaches the multi-core processor of claim 1. Sutardja does not specifically teach wherein there are at least two cores that are constructed of the logic gates that consume less power.

35. However, Grochowski teaches that a plurality of smaller 'B cores' may be enabled to reduce the throughput performance discontinuity gap when switching off a larger 'A core' ([0033]).

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36. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a plurality of smaller and lower power cores in an asymmetric multiprocessing system such as taught by Grochowski in the invention of Sutardja. One would have been motivated to reduce the performance gap between a single low power core and a single high power core.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH NIELSEN whose telephone number is (571)270-3584. The examiner can normally be reached on Monday-Friday, 9:00am - 6:00pm, Alt. Friday, EDT.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on 571-272-3702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. N./
Examiner, Art Unit 2183

/BORIS GORNEY/
Supervisory Patent Examiner, Art Unit 2183

Notice of References Cited	Application/Control No. 13/335,257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.	
	Examiner KEITH NIELSEN	Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A US-2006/0095807	05-2006	Grochowski et al.	713/324
*	B US-2008/0288748	11-2008	Sutardja et al.	712/20
*	C US-2010/0153954	06-2010	Morrow et al.	718/102
*	D US-2006/0282692	12-2006	Oh, Jang Geun	713/300
	E US-			
	F US-			
	G US-			
	H US-			
	I US-			
	J US-			
	K US-			
	L US-			
	M US-			


FOREIGN PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N				
	O				
	P				
	Q				
	R				
	S				
	T				

NON-PATENT DOCUMENTS

*	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
U	Aruj, Ori. "Evolution: 20 years of switching fabric". September 2008. EE Times. Retrieved from http://www.eetimes.com/document.asp?doc_id=1272140 .
V	
W	
X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 13335257	Applicant(s)/Patent Under Reexamination GEORGE ET AL.
	Examiner KEITH NIELSEN	Art Unit 2183

CPC- SEARCHED		
Symbol	Date	Examiner
G06F1/3293,3296	12/26/2014	KN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
712	32,43	12/26/2014	KN

SEARCH NOTES		
Search Notes	Date	Examiner
East text search	12/26/2014	KN
Inventor name search	12/26/2014	KN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Receipt date: 12/30/2014

13335257 GAU:2183

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application No.	13/335,257
	Filing Date	December 22, 2011
	First Inventor	Varghese George, et al.
	Art Unit	2183
	Examiner Name	NIELSEN, KEITH A
Attorney Docket No.	42P38886	Conf. No. 6542

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

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- OR
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- It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Scott A. Simmons/	Date (MM-DD-YYYY)	12-30-2014
Name/Print	Scott A. Simmons	Registration Number	60206

Debbie Casias /Debbie Casias/ Date 12-30-2014

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /K.N./

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	13/335,257
	Filing Date	12/22/2011
	First Named Inventor	Varghese George
	Group Art Unit	2183
	Examiner Name	NIELSEN, KEITH A
Sheet 1 of 1	Attorney Docket No: 42P38886	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No. ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-2010/0083011	04/01/2010	ONOUCHI MASAFUMI et al.	
		US-7,992,020	08/02/2011	TUAN TIM et al.	
		US-2010/0058086	03/04/2010	LEE WAN YEON	
		US-2006/0282692	12/14/2006	OH JANG GEUN	
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initial*	Cite No. ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initial*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		PCT International Search Report for PCT Counterpart Application No. PCT/US2012/068274, 5 pgs., (February 22, 2013).	
		PCT Written Opinion of the International Searching Authority for PCT Counterpart Application No. PCT/US2012/068274, 6 pgs., (February 22, 2013).	
		PCT Notification concerning Transmittal of Copy of International Preliminary Report on Patentability (Chapter I of the Patent Cooperation Treaty) for PCT Counterpart Application No. PCT/US2012/068274, 8 pgs., (July 03, 2014).	

EXAMINER /Keith Nielsen/ DATE CONSIDERED 12/31/2014

Based on PTO/S&US(09-09) Substitute Disclosure Statement Form (PTO-1449) as modified by B672 03/26/07
 *EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 606. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /K.N./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	187	varghese near2 george.in. or sanjeev near2 jahagirdar.in. or deborah marr.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:22
L2	49	1 and core.clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:22
L3	73	1 and (disabl\$3 or enabl\$3 or activat\$3 or de\$1activat\$3) near4 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:23
L4	29	1 and (disabl\$3 or enabl\$3 or activat\$3 or de\$1activat\$3) near4 (core or processor).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:23
L5	6	1 and asymmetric	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:31
L6	28	deborah near2 marr.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:33
L7	1	6 and asymmetric	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:33
L8	7	6 and (disabl\$3 or enabl\$3 or activat\$3 or de\$1activat\$3) near6 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:34
L9	984	712/43,32.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:35
L10	254	9 and (disabl\$3 or enabl\$3 or activat\$3 or de\$1activat\$3) near4 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:36
L11	22	9 and asymmetric	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:36
L13	9	10 and 11	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:37
L14	930	g06f9/5094.cpc.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:47
L15	605	g06f1/3293.cpc.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:47
L16	2547	g06f1/3293,3296.cpc.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:48
L17	668	16 and (disabl\$3 or enabl\$3 or activat\$3 or de\$1activat\$3) near4	US-PGPUB; USPAT; EPO;	ADJ	ON	2014/12/26 19:49

		(core or processor)	JPO; IBM_TDB			
L18	411	17 and (less or lower or low) near4 (performance or power) near3 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 19:49
S25	967	(narrower or wider or larger or smaller) near4 (logic gate or driver) near3 transistor	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/25 14:55
S26	0	S25 same core near4 (power or frequency)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/25 14:56
S27	64	S25 and core with (power or frequency)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/25 14:56
S28	59	S25 and (core or processor) near6 (power or frequency)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/25 14:56
S29	32	S25 and (core or processor) near6 (power or frequency) near4 (high\$2 or low\$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/25 14:58
S30	1	"20080288748".pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/25 15:32
S31	7467	(low or lower) near2 power near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:18
S32	8570	(low or lower) near2 (power or performance) near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:18
S33	13230	(high or higher) near2 (power or performance) near2 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:19
S34	959	S32 same S33	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:19
S35	398	S34 and (low or lower) near2 (power or performance) near2 (cores! or processors!)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:19
S36	205	S35 and @pd<"20111222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:20
S37	153	S36 and "7"?? clas.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:20
S38	19	S37 and (disabl\$3 or deactivat\$3) near3 (core or processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:20
S39	4334	(disabl\$3 or deactivat\$3) near3 (core or processor) same1 power	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:27
S40	96	(plurality or multiple) adj3 (low or lower) near2 (power or performance) near3 (cores! or processors!)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:29
S42	42	S40 and @pd<"20111222"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:29
S43	284	asymmetric near multi\$1processor	US-PGPUB; USPAT; EPO;	ADJ	ON	2014/12/26 16:42

EAST Search History

			JPO; IBM_TDB			
S44	8	S39 and S43	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:42
S45	2	"6567839"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:47
S46	190	"6567839"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:47
S47	1	"6567839".pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:47
S48	1	"20060095807".pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2014/12/26 16:51

EAST Search History (Interference)

<This search history is empty>

12/ 26/ 2014 8:09:15 PM

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	13/335,257
Filing Date	December 22, 2011
First Inventor	Varghese George, et al.
Art Unit	2183
Examiner Name	NIELSEN, KEITH A
Attorney Docket No.	42P38886
	Conf. No. 6542

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None

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SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Scott A. Simmons/	Date (MM-DD-YYYY)	01-09-2015
Name/Print	Scott A. Simmons	Registration Number	60206

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

/Debbie Casias/

Date 01-09-15

This collection of information is required by 37 C.F.R. 1.97 and 1.98. The information is required to obtain or retain a benefit by the public, which is of the kind by the USPTO to process an application. Confidentiality is governed by 20 U.S.C. 122 and 37 C.F.R. 1.14. The collection is intended to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete the form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22315-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22315-1480.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	13/335,257
	Filing Date	12/22/2011
	First Named Inventor	Varghese George
	Group Art Unit	2183
	Examiner Name	NIELSEN, KEITH A
Sheet 1 of 1	Attorney Docket No: 42P38886	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No. ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Copy of Notice of Allowance from TW counterpart Application No. 101147200, (Atty. Docket No. 42P38886TW), Mailed September 29, 2014, 1 page.	

EXAMINER	DATE CONSIDERED
<small>Based on FTO/SR/PA(09-09) - Substitute Disclosure Statement Form (PTO-1449) as modified by SBTZ 03/08/07</small>	
<small>* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. † Applicant's unique citation designation number (optional). ‡ Applicant is to place a check mark here if English language translation is attached.</small>	

Electronic Acknowledgement Receipt

EFS ID:	21174802
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	45209
Filer:	Scott Alan Simmons/Debbie Casias
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	09-JAN-2015
Filing Date:	22-DEC-2011
Time Stamp:	18:04:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	42P38886IDS.pdf	104756 f534cbf93a482b01964232ea0493d528d2b8fbcf	no	2

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

2	Non Patent Literature	NPL1.pdf	38127	no	1
			3b0bf81d49078214e3777b293dd7a3416bf3ced8		

Warnings:

Information:

Total Files Size (in bytes): 142883

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application No.	13/335,257
	Filing Date	December 22, 2011
	First Inventor	Varghese George, et al.
	Art Unit	2183
	Examiner Name	NIELSEN, KEITH A
Attorney Docket No.	42P38886	Conf. No. 6542

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Signature	/Scott A. Simmons/	Date (MM-DD-YYYY)	12-30-2014
Name/Print	Scott A. Simmons	Registration Number	60206

Debbie Casias /Debbie Casias/ _____ Date 12-30-2014

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PATENT COOPERATION TREATY

SASTON
PCT/US2012/068274

ADVANCE E-MAIL

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
TRANSMITTAL OF COPY OF INTERNATIONAL
PRELIMINARY REPORT ON PATENTABILITY
(CHAPTER I OF THE PATENT COOPERATION
TREATY)
(PCT Rule 44bis.1(c))

To:

VINCENT, Lester J.
Blakely, Sokoloff, Taylor & Zafman LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085
ETATS-UNIS D'AMERIQUE

Date of mailing (day/month/year) 03 July 2014 (03.07.2014)		IMPORTANT NOTICE	
Applicant's or agent's file reference 42P38886PCT			
International application No. PCT/US2012/068274	International filing date (day/month/year) 06 December 2012 (06.12.2012)	Priority date (day/month/year) 22 December 2011 (22.12.2011)	
Applicant INTEL CORPORATION			

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

POW

<p>The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland</p> <p>Facsimile No. +41 22 338 82 70</p>	<p>Authorized officer Simin Baharlou</p> <p>e-mail: pt09.pct@wipo.int</p>
----------------------------------------------------------------------------------------------------------------------------------------------	-------------------------------------------------------------------------------

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44bis)

Applicant's or agent's file reference 42P38886PCT	FOR FURTHER ACTION		See item 4 below
International application No. PCT/US2012/068274	International filing date (<i>day/month/year</i>) 06 December 2012 (06.12.2012)	Priority date (<i>day/month/year</i>) 22 December 2011 (22.12.2011)	
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237			
Applicant INTEL CORPORATION			

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 bis.1(a).

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

<input checked="" type="checkbox"/>	Box No. I	Basis of the report
<input type="checkbox"/>	Box No. II	Priority
<input type="checkbox"/>	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
<input type="checkbox"/>	Box No. IV	Lack of unity of invention
<input checked="" type="checkbox"/>	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
<input type="checkbox"/>	Box No. VI	Certain documents cited
<input type="checkbox"/>	Box No. VII	Certain defects in the international application
<input checked="" type="checkbox"/>	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44bis.3(c) and 93bis.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44bis .2).

	Date of issuance of this report 24 June 2014 (24.06.2014)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Simin Baharlou
Facsimile No. +41 22 338 82 70	e-mail: pt09.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
VINCENT LESTER J.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279
OAKMEAD PARKWAY SUNNYVALE CA 94085 USA

PCT

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **22 FEBRUARY 2013 (22.02.2013)**

Applicant's or agent's file reference
42P38886PCT

FOR FURTHER ACTION
See paragraph 2 below

International application No. PCT/US2012/068274	International filing date (day/month/year) 06 DECEMBER 2012 (06.12.2012)	Priority date(day/month/year) 22 DECEMBER 2011 (22.12.2011)
-----------------------------------------------------------	------------------------------------------------------------------------------------	----------------------------------------------------------------

International Patent Classification (IPC) or both national classification and IPC

G06F 15/80(2006.01)i, G06F 1/32(2006.01)i, G06F 13/14(2006.01)i



Applicant
INTEL CORPORATION

1. This opinion contains indications relating to the following items:
- Box No. I Basis of the opinion
 - Box No. II Priority
 - Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
 - Box No. IV Lack of unity of invention
 - Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
 - Box No. VI Certain documents cited
 - Box No. VII Certain defects in the international application
 - Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**
If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

 Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Date of completion of this opinion 22 FEBRUARY 2013 (22.02.2013)	Authorized officer PARK, SEUNG CHUL Telephone No.82-42-481-5696
		

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US2012/068274

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
 - the international application in the language in which it was filed
 - a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
2. This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))
3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:
 - a. a sequence listing filed or furnished
 - on paper
 - in electronic form
 - b. time of filing or furnishing
 - contained in the international application as filed.
 - filed together with the international application in electronic form.
 - furnished subsequently to this Authority for the purposes of search.
4. In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2012/068274

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-19	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-19	NO
Industrial applicability (IA)	Claims	1-19	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2010-0083011 A1 (ONOUCHI MASAFUMI et al.) 01 April 2010
D2: US 7992020 B1 (TUAN TIM et al.) 02 August 2011
D3: US 2010-0058086 A1 (LEE WAN YEON) 04 March 2010
D4: US 2006-0282692 A1 (OH JANG GEUN) 14 December 2006

A. Novelty and Inventive Step

1. Claims 1-5

Claim 1 of the present invention relates to a multi-core processor. D1(see paragraphs [0092]-[0096], claims 1,2 and figure 2,17,18), which is the closest prior art to the subject matter of claim 1, discloses an information processing device, comprising: processor cores; on-chip-memory; and a bus commonly connected thereto.

When comparing claim 1 of the present invention with D1, claim 1 is different in at least one of the cores that consume less power. However, D2(see claim 1) discloses a packaged multi-die integrated circuit, including: a first integrated circuit die has a rate of power consumption that is lower than a second integrated die.

Accordingly, it would be obvious to a person skilled in the art to apply the features of D2 to the information processing device of D1. Therefore, claim 1 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 2-4 are dependent on claim 1. The additional features of claims 2-4 are identical to an oscillator PLLH of the clock with high amplitude and high frequency CLKH and oscillator PLLL of the clock with low amplitude and low frequency CLKL which are individually mounted of D1(see paragraph [0092]). Therefore, claims 2-4 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claim 5 is dependent on claim 1. The additional features of claim 5 are identical to the bus of D1(see claim 1). Therefore, claim 5 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

<Continued on Supplemental Box>

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2012/068274

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claims 9,16 are worded 'said second drop'. However, 'second drop' has not been worded in the previous, these claims do not meet the requirement of PCT Article 6.

The international search report and the written opinion has been established on the assumption that 'second drop' is worded in the previous.

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US2012/068274

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

<Box V>

2. Claims 6-13

Claim 6 of the present invention relates to a method. D1(see paragraphs [0092]-[0096], claims 1,2 and figure 2,17,18), which is the closest prior art to the subject matter of claim 1, discloses an information processing device, comprising: processor cores; on-chip-memory; and a bus commonly connected thereto.

When comparing claim 6 of the present invention with D1, claim 6 is different in a first core being higher performance and consuming more power than a second core. However, D2(see claim 1) discloses a packaged multi-die integrated circuit, including: a first integrated circuit die has a rate of power consumption that is lower than a second integrated die.

Accordingly, it would be obvious to a person skilled in the art to apply the features of D2 to the information processing device of D1. Therefore, claim 6 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 7-9 are dependent on claim 6. The additional features of claims 7-9 are identical to shutdown/adjust sequence and turn off/adjust regulator voltages for FPGA of D2(see figure 5). Therefore, claims 7-9 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claim 10 is dependent on claim 6. The additional features of claim 10 are identical to an oscillator PLLH of the clock with high amplitude and high frequency CLKH and oscillator PLLL of the clock with low amplitude and low frequency CLKL which are individually mounted of D1(see paragraph [0092]). Therefore, claim 10 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 11-13 are dependent on claim 6. The additional features of claims 11-13 are identical to shutdown/adjust sequence and turn off/adjust regulator voltages for FPGA of D2(see figure 5). Therefore, claims 11-13 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

3. Claims 14-19

Claim 14 of the present invention relates to a machine readable medium. D1(see paragraphs [0092]-[0096], claims 1,2 and figure 2,17,18), which is the closest prior art to the subject matter of claim 1, discloses an information processing device, comprising: processor cores; on-chip-memory; and a bus commonly connected thereto.

When comparing claim 14 of the present invention with D1, claim 14 is different in a first core being higher performance and consuming more power than a second core. However, D2(see claim 1) discloses a packaged multi-die integrated circuit, including: a first integrated circuit die has a rate of power consumption that is lower than a second integrated die.

<Continued on the Next Page>

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2012/068274

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

<the Previous Page>

Accordingly, it would be obvious to a person skilled in the art to apply the features of D2 to the information processing device of D1. Therefore, claim 14 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 15-19 are dependent on claim 14. The additional features of claims 15-19 are identical to shutdown/adjust sequence and turn off/adjust regulator voltages for FPGA of D2(see figure 5). Therefore, claims 15-19 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

B. Industrial Applicability

Claims 1-19 have industrial applicability and meet the requirement of PCT Article 33(4).

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
VINCENT LESTER J.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279
OAKMEAD PARKWAY SUNNYVALE CA 94085 USA

PCT

NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL SEARCH REPORT AND
THE WRITTEN OPINION OF THE INTERNATIONAL
SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

RECEIVED
SUNNYVALE
MAR 01 2013

Date of mailing
(day/month/year) 22 FEBRUARY 2013 (22.02.2013)

Applicant's or agent's file reference
42P38886PCT
BLAKELY SOKOLOFF
TAYLOR & ZAFMAN

FOR FURTHER ACTION See paragraphs 1 and 4 below

International application No.
PCT/US2012/068274

International filing date
(day/month/year)
06 DECEMBER 2012 (06.12.2012)

Applicant
INTEL CORPORATION


- The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.
Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):
When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.
Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes
1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70
For more detailed instructions, see PCT Applicant's Guide, International Phase, paragraphs 9.004 . 9.011.
- The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.
- With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:
 the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.
 no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.
- Reminders**
The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.
In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

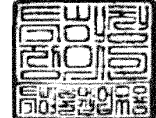
For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

MAR 01 2013
Roel
Entered into PTP
By: Roel

Name and mailing address of the ISA/KR
 Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan
City, 302-701, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer

COMMISSIONER

Telephone No. 82-42-481-8753


* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

<http://www.kipo.go.kr/en/> => PCT Services => PCT Services

ID : PCT international application number

PW : **3NMY3669**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: <http://www.ipkcenter.com>

Email: ipkc@ipkcenter.com

Phone: +1 703 388 1066

Fax: +1 703 388 1084

PATENT COOPERATION TREATY

PCT



INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 42P38886PCT	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US2012/068274	International filing date (<i>day/month/year</i>) 06 DECEMBER 2012 (06.12.2012)	(Earliest) Priority Date (<i>day/month/year</i>) 22 DECEMBER 2011 (22.12.2011)
Applicant INTEL CORPORATION		
This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau. This international search report consists of a total of <u>3</u> sheets. <input type="checkbox"/> It is also accompanied by a copy of each prior art document cited in this report.		
<p>1. Basis of the report</p> <p>a. With regard to the language, the international search was carried out on the basis of:</p> <p><input checked="" type="checkbox"/> the international application in the language in which it was filed</p> <p><input type="checkbox"/> a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))</p> <p>b. <input type="checkbox"/> This international search report has been established taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).</p> <p>c. <input type="checkbox"/> With regard to any nucleotide and/or amino acid sequence disclosed in the international application, see Box No. I.</p> <p>2. <input type="checkbox"/> Certain claims were found unsearchable (See Box No. II)</p> <p>3. <input type="checkbox"/> Unity of invention is lacking (See Box No. III)</p> <p>4. With regard to the title,</p> <p><input checked="" type="checkbox"/> the text is approved as submitted by the applicant.</p> <p><input type="checkbox"/> the text has been established by this Authority to read as follows:</p> <p>5. With regard to the abstract,</p> <p><input checked="" type="checkbox"/> the text is approved as submitted by the applicant.</p> <p><input type="checkbox"/> the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.</p> <p>6. With regard to the drawings,</p> <p>a. the figure of the drawings to be published with the abstract is Figure No. <u>6</u></p> <p><input checked="" type="checkbox"/> as suggested by the applicant.</p> <p><input type="checkbox"/> as selected by this Authority, because the applicant failed to suggest a figure.</p> <p><input type="checkbox"/> as selected by this Authority, because this figure better characterizes the invention.</p> <p>b. <input type="checkbox"/> none of the figure is to be published with the abstract.</p>		

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/068274

A. CLASSIFICATION OF SUBJECT MATTER		
<i>G06F 15/80(2006.01)i, G06F 1/32(2006.01)i, G06F 13/14(2006.01)i</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) G06F 15/80; G06F 1/10; G06F 1/26; G06F 15/76; G06F 1/00		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: multi, processor, power, and performance		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010-0083011 A1 (ONOUCHI MASAFUMI et al.) 01 April 2010 See abstract, paragraphs [0092]-[0096], claims 1,2 and figures 2,17,18.	1-19
Y	US 7992020 B1 (TUAN TIM et al.) 02 August 2011 See abstract, column 8, line 6 - column 9, line 37, claims 1,6 and figure 5.	1-19
A	US 2010-0058086 A1 (LEE WAN YEON) 04 March 2010 See abstract, paragraphs [0028]-[0033], claim 1 and figures 5,6.	1-19
A	US 2006-0282692 A1 (OH JANG GEUN) 14 December 2006 See abstract, paragraphs [0023]-[0029], claim 1 and figure 1.	1-19
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
Date of the actual completion of the international search 22 FEBRUARY 2013 (22.02.2013)		Date of mailing of the international search report 22 FEBRUARY 2013 (22.02.2013)
Name and mailing address of the ISA/KR  Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140		Authorized officer PARK, SEUNG CHUL Telephone No. 82-42-481-5696 

Form PCT/ISA/210 (second sheet) (July 2009)

Petitioner Mercedes Ex-1010, 0185

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2012/068274

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0083011 A1	01.04.2010	JP 2010-086030 A US 8239695 B2	15.04.2010 07.08.2012
US 7992020 B1	02.08.2011	None	
US 2010-0058086 A1	04.03.2010	KR 10-1072864 B1 KR 10-2010-0026989 A	17.10.2011 10.03.2010
US 2006-0282692 A1	14.12.2006	CN 100461072 C0 CN 1877492 A EP 1736851 A2 EP 1736851 A3 KR 10-1108397 B1 KR 10-2006-0128469 A US 7664971 B2	11.02.2009 13.12.2006 27.12.2006 07.10.2009 30.01.2012 14.12.2006 16.02.2010

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
VINCENT LESTER J.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279
OAKMEAD PARKWAY SUNNYVALE CA 94085 USA

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **22 FEBRUARY 2013 (22.02.2013)**

Applicant's or agent's file reference
42P38886PCT

FOR FURTHER ACTION
See paragraph 2 below

International application No. PCT/US2012/068274	International filing date (day/month/year) 06 DECEMBER 2012 (06.12.2012)	Priority date(day/month/year) 22 DECEMBER 2011 (22.12.2011)
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Applicant

INTEL CORPORATION

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For further options, see Form PCT/ISA/220.

 Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Date of completion of this opinion 22 FEBRUARY 2013 (22.02.2013)	Authorized officer PARK, SEUNG CHUL Telephone No.82-42-481-5696
-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	---------------------------------------------------------------------	-----------------------------------------------------------------------

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US2012/068274

Box No. 1 Basis of this opinion

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 - a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
2. This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))
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 - a. a sequence listing filed or furnished
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 - in electronic form
 - b. time of filing or furnishing
 - contained in the international application as filed.
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5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2012/068274

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	<u>1-19</u>	YES
	Claims	<u>NONE</u>	NO
Inventive step (IS)	Claims	<u>NONE</u>	YES
	Claims	<u>1-19</u>	NO
Industrial applicability (IA)	Claims	<u>1-19</u>	YES
	Claims	<u>NONE</u>	NO

2. Citations and explanations :

Reference is made to the following documents:

- D1: US 2010-0083011 A1 (ONOUCHI MASAFUMI et al.) 01 April 2010
 D2: US 7992020 B1 (TUAN TIM et al.) 02 August 2011
 D3: US 2010-0058086 A1 (LEE WAN YEON) 04 March 2010
 D4: US 2006-0282692 A1 (OH JANG GEUN) 14 December 2006

A. Novelty and Inventive Step

1. Claims 1-5

Claim 1 of the present invention relates to a multi-core processor. D1(see paragraphs [0092]-[0096], claims 1,2 and figure 2,17,18), which is the closest prior art to the subject matter of claim 1, discloses an information processing device, comprising: processor cores; on-chip-memory; and a bus commonly connected thereto.

When comparing claim 1 of the present invention with D1, claim 1 is different in at least one of the cores that consume less power. However, D2(see claim 1) discloses a packaged multi-die integrated circuit, including: a first integrated circuit die has a rate of power consumption that is lower than a second integrated die.

Accordingly, it would be obvious to a person skilled in the art to apply the features of D2 to the information processing device of D1. Therefore, claim 1 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 2-4 are dependent on claim 1. The additional features of claims 2-4 are identical to an oscillator PLLH of the clock with high amplitude and high frequency CLKH and oscillator PLLL of the clock with low amplitude and low frequency CLKL which are individually mounted of D1(see paragraph [0092]). Therefore, claims 2-4 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claim 5 is dependent on claim 1. The additional features of claim 5 are identical to the bus of D1(see claim 1). Therefore, claim 5 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

<Continued on Supplemental Box>

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2012/068274

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claims 9,16 are worded 'said second drop'. However, 'second drop' has not been worded in the previous, these claims do not meet the requirement of PCT Article 6.

The international search report and the written opinion has been established on the assumption that 'second drop' is worded in the previous.

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/068274

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

<Box V>

2. Claims 6-13

Claim 6 of the present invention relates to a method. D1(see paragraphs [0092]-[0096], claims 1,2 and figure 2,17,18), which is the closest prior art to the subject matter of claim 1, discloses an information processing device, comprising: processor cores; on-chip-memory; and a bus commonly connected thereto.

When comparing claim 6 of the present invention with D1, claim 6 is different in a first core being higher performance and consuming more power than a second core. However, D2(see claim 1) discloses a packaged multi-die integrated circuit, including: a first integrated circuit die has a rate of power consumption that is lower than a second integrated die.

Accordingly, it would be obvious to a person skilled in the art to apply the features of D2 to the information processing device of D1. Therefore, claim 6 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 7-9 are dependent on claim 6. The additional features of claims 7-9 are identical to shutdown/adjust sequence and turn off/adjust regulator voltages for FPGA of D2(see figure 5). Therefore, claims 7-9 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claim 10 is dependent on claim 6. The additional features of claim 10 are identical to an oscillator PLLH of the clock with high amplitude and high frequency CLKH and oscillator PLLL of the clock with low amplitude and low frequency CLKL which are individually mounted of D1(see paragraph [0092]). Therefore, claim 10 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 11-13 are dependent on claim 6. The additional features of claims 11-13 are identical to shutdown/adjust sequence and turn off/adjust regulator voltages for FPGA of D2(see figure 5). Therefore, claims 11-13 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

3. Claims 14-19

Claim 14 of the present invention relates to a machine readable medium. D1(see paragraphs [0092]-[0096], claims 1,2 and figure 2,17,18), which is the closest prior art to the subject matter of claim 1, discloses an information processing device, comprising: processor cores; on-chip-memory; and a bus commonly connected thereto.

When comparing claim 14 of the present invention with D1, claim 14 is different in a first core being higher performance and consuming more power than a second core. However, D2(see claim 1) discloses a packaged multi-die integrated circuit, including: a first integrated circuit die has a rate of power consumption that is lower than a second integrated die.

<Continued on the Next Page>

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US2012/068274

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

<the Previous Page>

Accordingly, it would be obvious to a person skilled in the art to apply the features of D2 to the information processing device of D1. Therefore, claim 14 is considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

Claims 15-19 are dependent on claim 14. The additional features of claims 15-19 are identical to shutdown/adjust sequence and turn off/adjust regulator voltages for FPGA of D2(see figure 5). Therefore, claims 15-19 are considered to be novel under PCT Article 33(2) but not to involve an inventive step under PCT Article 33(3).

B. Industrial Applicability

Claims 1-19 have industrial applicability and meet the requirement of PCT Article 33(4).

Electronic Acknowledgement Receipt

EFS ID:	21094843
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	Varghese George
Customer Number:	45209
Filer:	Scott Alan Simmons/Debbie Casias
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886
Receipt Date:	30-DEC-2014
Filing Date:	22-DEC-2011
Time Stamp:	21:26:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	42P38886IDS.pdf	114050 <small>9d728b29dba0c5e4b877a54eac633451f8688e9f</small>	no	2

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Information:

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2	Non Patent Literature	NPL1.pdf	1014665	no	8
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Warnings:					
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3	Non Patent Literature	NPL2.pdf	775151	no	5
			1246930476313fc2e63d17b4c2162bbc1a73d71		
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Total Files Size (in bytes):			2664302		
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Table with 4 columns: APPLICATION NUMBER (13/335,257), FILING OR 371(C) DATE (12/22/2011), FIRST NAMED APPLICANT (Varghese George), ATTY. DOCKET NO./TITLE (42P38886)

CONFIRMATION NO. 6542

45209
Mission/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

PUBLICATION NOTICE



Title:ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

Publication No.US-2012-0198207-A1

Publication Date:08/02/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
13/335,257

APPLICATION AS FILED - PART I

(Column 1)		(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 = *	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
Total (37 CFR 1.16(i))	*	Minus **	**	=		OR	x	=
Independent (37 CFR 1.16(h))	*	Minus ***	***	=		OR	x	=
Application Size Fee (37 CFR 1.16(s))						OR		
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						OR		
				TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
Total (37 CFR 1.16(i))	*	Minus **	**	=		OR	x	=
Independent (37 CFR 1.16(h))	*	Minus ***	***	=		OR	x	=
Application Size Fee (37 CFR 1.16(s))						OR		
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						OR		
				TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.



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Table with 7 columns: APPLICATION NUMBER, FILING or 371(c) DATE, GRP ART UNIT, FIL FEE REC'D, ATTY DOCKET NO, TOT CLAIMS, IND CLAIMS. Row 1: 13/335,257, 12/22/2011, 2825, 1680, 42P38886, 19, 3

CONFIRMATION NO. 6542

UPDATED FILING RECEIPT

45209
MISSION/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040



Date Mailed: 04/20/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections

Applicant(s)

Varghese George, Folsom, CA;
Sanjeev S. Jahagirdar, Folsom, CA;
Deborah T. Marr, Portland, OR;

Power of Attorney: The patent practitioners associated with Customer Number 45209

Domestic Priority data as claimed by applicant

Foreign Applications (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 01/09/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 13/335,257

Projected Publication Date: 08/02/2012

Non-Publication Request: No

Early Publication Request: Yes

Title

ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

Preliminary Class

716

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Attorney's Docket No.: 42P38886
PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe I am the original and first inventor (if only one name is listed below) or an original and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE (ISA)

the specification of which (check one):

is attached hereto.
 was filed on 12/22/2011 as
United States Application Number 13/335,257
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed?		Certified Copy Attached?	
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No

Attorney's Docket No.: 42P38886
PATENT

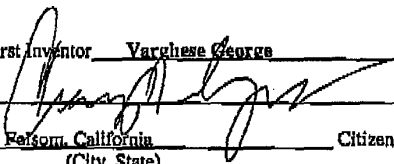
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transact all business in the United States Patent and Trademark Office connected therewith.

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c/o BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, California 94085-4040 U.S.A.
Telephone: (408) 720-8300
Fax: (408) 720-8383

Attorney's Docket No.: 42P38886
PATENT

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Full Name of Sole/First Inventor Varghese George
Inventor's Signature  Date 3/14/12
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Full Name of Second/Joint Inventor Santeev S. Jahagirdar
Inventor's Signature _____ Date _____
Residence Folsom, California 95630 Citizenship USA
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Full Name of Third/Joint Inventor Deborah T. Marr
Inventor's Signature _____ Date _____
Residence Portland, Oregon Citizenship USA
(City, State) (Country)
Post Office Address 2564 NW Pettygrove Street
Portland, Oregon 97210 USA

Attorney's Docket No.: 42P38886
PATENT

Title 37, Code of Federal Regulations, Section 1.56
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(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

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 - (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.
- (b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and
- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
 - (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

- (c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:
- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
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- (e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe I am the original and first inventor (if only one name is listed below) or an original and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE (ISA)

the specification of which (check one):

_____ is attached hereto.
 was filed on 12/22/2011 as
 United States Application Number 13/335,257
 or PCT International Application Number _____
 and was amended on _____
 (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application(s)</u>			<u>Priority Claimed?</u>		<u>Certified Copy Attached?</u>	
<u>(Number)</u>	<u>(Country)</u>	<u>(Foreign Filing Date - MM/DD/YYYY)</u>	<u>Yes</u>	<u>No</u>	<u>Yes</u>	<u>No</u>
_____	_____	_____	_____	_____	_____	_____
_____	_____	_____	_____	_____	_____	_____
_____	_____	_____	_____	_____	_____	_____

I hereby appoint practitioners associated with the Customer Number: 45209
as my/our attorney(s) or agents(s), with full power of substitution and revocation, to prosecute this application and to
transact all business in the United States Patent and Trademark Office connected therewith.

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45209

c/o BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, California 94085-4040 U.S.A.
Telephone: (408) 720-8300
Fax: (408) 720-8383

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Varghese George

Inventor's Signature _____ Date _____

Residence Folsom, California Citizenship USA
(City, State) (Country)

Post Office Address 1113 Halidon Way
Folsom, California 95630 USA

Full Name of Second/Joint Inventor Sanjeev S. Jahagirdar

Inventor's Signature  Date 03/20/12

Residence Folsom, California 95630 Citizenship USA
(City, State) (Country)

Post Office Address 1675 Stronsay Court
Folsom, California 95630 USA

Full Name of Third/Joint Inventor Deborah T. Marr

Inventor's Signature _____ Date _____

Residence Portland, Oregon Citizenship USA
(City, State) (Country)

Post Office Address 2564 NW Pettygrove Street
Portland, Oregon 97210 USA

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

(e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe I am the original and first inventor (if only one name is listed below) or an original and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE (ISA)

the specification of which (check one):

 is attached hereto.
 X was filed on 12/22/2011 as
 United States Application Number 13/335,257
 or PCT International Application Number
 and was amended on
 (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application(s)</u>			<u>Priority Claimed?</u>		<u>Certified Copy Attached?</u>	
<u>(Number)</u>	<u>(Country)</u>	<u>(Foreign Filing Date - MM/DD/YYYY)</u>	<u>Yes</u>	<u>No</u>	<u>Yes</u>	<u>No</u>
<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
<u>(Number)</u>	<u>(Country)</u>	<u>(Foreign Filing Date - MM/DD/YYYY)</u>	<u>Yes</u>	<u>No</u>	<u>Yes</u>	<u>No</u>
<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
<u>(Number)</u>	<u>(Country)</u>	<u>(Foreign Filing Date - MM/DD/YYYY)</u>	<u>Yes</u>	<u>No</u>	<u>Yes</u>	<u>No</u>

Attorney's Docket No.: 42P38886
PATENT

I hereby appoint practitioners associated with the Customer Number: **45209**
as my/our attorney(s) or agents(s), with full power of substitution and revocation, to prosecute this application and to
transact all business in the United States Patent and Trademark Office connected therewith.

Please direct all correspondence to the Correspondence Address Below:

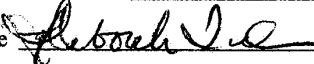
45209

c/o BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
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Sunnyvale, California 94085-4040 U.S.A.
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date _____
Residence Folsom, California Citizenship USA
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(City, State) (Country)
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Folsom, California 95630 USA

Full Name of Third/Joint Inventor Deborah T. Marr
Inventor's Signature  Date 4/11/2012
Residence Portland, Oregon Citizenship USA
(City, State) (Country)
Post Office Address 2564 NW Pettygrove Street
Portland, Oregon 97210 USA

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- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
 - (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.
- (b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
- (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

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- (c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:
- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
- (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.
- (e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

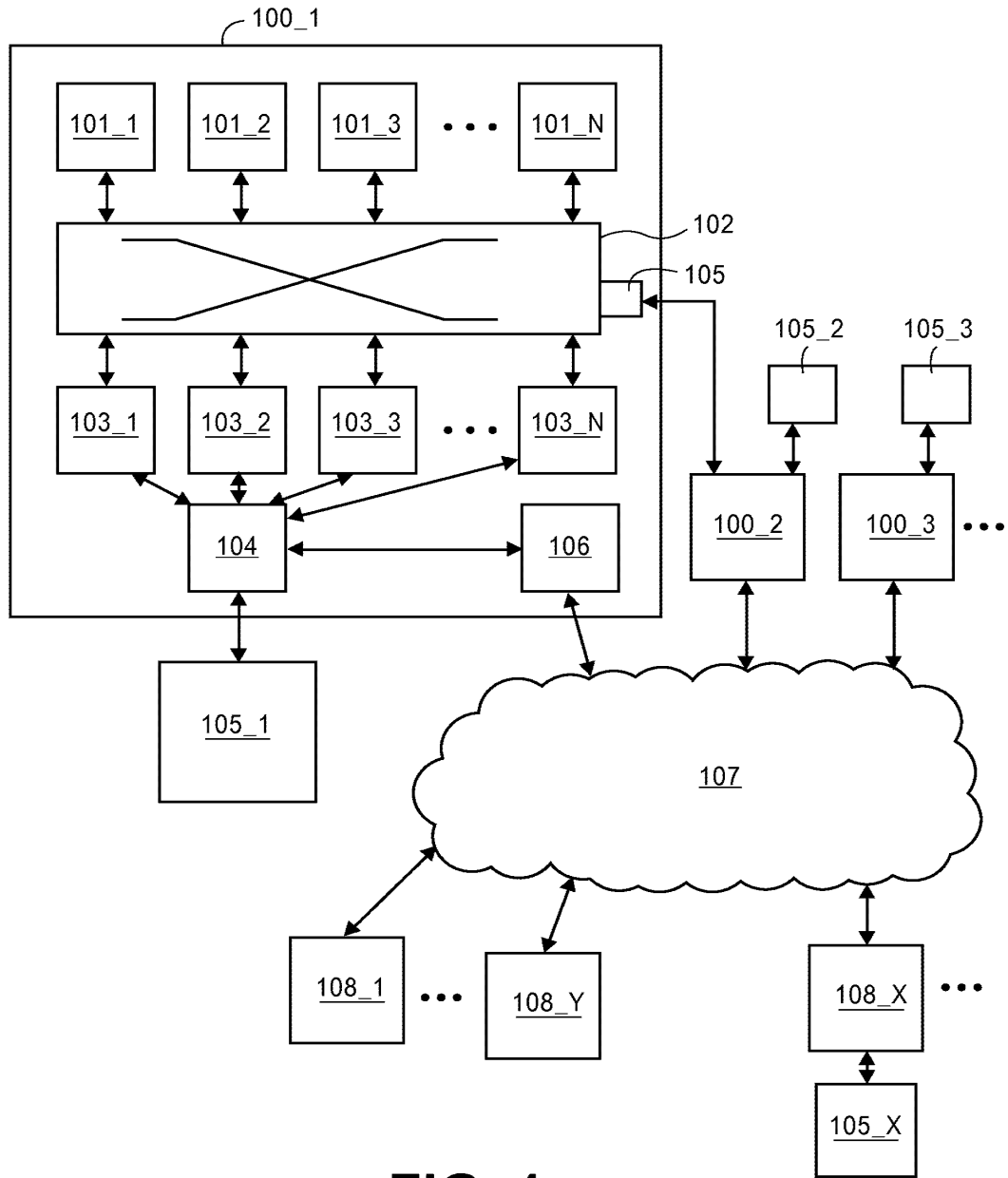


FIG. 1

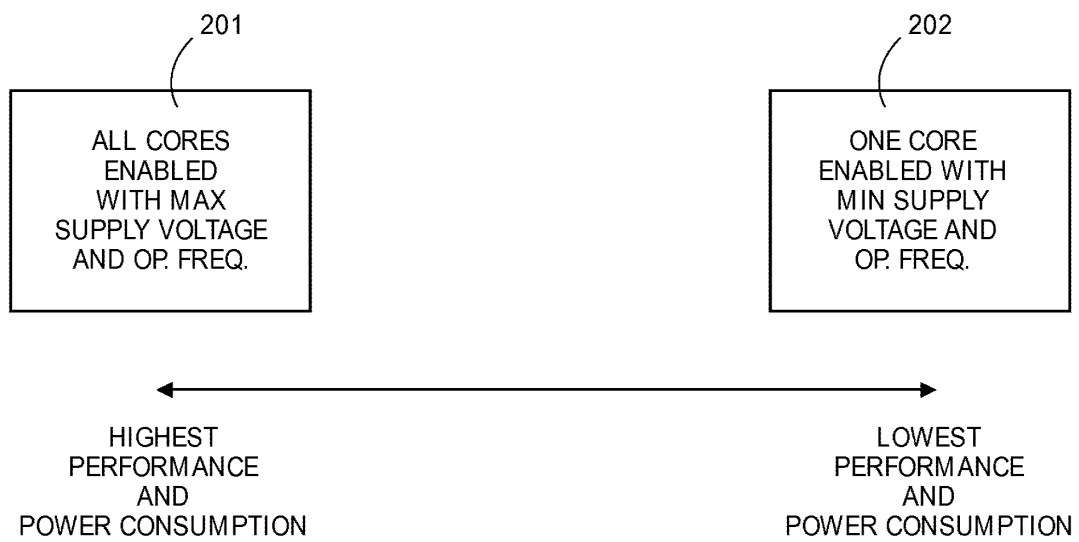


FIG. 2

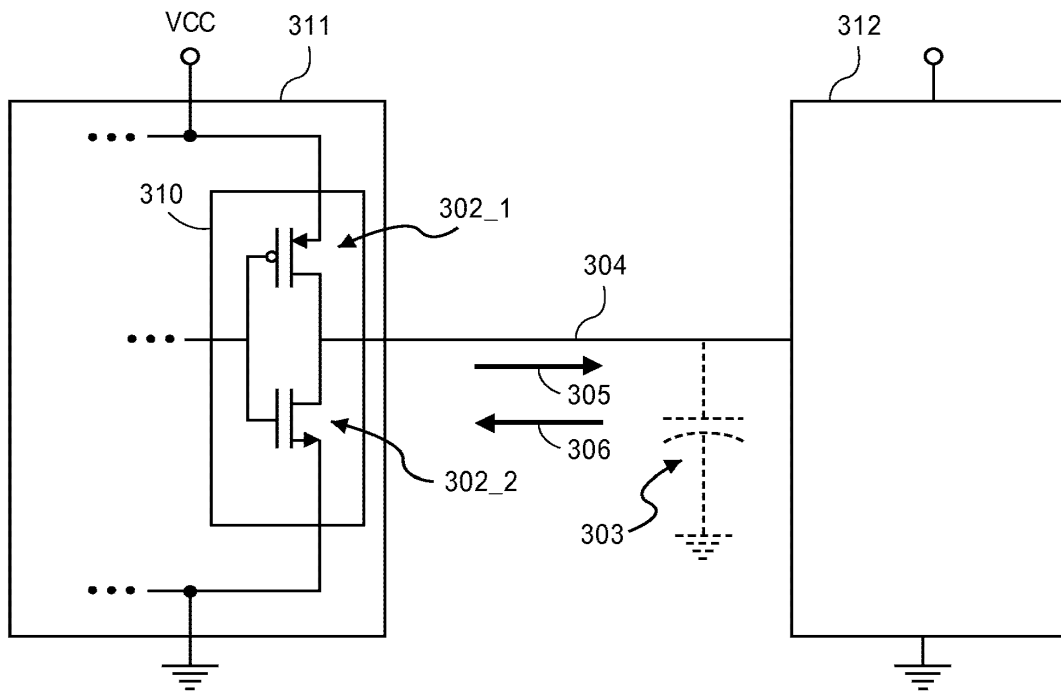


FIG. 3

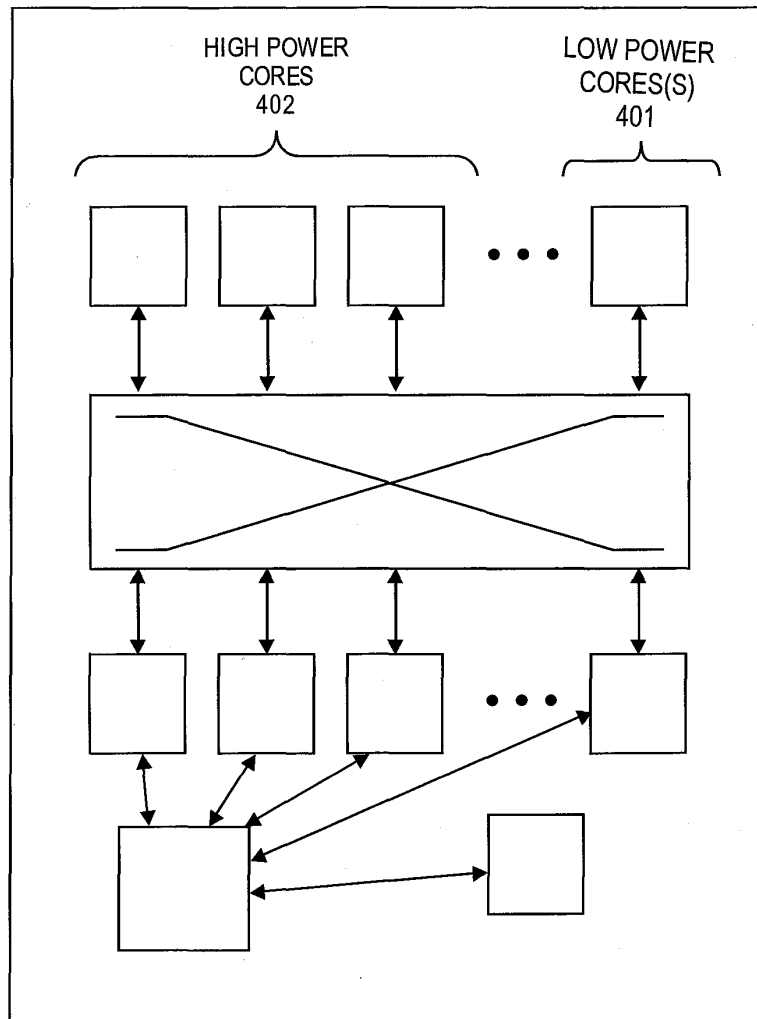


FIG. 4

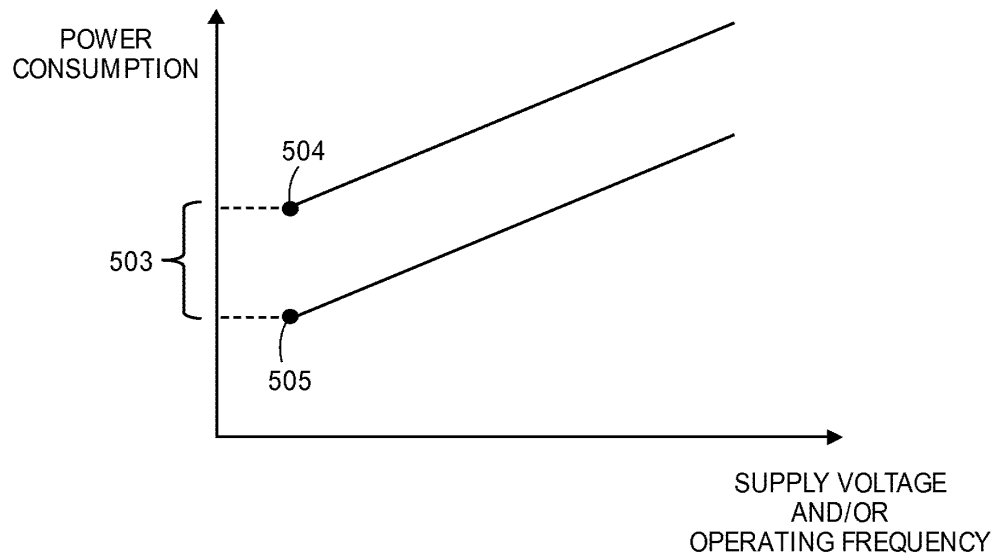


FIG. 5

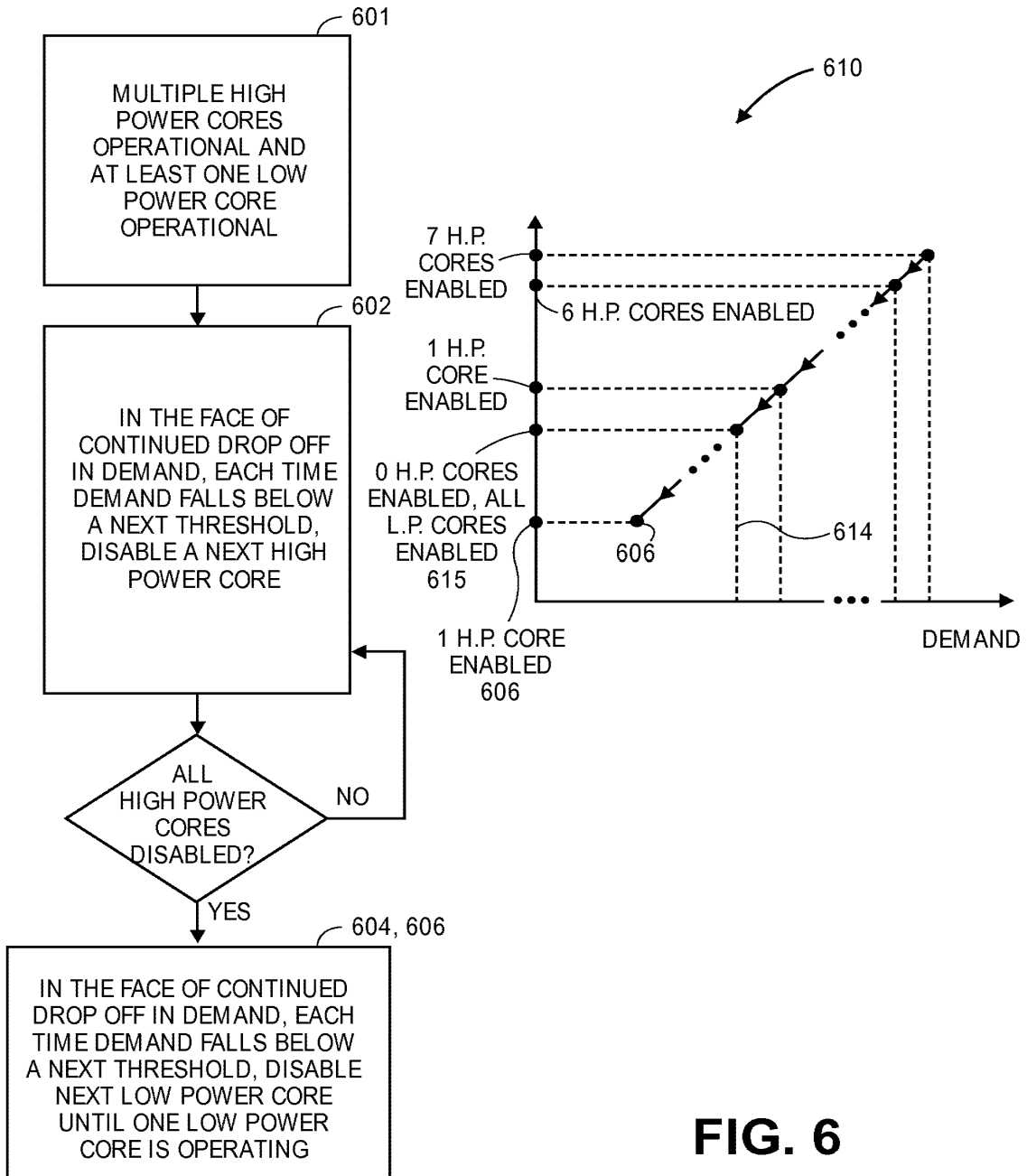


FIG. 6

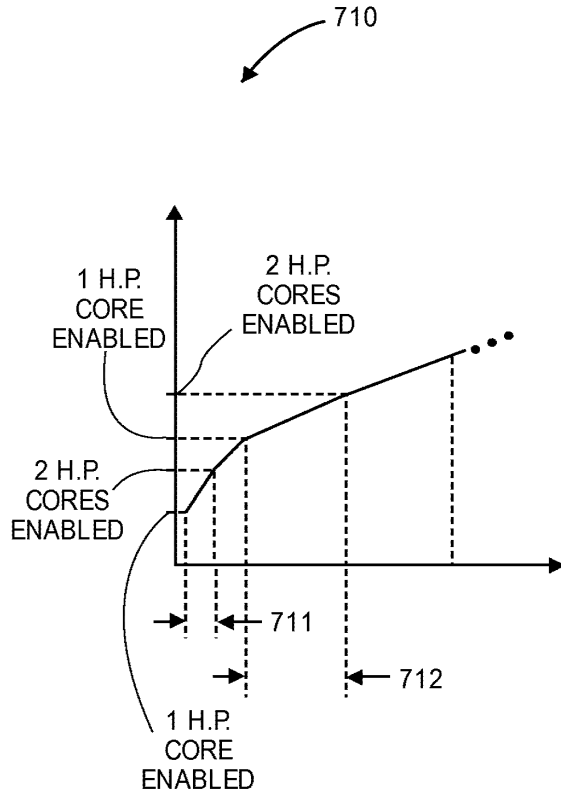
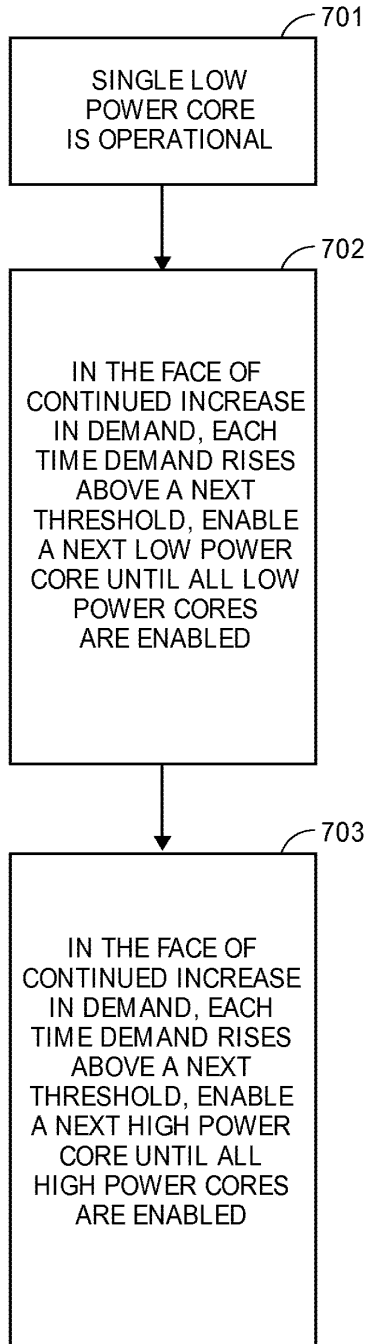


FIG. 7

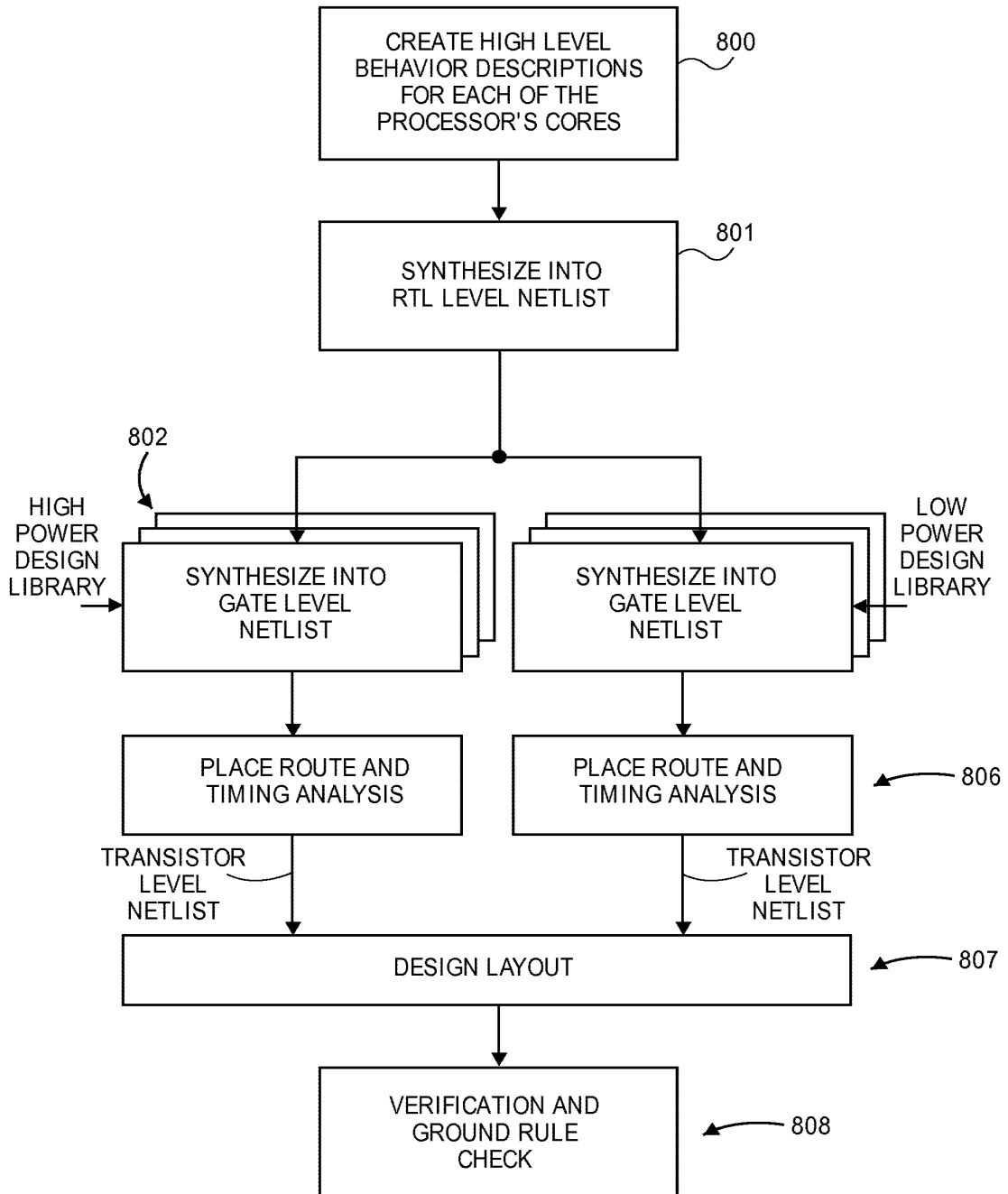


FIG. 8

Electronic Patent Application Fee Transmittal

Application Number:	13335257			
Filing Date:	22-Dec-2011			
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE			
First Named Inventor/Applicant Name:	George Varghese			
Filer:	Robert O'Rourke/c v			
Attorney Docket Number:	42P38886			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	1251	1	150	150
Miscellaneous:				
Total in USD (\$)				280

Electronic Acknowledgement Receipt

EFS ID:	12541969
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	George Varghese
Customer Number:	45209
Filer:	Robert O'Rourke/c v
Filer Authorized By:	Robert O'Rourke
Attorney Docket Number:	42P38886
Receipt Date:	13-APR-2012
Filing Date:	22-DEC-2011
Time Stamp:	17:48:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$280
RAM confirmation Number	4992
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)
 Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)
 Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	42P38886_DECLARATION_04_13_12.PDF	520307 92f448232cef9c931aa76e9d4b5a2571da964e13	no	12

Warnings:

Information:

2	Drawings-only black and white line drawings	42P38886_Replacement_Sheets_04_13_12.pdf	197120 8c00ee90eb911d62a24685930f599889276a3ada	no	8
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Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	32655 595b87ad5ee2d0e27a87baf442b55517caf85492	no	2
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Warnings:

Information:

Total Files Size (in bytes): 750082

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,257	12/22/2011	George Varghese	42P38886	6542
45209	7590	03/06/2012	EXAMINER	
MISSION/BSTZ BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085-4040			ART UNIT	PAPER NUMBER
			2825	
			MAIL DATE	DELIVERY MODE
			03/06/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



MISSION/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE CA 94085-4040

MAR 06 2012

In re Application of	:	
GEORGE VARGHESE	:	DECISION ON PETITION
Application No. 13/335,257	:	TO MAKE SPECIAL UNDER
Filed: December 22, 2011	:	THE GREEN TECHNOLOGY
Attorney Docket No. 42P38886	:	PILOT PROGRAM

This is a decision on the petition under 37 CFR 1.102, filed December 22, 2011, to make the above-identified application special under the pilot program for applications pertaining to Green Technologies as set forth in 74 Federal Register Notice 64666 (December 8, 2009) and amended by 75 Federal Register Notice 28554 (May 21, 2010), 75 Federal Register Notice 69049 (November 10, 2010) and 76 Federal Register Notice 77979 (December 15, 2011).

The latest Notice extended the Green Technology Pilot Program to a total of 3,500 applications or March 30, 2012, whichever occurs earlier. As the program limit of 3500 granted petitions was reached for applications ready for decision on petition as of February 16, 2012, the program is now terminated. No further applications will be considered.

Accordingly, the petition is **DENIED**.

Additional information regarding the Green Technology Petition Pilot can be found at:
http://www.uspto.gov/patents/init_events/green_tech.jsp.

/Blaine Copenheaver/

Blaine Copenheaver
Quality Assurance Specialist
Technology Center 1700



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Table with 7 columns: APPLICATION NUMBER, FILING or 371(c) DATE, GRP ART UNIT, FIL FEE REC'D, ATTY DOCKET NO, TOT CLAIMS, IND CLAIMS. Row 1: 13/335,257, 12/22/2011, 2825, 1550, 42P38886, 19, 3

CONFIRMATION NO. 6542

FILING RECEIPT

45209
MISSION/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040



Date Mailed: 01/13/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections

Applicant(s)

George Varghese, Residence Not Provided;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 01/09/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 13/335,257

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: Yes

Title

ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

Preliminary Class

716

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage, facilitate, and accelerate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.



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Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 4 columns: APPLICATION NUMBER (13/335,257), FILING OR 371(C) DATE (12/22/2011), FIRST NAMED APPLICANT (George Varghese), ATTY. DOCKET NO./TITLE (42P38886)

CONFIRMATION NO. 6542

FORMALITIES LETTER

45209
MISSION/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040



Date Mailed: 01/13/2012

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 1-8.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is **\$130** for a non-small entity
• **\$130** Surcharge.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://portal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/jmilani/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
13/335,257

APPLICATION AS FILED - PART I

(Column 1)		(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 = *	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		x =	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 42P38886
(maximum 12 characters)

First Named Inventor George Varghese

Title: AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE (ISA)

ADDRESS TO: **Commissioner for Patents**
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. **Fee Transmittal Form (e.g., PTO/SB/17)**
(Submit an original and a duplicate for fee processing)
2. **Applicant Claims Small Entity Status. (37 CFR 1.27)**
3. **Specification (Total Pages 16)**
(preferred arrangement set forth below)
 - Descriptive Title of the Invention
 - Cross Reference to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference sequence listing, a table,
or a computer program listing appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
4. **Drawings(s) (35 USC 113) (Total Sheets 8)**
5. **Oath or Declaration (Total Pages)**
 - a. Newly Executed (Original or Copy)
 - b. Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 18 completed)
 - i. DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
 - c. Unsigned.
6. **Application Data Sheet. (37 CFR 1.76)**
7. CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. CD-ROM or CD-R (2 copies); or
 - ii. paper
 - c. Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. **Assignment Papers (cover sheet & documents(s))**
10. a. Separate 37 CFR 3.73(b) Statement (where there is an assignee)
- b. Power of Attorney
11. English Translation Document (if applicable)
12. a. Information Disclosure Statement (IDS)/PTO-1449 (or PTO/SB/08)
- b. Copies of IDS Citations
13. **Preliminary Amendment**
14. **Return Receipt Postcard (MPEP 503) (Should be specifically itemized)**
15. Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. **Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.**
- 17A. Claim for Foreign Priority
- 17B. Other: Petition to Make Special Under the Green Technology Pilot Program, and Statement of Special Status

17C. Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

18. If a **CONTINUING APPLICATION**, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title (e.g., by way of preliminary amendment), or in an Application Data Sheet Under 37 C.F.R. 1.76:

Continuation Divisional Continuation-in-part (CIP)
 Of Prior Application No.: _____ Examiner _____ Group Art Unit _____
 (which is a continuation/ divisional/ CIP of prior application no. _____,
 which is a continuation/ divisional/ CIP of prior application no. _____) (List entire chain of priority)

Applicant(s): Also include a Preliminary Amendment to amend the specification to claim priority.
 For CONTINUATION AND DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation **can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.**

19. Correspondence Address
 Customer Number or Bar Code Label 45209
 or
 (Insert Customer No. or Attach Bar Code Label here)
 Correspondence Address Below
 NAME Robert B. O'Rourke Registration No.: 46,972
 SIGNATURE /Robert B. O'Rourke/
 DATE December 22, 2011
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
 ADDRESS 1279 Oakmead Parkway
 CITY Sunnyvale STATE California ZIP CODE 94085
 Country U.S.A. TELEPHONE (408) 720-8300 FAX (408) 720-8383

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Name (PRINT/TYPE): Alma Goldchain

Signature: /Alma Goldchain/ Date: 12/22/11

Electronic Patent Application Fee Transmittal

Application Number:					
Filing Date:					
Title of Invention:	AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE				
First Named Inventor/Applicant Name:	George Varghese				
Filer:	Robert O'Rourke/Alma Goldchain				
Attorney Docket Number:	42P38886				
Filed as Large Entity					
Utility under 35 USC 111(a) Filing Fees					
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)	
Basic Filing:					
Utility application filing	1011	1	380	380	
Utility Search Fee	1111	1	620	620	
Utility Examination Fee	1311	1	250	250	
Pages:					
Claims:					
Miscellaneous-Filing:					
Publ. Fee- early, voluntary, or normal	1504	1	300	300	
Petition:					

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1550

Electronic Acknowledgement Receipt

EFS ID:	11693011
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	George Varghese
Customer Number:	45209
Filer:	Robert O'Rourke/Alma Goldchain
Filer Authorized By:	Robert O'Rourke
Attorney Docket Number:	42P38886
Receipt Date:	22-DEC-2011
Filing Date:	
Time Stamp:	16:32:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1550
RAM confirmation Number	4202
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Green Tech Petition under 37 CFR 1.102	sb0420_Petition_To_Make_Special_Under_The_Green_Technology_Pilot_Program_12-22-2011.pdf	152973 6753b4a7cc7f818dfba5a4d6958eca2287d71	no	3
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	42P38886_Statement_of_Special_Status_12-22-2011.pdf	17721 18a602fb37c91069295096f06b41178e9cdd391	no	2
Warnings:					
Information:					
3		42P38886_APPLICATION_12-22-2011.pdf	108490 eb73681cf710277b6e900a57b4c8f9e32f386dd	yes	16
Multipart Description/PDF files in .zip description					
		Document Description	Start	End	
		Specification	1	12	
		Claims	13	15	
		Abstract	16	16	
Warnings:					
Information:					
4	Drawings-only black and white line drawings	42P38886_FIGURES_12-22-2011.PDF	119862 c734c484ec36ee8f52312a3e9f2ce7dfc6e0beb5	no	8
Warnings:					
Information:					
5	Transmittal of New Application	42P38886_Utility_TRANSMITTAL_12-22-2011.pdf	26087 081f7e3cdf143e89b1db94acac6bed3c5bc5b796	no	2
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	36701 c3059cb3b6f94337bace9bc9bfc9bae08b8f8ab9	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			461834		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	11693011
Application Number:	13335257
International Application Number:	
Confirmation Number:	6542
Title of Invention:	AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	George Varghese
Customer Number:	45209
Filer:	Robert O'Rourke/Alma Goldchain
Filer Authorized By:	Robert O'Rourke
Attorney Docket Number:	42P38886
Receipt Date:	22-DEC-2011
Filing Date:	
Time Stamp:	16:32:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1550
RAM confirmation Number	4202
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Green Tech Petition under 37 CFR 1.102	sb0420_Petition_To_Make_Special_Under_The_Green_Technology_Pilot_Program_12-22-2011.pdf	152973 6753b4a7cc7f818dfba5a4d6958eca2287d71	no	3
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	42P38886_Statement_of_Special_Status_12-22-2011.pdf	17721 18a602fb37c91069295096f06b41178e9cdd391	no	2
Warnings:					
Information:					
3		42P38886_APPLICATION_12-22-2011.pdf	108490 eb73681cf710277b6e900a57b4c8f9e32f386dd	yes	16
Multipart Description/PDF files in .zip description					
		Document Description	Start	End	
		Specification	1	12	
		Claims	13	15	
		Abstract	16	16	
Warnings:					
Information:					
4	Drawings-only black and white line drawings	42P38886_FIGURES_12-22-2011.PDF	119862 c734c484ec36ee8f52312a3e9f2ce7dfc6e01eb5	no	8
Warnings:					
Information:					
5	Transmittal of New Application	42P38886_Utility_TRANSMITTAL_12-22-2011.pdf	26087 081f7e3cdf143e89b1db94acac6bed3c5bc5b796	no	2
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	36701 c3059cb3b6f94337bace9bc9bfc9bae08b8f8ab9	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			461834		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PETITION TO MAKE SPECIAL UNDER THE GREEN TECHNOLOGY PILOT PROGRAM		
Attorney Docket Number: 42P38886	Application Number (if known):	Filing date: 12/22/2011
First Named Inventor: VARGHESE		
Title: AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE...		
APPLICANT HEREBY REQUESTS TO PARTICIPATE IN THE GREEN TECHNOLOGY PILOT PROGRAM FOR THE ABOVE-IDENTIFIED APPLICATION. See Instruction Sheet on page 2.		
This petition must be timely filed electronically using the USPTO electronic filing system, EFS-Web.		
1. By filing this petition:		
Applicant is requesting early publication: Applicant hereby requests early publication under 37 CFR 1.219 and the publication fee set forth in 37 CFR 1.18(d) accompanies this request.		
2. By filing this petition: applicant is agreeing to make an election without traverse in a telephonic interview and elect an invention that meets the eligibility requirements for the Green Technology Pilot Program, if the Office determines that the claims are not obviously directed to a single invention. See Instruction Sheet.		
3. This request is accompanied by statements of special status for the eligibility requirement.		
4. The application contains no more than three (3) independent claims and twenty (20) total claims.		
5. The application does not contain any multiple dependent claims.		
6. Other attachments: _____		

Signature /Robert B. O'Rourke/	Date /12-22-2011/
Name (Print/Typed) Robert B. O'Rourke	Registration Number 46,972
Note: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below*.	
<input type="checkbox"/> *Total of <u>1</u> forms are submitted.	

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**Instruction Sheet for
Petition to Make Special Under the Green Technology Pilot Program**
(Not to be Submitted to the USPTO)

The following is a summary of the requirements (for more information see the notices (i) "Pilot Program for Green Technologies Including Greenhouse Gas Reduction," (ii) "Elimination of Classification Requirement in the Green Technology Pilot Program," and (iii) "Expansion and Extension of the Green Technology Pilot Program," available on the USPTO web site at http://www.uspto.gov/patents/init_events/green_tech.jsp):

- (1) The application must be a non-reissue, non-provisional utility application filed under 35 U.S.C. 111(a), or an international application that has entered the national stage in compliance with 35 U.S.C. 371, irrespective of the filing date of the application. Reexamination proceedings are excluded from this pilot program.
- (2) The application must contain three or fewer independent claims and twenty or fewer total claims. The application must not contain any multiple dependent claims. For an application that contains more than three independent claims or twenty total claims, or multiple dependent claims, applicant must file a preliminary amendment in compliance with 37 CFR 1.121 to cancel the excess claims and/or the multiple dependent claims at the time the petition to make special is filed.
- (3) The claims must be directed to a single invention that materially enhances the quality of the environment, or that materially contributes to: (1) the discovery or development of renewable energy resources; (2) the more efficient utilization and conservation of energy resources; or (3) green house gas emission reduction (see the eligibility requirements of sections II and III of the notice (i) cited above). The petition must include a statement that, if the USPTO determines that the claims are directed to multiple inventions (e.g., in a restriction requirement), applicant will agree to make an election without traverse in a telephonic interview, and elect an invention that meets the eligibility requirements in section II or III of the notice (i) cited above.
- (4) The petition to make special must be timely filed electronically using the USPTO electronic filing system, EFS-Web, and selecting the document description of "Petition for Green Tech Pilot" on the EFS-Web screen. Applicant should use form PTO/SB/420, which is available as a Portable Document Format (PDF) fillable form in EFS-Web and on the USPTO Web site.
- (5) The petition to make special must be filed at least one day prior to the date that a first Office action (which may be an Office action containing only a restriction requirement) appears in the Patent Application Information Retrieval (PAIR) system. Applicant may check the status of the application using PAIR.
- (6) The petition to make special must be accompanied by a request for early publication in compliance with 37 CFR 1.219 and the publication fee set forth in 37 CFR 1.18(d).

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No.: 42P38886

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: VARGHESE

Application No.: TBD

Art Unit: TBD

Filed: TBD

Confirmation No.: TBD

For: AN ASYMMETRIC PERFORMANCE
MULTICORE ARCHITECTURE WITH
SAME INSTRUCTION SET
ARCHITECTURE (ISA)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT OF SPECIAL STATUS

Dear Sir/Mdm:

Applicants respectfully submit that the above-identified application is eligible for the Green Technology Pilot Program in that the described subject matter materially contributes to the more efficient utilization and conservation of energy resources.

In this regard, the application describes a method and system for determining an energy-efficient operating point of a platform. The platform has logic to dynamically manage setting(s) of the processing cores and/or platform components in the platform to achieve maximum system energy efficiency by using the characteristics of the workload and/or platform.

It is respectfully submitted that the above petition should be granted and the above application should be accorded special status under the Green Technology Pilot Program.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: /12-22-2011/

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PATENT

UNITED STATES PATENT APPLICATION

For

**AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE
WITH SAME INSTRUCTION SET ARCHITECTURE (ISA)**

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Attorney's Docket No. 42P38886

Petitioner Mercedes Ex-1010, 0247

AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE (ISA)

BACKGROUND

Field of Invention

[0001] The field of invention relates generally to computing system architecture, and, more specifically, to an asymmetric performance multicore architecture with same instruction set architecture (ISA).

Background

[0002] Fig. 1 shows a typical multi-core processor 100_1. As observed in Fig. 1, the multi-core processor 100_1 includes a plurality of processor cores 101_1 to 101_N on a same semiconductor die 100_1. Each of the processor cores typically contain at least one caching layer for caching data and/or instructions. A switch fabric 102 interconnects the processor cores 101_1 to 101_N to one another and to one or more additional caching layers 103_1 to 103_N. According to one approach, the processors 101_1 to 101_N and the one or more caching layers have internal coherency logic to, for example, prevent two different cores from concurrently modifying the same item of data.

[0003] A system memory interface (which may also include additional coherency logic) 104 is also included. Here, if a core requests a specific cache line having a needed instruction or item of data, and, the cache line is not found in any of the caching layers, the request is presented to the system memory interface 104. If the looked for cache line is not in the system memory 105_1 that is directly coupled to interface 104, the request is forwarded through system network interface 106 to another multi-core processor to fetch the desired data/instruction from its local system memory (e.g., system memory 105_X of multi-core processor 100_X). A packet switched network 107 exists between the multi-processor cores 100_1 to 100_X to support these kinds of system memory requests.

[0004] Interfaces to system I/O components 108_1 to 108_Y (e.g., deep non volatile storage such as a hard disk drive, printers, external network interfaces, etc.) are also included on the multi-processor core. These interfaces may take the form of high speed link interfaces such as high speed Ethernet interfaces and/or high speed PCIe interfaces.

[0005] Some multi core processors may also have a port 105 to the switch fabric 102 to scale upwards the number of processor cores associated with a same (also scaled upward) caching

structure. For example, as observed Fig. 1, multi-processor cores 101_1 and 101_2 are coupled through the switch fabric port 105 to effectively form a platform of 2N cores that share a common caching structure (processor 100_2 is coupled to processor 100_1 through a similar port to its switch fabric).

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

[0007] Figure 1 shows a multicore processor and surrounding computer system (prior art);

[0008] Figure 2 shows a power management strategy (prior art);

[0009] Figure 3 shows a logic gate drive circuit;

[0010] Figure 4 shows multi core processor having high power and low power cores that support the same instruction set;

[0011] Figure 5 compares power consumption of a high power core and low power core;

[0012] Figure 6 shows a first power management method;

[0013] Figure 7 shows a second power management method;

[0014] Figure 8 shows a design method.

DETAILED DESCRIPTION

Overview

Detailed Description

[0015] Computing system power consumption is becoming more and more of a concern. As such, a number of different power management schemes are incorporated into modern day computing systems. Typically, the power management component of the system will scale up the processing performance of the system as the system's workload increases, and, scale down the processing performance of the system as the system's workload decreases. Decreasing the processing performance of the system corresponds to power savings as the power consumption of the system is strongly correlated with its performance capabilities.

[0016] A typical way to scale processing performance and power consumption with workload is to enable/disable entire cores and raise/lower their supply voltages and operating frequencies in response to system workload. For example, as observed in Fig. 2, under a maximum performance and power consumption state 201 all cores are enabled and each core is provided with a maximum supply voltage and maximum clock frequency. By contrast, under a minimum performance and power consumption state 202 (at which program code can still be executed), only one core is enabled. The single core is provided with a minimum supply voltage and minimum operating frequency.

[0017] Some basic concepts of electronic circuit power consumption are observed in Fig. 3. Here, the driver circuit 310 portion of a logic gate 311 is observed driving a next one or more logic gate(s) 312. Specifically, the speed of operation of interconnected logic gates 311, 312 rises as the width of its driving transistors 302_1, 302_2 (measured, for each transistor, along the semiconductor surface perpendicular to the direction of current flow) increase and the capacitance 303 of the line 304 (and input capacitance of the load logic gate(s) 312) it is driving decreases. Here, in order to raise the voltage on the line from a logic low level to a logic high level, a sufficiently strong current 305 needs to be driven by the source transistor 302_1 through the line to rapidly apply charge to the capacitance 303 (and thereby raise the voltage on the line). Similarly, in order to lower the voltage on the line from a logic high level to a logic low level, a sufficiently strong current 306 needs to be "sunk" by the sink transistor 302_2 through the line to rapidly draw charge off the capacitance (and thereby lower the voltage on the line).

[0018] Essentially, the amount of current the transistors 302_1, 302_2 will source/sink is a function of their respective widths. That is, the wider the transistors are, the more current they will source/sink. Moreover, the amount of current the transistors 302_1, 302_2 will source/sink

is also a function of the supply voltage VCC that is applied to the driver circuit 310 observed in Fig. 3. Essentially, the higher the supply voltage, the stronger the source/sink currents will be.

[0019] Further still, the rate at which the transistors will be able to apply/draw charge to/from the capacitor is a function of the size of the capacitance 303 of the line 304 being driven. Specifically, the transistors will apply/draw charge slower as the capacitance 304 increases and apply/draw charge faster as the capacitance 304 decreases. The capacitance 304 of the line is based on its physical dimensions. That is, the capacitance 304 increases the longer and wider the line, and by contrast, the capacitance 304 decreases the shorter and narrower the line is. The line itself is of fixed dimensions once the circuit is manufactured. Nevertheless, line width and line length are design parameters that designers must account for. The width of the line cannot be narrowed too much or else it will have the effect of increasing the line's resistance which will also slow down the rate of charge applied/drawn to/from the capacitor.

[0020] A final speed factor is the frequency of the signal itself on the line. Essentially, circuits driven with a faster clock signal will more rapidly switch between applying and drawing charge to/from the line capacitance 304 than circuits with a slower clock signal. Here, more rapid switching corresponds to a circuit that is sending binary information faster.

[0021] All of the factors described above for increasing the rate at which the charge on the capacitor is applied/drawn also lead to a circuit that consumes more power. That is, a circuit that is designed to have relatively wide source/sink transistors, a high supply voltage, short load lines and receive a higher frequency clock signal will operate faster and therefore consume more power than circuits oppositely oriented as to these same parameters.

[0022] Recalling the discussion of Figs. 1 and 2, note that prior art multi core processor power management schemes have been implemented on processors whose constituent cores are identical. That is, referring to Fig. 1, all of cores 101_1 to 101_N are identical in design. In other approaches, the cores are not identical but are radically different. Specifically, one of the cores is a low power core but the lower power characteristic is achieved by stripping out sizable chunks of logic circuitry as compared to the other cores. More specifically, the sizable chunks that are stripped out correspond to the logic that executes the program code instructions. Said another way, the low power core supports a reduced instruction set as compared to the higher performance cores. A problem with this approach, however, is that it is difficult for system software to adjust switch operation between processor cores having different instruction sets.

[0023] Fig. 4 depicts a new approach in which at least one of the cores 401 is designed to be lower performance and therefore consume less power than other cores 402 in the processor. However, the lower power core(s) 401 has a same logic design as the higher power core(s) 402

and therefore supports the same instruction set 403 as the high power core(s) 402. The low power core(s) 401 achieve a lower power design point by having narrower drive transistor widths than the higher power core(s) and/or having other power consumption related design features, such as any of those discussed above with respect to Fig. 3, that are oppositely oriented than the same design features in the higher power cores.

[0024] According to one approach, discussed in more detail below, when the multi-processor core is being designed, the same high level description (e.g., the same VHDL or Verilog description) is used for both the higher performance/power core(s) and the lower performance/power core(s). When the higher level descriptions are synthesized into RTL netlists, however, for the subsequent synthesis from an RTL netlist into a transistor level netlist, different technology libraries are used for the low power core(s) than the high power core(s). As alluded to above, the drive transistors of logic gates associated with the libraries used for the low power core(s) have narrower respective widths than the “same” transistors of the “same” logic gates associated with the libraries used for the high power cores.

[0025] By design of the multiprocessor, referring to Fig. 5, the lower power core(s) exhibit inherently lower power consumption (and processing performance) than the higher power core(s). That is, for a same applied clock or operating frequency, because of its narrower drive transistor widths, for example, a lower power core will consume less power than a higher power core. Because of the narrower drive transistor widths, however, the lower power core has a maximum operating frequency that is less than the maximum operating frequency of the higher power core.

[0026] The import of the lower power core, however, is that the multi-processor is able to entertain a power management strategy that is the same/similar to already existing power management strategies, yet, still achieve an even lower power consumption in the lower/lowest performance/power states. Specifically, recall briefly power state 202 of Fig. 2 in which only one core is left operable (the remaining cores are disabled). Here, if the one remaining operable core is the low power core, the processor will exhibit even lower power consumption than the prior art low power state 202.

[0027] The amount of reduced power savings 503 is directly observable in Fig. 5. Here, recall that all the processors were identical in the multi-processor that was discussed with respect to the prior art low power state 202 of Fig. 2. As such, even if the supply voltage and operating voltage was reduced to a minimum, the power consumption would be that of a higher power processor (e.g., having wider drive transistor widths). This operating point is represented by point 504 of Fig. 5. By contrast, in the lowest power operating state of the improved multi-processor, if the

operable core is a low power core it will consume power represented by point 505 of Fig. 5. As such, the improved processor exhibits comparatively lower power consumption at the lower/lowest performance operating states than the prior art multi-processor, while, at the same time, fully supporting the instruction set architecture the software is designed to operate on.

[0028] Fig. 6 shows a power management process flow that can be executed, for example, with power management software that is running on the multi-processor (or another multi-processor or separate controller, etc.). Conversely, the power management process flow of Fig. 6 can be executed entirely in hardware on the multi-processor or by some combination of such hardware and software.

[0029] According to the process flow of Fig. 6, from an initial state 601 where at least some high power processor cores and the low power core(s) are operating, in response to a continued drop in demand on the multi-processor, another high power core is disabled each time the continued drop in demand falls below some next lower threshold. For example, in a multi-processor core having sixteen cores where fourteen cores are high power cores and two cores are low power cores, the initial state 601 may correspond to a state where seven of the high power cores and both of the low power cores are operational.

[0030] In response to continued lower demand placed on the multi-processor, the seven high power cores will be disabled one by one with each new lower demand threshold 602. For instance, as observed at inset 610, demand level 611 justifies enablement of the seven high power cores and both low power cores. As the demand continually drops to a next lower threshold 612, one of the high power cores is disabled 613 leaving six operable high power cores and two low power cores.

[0031] Before the high power core is disabled, as a matter of designer choice, the core's individual operating frequency, or the operating frequency of all (or some of) the enabled high power cores, or the operating frequency of all (or some of) the enabled high power cores and the low power cores may be lowered to one or more lower operating frequency levels.

[0032] A similar designer choice exists with respect to the supply voltages applied to the cores. That is, before the high power core is disabled, as a matter of designer choice, the core's individual supply voltage, or the supply voltage of all (or some of) the enabled high power cores, or the supply voltage of all (or some of) the enabled high power cores and the low power cores may be lowered to one or more lower supply voltages. Supply voltages may be lowered in conjunction with the lowering of operating frequency, or, just one or none of these parameters may be lowered as described above.

[0033] Eventually, with the continued drop in demand, the last remaining high power core will be disabled 615 after demand falls below some lower threshold 614. This leaves only the low power cores in operation. Operating frequency and/or supply voltage of the low power core(s) may likewise be lowered as demand continues to drop beneath level 614. With continued drop in demand a similar process of disabling cores as demand falls below each next lower demand threshold 604 continues until the multi-processor core is left with only one low power core remaining as its sole operating core 606.

[0034] State 606 is reached of course with the disablement of the last high power core in implementations where the processor only has one lower power core. Again supply voltage and/or operating frequency of the sole remaining low power core may be lowered as demand continues to fall. Importantly, in state 606, as discussed above, the multi-processor will exhibit lower power consumption than other multi-processor cores having an identical power management scheme but whose constituent cores are all high power cores. Even lower power consumption can be provided for in state 606 if the sole operating low power core is provided with a lower supply voltage and/or lower operating frequency that the lowest operating supply voltage and/or operating frequency applied to the high power cores.

[0035] No special adjustment needs to be made by or for application software, virtual machine or virtual machine monitor when the system is running only on the low power core(s) after all the high power cores are disabled. Again, the preservation of the same instruction core across all cores in the system corresponds to transparency from the software's perspective as to the underlying cores. Lower performance may be recognized with lower cores but no special adjustments as to the content of the instruction streams should be necessary. In various alternate implementations: 1) the hardware/machine readable firmware can monitor and control the core mix; or, 2) the hardware can relinquish control to the Operating system and let it monitor the demand and control the core mix.

[0036] Fig. 7 shows essentially a reverse of the processes described above. As observed in Fig. 7, starting from a state in which only a single low power core is operating 701 additional low power cores are enabled (if any more) 702 as demand on the multi-processor continually increases. Eventually, high power cores are enabled 703. Notably, the demand threshold needed to enable a next processor from an operating low power processor may correspond to a lower demand increment than the demand threshold needed to enable to a next processor from an operating high power processor.

[0037] That is, inset 710 shows the increase in demand 711 needed after a low power processor is first enabled to trigger the enablement of a next processor in the face of increased demand.

The increase in demand 712 needed after a high power processor is first enabled to trigger enablement of a next high power processor in the face of increased demand is greater than the aforementioned demand 711. This is so because a high power processor is able to handle more total demand than a low power processor and therefore does not need to have additional “help” as soon as a low power processor does.

[0038] Operating frequency and/or supply voltage may also be increased in conjunction with the enablement of cores in the face of increased demand in a logically inverse manner to that discussed above with respect to the disablement of cores.

[0039] Fig. 8 shows a design process for designing a multi-core processor consistent with the principles discussed above. As part of the design process, high level behavioral descriptions 800 (e.g., VHDL or Verilog descriptions) for each of the processor’s cores are synthesized into a Register Transfer Level (RTL) netlist 801. The RTL netlist is synthesized 802 into corresponding higher power core gate level netlist(s) (one for each high power core) with libraries corresponding to a higher power/performance design (such as logic circuits having wider drive transistors). The RTL netlist is also synthesized 803 into corresponding lower power core gate level netlist(s) (one for each low power core) with libraries corresponding to a lower power/performance design (such as logic circuits having wider drive transistors). Here, the logic designs for the high power and low power cores are the same but the design of their corresponding logic circuits have different performance/power design points.

[0040] The transistor level netlists for the respective cores are then used as a basis for performing a respective place, route and timing analysis 806 and design layout 807. Here, the lower power/performance cores may have more relaxed placement and timing guidelines owing to the larger permissible propagation delay through and between logic circuits. Said another way, recalling from the discussion of Fig. 3 that longer load lines result in slower rise and fall times, the lower performance cores may permit longer load lines between transistors and gates because these cores are designed to have slower operation (of course, if load lines are increased to much along with the inclusion of narrower drive transistors, the drop in performance may be more than desired).

[0041] Upon completion of the layout and timing analysis, the cores are cleared for manufacture upon a clean manufacturing ground rule check 808.

[0042] Processes taught by the discussion above may be performed with program code such as machine-executable instructions that cause a machine that executes these instructions to perform certain functions. In this context, a “machine” may be a machine that converts intermediate form (or “abstract”) instructions into processor specific instructions (e.g., an abstract execution

environment such as a “virtual machine” (e.g., a Java Virtual Machine), an interpreter, a Common Language Runtime, a high-level language virtual machine, etc.), and/or, electronic circuitry disposed on a semiconductor chip (e.g., “logic circuitry” implemented with transistors) designed to execute instructions such as a general-purpose processor and/or a special-purpose processor. Processes taught by the discussion above may also be performed by (in the alternative to a machine or in combination with a machine) electronic circuitry designed to perform the processes (or a portion thereof) without the execution of program code.

[0043] It is believed that processes taught by the discussion above may also be described in source level program code in various object-orientated or non-object-orientated computer programming languages (e.g., Java, C#, VB, Python, C, C++, J#, APL, Cobol, Fortran, Pascal, Perl, etc.) supported by various software development frameworks (e.g., Microsoft Corporation’s .NET, Mono, Java, Oracle Corporation’s Fusion, etc.). The source level program code may be converted into an intermediate form of program code (such as Java byte code, Microsoft Intermediate Language, etc.) that is understandable to an abstract execution environment (e.g., a Java Virtual Machine, a Common Language Runtime, a high-level language virtual machine, an interpreter, etc.) or may be compiled directly into object code.

[0044] According to various approaches the abstract execution environment may convert the intermediate form program code into processor specific code by, 1) compiling the intermediate form program code (e.g., at run-time (e.g., a JIT compiler)), 2) interpreting the intermediate form program code, or 3) a combination of compiling the intermediate form program code at run-time and interpreting the intermediate form program code. Abstract execution environments may run on various operating systems (such as UNIX, LINUX, Microsoft operating systems including the Windows family, Apple Computers operating systems including MacOS X, Sun/Solaris, OS/2, Novell, etc.).

[0045] An article of manufacture may be used to store program code. An article of manufacture that stores program code may be embodied as, but is not limited to, one or more memories (e.g., one or more flash memories, random access memories (static, dynamic or other)), optical disks, CD-ROMs, DVD ROMs, EPROMs, EEPROMs, magnetic or optical cards or other type of machine-readable media suitable for storing electronic instructions. Program code may also be downloaded from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals embodied in a propagation medium (e.g., via a communication link (e.g., a network connection)).

[0046] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications

and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims.

CLAIMS

What is claimed is:

1. A multi-core processor comprising a plurality of cores that support a same instruction set, where, at least one of the cores is constructed of logic gates that consume less power, for a same applied operating frequency and supply voltage, than the same corresponding logic gates of at least one other of the cores.

2. The multi-core processor of claim 1 wherein the logic gates that consume less power have narrower logic gate driver transistors than the same corresponding logic gates of the at least one other of the cores.

3. The multi-core processor of claim 1 wherein there are at least two cores that are constructed of the logic gates that consume less power.

4. The multi-core processor of claim 1 wherein only one of the cores is constructed of the logic gates that consume less power.

5. The multi-core processor of claim 1 further comprising a switch fabric between the cores and a system memory interface.

6. A method, comprising:

operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency.

7. The method of claim 6 further comprising:

disabling the first core but leaving the second core operable in response to lower demand being offered to the multi-core processor.

8. The method of claim 7 further comprising enabling the first core after it is disabled in response to higher demand being offered to the multi-core processor.

9. The method of claim 8 wherein said method further comprises:

disabling said first core after detecting a first drop in demand offered to said multi-core processor;

enabling said first core after detecting a first rise in demand offered to said multi-core processor, the amount of demand associated with said first drop being greater than the amount of demand associated with said second drop.

10. The method of claim 6 wherein the operating of the first core includes driving load lines with wider transistor widths than corresponding transistor widths in said second core.

11. The method of claim 6 further comprising lowering a supply voltage and/or operating frequency of said first core in response to lower demand being offered to said multi-core processor.

12. The method of claim 6 further comprising raising a supply voltage and/or operating frequency of said first core in response to higher demand being offered to said multi-core processor.

13. The method of claim 6 further comprising:

disabling said first core in response to a drop in demand applied to said multi-core processor; and,

lowering a supply voltage and/or operating frequency of said second core in response to an additional drop in demand applied to said multi-core processor.

14. A machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency;

disabling the first core but leaving the second core operable in response to lower demand being offered to the multi-core processor;

15. The machine readable medium of claim 14 wherein said method further comprises enabling the first core after it is disabled in response to higher demand being offered to the multi-core processor.

16. The machine readable medium of claim 15 wherein said method further comprises:
disabling said first core after detecting a first drop in demand offered to said multi-core processor;

enabling said first core after detecting a first rise in demand offered to said multi-core processor, the amount of demand associated with said first drop being greater than the amount of demand associated with said second drop.

17. The machine readable medium of claim 14 wherein said method further comprises lowering a supply voltage and/or operating frequency of said first core in response to lower demand being offered to said multi-core processor.

18. The machine readable medium of claim 14 wherein said method further comprises raising a supply voltage and/or operating frequency of said first core in response to higher demand being offered to said multi-core processor.

19. The machine readable medium of claim 14 wherein said method further comprises:
disabling said first core in response to a drop in demand applied to said multi-core processor; and,

lowering a supply voltage and/or operating frequency of said second core in response to an additional drop in demand applied to said multi-core processor.

ABSTRACT

A method is described that entails operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency.

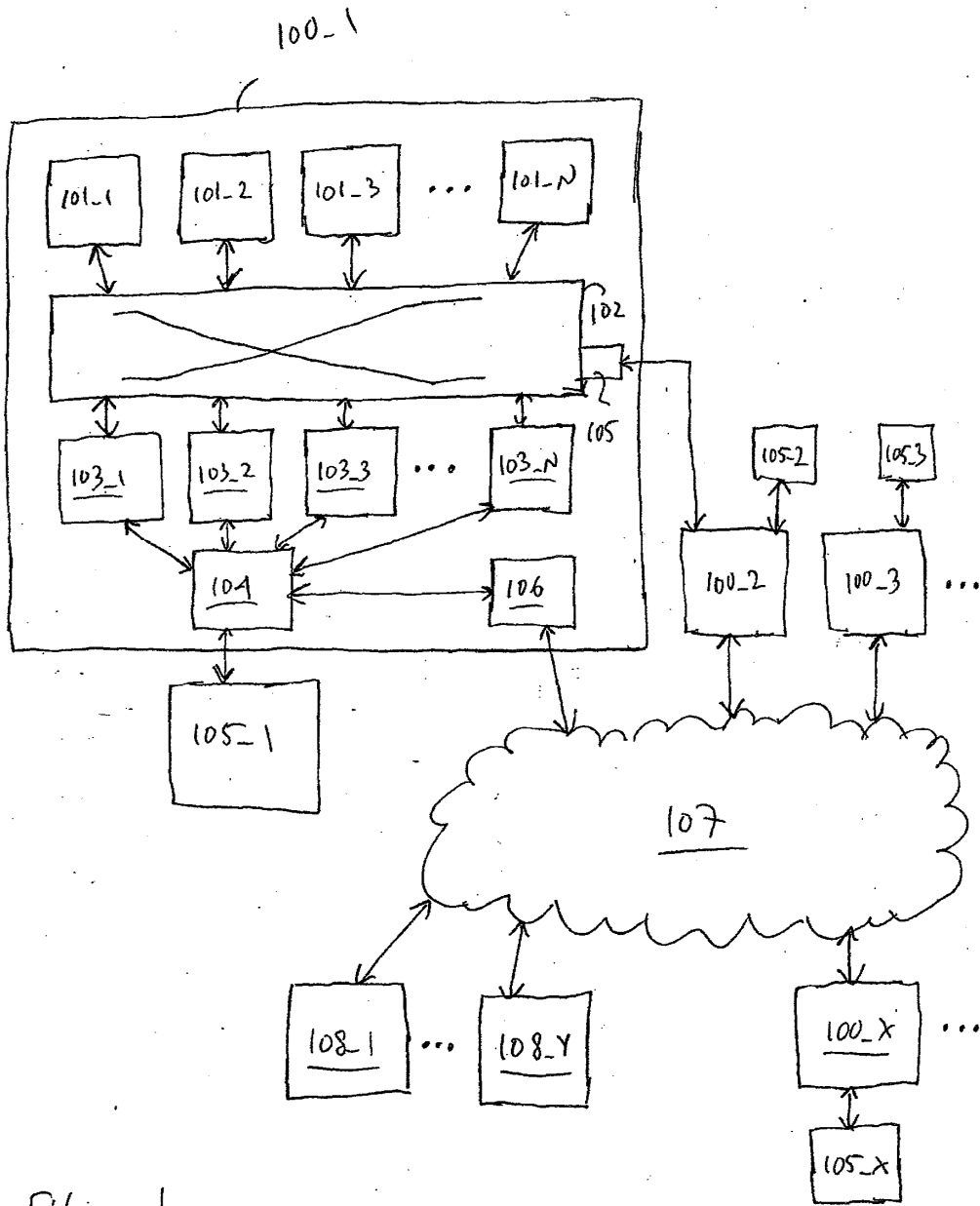


Fig. 1

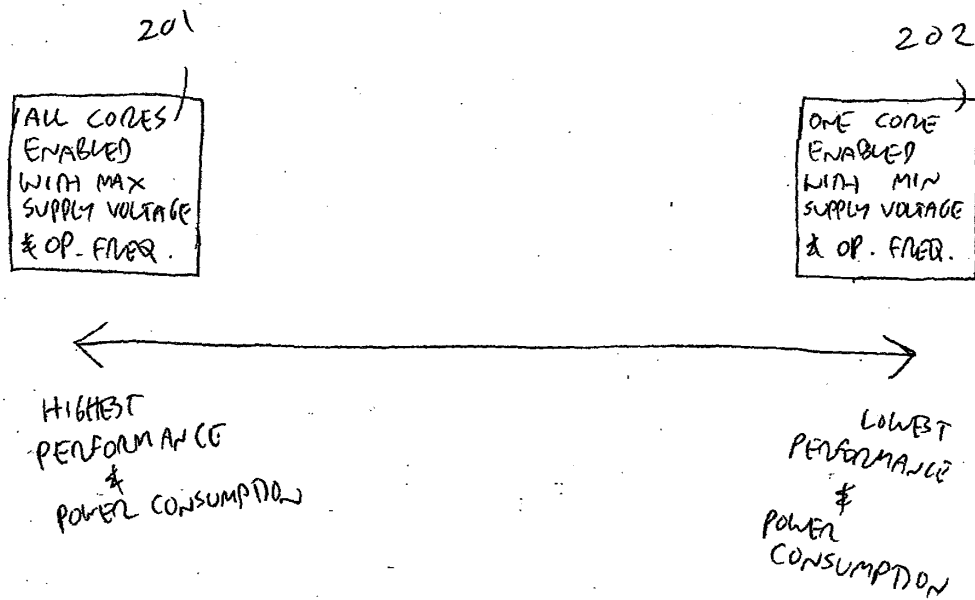


FIG. 2

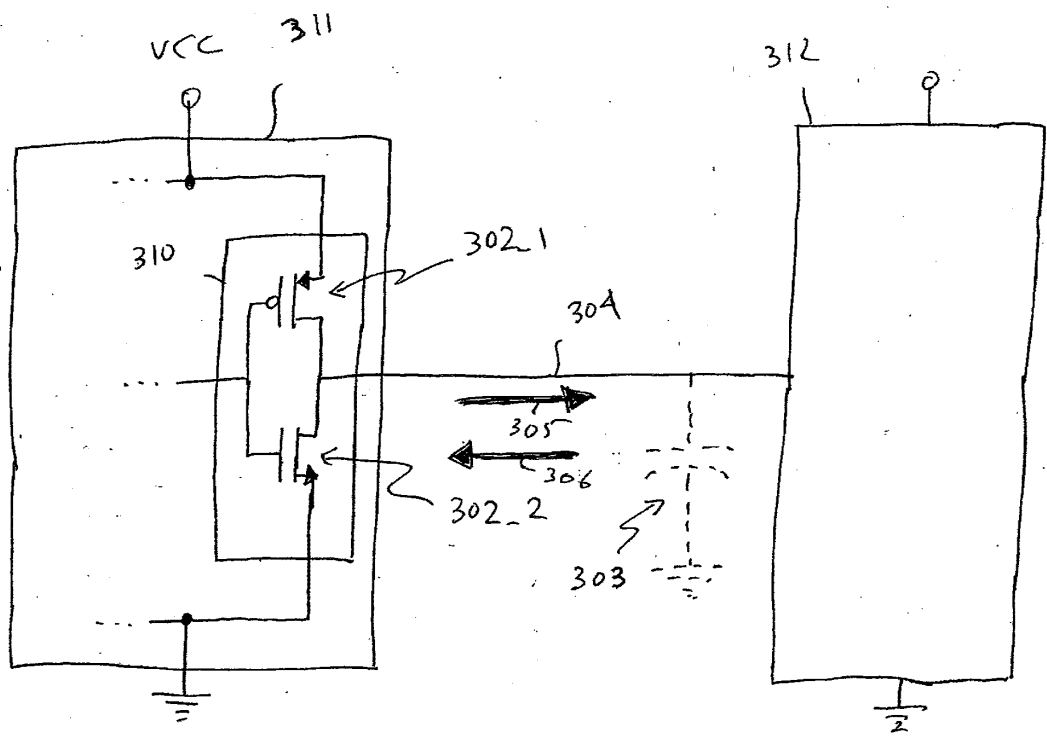


FIG. 3

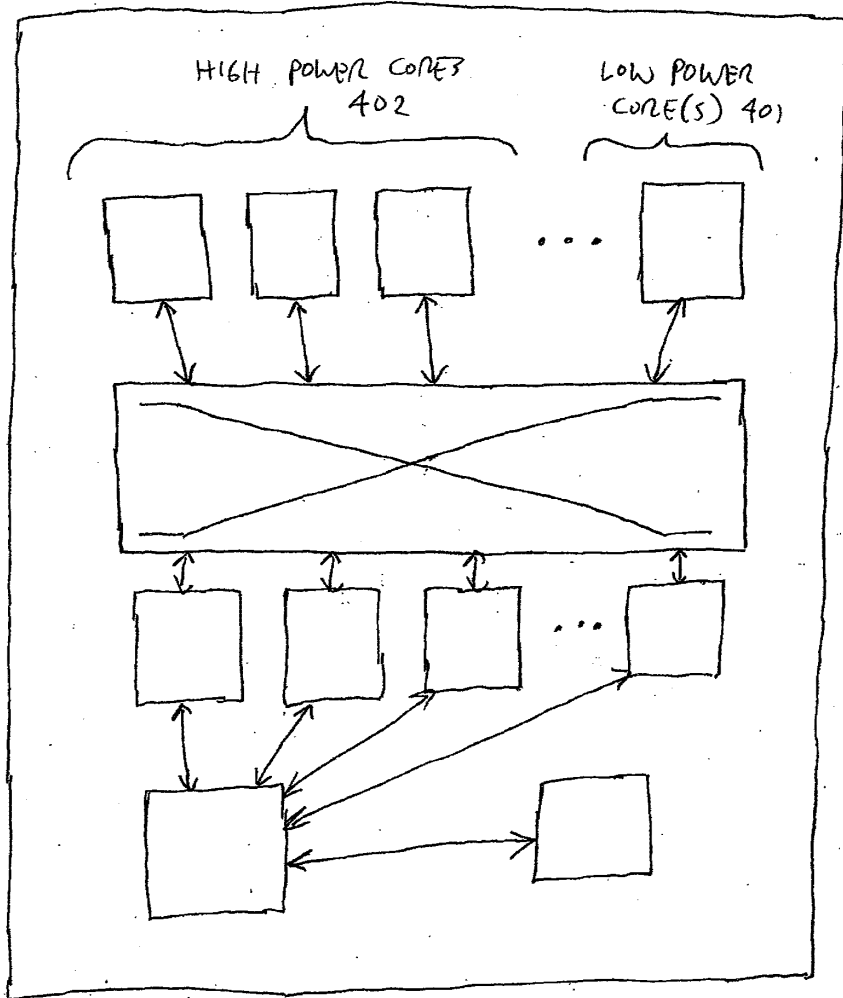


FIG. 4

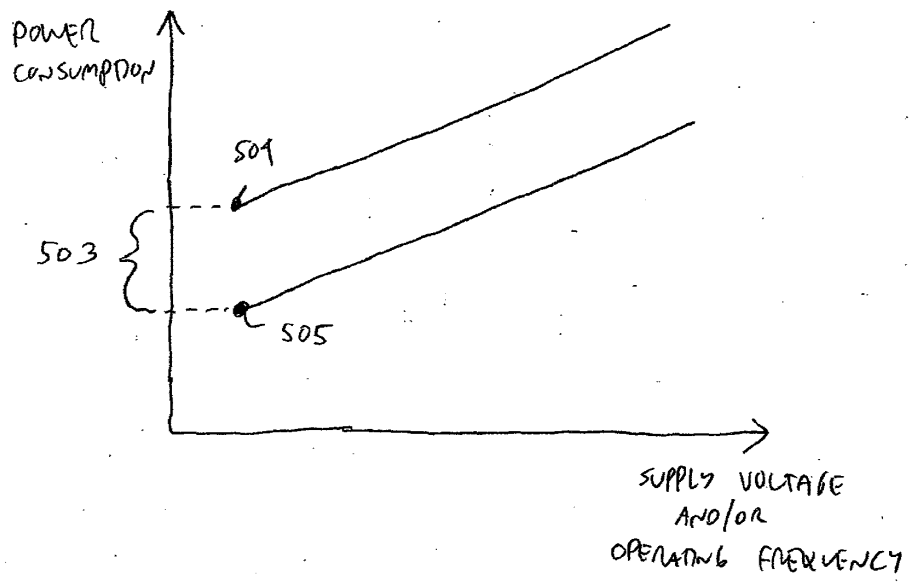


FIG. 5

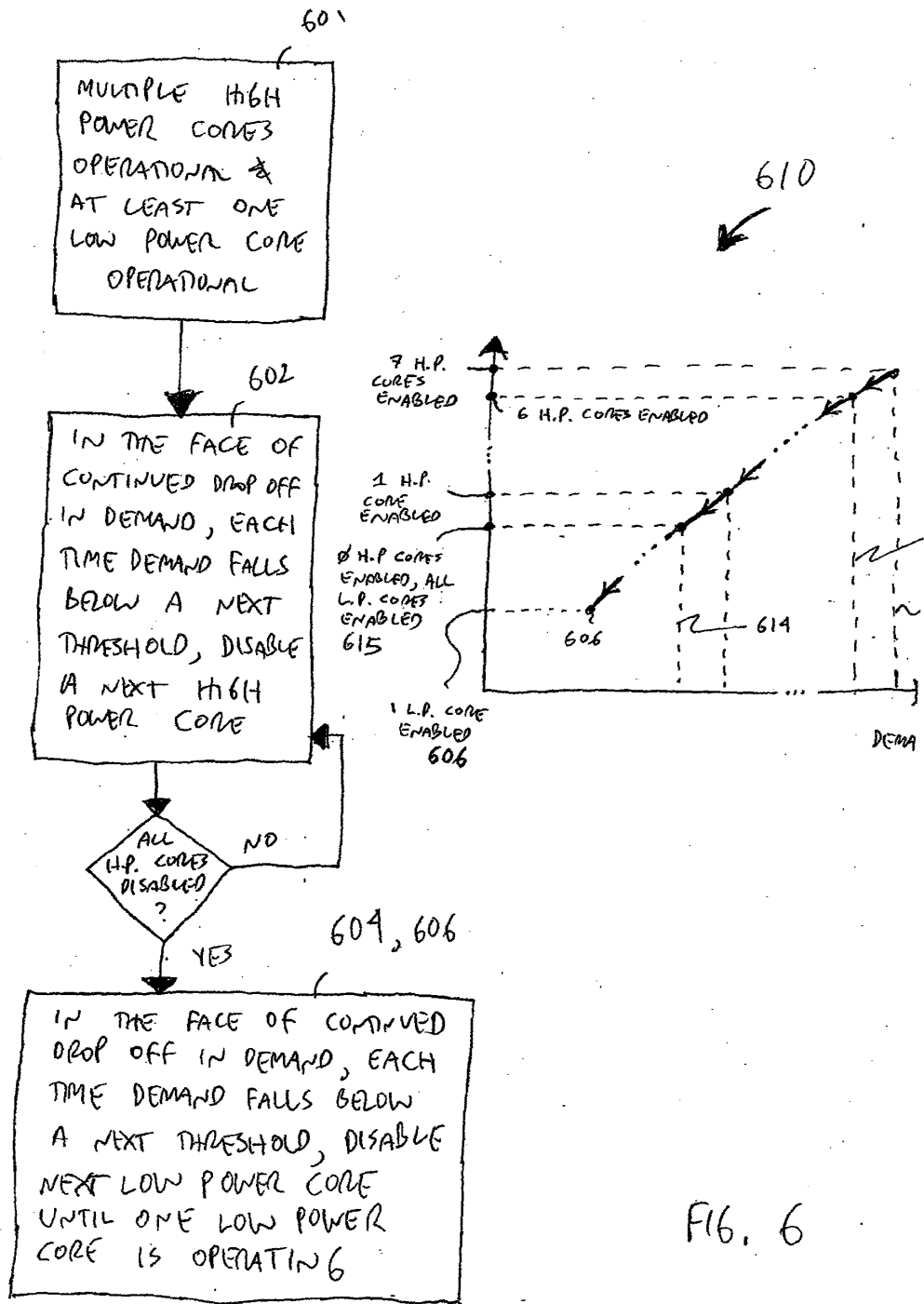


FIG. 6

701
SINGLE LOW
POWER CORE
IS OPERATIONAL

702
IN THE FACE OF
CONTINUED INCREASE
IN DEMAND, EACH
TIME DEMAND RISES
ABOVE A NEXT
THRESHOLD, ENABLE
A NEXT LOW
POWER CORE
UNTIL ALL ALL
LOW POWER CORES
ARE ENABLED

703
IN THE FACE OF
CONTINUED INCREASE
IN DEMAND, EACH
TIME DEMAND RISES
ABOVE A NEXT
THRESHOLD, ENABLE
A NEXT HIGH POWER
CORE UNTIL ALL
HIGH POWER CORES
ARE ENABLED

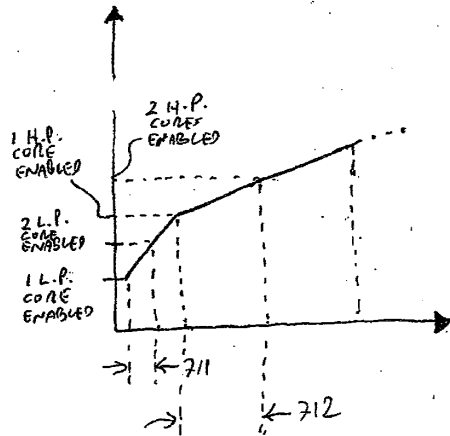


FIG. 7

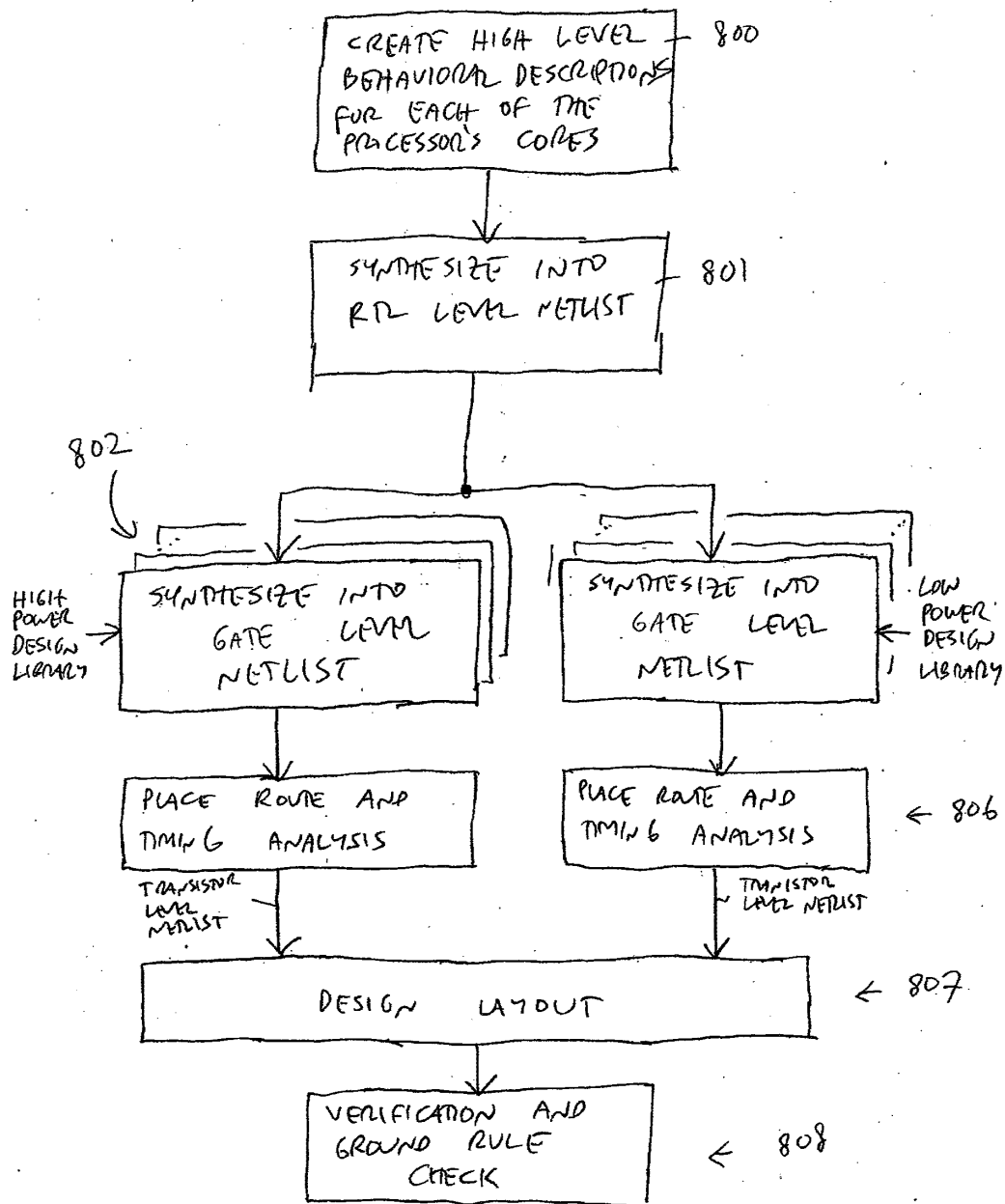


FIG. 8