AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22cv352	9/12/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
Daedalus Prime LLC	Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Taiwan Semiconductor Manufacturing Company Limited

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,775,833	7/8/2014	Daedalus Prime LLC
2	8,898,494	11/25/2014	Daedalus Prime LLC
3	10,049,080	8/14/2018	Daedalus Prime LLC
4	10,705,588	7/7/2020	Daedalus Prime LLC
5	9,831,306	11/28/2017	Daedalus Prime LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

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DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22cv352	9/12/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
Daedalus Prime LLC	Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Taiwan Semiconductor Manufacturing Company Limited

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,319,812	6/11/2019	Daedalus Prime LLC
2	10,700,178	6/30/2020	Daedalus Prime LLC
3	11,251,281	2/15/2022	Daedalus Prime LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	8/23/2022	District of Delaware

PLAINTIFF	DEFENDANT
Daedalus Prime LLC	Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC, Qualcomm Inc., Qualcomm Technologies, Inc., and Visteon Corporation

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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1	US 8,775,833 B2	7/8/2014	Daedalus Prime LLC
2	US 8,898,494 B2	11/25/2014	Daedalus Prime LLC
3	US 9,575,895 B2	2/21/2017	Daedalus Prime LLC
4	US 10,049,080 B2	8/14/2018	Daedalus Prime LLC
5	US 10,394,300 B2	8/27/2019	Daedalus Prime LLC
6	US 10,705,588 B2	7/7/2020	Daedalus Prime LLC

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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	8/23/2022	District of Delaware

PLAINTIFF	DEFENDANT
Daedalus Prime LLC	Arrow Electronics, Inc.; Avent, Inc.; Digi-Key Electronics; Future Electronics Inc.; Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc.; Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC; Mouser Electronics, Inc.; Newark; NXP Semiconductors N.V., NXP USA, Inc.; Rochester Electronics, LLC; and Visteon Corporation

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	8/23/2022	District of Delaware

PLAINTIFF	DEFENDANT
Daedalus Prime LLC	Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., MediaTek Inc., MediaTek USA Inc., Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC, and Visteon Corporation

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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6	US 10,705,588 B2	7/7/2020	Daedalus Prime LLC

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/431,527	08/14/2018	10049080	42P38886C	4542

131413 7590 07/25/2018

NDWE LLP/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

VARGHESE GEORGE, Folsom, CA;
Intel Corporation, Santa Clara, CA;
SANJEEV S. JAHAGIRDAR, Folsom, CA;
DEBORAH T. MARR, Portland, OR;

Doc Code: MFEE.C.AD

Document Description: Maintenance Fee Address Change

PTO/SB/47-EFS

FEE ADDRESS INDICATION FORM

Application Number	15431527	Art Unit	2183
Filing Date	13-Feb-2017	Examiner Name	ERIC COLEMAN
First Name Inventor	VARGHESE GEORGE	Attorney Doc. Number	42P38886C

INSTRUCTIONS: In order for the fee address identified on this form to be effective, the issue fee must have been paid for the application listed on this form. Only an address represented by a customer number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. For more information on customer numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

Please recognize as the Fee Address under the provisions of 37 CFR 1.363 the address associated with:

Customer Number:	000197 CPA GLOBAL LIMITED 2318 Mill Road 12th Floor ALEXANDRIA VA 22314 UNITED STATES 7037392234

Signature :

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application.

Signature	/Scott A. Simmons/	**Date**	07-11-2018
Name	Scott A. Simmons	**Registration Number**	60206

Electronic Patent Application Fee Transmittal

Application Number:	15431527
Filing Date:	13-Feb-2017
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Filer:	Scott Alan Simmons/Allison Prentice
Attorney Docket Number:	42P38886C

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	33154960
Application Number:	15431527
International Application Number:	
Confirmation Number:	4542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Customer Number:	131413
Filer:	Scott Alan Simmons/Allison Prentice
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886C
Receipt Date:	11-JUL-2018
Filing Date:	13-FEB-2017
Time Stamp:	23:33:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	071218INTEFSW23335400
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46318 d92b5ee5faa2d63b72ca0381582e9791b2375d50	no	2
Warnings:					
Information:					
2	Maintenance Fee Address Change	web85feeaddress.pdf	32539 c851a0490f05d1471fc02bc42c277d379f10b0d3	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31876 263b56b2de5e96d720cdeb33ab5800568169038b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	110733		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
15431527	13-Feb-2017	VARGHESE GEORGE	42P38886C	4542

TITLE OF INVENTION :

ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Regular Undiscounted	Utility under 35 USC 111(a)	2183	032000	ERIC COLEMAN

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$1000	$0	$1000	12-Jul-2018	$0

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
131413 NDWE LLP/Intel 99 Almaden Boulevard, Suite 710 San Jose CA 95113 UNITED STATES 408-675-0441 ndwe_docketing@cardinal-ip.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☒ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

○ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

◉ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☒ Issue Fee	☐ I authorize USPTO to apply my previously paid issue fee to the current fees due
☐ Publication Fee	☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number _____
☐ Advance Order - # of copies _____	☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency or credit any overpayment, to Deposit Account Number 506674 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. NICHOLSON DE VOS WEBSTER & ELLIOTT LLP
2.
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
INTEL CORPORATION	Santa Clara	CALIFORNIA	united states	corporation

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Scott A. Simmons/	**Date**	07-11-2018
Name	Scott A. Simmons	**Registration Number**	60206

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

131413 7590 04/12/2018

NDWE LLP/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

EXAMINER
COLEMAN, ERIC

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/12/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/431,527	02/13/2017	VARGHESE GEORGE	42P38886C	4542

TITLE OF INVENTION: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	07/12/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

131413 7590 04/12/2018
NDWE LLP/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/431,527	02/13/2017	VARGHESE GEORGE	42P38886C	4542

TITLE OF INVENTION: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	07/12/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
COLEMAN, ERIC	2183	712-032000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/431,527	02/13/2017	VARGHESE GEORGE	42P38886C	4542

131413 7590 04/12/2018

NDWE LLP/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/12/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/431,527	Applicant(s) GEORGE ET AL.	
	Examiner ERIC COLEMAN	Art Unit 2183	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 01/08/2018*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *20-43*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 03/02/2018
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ERIC COLEMAN/
Primary Examiner, Art Unit 2183

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	Art Unit
	ERIC COLEMAN	2183

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2017	03/29/2018							
	1	-	-							
	2	-	-							
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1	20	✓	=							
2	21	✓	=							
3	22	✓	=							
4	23	✓	=							
5	24	✓	=							
6	25	✓	=							
7	26	✓	=							
8	27	✓	=							
9	28	✓	=							
10	29	✓	=							
11	30	✓	=							
12	31	✓	=							
13	32	✓	=							
14	33	✓	=							
15	34	✓	=							
16	35	✓	=							
17	36	✓	=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	**Art Unit**
	ERIC COLEMAN	2183

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2017	03/29/2018							
18	37	✓	=							
19	38	✓	=							
20	39	✓	=							
21	40	✓	=							
22	41	✓	=							
23	42	✓	=							
24	43	✓	=							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	Art Unit
	ERIC COLEMAN	2183

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
712/32	08/30/2017	EC
G06F15/80 1/3206 1/3293 1/3296 13/4022	08/30/2017	EC
inventor name search	08/30/2017	EC
searched google scholar search terms high low small large power core processor turbo demand threshold thread active usage idle driver gate group cluster multiple core	08/30/2017	EC
updated above	03/29/2018	EC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
G06F	15/80 1/3206 1/3293 1/3296 13/4022	03/29/2018	EC
712	32	03/29/2018	EC

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15431527
Filing Date	2017-02-13
First Named Inventor	GEORGE; Varghese
Art Unit	2183
Examiner Name	COLEMAN, ERIC
Attorney Docket Number	42P38886C

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	None				

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	None				

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	None						

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15431527
	Filing Date	2017-02-13
	First Named Inventor	GEORGE; Varghese
	Art Unit	2183
	Examiner Name	COLEMAN, ERIC
	Attorney Docket Number	42P38886C

	1	Fourth Office Action from foreign counterpart China Patent Application No. 201280063860.9 (Atty. Docket No. 42P38886CN), mailed October 09, 2017, 10 pages.	☒
	2	Notice on Grant of Patent Right for Invention from foreign counterpart Chinese Patent Application No. 201280063860.9 (Atty. Docket No. 42P38886CN), mailed January 24, 2018, 4 pages.	☒

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/ERIC COLEMAN/	Date Considered	03/29/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	15431527
	Filing Date	2017-02-13
	First Named Inventor	GEORGE; Varghese
	Art Unit	2183
	Examiner Name	COLEMAN, ERIC
	Attorney Docket Number	42P38886C

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott A. Simmons/	Date (YYYY-MM-DD)	2018-03-02
Name/Print	Scott A. Simmons	Registration Number	60,206

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.C/

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	**Art Unit**
	ERIC COLEMAN	2183

CPC						
Symbol					**Type**	**Version**
G06F		15	/	80	F	2013-01-01
G06F		13	/	4022	I	2013-01-01
G06F		1	/	3206	I	2013-01-01
G06F		1	/	3293	I	2013-01-01
G06F		1	/	3296	I	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 24	
/ERIC COLEMAN/ Primary Examiner.Art Unit 2183 (Primary Examiner)	03/29/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	**Art Unit**
	ERIC COLEMAN	2183

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
712	32	G	0	6	F	15 / 80 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 24	
/ERIC COLEMAN/ Primary Examiner.Art Unit 2183 (Primary Examiner)	03/29/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	**Art Unit**
	ERIC COLEMAN	2183

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	14	33										
	2		18	15	34										
	3		19	16	35										
	4	1	20	17	36										
	5	2	21	18	37										
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	7	4	23	20	39										
	8	5	24	21	40										
	9	6	25	22	41										
	10	7	26	23	42										
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	15	12	31												
	16	13	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 24	
/ERIC COLEMAN/ Primary Examiner.Art Unit 2183 (Primary Examiner)	03/29/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2038	(high adj power or turbo) near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:40
L2	2852	(low adj power) near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:41
L3	386	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:41
L4	233	3 and threshold	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:41
L5	919	712/32.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:41
L7	19368	(G06F15/80 OR G06F1/3206 OR G06F1/3293 OR G06F1/3296 OR G06F13/4022).CPC.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:43
L8	82	4 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:43
L9	4	narrow$3 near3 logic adj gate adj (driver or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:44
L10	3	less adj power near3 logic adj gate near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:44
L11	2	less adj power near3 logic adj gate adj(driver or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:46
L12	469	less adj power near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:46
L13	414	less adj power near3 gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:47

L14	3	12 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:51
L15	4	1 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:51
L16	4	2 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:51
L17	2364	demand near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:51
L18	23	3 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:51
L19	12	18 and gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:51
L20	26	disabl$3 near3 power near3 manage	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:51
L21	15922	group$3 near cores	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:53
L22	977	((high or low) adj power) and 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:53
L23	541	22 and (demand or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:54
L24	236	23 and operating adj system	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:54
L25	9	23 and operating adj system with (demand or (threshold))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:54
L26	333	multi$3 adj core near3 operating adj system	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:56
L27	2	24 and 26	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/29 11:57

3/29/2018 11:58:37 AM

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BIB DATA SHEET

CONFIRMATION NO. 4542

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/431,527	02/13/2017	712	2183	42P38886C

APPLICANTS
Intel Corporation, Santa Clara, CA;

INVENTORS
VARGHESE GEORGE, Folsom, CA;
SANJEEV S. JAHAGIRDAR, Folsom, CA;
DEBORAH T. MARR, Portland, OR;

**** CONTINUING DATA ***************************
This application is a CON of 13/335,257 12/22/2011 PAT 9569278

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
02/22/2017

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ERIC COLEMAN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	8	19	3

ADDRESS
NDWE LLP/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113
UNITED STATES

TITLE
ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

FILING FEE RECEIVED		
2060	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15431527
Filing Date	2017-02-13
First Named Inventor	GEORGE; Varghese
Art Unit	2183
Examiner Name	COLEMAN, ERIC
Attorney Docket Number	42P38886C

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	None				

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	None						

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15431527
	Filing Date	2017-02-13
	First Named Inventor	GEORGE; Varghese
	Art Unit	2183
	Examiner Name	COLEMAN, ERIC
	Attorney Docket Number	42P38886C

	1	Fourth Office Action from foreign counterpart China Patent Application No. 201280063860.9 (Atty. Docket No. 42P38886CN), mailed October 09, 2017, 10 pages.	☒
	2	Notice on Grant of Patent Right for Invention from foreign counterpart Chinese Patent Application No. 201280063860.9 (Atty. Docket No. 42P38886CN), mailed January 24, 2018, 4 pages.	☒

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15431527
	Filing Date	2017-02-13
	First Named Inventor	GEORGE; Varghese
	Art Unit	2183
	Examiner Name	COLEMAN, ERIC
	Attorney Docket Number	42P38886C

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott A. Simmons/	Date (YYYY-MM-DD)	2018-03-02
Name/Print	Scott A. Simmons	Registration Number	60,206

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Electronic Patent Application Fee Transmittal

Application Number:	15431527
Filing Date:	13-Feb-2017
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Filer:	David F. Nicholson/Amarnath S
Attorney Docket Number:	42P38886C

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	31949093
Application Number:	15431527
International Application Number:	
Confirmation Number:	4542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Customer Number:	131413
Filer:	David F. Nicholson/Amarnath S
Filer Authorized By:	David F. Nicholson
Attorney Docket Number:	42P38886C
Receipt Date:	02-MAR-2018
Filing Date:	13-FEB-2017
Time Stamp:	19:56:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$240
RAM confirmation Number	030518INTEFSW19575700
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	42P38886C_IDS.pdf	1053839 4f29db3a12cfb9150253ddfdb0c593d6d78c1ab1	no	4
Warnings:					
Information:					
2	Non Patent Literature	FOURTHOA_CN201280063860_09OCT2017_10PGS_EFS.PDF	1155807 ea9f2e0e8ac284803417935804d8d18e2ce02a59	no	10
Warnings:					
Information:					
3	Non Patent Literature	NOA_CN201280063860_24JAN2018_4PGS_EFS.PDF	1207042 b4a53c9e0d69aff824bc93a4ed8a42d934734003	no	4
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30701 5ed541a584e011d731f16844ca5be661349c00e6	no	2
Warnings:					
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		Total Files Size (in bytes):	3447389		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/01 (08-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ■ United States application or PCT international application number 15/431,527 filed on February 13, 2017.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: VARGHESE GEORGE Date (Optional): 8/15/17

Signature: /Varghese George/

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ■ United States application or PCT international application number 15/431,527 filed on February 13, 2017.

The above-identified application was made or authorized to be made by me.

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LEGAL NAME OF INVENTOR

Inventor: SANJEEV S. JAHAGIRDAR Date (Optional): _____

Signature: SANJEEV S. JAHAGIRDAR

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 15/431,527

filed on February 13, 2017.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: DEBORAH T. MARR Date (Optional) : _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Varghese George	Examiner: Eric Coleman
Application No.: 15/431,527	Art Unit: 2183
Filed: February 13, 2017	Confirmation No.: 4542
For: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE	

Mail Stop Amendment
Commissioner for Patents
e-Filed via EFS-WEB

RESPONSE AND AMENDMENT

Sir:

In response to the Office action transmitted on September 6, 2017, Applicant respectfully requests the Examiner enter the following amendments and consider the following remarks.

CERTIFICATE OF EFS-Web

I hereby certify that this correspondence is being submitted electronically via EFS-Web on the date shown below to the United States Patent and Trademark Office.

Date of Deposit: January 8, 2018
Name of Person Mailing Correspondence: Allison Prentice
Signature: /Allison Prentice/

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application: What is claimed is:

1.-19. (Cancelled).

20. (Currently amended) A multi-core processor comprising:

a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

21. (Previously presented) The multi-core processor of claim 20, wherein the second plurality of cores comprise logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.

22. (Previously presented) The multi-core processor of claim 20, wherein the second plurality of cores comprise logic gates that consume less power than corresponding logic gates of the first plurality of cores.

23. (Previously presented) The multi-core processor of claim 20, wherein the second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.

24. (Previously presented) The multi-core processor of claim 20, wherein the power management hardware is to disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of

cores remains enabled, and lower an operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

25. (Previously presented) The multi-core processor of claim 24, wherein the power management hardware is to raise a supply voltage or an operating frequency of said one core in response to higher demand.

26. (Previously presented) The multi-core processor of claim 20, wherein the first plurality of cores are at a maximum operating frequency in the state.

27. (Previously presented) The multi-core processor of claim 20, wherein the power management hardware is to enable all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

28. (Previously presented) A method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

29. (Previously presented) The method of claim 28, wherein the operating of the second plurality of cores comprises driving logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.

30. (Previously presented) The method of claim 28, wherein the operating of the second plurality of cores comprises driving logic gates that consume less power than corresponding logic gates of the first plurality of cores.

31. (Previously presented) The method of claim 28, wherein the operating comprises operating the second plurality of cores at a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.

32. (Previously presented) The method of claim 28, further comprising disabling, with the power management hardware, an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lowering an operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

33. (Previously presented) The method of claim 32, further comprising raising, with the power management hardware, a supply voltage or an operating frequency of said one core in response to higher demand, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

34. (Previously presented) The method of claim 28, wherein the operating comprises operating the first plurality of cores at a maximum operating frequency in the state.

35. (Previously presented) The method of claim 28, further comprising enabling, with the power management hardware, all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

36. (Previously presented) A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

37. (Previously presented) The non-transitory machine readable medium of claim 36, wherein the operating of the second plurality of cores comprises driving logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.

38. (Previously presented) The non-transitory machine readable medium of claim 36, wherein the operating of the second plurality of cores comprises driving logic gates that consume less power than corresponding logic gates of the first plurality of cores.

39. (Previously presented) The non-transitory machine readable medium of claim 36, wherein the operating comprises operating the second plurality of cores at a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.

40. (Previously presented) The non-transitory machine readable medium of claim 36, further comprising disabling, with the power management hardware, an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lowering an operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

41. (Previously presented) The non-transitory machine readable medium of claim 40, further comprising raising, with the power management hardware, a supply voltage or an operating frequency of said one core in response to higher demand, wherein an operating system

executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

42. (Previously presented) The non-transitory machine readable medium of claim 36, wherein the operating comprises operating the first plurality of cores at a maximum operating frequency in the state.

43. (Previously presented) The non-transitory machine readable medium of claim 36, further comprising enabling, with the power management hardware, all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

REMARKS

The enclosed is responsive to the Examiner's Office action transmitted on September 6, 2017. Claims 20–36 are pending, with claims 20, 28, and 36 being independent. Claim 20 has been amended. No new subject matter has been added. Applicant respectfully requests reconsideration of the present application and the allowance of all claims now presented.

35 U.S.C. §§ 102 & 103 Rejections

Claims 20, 23-28, 31-36, and 39-43 were rejected under pre-AIA 35 U.S.C. 102(b) as being allegedly anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as being allegedly obvious over Grochowski, U.S. Publication No. 2006/0095807 (hereinafter "Grochowski"). Claims 21-22, 29-30, 37, and 38 were rejected under pre-AIA 35 U.S.C. 103(a) as being allegedly unpatentable over Grochowski as applied to claims 20, 28, and 36, above, and further in view of Sutardja, U.S. Publication No. 2008/0263324 (hereinafter "Sutardja").

Prima Facie Anticipation

The Office action has not made a prima facie case of anticipation for any of the claims. MPEP § 2131 states that "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)" (emphasis added). "'The identical invention must be shown in as complete detail as is contained in the ... claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)" (emphasis added). "Every element of the claimed invention must be literally present, arranged as in the claim." *Id.* (emphasis added).

The Office action failed to show how "each and every element" of the claims is disclosed by the cited portions of Grochowski. The Office action merely cut and pasted the claims with brief citations at the ends of certain lines. No reasoning is provided explaining why the citations are believed to disclose each and every element of the claims, nor are the citations matched to each and every element of the claims.

As such, Applicant cannot reasonably determine which elements of the claims are believed to correspond with the citations of Grochowski in this Office action. For example, the Office action on pages 2-3 does not describe what elements of Applicant's claims are alleged to have been anticipated by the citations. Thus, Applicant is not put on notice as to the rationale behind these rejections and cannot adequately determine whether such basis is proper. Applicant respectfully submits that these rejections are improper for at least these reasons.

Prima Facie Obviousness

The Office action has not made a prima facie case of obviousness for the claims. MPEP § 2143 states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit" (emphasis added). "(T)here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006); 441 F.3d 977, 988.

The Office action failed to clearly articulate how "each and every element" of the claims is disclosed by the cited sections of the references. For example, as to Applicant's independent claims 20, 28, and 36, pages 3-4 of the Office action allege that:

> In the alternative 103 rejection, Grochowski taught the situation where all B cores are turned off while A cores are turned on, and the separate situation where one or more B cores are left on when the other B cores were turned off (e.g., see paragraph 0034); as understood the alternatives would have been selected depending on the situation such as how many cores are turned and how much the possible discontinuity at the point of switching would affect the throughput. Consequently when the number of cores was such that the discontinuity at the point of switching was minimal one of ordinary skill would have been motivated to turn off all of the B cores to reduce the use of power.
>
> Due to the similarities between claims 20 and 28 and 36; claims 28 and 36 are rejected for the same reasons as claim 20.

The Office action (e.g., the above quotation) does not clearly articulate how or why the Applicant's claims would have been obvious in view of the cited portions of Grochowski, and does not have any explicit analysis for this alleged obviousness. Thus, Applicant is not put on notice as to the rationale behind the rejections and cannot adequately determine whether such basis is proper. Applicant respectfully submits that the rejections are improper for at least these reasons.

§§102 and 103 Rejections

Merely in the interest of compact prosecution, the Applicant notes that the cited portions of Grochowski do not appear to teach or suggest the Applicant's claims. For example, the cited portions of Grochowski do not appear to teach or suggest:

> 20. A multi-core processor comprising:
> a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and
> **power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand**. (Emphasis added.)

as in Applicant's independent claim 20, or:

> 28. A method comprising:
> operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and
> **disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand**. (Emphasis added.)

as in Applicant's independent claim 28, or:

36. A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand. (Emphasis added.)

as in Applicant's independent claim 36.

Because the Applicant has demonstrated the patentability of all pending independent claims, the Applicant respectfully submits that all pending claims are allowable. The Applicant's silence with respect to the dependent claims should not be construed as an admission by the Applicant that the Applicant is complicit with the Examiner's rejection of these claims. Because the Applicant has demonstrated the patentability of the independent claims, the Applicant need not substantively address the theories of rejection applied to the dependent claims.

Double Patenting

Claims 20-43 were rejected on the grounds of non-statutory double patenting as being allegedly unpatentable over claims 1-20 of U.S. Patent No. 9,569,278. As none of the Applicant's claims herein are indicated as allowed, Applicant submits that a terminal disclaimer would be premature. If the Office maintains this rejection after there is an indication of allowance, the Applicant is willing to address the double patenting rejection at that time.

In light of the comments above, Applicant respectfully requests the allowance of all claims.

CONCLUSION

Applicant respectfully submits that all rejections have been overcome and that all pending claims are in condition for allowance. If the Examiner believes an additional telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Scott A. Simmons at (408) 675-0441. Authorization is hereby given to charge our Deposit Account No. 506674 for any charges that may be due.

Respectfully submitted,
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP

Date: January 8, 2018

/Scott A. Simmons/
Scott A. Simmons
Reg. No.: 60,206

99 Almaden Blvd., Ste. 710
San Jose, Ca 95113
408-675-0441

Electronic Patent Application Fee Transmittal

Application Number:	15431527
Filing Date:	13-Feb-2017
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Filer:	Scott Alan Simmons/Allison Prentice
Attorney Docket Number:	42P38886C

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**200**

Electronic Acknowledgement Receipt	
EFS ID:	31440365
Application Number:	15431527
International Application Number:	
Confirmation Number:	4542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Customer Number:	131413
Filer:	Scott Alan Simmons/Allison Prentice
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886C
Receipt Date:	08-JAN-2018
Filing Date:	13-FEB-2017
Time Stamp:	18:56:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$200
RAM confirmation Number	010918INTEFSW18564700
Deposit Account	506674
Authorized User	Allison Madsen
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	P38886C_Decs_signed_ALL.pdf	2546354 0fe1d164f48c6e2becd8c11430308c923598 89d0	no	3
Warnings:					
Information:					
2		P38886C_ROA_01_08_18.pdf	91072 1a506558104d87605cebafe5a36d6078ccac d535	yes	11

Multipart Description/PDF files in .zip description

Document Description	Start	End
Applicant Arguments/Remarks Made in an Amendment	1	1
Claims	2	6
Applicant Arguments/Remarks Made in an Amendment	7	11

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30788 c670fd41e75d4072e612cd5f7e22449625f8 a264	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2668214		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/431,527	Filing Date 02/13/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 01/08/2018

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 24	Minus	** 24	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
ADAMA JONES

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/431,527	02/13/2017	VARGHESE GEORGE	42P38886C	4542

131413 7590 09/06/2017

NDWE LLP/ Intel
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
09/06/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ndwe_docketing@cardinal-ip.com
inteldocs_docketing@cpaglobal.com
patent@ndwe.com

Office Action Summary	Application No. 15/431,527	Applicant(s) GEORGE ET AL.	
	Examiner ERIC COLEMAN	Art Unit 2183	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/17/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *20-43* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *20-43* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *02/13/2017* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *08/10/17;02/13/17*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim(s) 20, 23-28, 31-36, and 39-43 is/are rejected under pre-AIA 35 U.S.C. 102 (b) as anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as obvious over Grochowski (patent application publication No. 2006/0095807).

1.-19. (Cancelled).

Grochowski taught the invention substantially as claimed (as to claim 20) including a multi-core processor comprising:

a first plurality of cores(B cores) and a second plurality of cores(A cores) that support/execute the same instruction set ,(e.g., see paragraph 0026) wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores(e.g., see paragraph 0031); and

power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand (e.g., see paragraph 0034).

In the alternative 103 rejection, Grochowski taught the situation where all B cores are turned off while A cores are turned on, and the separate situation where one or more B cores are left on when the other B cores were turned off (e.g., see paragraph 0034); as understood the alternatives would have been selected depending on the situation such as how many cores are turned and how much the possible discontinuity at the point of switching would affect the throughput. Consequently when the number of cores was such that the discontinuity at the point of switching was minimal one of ordinary skill would have been motivated to turn off all of the B cores to reduce the use of power.

Due to the similarities between claims 20 and 28 and 36; claims 28 and 36 are rejected for the same reasons as claim 20.

As to claims 23,31,39 Grochowski taught changing frequencies of cores (e.g., see paragraph 0078 but did not expressly detail The multi-core processor of claim 20,

wherein the second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores. Sutardja however taught higher performance core operating at a higher maximum frequency than a lower performance core (e.g., see paragraph 0013)[as applied to the Grochowski teachings the plurality of higher performance processors would have had a higher maximum operating frequency than the highest frequency of the plurality of lower performance processors].

As to claims 24, 32, 40 Grochowski taught The multi-core processor of claim 20, wherein the power management hardware is to disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lower an operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold (e.g., see paragraph 0034,0036).

As to claims 25,33,41 Grochowski taught The multi-core processor of claim 24, wherein the power management hardware is to raise a supply voltage or an operating frequency of said one core in response to higher demand (e.g., see paragraphs 0025 0036-0037) [note in the case in table 1 after paragraph 0036 when the number for running thread is increased from zero to one to two, only A cores are employed and Grochowski taught throttle module increasing the voltage and clock frequency when

parallelism increased in paragraph 0025]. Grochowski also taught wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand (e.g., see paragraph 0034).

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As to claims 26, 34,42 Grochowski taught The multi-core processor of claim 20, wherein the first plurality of cores are at a maximum operating frequency in the state (e.g., see paragraphs 0070-0072).

As to claims 27,35,43 Grochowski taught The multi-core processor of claim 20, wherein the power management hardware is to enable all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand (e.g., see paragraphs 36-37)[the increase of running threads from zero to twelve the number of A cores is maximized without disabling any B cores).

Claims 21-22,29-30,37,38 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Grochowski as applied to claims 20,28,36, above, and further in view of Sutardja (patent application publication No. 2008/0263324).

As to claims 21, 29, 37 Sutardja taught The multi-core processor of claim 20, wherein the second plurality of cores comprise logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores (e.g., see paragraph 0230) [As to driving these gates the characteristics specified in paragraph 0230 of Sutardja are produced when the gates are driven therefore the gates are understood as driven].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Grochowski and Sutardja. Both references were directed toward the problems of operating plural processors with one or more processor capable of a higher performance than the other one or more processors in a data processor. One of ordinary skill would have been motivated to incorporate the Sutardja teachings of providing the second lower performance transistors with narrower gate transistors that consume less power at least to reduce system size and conserve power. Also the addition of the Sutardja teachings would have yielded predictable results at least because both references directed toward data processing using programmable processors.

As to claims 22, 30, 38 Sutardja taught The multi-core processor of claim 20, wherein the second plurality of cores comprise logic gates that consume less power than corresponding logic gates of the first plurality of cores (e.g., see paragraphs 0230,0027) [As to driving these gates, the characteristics specified in paragraph 0230 of

Sutardja are produced when the gates are driven therefore the gates are understood as driven].

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) -

706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

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Claims 20-43 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9,569,278. Although the claims at issue are not identical, they are not patentably distinct from each other because the side by side showing a representative claims of the instant application and the patent below show that both are directed to common subject matter.

Instant application (SN 15/431,527)	Patent No. 9,569,278
1.-19. (Cancelled). 20. A multi-core processor comprising: a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second	1. A multi-core processor comprising: a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second

plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.	plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and power management hardware to, from an initial state where the first plurality of cores and the second plurality of cores are enabled, disable an additional core of the first plurality of cores for each continued drop in demand below a next lower threshold without disabling any of the second plurality of cores until the first plurality of cores is disabled, disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lower at least one of an operating frequency and a supply voltage of the one core of the second plurality of cores as demand drops below a next lower

	threshold.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

HA (patent application publication No. 2006/0279152) disclosed system for implementing a hybrid mode for a multi-core processor (e.g., see abstract).

Memon (patent application publication No. 2010/0131781) disclosed reducing network latency during low power operation (e.g., see abstract).

Flachs (patent application publication No. 2011/0252260) disclosed reducing power requirements of a multi-core processor (e.g., see abstract).

Talwar (patent application publication No. 2009/0271646) disclosed power management using clustering in a multicore system (e.g., see abstract).

Kruglick (patent application No. 2011/0093733) disclosed power channel monitor for a multi-core processor (e.g., see abstract).

Regini (patent application publication No. 2012/0260258) disclosed system for dynamically controlling power to multiple cores in a multicore processor of a portable computing device (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC COLEMAN whose telephone number is (571)272-4163. The examiner can normally be reached on Monday-Friday.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aimee Li can be reached on (571) 272-4169. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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EC

/ERIC COLEMAN/
Primary Examiner, Art Unit 2183

Notice of References Cited	Application/Control No. 15/431,527	Applicant(s)/Patent Under Reexamination GEORGE ET AL.	
	Examiner ERIC COLEMAN	Art Unit 2183	Page 1 of 1

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*	B	US-2008/0263324 A1	10-2008	Sutardja; Sehat	G06F1/3203	712/43
*	C	US-2006/0279152 A1	12-2006	HA; Min Hoon	G06F1/3203	310/114
*	D	US-2010/0131781 A1	05-2010	Memon; Mazhar I.	G06F1/3209	713/310
*	E	US-2011/0252260 A1	10-2011	Flachs; Brian K.	G06F1/3287	713/324
*	F	US-2009/0271646 A1	10-2009	Talwar; Vanish	G06F1/3203	713/322
*	G	US-2011/0093733 A1	04-2011	Kruglick; Ezekiel John Joseph	G06F1/3203	713/340
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15431527
Filing Date	2017-02-13
First Named Inventor	GEORGE; Varghese
Art Unit	2183
Examiner Name	COLEMAN, ERIC
Attorney Docket Number	42P38886C

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Application Number	15431527
Filing Date	2017-02-13
First Named Inventor	GEORGE; Varghese
Art Unit	2183
Examiner Name	COLEMAN, ERIC
Attorney Docket Number	42P38886C

	1	Final Office Action from U.S. Patent Application No. 13/335,257 (Atty. Docket No. 42P38886), mailed May 05, 2015, 13 pages.	
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	Filing Date	2017-02-13
	First Named Inventor	GEORGE; Varghese
	Art Unit	2183
	Examiner Name	COLEMAN, ERIC
	Attorney Docket Number	42P38886C

CERTIFICATION STATEMENT

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott A. Simmons/	Date (YYYY-MM-DD)	2017-08-10
Name/Print	Scott A. Simmons	Registration Number	60,206

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Varghese George
	Art Unit	
	Examiner Name	
	Attorney Docket Number	42P38886C

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	1	7992020	B1	2011-08-02	Tuan Tim et al.	
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	2	20080127192	A1	2008-05-29	Capps et al.	
	3	20090271646	A1	2009-10-29	Talwar et al.	
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	Filing Date	
	First Named Inventor	Varghese George
	Art Unit	
	Examiner Name	
	Attorney Docket Number	42P38886C

	6	20100131781	A1	2010-05-27	Memon et al.	
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	14	20100083011	A1	2010-04-01	Onouchi Masafumi et al.	
	15	20100058086	A1	2010-03-04	Lee Wan Yeon	

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	1	Copy of Notice of Allowance from TW counterpart Application No. 101147200, (Atty. Docket No. 42P38886TW), mailed September 29, 2014, 1 page.	
	2	Aruj, Ori. "Evolution: 20 years of switching Fabric", September 2008. EE Times. Retrieved from http://www.eetimes.com/document.asp?doc_id=1272140.	
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	4	PCT Written Opinion of the International Searching Authority for PCT Counterpart Application No. PCT/US2012/068274, 6 pgs., (February 22, 2013).	
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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott A. Simmons/	Date (YYYY-MM-DD)	2017-02-13
Name/Print	Scott A. Simmons	Registration Number	60,206

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.C/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1923	(high adj power or turbo)near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 10:12
L2	2581	(low adj power)near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 10:12
L3	340	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 10:12
L4	202	3 and threshold	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 10:17
L5	898	712/32.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:13
L6	17464	(G06F15/80 OR G06F1/3206 OR G06F1/3293 OR G06F1/3296 OR G06F13/4022).CPC.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:15
L7	70	4 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:15
L8	4	narrow$3 near3 logic adj gate adj (driver or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:15
L9	3	less adj power near3 logic adj gate near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:19
L10	2	less adj power near3 group near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:21
L11	440	less adj power near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:22
L12	406	less adj power near3 gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:22

L13	3	11 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:22
L14	4	1 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:23
L15	4	2 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:23
L16	2252	demand near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:23
L17	23	3 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:24
L18	12	17 and gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:24
L19	7	disabl$3 near power near3 manage	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:26
L20	14847	group$3 near cores	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:27
L21	895	((high or low) adj power) and 20	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:28
L22	493	21 and (demand or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:28
L23	216	22 and operating adj system	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:29
L24	9	22 and operating adj system with (demand or (threshold))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/08/29 11:30

8/29/2017 11:32:08 AM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	Art Unit
	ERIC COLEMAN	2183

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
712/32	08/30/2017	EC
G06F15/80 1/3206 1/3293 1/3296 13/4022	08/30/2017	EC
inventor name search	08/30/2017	EC
searched google scholar search terms high low small large power core processor turbo demand threshold thread active usage idle driver gate group cluster multiple core	08/30/2017	EC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/ERIC COLEMAN/ Primary Examiner, Art Unit 2183

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15431527	GEORGE ET AL.
	Examiner	Art Unit
	ERIC COLEMAN	2183

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2017								
	1	-								
	2	-								
	3	-								
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	32	✓								
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	34	✓								
	35	✓								
	36	✓								

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CLAIM		DATE								
Final	Original	08/30/2017								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								
	43	✓								

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	15431527
	Filing Date	2017-02-13
	First Named Inventor	GEORGE; Varghese
	Art Unit	2183
	Examiner Name	COLEMAN, ERIC
	Attorney Docket Number	42P38886C

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	None				

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	101076770	CN	A	2007-11-21	INTEL CORP [US]		X

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	1	Final Office Action from U.S. Patent Application No. 13/335,257 (Atty. Docket No. 42P38886), mailed May 05, 2015, 13 pages.	
	2	First Office Action from foreign counterpart China Patent Application No. 201280063860 (Atty. Docket No. 42P38886CN), mailed December 21, 2015, 19 pages.	☒
	3	Non-Final Office Action from U.S. Patent Application No. 13/335,257 (Atty. Docket No. 42P38886), mailed January 12, 2015, 15 pages.	☐
	4	Non-Final Office Action from U.S. Patent Application No. 13/335,257 (Atty. Docket No. 42P38886) mailed May 26, 2016, 10 pages.	☐
	5	Notice of Allowance from U.S. Patent Application No. 13/335,257 (Atty. Docket No. 42P38886) mailed September 27, 2016, 6 pages.	☐
	6	Second Office Action from foreign counterpart China Patent Application No. 201280063860 (Atty. Docket No. 42P38886CN), mailed July 21, 2016, 12 pages.	☒
	7	Third Office Action from foreign counterpart China Patent Application No. 201280063860 (Atty. Docket No. 42P38886CN), mailed December 15, 2016, 31 pages.	☒

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Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Espacenet

Bibliographic data: CN101076770 (A) — 2007-11-21

Method and apparatus for varying energy per instruction according to the amount of available parallelism

Inventor(s): MURALI GROCHOWSKI EDWARD SHEN [US] ± (GROCHOWSKI EDWARD,SHEN JOHN,WANG HONG,ORENSTEIN DORON,SHEAFFER GAD,RONEN RONNY,ANNAVARAM MURALI, ; GROCHOWSKI EDWARD, ; SHEN JOHN, ; WANG HONG, ; ORENSTEIN DORON, ; SHEAFFER GAD, ; RONEN RONNY, ; ANNAVARAM MURALI)

Applicant(s): INTEL CORP [US] ± (INTEL CORP)

Classification: **- international:** *G06F1/20*
- cooperative: G06F1/206; G06F1/3203; G06F1/329; G06F9/3851; G06F9/3885; G06F9/3891; G06F9/3897; Y02B60/1275; Y02B60/144; Y02B60/32

Application number: CN2005832835 20050928

Priority number(s): US20040952627 20040928

Also published as: CN100565426 (C) WO2006037119 (A2) WO2006037119 (A3) US2006095807 (A1) US7437581 (B2) more

Abstract of CN101076770 (A)

A method and apparatus for changing the configuration of a multi-core processor is disclosed. In one embodiment, a throttle module (or throttle logic) may determine the amount of parallelism present in the currently-executing program, and change the execution of the threads of that program on the various cores. If the amount of parallelism is high, then the processor may be configured to run a larger amount of threads on cores configured to consume less power. If the amount of parallelism is low, then the processor may be configured to run a smaller amount of threads on cores configured for greater scalar performance.

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
G06F 1/20 (2006.01)

[12] 发明专利申请公布说明书

[21] 申请号 200580032835.4

[43] 公开日 2007 年 11 月 21 日

[11] 公开号 CN 101076770A

[22] 申请日 2005.9.28
[21] 申请号 200580032835.4
[30] 优先权
[32] 2004. 9.28 [33] US [31] 10/952,627
[86] 国际申请 PCT/US2005/035145 2005.9.28
[87] 国际公布 WO2006/037119 英 2006.4.6
[85] 进入国家阶段日期 2007.3.28
[71] 申请人 英特尔公司
地址 美国加利福尼亚州
[72] 发明人 E·格罗乔夫斯基 J·沈 H·王
D·奥伦斯坦 G·希菲尔
R·罗宁 M·安纳瓦拉姆

[74] 专利代理机构 中国专利代理(香港)有限公司
代理人 刘 红 梁 永

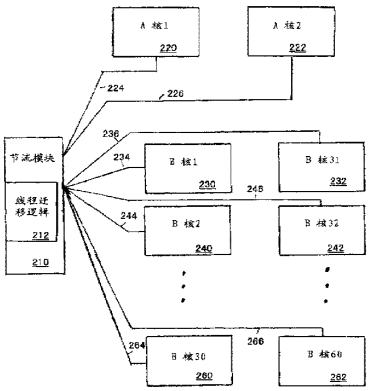
权利要求书 5 页 说明书 21 页 附图 11 页

[54] 发明名称

根据可用并行数目改变每条指令能量的方法和设备

[57] 摘要

本发明揭示了用于改变多核处理器配置的方法和设备。在一个实施例中，节流模块(或者节流逻辑)可确定当前执行程序中存在的并行数量，并改变各种核上该程序的线程的执行。如果并行数量大，则处理器可以配置成在配置成消耗更低功率的核上运行更大数量的线程。如果并行数量小，则处理器可以配置成在配置成用于更高标量性能的核上运行更小数量的线程。



1. 一种处理器，包括:

监测逻辑，监测所述处理器核属性的数值;

转换逻辑，响应于所述核的所述属性确定所述处理器功耗的测量;以及

控制逻辑，响应于所述功耗的测量调整所述处理器的每条指令能量的度量。

2. 权利要求 1 的处理器，其中所述核的所述属性为核运行状态。

3. 权利要求 2 的处理器，其中通过将所述核运行状态乘以当所述核处于所述核运行状态时每个时钟耗费的能量数量，确定所述功耗的测量。

4. 权利要求 1 的处理器，其中所述核的所述属性为每个时钟退回的指令的数目。

5. 权利要求 4 的处理器，其中通过将所述每个时钟退回的指令的数目乘以每个时钟每条指令耗费的能量数量，确定所述功耗的测量。

6. 权利要求 1 的处理器，其中所述核的所述属性为所述核的功能块的活动状态。

7. 权利要求 6 的处理器，其中通过将所述功能块的所述活动状态乘以当所述功能块处于所述活动状态时每个时钟耗费的能量数量，确定所述功耗的测量。

8. 权利要求 1 的处理器，其中所述属性为核源电流。

9. 权利要求 8 的处理器，其中所述功耗的测量包括所述核源电流。

10. 权利要求 1 的处理器，其中所述控制逻辑响应于所述功耗的测量而调整所述处理器的工作电压和工作频率。

11. 权利要求 1 的处理器，其中所述控制逻辑响应于所述功耗的测量而在所述处理器的大核和小核之间迁移程序的线程。

12. 权利要求 1 的处理器，其中所述控制逻辑响应于所述功耗的测量而接通所述处理器的所述核内的可选性能电路。

13. 权利要求 1 的处理器，其中所述控制逻辑响应于所述功耗的测量而接通所述处理器的所述核内的可选预测电路。

14. 权利要求 1 的处理器，还包括差值逻辑以计算所述功耗的测量和期望功耗之间的差值。

15. 权利要求 14 的处理器，还包括积分电路以确定所述功耗的测量和期望功耗之间的所述差值的时间积分。

16. 权利要求 14 的处理器，还包括采样电路以根据采样方法将所述功耗的测量供给到所述控制逻辑。

17. 权利要求 1 的处理器，还包括时钟节流电路以允许快反馈控制。

18. 一种处理器，包括:

第一多个第一类型的核;

第二多个第二类型的核；以及

模块，将线程分配到所述第一多个的所述第一类型核或者所述第二多个的所述第二类型核之一。

19. 权利要求 18 的处理器，其中所述模块根据功率预算分配所述线程。

20. 权利要求 18 的处理器，其中所述模块根据分配表分配所述线程。

21. 权利要求 18 的处理器，其中所述模块包括线程迁移逻辑，将新线程分配到所述第二多个核之一并将已有线程从所述第一多个核之一迁移到所述第二多个核之一。

22. 权利要求 21 的处理器，其中所述线程迁移逻辑包括用于将逻辑核映射到物理核的表。

23. 权利要求 21 的处理器，其中所述线程迁移逻辑响应于操作系统调度程序。

24. 权利要求 18 的处理器，其中所述第一类型的核的性能故意高于所述第二类型的核的性能。

25. 权利要求 18 的处理器，其中所述第一类型的核的性能通过配置高于所述第二类型的核的性能。

26. 一种方法，包括:

将线程集分配到处理器核集;

监测所述处理器核的消耗功率;

计算所述消耗功率和期望功率之间的误差数值；以及

基于所述误差数值从所述分配进行转变。

27. 权利要求 26 的方法，其中所述转变包括在所述处理器核集内功率大的核和功率小的核之间改变所述线程集的所述分配。

28. 权利要求 26 的方法，其中所述转变包括通过配置所述处理器核

集内所述功率大的核和所述功率小的核而改变所述功率大的核和所述功率小的核之间所述线程集的分配。

29. 权利要求 26 的方法，还包括对所述误差数值随时间积分。

30. 权利要求 26 的方法，还包括随时间采样所述误差数值。

31. 一种方法，包括:

确定运行线程集；以及

将各个所述线程分配到处理器核集之一，其中所述分配响应于功率预算。

32. 权利要求 31 的方法，其中所述处理器核集包括能够作为第一类型和第二类型核的可配置核。

33. 权利要求 31 的方法，其中所述处理器核集包括设计成第一类型和第二类型核的核。

34. 权利要求 31 的方法，还包括将新线程分配到来自所述处理器核集的第二类型核，并将所述运行线程集之一从所述处理器核集内的第一类型核迁移到所述第二类型核。

35. 权利要求 34 的方法，其中所述迁移由线程迁移逻辑执行。

36. 权利要求 34 的方法，其中所述迁移响应于操作系统调度程序。

37. 一种系统，包括:

处理器，包括监测逻辑以监测所述处理器核的属性的数值，转换逻辑以响应于所述核的所述属性确定所述处理器的功耗测量，以及控制逻辑以响应于所述功耗测量调整所述处理器的每条指令能量的度量;

音频输入/输出逻辑；以及

接口，将所述处理器耦合到所述音频输入/输出逻辑。

38. 权利要求 37 的系统，其中所述核的所述属性为核运行状态，且其中通过将所述核运行状态乘以当所述核处于所述核运行状态时每个时钟耗费的能量数量，确定所述功耗的测量。

39. 权利要求 37 的系统，其中所述核的所述属性为每个时钟退回的指令数目，且其中通过将所述每个时钟退回的指令数目乘以每个时钟每条指令耗费的能量数量，确定所述功耗的测量。

40. 权利要求 37 的系统，其中所述核的所述属性为所述核的功能块的活动状态，且其中通过将所述功能块的所述活动状态乘以当所述功能块处于所述活动状态时每个时钟耗费的能量数量，确定所述功耗的测

量。

41. 权利要求 37 的系统，其中所述属性为核源电流，且其中所述功耗的测量包括所述核源电流。

42. 权利要求 37 的系统，其中所述控制逻辑响应于所述功耗的测量而调整所述处理器的工作电压和工作频率。

43. 权利要求 37 的系统，其中所述控制逻辑响应于所述功耗的测量而在所述处理器的大核和小核之间迁移程序的线程。

44. 权利要求 37 的系统，其中所述控制逻辑响应于所述功耗的测量而接通所述处理器的所述核内的可选性能电路。

45. 权利要求 37 的系统，其中所述控制逻辑响应于所述功耗的测量而接通所述处理器的所述核内的可选预测电路。

45. 权利要求 37 的系统，其中所述处理器还包括差值逻辑以计算所述功耗的测量和期望功耗之间的差值。

45. 权利要求 45 的系统，其中所述处理器还包括积分电路以确定所述功耗的测量和期望功耗之间的所述差值的时间积分。

46. 权利要求 45 的处理器，还包括采样电路以根据采样方法将所述功耗的测量供给到所述控制逻辑。

47. 一种系统，包括:

处理器，包括第一多个第一类型的核；第二多个第二类型的核；以及模块，将线程分配到所述第一多个的所述第一类型核或者所述第二多个的所述第二类型核之一;

音频输入/输出逻辑；以及

接口，将所述处理器耦合到所述音频输入/输出逻辑。

48. 权利要求 47 的系统，其中所述模块根据功率预算分配所述线程。

49. 权利要求 47 的系统，其中所述模块根据分配表分配所述线程。

50. 权利要求 47 的系统，其中所述模块包括线程迁移逻辑，将新线程分配到所述第二多个核之一并将已有线程从所述第一多个核之一迁移到所述第二多个核之一。

51. 权利要求 50 的系统，其中所述线程迁移逻辑包括用于将逻辑核映射到物理核的表。

52. 一种处理器，包括:

用于将线程集分配到处理器核集的装置;

用于监测所述处理器核的消耗功率的装置;

用于计算所述消耗功率和期望功率之间的误差数值的装置;以及

用于基于所述误差数值从所述分配进行转变的装置。

52. 权利要求 52 的处理器,其中所述用于转变的装置包括用于在所述处理器核集内功率大的核和功率小的核之间改变所述线程集的分配的装置。

53. 权利要求 52 的处理器,其中所述用于转变的装置包括用于通过配置所述处理器核集内所述功率大的核和所述功率小的核而改变所述功率大的核和所述功率小的核之间所述线程集的所述分配的装置。

54. 权利要求 52 的处理器,还包括用于对所述误差数值随时间积分的装置。

55. 权利要求 52 的处理器,还包括用于随时间采样所述误差数值的装置。

56. 一种处理器,包括:

用于确定运行线程集的装置;以及

用于将各个所述线程分配到处理器核集之一的装置,其中所述分配响应于功率预算。

57. 权利要求 56 的处理器,其中所述处理器核集包括能够作为第一类型和第二类型核的可配置核。

58. 权利要求 56 的处理器,其中所述处理器核集包括设计成第一类型和第二类型核的核。

59. 权利要求 56 的处理器,还包括用于将新线程分配到来自所述处理器核集的第二类型核的装置,以及用于将所述运行线程集之一从所述处理器核集内的第一类型核迁移到所述第二类型核的装置。

根据可用并行数目改变每条指令能量的方法和设备

技术领域

本发明一般涉及可以执行具有变化数量的标量和并行资源需求的程序的微处理器，更具体地涉及采用多个核的微处理器。

背景技术

在一些实施例中，计算机工作负荷连续地从具有少量内在并行(parallelism)(主要为标量)的工作负荷转到具有显著数量的并行(主要为并行)的工作负荷，且这种本性在软件的不同程序段之间可能不同。典型的标量工作负荷包括软件开发工具、办公室生产力套装软件、和操作系统内核例程。典型的并行工作负荷包括 3D 图形、媒体处理、和科学应用。标量工作负荷可退回范围 0.2 至 2.0 的 IPC(每个时钟执行的指令)，而并行工作负荷可以获得范围为 4 至几千 IPC 的吞吐量。后一种的高 IPC 通过使用指令级的并行和线程级的并行可以得到。

现有技术微处理器通常设计成以标量或并行计算机性能为主要目标。为了实现高的标量性能，经常期望尽可能地减小执行潜伏期。减小有效潜伏期的微架构技术包括预测执行、分支预测、和高速缓存。对高标量性能的追求已经实现了大的乱序、高度预测、深管线微处理器。为了获得高的并行计算机性能，则期望提供尽可能大的执行吞吐量(带宽)。提高吞吐量的微架构技术包括宽超标量处理、单指令多数据的指令、芯片级多处理、以及多线程。

当尝试构建可同时在标量和并行任务上执行良好的微处理器时会产生问题。一个问题可能起因于如下理解，即，实现短潜伏期所需的设计技术在某些情形中可能与实现高吞吐量所需的设计技术大相迥异。

附图说明

在附图中示范性地而非限制性地阐述本发明，其中在附图中使用相似的参考数字表示相似的元件。附图中：

图 1 为根据一个实施例的包括可由电压和频率配置的核的处理器的示意性图示。

图 2 为根据一个实施例的包括通过处理功率和功耗可选择的核的

处理器示意性图示。

图 3 为根据一个实施例的包括由可选的性能电路配置的核的处理器的示意性图示。

图 4 为根据本发明一个实施例的包括可由可选的预测电路配置的核的处理器的示意性图示。

图 5 为根据本发明一个实施例的包括核的处理器以及节流细节的示意性图示。

图 6 为示出了根据本发明一个实施例的转变到不同核配置的流程图。

图 7 为示出了根据本发明另一个实施例的转变到不同核配置的流程图。

图 8 为示出了根据本发明另一个实施例的转变到不同核配置的流程图。

图 9 为示出了根据本发明另一个实施例的转变到不同核配置的流程图。

图 10A 为根据本发明一个实施例的包括具有节流和多个核的处理器的系统的示意性图示。

图 10B 为根据本发明另一实施例的包括具有节流和多个核的处理器的系统的示意性图示。

发明详述

下述描述了根据软件程序中可用的并行数量而改变耗费以处理各个指令的能量数量的技术。在下述描述中，陈述了许多具体细节以提供对本发明的更彻底的理解，例如逻辑实施、软件模块分配、总线以及其他界面信号技术。然而，本领域技术人员将会了解，无需这些具体细节亦可实践本发明。在其他情形中，没有详细地示出控制结构、门级电路以及完整软件指令序列以免本发明变得不明确。本领域普通技术人员借助于此处的描述将能够实施恰当的功能而无需过多的实验。在某些实施例中，本发明披露成例如由 Intel®公司制造的 Pentium®兼容处理器的多核实施的形式。然而，本发明可以实践于其他类型的处理器，例如 Itanium 处理器系列兼容处理器、X-Scale®系列兼容处理器、或者来自其他厂商或设计者的任何处理器架构的任何各种不同的通用处理器。另外，一些实施例可包括或者可以是专用处

理器，例如图形、网络、图像、通信、或者任何其他已知或以其他方式可得到类型的处理器。

可以基于每瓦特的每秒指令数(IPS)测量功率效率。IPS/瓦特度量等效于每条指令能量，或者更精确而言，IPS/瓦特正比于每条指令能量的倒数，即：

(IPS)/(瓦特)=(指令)/(焦耳)　　方程 1

每条指令能量这个度量的重要性质为该度量与处理指令所需的时间数量无关。这使得每条指令能量是用于吞吐量性能的有用的度量。

通过将微处理器模拟成每条指令被执行时充电或者放电的电容器，由此可以执行对微处理器功耗的近似分析(为了简化，可以忽略漏电流和短路开关电流)。在该假设下，每条指令能量仅取决于两个方面：被触发以处理各个指令的电容数量(从拾取到退回)和电源电压。通常用于电容器的如下公知公式：

$E=CV^2/2$　　方程 2

也可以用于微处理器。E 为处理指令所需的能量；C 为在处理该指令时触发的电容数量；V 为电源电压。

微处理器可以在例如 100 瓦特的固定功率预算范围内工作。在某些时间段内进行平均，无论微处理器或软件工作内容如何，微处理器的功耗不应超过该功率预算。为了实现该目标，微处理器可结合某些形式的动态热管理。类似地芯片级的多处理器可以调节(节流)其活动以保持在固定功率预算范围内，无论其是否正退回例如 0.2 个每个时钟执行的指令(IPC)或者 20 IPC。为了提供良好性能，在本示例中芯片级多处理器应该能够将其 MIPS/瓦特或者等效地其能量/指令改变到 100:1 的范围以上。

设计可同时实现高的标量性能和高吞吐量性能的微处理器的一种方法是根据软件中可用的或者估算可用的并行数量而动态地变化耗费用于处理各个指令的能量数量。换而言之，如果存在少量的并行，则微处理器可将所有可用的能量耗费用于处理少数指令；但是如果存在大量的并行，则微处理器将非常少的能量耗费用于处理各个指令。这可以表达成：

P=(EPI)×(IPS)　　方程 3

其中 P 为固定功率预算，EPI 为每个退回指令的平均能量，IPS

为所有处理器核上每秒退回的指令总数。本实施例尝试将总的多处理器芯片功率维持在几乎恒定的水平。

互补型金属氧化物半导体(CMOS)电压和频率缩放可用于获得不同的每条指令能量比率。在一个实施例中，根据所期望的性能和功率水平，逻辑相关地变化微处理器的源电压和时钟频率。为了将芯片级微处理器的总功耗维持在固定功率预算范围内，可以如下所述动态地进行电压和频率缩放。对于低的线程并行，可以使用高的源电压和高频运行少数核以得到最佳标量性能。对于高的线程并行，可以使用低的源电压和低频运行许多核以得到最佳的吞吐量性能。由于非活动核可能期望低的功耗，因此例如动态睡眠晶体管和体偏压的漏电控制技术可以被采用。

现在参照图 1，示出了根据一个实施例的包括可由电压和频率配置的核的处理器的示意性图示。示出了核 1 120、核 2 130、核 3 140 和核 4 150，但是在其他实施例中，处理器中可能存在多于四个或者少于四个核。一个或多个这些核可具有电压控制电路和时钟频率控制电路。图 1 清楚地示出了核 1 120 具有电压控制电路 122 和频率控制电路 124，但是其他核也可以具有等效电路，或者该电压控制和频率控制逻辑可以是并不直接与具体核相关联的分离的逻辑。

节流模块 110 可用于收集信息并确定或者评估执行软件程序中存在的并行数量。在一个实施例中，并行数量可以为得到支持的同时发生的线程数目。在其他实施例中，其他度量可用于表达并行数量，例如每秒退回的指令总数，或者可支持预测多线程执行的分支指令的数目。节流模块 110 可利用由操作系统提供的信息以辅助确定该并行数量。在其他实施例中，节流模块 110 可以使用处理器内的硬件逻辑及其核进行该确定。可以连续地或者周期性地进行该确定。

每次节流模块 110 确定程序中并行的数量时，该节流模块可通过信号线 112、114、116 和 118 指示核 120、130、140、150 改变其电压和时钟频率。在一个实施例中，信号线 112、114、116 和 118 也可以用于接通或关闭核，或者从包含核的功率井除去功率。在其他实施例中，可以通过时钟门控或者指令饥饿（instruction starvation）技术关闭核。在一个实施例中，如果线程级当前的并行数量超过先前数量的值大于阈值，则节流模块通过降低各个核中的电压和时钟频率

可启动转变到运行更多数目的线程，但是在更多数目的核上运行这些线程。先前关闭的核可以被接通以支持更大数目的线程。类似地，如果线程级当前的并行数量低于预先数量的值大于阈值，则节流模块通过提高某些核中的电压和时钟频率可启动转变到运行更少数目的线程，但是在更少数目的这些核上运行这些线程。由于不再需要这些核以支持更少数目的线程，先前接通的某些核被关闭。

在一个实施例中，可以设计单指令集架构(ISA)异类多核微处理器，其中可以使用不同的微架构跨过性能和功率范围。在一个实施例中，芯片级多处理器可以由两种处理器核构成，该处理器核称为大核和小核。该两种类型的核可以实施相同的指令集架构，使用超高速缓存相关性以实施共用存储器，且仅仅在微架构方面不同。在其他实施例中，该两种类型的核可以实施相似的指令集架构，或者小核可以实施大核的指令集的子集。大核可能是乱序、超级标量、深管线机器，而小核可能是有序、标量、短管线机器。Intel Pentium 4 处理器和Intel i486 处理器是这两类核的代表。在其他实施例中，可以使用运行基本上相似或相同的指令集架构的两种以上类型或性能水平的核。

在一个实施例中，芯片级多处理器包括一个大核和 25 个小核，这两种核的功耗比率为 25:1，标量性能比率为 5:1，每条指令能量为 5:1 的范围。本实施例的芯片级多处理器按照下述工作。对于低的线程级并行，可以运行该大核以得到最佳标量性能。对于高的线程级并行，可以运行多个小核以得到最佳的吞吐量性能。

在任意时刻，微处理器可以运行一个大核或者 25 个小核。由于可用的软件线程的数目随时间变化，非对称的多处理器能够在大核和小核之间迁移线程。可以实施线程迁移逻辑以支持该功能。

实际上，期望少量的小核与该大核同时运行，从而在关闭大核时减小吞吐量性能不连续。在先前示例中，3 个单位的吞吐量不连续可能是由于关闭大核和接通两个小核。为了减小总吞吐量损失的百分比，通过允许例如多达 5 个小核与大核同时运行，如果电源能短时间支持该动作，则可以将该不连续转移到发生于更大数目的正在运行的线程的情况下。

使用代表当前微处理器的两种类型的核，可以获得范围为 4:1 的每条指令能量。随着未来的微处理器继续达到更高水平的标量性能，

可能的每条指令能量的范围预期可能增大到 6:1，或者将远远超出这个范围。

现在参考图 2，示出了根据一个实施例，包含通过处理功率和功耗可选择的核的处理器的示意性图示。该处理器可包括少数大核，即 A 核，还包括大量的小核，即 B 核。示出了 A 核 1 220、A 核 2 222、和 B 核 1 至 60 230-262，但是在其他实施例中处理器中可能存在比两个 A 核与六十个 B 核更多或者更少的核。

节流模块 210 可再次用于收集信息并确定执行软件程序中存在的并行数量。在一个实施例中，并行数量可以为得到支持的同时发生的线程数目。在其他实施例中，如前所述，其他度量可用于表达并行数量。节流模块 210 可利用由操作系统提供的信息以辅助确定该并行数量。在其他实施例中，节流模块 210 可以使用处理器内的硬件逻辑及其核进行该确定。可以连续地或者周期性地进行该确定。

由于可用的软件线程的数目可能随时间变化，图 1 的处理器可包括能够在大的 A 核和小的 B 核之间迁移线程的线程迁移逻辑 212。期望允许少量的小 B 核与大的 A 核同时运行，从而在关闭大的 A 核时减小吞吐量性能不连续。为了减小总吞吐量损失的百分比，通过允许例如多达 5 个小核与大核同时运行，则可以将该不连续转移到发生于更大数目的正在运行的线程的情况下。

每次节流模块 210 确定程序中并行的数量时，该节流模块可使用信号线 224 至 266 启动 A 核和 B 核的上电或下电。在一个实施例中，如果当前的并行数量超过先前数量的值大于阈值，则节流模块 210 可使用线程迁移逻辑 212 启动转变到运行更多数目的线程，这些线程可以在更多数目的 B 核上运行。先前关闭的 B 核可以被接通以支持更大数目的线程，且已经被接通的任何 A 核可以被关闭。类似地，如果当前的并行数量低于预先数量的值大于阈值，则节流模块可通过在更少数目的 A 核上运行这些线程而启动转变到运行更少数目的线程。先前接通的 B 核可以被关闭，因为不再需要这些核以支持更少数目的线程，且 A 核被接通以支持该更少数目的线程。如前所述，期望少量的 B 核与 A 核同时运行，从而在关闭大核时减小吞吐量性能不连续。

在一个实施例中，节流模块可以实施为不需要反馈回路的方式。这里，节流的控制动作(例如决定运行线程的核的类型和数目)并不返

回以影响输入值(例如用于线程的核的分配和配置)。在该实施例中，可以假设各个 A 核 220、222 可能消耗与 B 核 230 至 262 中的 25 个相同的功率数量。在其他实施例中，可以使用不同的功耗比率。处理器可以将其总功率预算划分成两个部分。对于各个部分，该功率预算可允许一个 A 核与多达 5 个 B 核同时工作，或者零个 A 核与多达 30 个 B 核同时工作。在其他实施例中，该功率预算可以按照其他方式划分成多个部分。

在一个实施例中，可以根据表 I 将运行线程的数目(RT)分配给一些 A 核(QAC)和一些 B 核(QBC)。

表 I

RT	QAC	QBC	RT	QAC	QBC
0	0	0	29	1	28
1	1	0	30	1	29
2	2	0	31	1	30
3	2	1	32	1	31
4	2	2	33	1	32
...			34	1	33
10	2	8	35	1	34
11	2	9	36	1	35
12	2	10	37	0	37
13	1	12	38	0	38
14	1	13	39	0	39
15	1	14	40	0	40
...			...		
28	1	27	60	0	60

当运行线程的数目增大且新线程启动(在一个实施例中通过处理器间中断)时，该节流模块可确定当前运行线程的数目。取决于当前运行线程的数目，该新线程可以根据上述表 I 被指派至 A 核或 B 核。在本实施例中，对于某些情形，例如当从 12 个线程增大到 13 个线程，或者从 36 个线程增大到 37 个线程时，在 A 核上运行的现有线程将迁移到在 B 核上运行。当该迁移完成时，现有迁移线程和新线程都可以启动。因此，在本实施例中，新线程可能呈现启动延迟。

当运行线程数目减小时，类似的过程可能发生。当特定线程终止且其核停止时，各种方法可以用于潜在地将剩余线程之一从在 B 核上运行迁移到在 A 核上运行。这个过程可能发生于例如当运行线程的数目从 13 个线程减小到 12 个线程，或者从 37 个线程减小到 36 个线程时。在一个实施例中，可以使用周期定时器以允许在特定时间间隔内仅发生一次迁移。在线程快速产生和终止的情形中，这可以有利地防止太频繁的线程迁移。受影响的线程仍运行于 B 核上，直到该特定时间间隔。

在一个实施例中，节流模块可按照对软件是透明的方式执行从 A 核到 B 核的迁移。节流模块的线程迁移机制可包括将逻辑核映射到物理核的表，可能需要的向核发出迁移信号的中断、复制核的处理器状态的微代码或硬布线逻辑、以及处理器核之间的互连网络。逻辑核的数目可以等于 B 核的数目。

在另一个实施例中，节流模块可按照对软件非透明的方式执行从 A 核到 B 核的迁移。线程迁移可以由操作系统调度程序执行。操作系统可以使用当前运行线程追踪核数目，将新的线程指派到核，并将线程从 A 核迁移到 B 核(或者从 B 核到 A 核)。软件线程迁移可以使用与硬件实施中所述功能等效的功能。在一个实施例中，节流模块操作对于应用程序可能是透明的，尽管对于操作系统是不透明的。

调制功耗的一个备选方式是调整逻辑块的尺寸或功能。当不需要大的阵列尺寸时，例如尺寸可变的调度程序、超高速缓冲存储器、转换后备缓冲器(TLB)、分支预测器、和其他可选的性能电路可以用于减小开关电容(并因此减小能量)。除了动态调整阵列大小之外，还可以设计大核，其通过动态地禁止执行单元、管线级、和其他可选的性能电路而使其性能退化到较小核的性能。这些技术共同地称为适应性处理。

芯片级多处理器的一个实施例可按下述工作。对于低的线程并行，可以运行少量的核，在各个核上使用可用的可选性能电路的第一集合(例如所有或许多该性能电路)以得到良好的标量性能。对于高的线程并行，可以运行许多核，在各个核上使用更少的可选性能电路以得到良好的吞吐量性能。

减小阵列尺寸和禁止执行单元的最终结果为减小每条指令触发的

电容。然而，如果设计本来就更小的核，则无法如此大程度地减小开关电容。尽管不用的执行硬件可以被门控掉，但是核的物理尺寸没有变化，因此与该仍然活动的硬件块相关联的布线长度仍长于小核。

通过检查大的乱序微处理器的平面布置图并确定可以将多少个可选的性能电路关闭以将处理器转换为小的有序机器(记住，这些块不能被物理去除)，由此可以评估每条指令能量的可能减少。随后可以量化被关闭的处理器核面积的百分比，该百分比可能接近开关电容的减少。从方程(2)，每条指令能量大约与开关电容的数量成正比。

大约估算的结果为，在某些情形中，多达 50％的开关电容可以被关闭，导致每条指令能量的减少为 1× 至 2×。在一些实施例中，除了时钟门控之外，使用例如动态睡眠晶体管和体偏压的漏电控制技术有助于减少每条指令消耗的能量。

现在参考图 3，示出了根据一个实施例包括由可选性能电路配置的核的处理器的示意性图示。图 3 处理器可包括四个核，即核 1 320、核 2 370、核 3 380 和核 4 390。在其他实施例中，可以使用比四个核更多或更少的核。核 1 320 显示各种可选的性能电路。调度程序 A 334 可耦合到可选调度程序 B 336，该可选调度程序 B 336 在接通时可以提高性能。执行单元 1 340 可以耦合到可选执行单元 2 至 4 342、344、346，这些可选执行单元在接通时可以提高性能。零级(L0)高速缓存 A 322 可以耦合到 L0 高速缓存 B 324，该 L0 高速缓存 B 324 接通时可以提高性能。TLB A 326 可以耦合到 TLB B 328，该 TLB B 328 接通时可以提高性能。重排序缓冲器(ROB)338 可具有可变数目的线路，或者可以全部关闭以抑制乱序执行。最后，与其他管线级 330 分离的预拾取级 332 在被上电时可以执行预测拾取。在其他实施例中，可以使用其他可选性能电路。

节流模块 310 可再次用于收集信息并确定执行软件程序中存在的并行数量。节流模块 310 可以与结合图 1 和 2 所述节流模块相似。每次节流模块 310 确定程序中并行的数量时，该节流模块可通过信号线 312、314、316、和 318 指示核 320、370、380、和 390 改变上电或下电的可选性能电路数目。在一个实施例中，信号线 312、314、316、和 318 还可以用于接通或关闭核 320、370、380、和 390。在一个实施例中，如果当前的并行数量超过先前数量的值大于阈值，则该节流模

块可通过减小每个核内被接通的可选性能电路而在更大数目的这些核上运行这些线程，由此转变到运行更大数目的线程。先前关闭的核可以被接通以支持更大数目的线程。类似地，如果当前的并行数量低于预先数量的值大于阈值，则节流模块可通过增加某些核内被接通的可选性能电路而在更少数目的这些核上运行这些线程，由此转变到运行更少数目的线程。先前接通的核可以被关闭，因为不再需要这些核以支持更少数目的线程。

已经提出各种形式的预测控制以减小由于错误预测指令例如错误预测分支之后的指令而浪费的能量。附加的能量源于被触发以处理错误预测指令的电容。尽管错误预测指令的结果可以被抛弃，但是能量已经耗费。通过将其充电到下一个正确预测(退回)指令，由此可以解释该能量。

管线门控是一种避免管线填满由于一个或多个低置信度分支预测而可能被抛弃的指令的技术。在使用预测控制的一个实施例中，芯片级多处理器可按下述工作。对于低的线程并行，使用增大数量的预测运行少数核，以得到良好的标量性能。对于高的线程并行，在各个核上使用减小数量的预测运行许多核，以得到良好的吞吐量性能。

尺寸可变的核技术和预测控制之间可能存在某些交叠，因为减小调度程序和重排序缓冲器入口的数目还减小了可以预测的指令的数目。例如高速缓存、TLB和分支预测器的其他处理器资源的尺寸对可能的预测数量的影响不会这么大。

现在参考图 4，示出了根据本发明一个实施例的包括由可选的预测电路配置的核的处理器的示意性图示。图 4 处理器可包括四个核，即核 1 420、核 2 470、核 3 480 和核 4 490。在其他实施例中，可以使用比四个核更多或更少的核。核 1 420 显示各种可选的预测电路。预拾取级 430 可用于预测拾取指令。分支预测器 434 可用于支持程序分支的预测执行。在某些实施例中，其他预测器 436 可以是回路预测器或其他形式的预测器以支持其他形式的预测执行。在其他实施例中，可以使用另外的可选的预测电路。

节流模块 410 可再次用于收集信息并确定执行软件程序中存在的并行数量。节流模块 410 通常与结合图 1、2 和 3 所述节流模块相似地工作。每次节流模块 410 确定程序中并行的数量时，该节流模块可通

过信号线 412、414、416、和 418 指示核 420、470、480、和 490 改变上电或下电的可选预测电路的数目。在一个实施例中，信号线 412、414、416、和 418 还可以用于接通或关闭核 420、470、480、和 490。在一个实施例中，如果当前的并行数量超过先前数量的值大于阈值，则该节流模块可通过减小每个核内被接通的可选预测电路而在更大数目的这些核上运行这些线程，由此转变到运行更大数目的线程。先前关闭的核可以被接通以支持更大数目的线程。类似地，如果当前的并行数量低于预先数量的值大于阈值，则节流模块可通过增加某些核内被接通的可选预测电路而在更少数目的这些核上运行这些线程，由此转变到运行更少数目的线程。先前接通的某些核可以被关闭，因为不再需要这些核以支持更少数目的线程。

对于结合图 1、2、3 和 4 上述的各种技术，节流模块可以调节多处理器的工作以将总芯片功率维持在固定功率预算内。通过与每秒退回的指令的总数成反比地改变每条指令能量数量，节流模块硬件可满足方程(3)。响应于过功率的情形，在诸多实施例中节流模块可以采取下述动作中的一个或多个：降低电压和频率(对于图 1 的电压和频率缩放的情形)，将线程从大核迁移到小核(对于图 2 的非对称核的情形)，减小可选性能电路的电容(对于图 3 的尺寸可变的核的情形)，或者减小预测数量(对于图 4 的预测控制的情形)。

在各种情形中，软件程序可将处理器视为大的对称的芯片级多处理器，尽管出现不正常的性能，即由于软件请求硬件同时运行更多线程而使得现有线程变得更慢，即使最终的吞吐量增大。采用这种方法，为目前的共用存储器多处理器编程模型编写的软件可以继续运行而无需调整。

现在参考图 5，示出了根据本发明一个实施例的包括核的处理器以及节流模块的细节的示意性图示。M 个处理器核 1 至 M 502 至 508 在多个实施例中可以是可由电压和频率配置的图 1 的核、处理功率和功耗变化的图 2 的大核和小核、可由可选性能电路配置的图 3 的核、可由可选预测电路配置的图 4 的核、或者部分或所有这些类型的核的混合。在其他实施例中还可以使用其他类型的核。

监视器 1 至 M 512 至 518 可以监视相关核和辅助处理器电路的一个或多个属性。在一些实施例中，这些属性可包括该核是否在运行或

者停止、每个时钟周期退回的指令的瞬时数目、核的特定功能块是活动的还是空闲的、除了核内的功能块之外的处理器的特定功能块是活动的还是空闲的、以及核的源电流和温度(或者管芯温度)。除了核内的功能块之外的处理器的功能块可包括例如共用高速缓存或者存储控制器的电路。可以通过电流传感器电阻和模数(A/D)转换器测量该源电流。可以通过热敏二极管和 A/D 转换器测量该温度。各个监视器 1 至 M 512 至 518 的输出可以是所有或者某些部分这些属性的监测值。

转换至功率的逻辑 530 可从监视器 1 至 M 512 至 518 接收一个或几个监测值。在各种实施例中，监测值可以转换成功耗的测量。在监测值反映核是否在运行或者停止的实施例中，通过将核运行(或者停止)状态乘以当核处于运行(或者停止)状态时每个时钟耗费的能量的平均数量，该监测值可以转换成功耗。随后可以对处理器内的所有核的这些乘积求和。在监测值反映每个时钟周期退回的指令的瞬时数目的实施例中，通过将指令数目乘以每个时钟每条指令耗费的能量的平均数量，该监测值可以转换成功耗。随后可以对处理器内的所有核的这些乘积求和。在监测值反映核的特定功能块是否是活动的或者空闲的实施例中(或者在某些实施例中，反映除了核内的功能块之外的处理器的特定功能块是否是活动或者空闲的)，通过将该活动(或者空闲)状态乘以块处于活动(或者空闲)状态时每个时钟耗费的能量的平均数量，该监测值可以转换成功耗。随后可以对各个核中的所有块以及处理器内的所有核的这些乘积求和。当考虑不在该核内的块时，该乘积可包括在该求和内。在各个这些实施例中，通过乘以正比于时钟频率与源电压平方的乘积的值而针对电压和频率调整所得到的总和。

在监测值反映各个核的源电流的实施例中，通过将源电流乘以源电压，该监测值可以转换成功耗。

在监测值反映核或管芯温度的实施例中，图 5 的电路可以用于维持几乎恒定的核或者管芯温度，而不是维持几乎恒定的功耗。

计算差值的逻辑 534 可用于计算转换至功率的逻辑 530 的转换功耗(或者管芯温度)输出与期望的功耗值(或者期望的管芯温度值)之间的差值。该差值可以用作“误差”数值。

积分逻辑 538 可在一个实施例中提供与由计算差值的逻辑 534 供给的误差数值随时间的积分成正比的积分数值。在一个实施例中，可

以使用累加器计算该积分，其中可以使用加法器和寄存器实施该累加器。该累加器在上界和下界可以饱和以避免溢出。在一个实施例中，该累加器输出可以是固定点的二进制数，例如 2 至 6 个整数位和 2 至 16 个小数位。可以检查累加器的最高有效位，这可以有利地实现使输出变化缓慢的性能。使用积分逻辑 538 可以帮助慢反馈回路 550 从而随着时间将该误差数值减小到零。当误差数值为功率时，使用该积分逻辑 538 是最为有利的，这是因为不同时钟周期之间的瞬时功耗可能发生显著变化。

在其他实施例中，积分逻辑 538 可以被逻辑替代以得到与该误差数值成比例的数值，当误差数值是温度时这是有利的。在另外实施例中，该逻辑可以得到与该误差数值的时间微分成比例的数值，或者所有上述数值的某些线性组合。

采样逻辑 544 可以用于某些实施例。来自积分逻辑 538 的积分数值可以随着各个时钟周期而改变，即使该积分数值的提取可能相对于图 5 逻辑的速度发生缓慢的变化。某些控制技术可以在每个时钟周期改变其动作而仅需很少的系统成本。这种情况下可能无需采样。在其他控制技术中，当积分逻辑 538 的输出接近转变点时，有利地使用采样以帮助减小随各个时钟振荡的数值。

在一个实施例中，固定采样技术可以用于采样逻辑 544。每固定数目 N 个时钟周期采样一次该数值。这可以防止该数值变化得比每 N 个时钟周期一次快。然而，这种技术无法实现在短于 N 个时钟周期的时间段内进行控制，且当与 N 个时钟周期的时间段相比积分缓慢时该技术可以最佳地工作。

在另外实施例中，滞后技术可以用于采样逻辑 544。只有当输入和输出数值超过阈值 T 时，采样逻辑 544 的输出才改变。当差值超过 T 时，输出数值被输入数值替代，否则输出数值可保持不变。

对于使用慢反馈回路 550 的实施例，可以使用控制逻辑 548。在一个实施例中，例如核通过改变源电压和频率可以改变功耗的图 1 的实施例，控制逻辑 548 可以指示源电压和频率的变化。在这些实施例中，应该注意，电源电压的变化可能花费相对长的时间，例如 100 毫秒。在一个实施例中，表或逻辑块可以用于设定电源电压和频率。表 II 给出了用于各种控制值(CV)的数值的这种表或逻辑块的一个示例。

表 II

CV	伏特	频率(GHz)
0	1.4	4
1	1.4	4
2	1.4	4
3	1.2	3.3
4	1.1	2.9
5	1.0	2.5
6	1.0	2.5
7	0.9	2.2

在一个实施例中，例如线程可以分配到大核和小核的图 2 的实施例，控制逻辑 948 可以将线程分配到核并根据对于软件是透明的控制值而迁移线程。线程迁移机制可包括用于将“逻辑”处理器核映射到“物理”处理器核的表或逻辑块。该线程迁移机制还可包括需要的发出迁移信号的中断、复制处理器状态的微代码或等效逻辑、以及各种处理器核之间的互连网络。软件看到的逻辑处理器的数目可以等于正在运行的小核的数目。当功率预算允许时，大核可以替代小核。在一个实施例中，用于预算作为控制值函数的大核使用的表或逻辑块示于表 III。

表 III

CV	大核的数量
0	2
1	1
2	0

这里进行了一个简化的假设，即，当大核无法使用时，线程可以在小核上运行。

在一个实施例中，例如线程可以分配到其资源可以动态变化的核的图 3 的实施例，控制逻辑 548 可以给出改变核的功能单元的数量或者容量的控制值。在改变核容量要求阵列被填充或往回写或者管线需要被重新填充的一些实施例中，用于这些改变的时间范围可以为 10 微妙。可以使用表或逻辑块预算作为控制值函数的核功能单元的使用。在一个实施例中，用于预算作为控制值函数的功能单元使用的表或逻

辑块示于表 IV，其中该功能单元可以是核内的执行单元。

表 IV

CV	执行单元
0	4
1	4
2	4
3	2
4	2
5	1
6	1
7	1
8	1

在一个实施例中，例如线程可以分配到其预测数量可动态变化的核的图 4 实施例，控制逻辑 548 可以给出改变核内容许的预测数量的控制值。可以使用表或逻辑块预算作为控制值函数的核内预测数量的使用。在一个实施例中，用于调整作为控制值函数的预测数量的表或逻辑块示于表 V，其中预测的数量可以由核中在非预测指令之前预测执行指令的数目给出。

表 V

CV	预测指令
0	128
1	128
2	128
3	85
4	64
5	51
6	42
7	36
8	32

在许多实施例中，处理器核可以包括多个上述属性。例如，处理器可以具有能够进行电压和频率缩放的核，且还具有可调整数量的预测执行。在一个实施例中，图 2 的大的 A 核和小的 B 核还可以具有如

图 1 所示的电压和频率缩放。对于一个实施例，电压和频率可以固定，将大的 A 核配置成运行于高电压而小的 B 核配置成运行于低电压。在另外实施例中，大的 A 核和小的 B 核之间的电压和频率调整范围可以不同。为了辅助大的 A 核和小的 B 核之间的迁移，线程可以从大的 A 核迁移到小的 B 核，而小的 B 核最初运行于高的电压和频率。一旦大的 A 核不运行，则 B 核的电压和频率可以随后降低。

此外，可以使用表或逻辑块将线程分配到大的 A 核或小的 B 核，并进一步分配核的电压和频率。在一个实施例中，用于作为控制值函数进行这些调整的表或逻辑块示于表 VI。

表 VI

CV	大核的数量	电压	频率
0	2	1.4	4
1	2	1.4	4
2	1	1.4	4
3	1	1.4	4
4	0	1.4	4
5	0	1.2	3.3
6	0	1.1	2.9
7	0	1.0	2.5
8	0	1.0	2.5
9	0	0.9	2.2

有利地在慢反馈回路 550 附近维持略微恒定的增益，其中在该表或逻辑块内通过使各级的功率效应的大小相似可以实现这一点。

在某些实施例中，快反馈回路 560 可以与先前讨论的慢反馈回路 550 结合使用。在一个实施例中，可以使用时钟节流 540，即使时钟节流不会影响每条指令能量数量。当与前述的一个或多个慢反馈回路 550 结合使用时，使用时钟节流 540 是有利的。

在某些情况下，快反馈回路 560 可以施加了短潜伏期以防止过功率情形，且该施加只有当慢反馈回路 550 有时间作出响应时才保持有效。在未实施快反馈回路 960 的实施例中，处理器及其功率发送系统应该设计成能够处理持续时间与慢反馈回路 550 的响应时间一样长的过功率情形。当添加快反馈回路 560 时，过功率情形持续时间不会长

于快反馈回路 560 的响应时间，该响应时间的范围为 10 纳秒。

时钟节流 540 可以门控核时钟接通和关闭特定的负载周期，使用在计算差值的逻辑 534 中计算得到的误差数值作为其输入。在一个简单的实施例中，当误差数值超过固定阈值时，时钟可以停止特定数目的周期。该计算在各个时钟周期被执行并完全管线化。可以选择特定数目的周期以将功率限制为略高于期望功率(其允许慢反馈回路 550 作出响应)，但是不大于最大功率。

在另外实施例中，时钟节流 550 可以响应于由计算差值的逻辑 535 供给的误差数值的大小(例如处理器目前的运行功率比功率阈值高多少)而调制该负载周期。在一个实施例中，负载周期和误差数值之间关系如表 VII 所示。

表 VII

误差数值	负载周期	误差数值	负载周期
-2	100%	7	100%
-1	100%	8	94%
0	100%	9	88%
1	100%	10	81%
2	100%	11	75%
3	100%	12	69%
4	100%	13	63%
5	100%	14	56%
6	100%	15	50%

现在参考图 6，示出了根据本发明一个实施例的转变到不同核配置的流程图。处理开始于块 610，其包括将各种软件线程分配到可用的核。在一个实施例中，线程的数目被确定，且各个线程分配到一个核。在某些实施例中，这种确定可以由软件例如操作系统完成。在其他实施例中，这种确定可以由硬件逻辑，或者由硬件与软件的组合完成。在块 614，监测各个核消耗的功率数量，并计算观测的功耗和期望的功耗之间的误差数值。在各种实施例中，可以使用结合图 5 上述讨论的任意监测技术。接着在块 618 中，块 614 的误差数值可经历积分或采样技术之一或二者兼有，如结合图 5 如上所述。在某些实施例中，块 618 是可选的。块 618 的输出可以是控制值，该控制值抑制核配置直到

该误差数值在一时间段内被确定为基本上足以保证改变核配置的性能惩罚时才改变。

在决定块 622，确定该时间内的误差数值是否足以保证改变核的配置。如果差值不够大，则该处理在决定块 622 之后沿“否”（NO）路径且该处理重复。然而，如果该差值足够大，则该处理在决定块 622 之后沿“是”（YES）路径。

在块 626，可以根据该控制值改变电压和频率。在一个实施例中，可以如表 II 所示针对控制值改变电压和频率。在一个实施例中，各种核的电压和频率可以全部相似地改变。在其他实施例中，可以不同地改变各种核上的电压和频率。在任何情形下，该处理在块 610 重复。

现在参考图 7，示出了根据本发明一个实施例的转变到不同核配置的流程图。处理开始于块 710，其包括将各种软件线程分配到可用的核。在一个实施例中，线程的数目被确定，且各个线程分配到一个核。在某些实施例中，这种确定可以由软件例如操作系统完成。在其他实施例中，这种确定可以由硬件逻辑，或者由硬件与软件的组合完成。在块 714，监测各个核消耗的功率数量，并计算观测的功耗和期望的功耗之间的误差数值。在各种实施例中，可以使用结合图 5 上述的任意监测技术。接着在块 718 中，块 714 的误差数值可经历积分或采样技术之一或二者兼有，如结合图 5 如上所述。在某些实施例中，块 718 是可选的。块 718 的输出可以是控制值，该控制值抑制核配置直到该误差数值在一时间段内被确定为基本上足以保证改变核配置的性能惩罚时才改变。

在决定块 722，确定该时间内的误差数值是否足以保证改变核的配置。如果差值不够大，则该处理在决定块 722 之后沿“否”（NO）路径且该处理重复。然而，如果该差值足够大，则该处理在决定块 722 之后沿“是”（YES）路径。

在块 726，可以根据控制值而将线程重新分配到核。在一个实施例中，可以如上表 III 所示针对控制值将线程重新分配到特定数目的大核。在一个实施例中，大核的数目示出于表 III，且不在大核上运行的线程可以重新分配到小核。在其他实施例中，可以使用其他方案将线程重新分配到核。在任何情形下，该处理在块 710 重复。

现在参考图 8，示出了根据本发明一个实施例的转变到不同核配

置的流程图。处理开始于块 810，其包括将各种软件线程分配到可用的核。在一个实施例中，线程的数目被确定，且各个线程分配到一个核。在某些实施例中，这种确定可以由软件例如操作系统完成。在其他实施例中，这种确定可以由硬件逻辑，或者由硬件与软件的组合完成。在块 814，监测各个核消耗的功率数量，并计算观测的功耗和期望的功耗之间的误差数值。在各种实施例中，可以使用结合图 5 上述讨论的任意监测技术。接着在块 818 中，块 814 的误差数值可经历积分和采样技术之一或二者兼有，如结合图 5 如上所述。在某些实施例中，块 818 是可选的。块 818 的输出可以是控制值，该控制值抑制核配置直到该误差数值在一时间段内被确定为基本上足以保证改变核配置的性能惩罚时才改变。

在决定块 822，确定该时间内的误差数值是否足以保证改变核的配置。如果差值不够大，则该处理在决定块 822 之后沿“否”（NO）路径且该处理重复。然而，如果该差值足够大，则该处理在决定块 822 之后沿“是”（YES）路径。

在块 826，可以根据控制值如表 IV 所示接通或关闭核内可选电路的数量。在一个实施例中，可以如上表 IV 所示针对控制值改变上电或下电的执行单元的数量。在其他实施例中，可以根据控制值接通和关闭其他可选的性能电路。这些其他可选的性能电路可包括调度程序、高速缓存、转换后备缓冲器、调度程序、和重排序缓冲器。在任何情形下，该处理在块 810 重复。

现在参考图 9，示出了根据本发明一个实施例的转变到不同核配置的流程图。处理开始于块 910，其包括将各种软件线程分配到可用的核。在一个实施例中，线程的数目被确定，且各个线程分配到一个核。在某些实施例中，这种确定可以由软件例如操作系统完成。在其他实施例中，这种确定可以由硬件逻辑，或者由硬件与软件的组合完成。在块 914，监测各个核消耗的功率数量，并计算观测的功耗和期望的功耗之间的误差数值。在各种实施例中，可以使用结合图 5 上述讨论的任意监测技术。接着在块 918 中，块 914 的误差数值可经历积分和采样技术之一或二者兼有，如结合图 5 如上所述。在某些实施例中，块 918 是可选的。块 918 的输出可以是控制值，该控制值抑制核配置直到该误差数值在一时间段内被确定为基本上足以保证改变核配置的性能

惩罚时才改变。

在决定块 922，确定该时间内的误差数值是否足以保证改变核的配置。如果差值不够大，则该处理在决定块 922 之后沿“否”（NO）路径且该处理重复。然而，如果该差值足够大，则该处理在决定块 922 之后沿“是”（YES）路径。

在块 926，可以根据控制值如表 V 所示改变核内预测数量。在一个实施例中，可以如上表 V 所示针对控制值改变预测执行的指令的数目。在其他实施例中，可以使用其他方法根据控制值改变预测数量。改变预测数量的这些其他方法可包括上电或下电预拾取单元、分支预测器、或者其他形式的预测器。在任何情形下，该处理在块 910 重复。

现在参考图 10A 和 10B，示出了根据本发明两个实施例的包括具有节流和多个核的处理器的系统的示意性图示。图 10A 系统一般示出了处理器、存储器、和输入/输出装置通过系统总线互连的系统，而图 10B 系统一般示出了处理器、存储器、和输入/输出装置通过多个点对点接口互连的系统。

图 10A 系统可包括一个或者多个处理器，此处为了清楚仅示出了两个处理器 40、60。处理器 40、60 可包括一级高速缓存 42、62。图 10A 系统可具有通过总线接口 44、64、12、8 与系统总线 6 连接的多个功能。在一个实施例中，系统总线 6 可以是用于由 Intel® Corporation 制造的 Pentium®系列微处理器的前端总线(FSB)。在其他实施例中，可以使用其他总线。在某些实施例中，存储控制器 34 和总线桥 32 可统称为芯片组。在某些实施例中，芯片组的功能在物理芯片之间的划分可能不同于图 10A 实施例所示。

存储控制器 34 允许处理器 40、60 从系统存储器 10 以及从基本输入/输出系统（BIOS）可擦除编程只读存储器（EPROM）36 进行读写。在某些实施例中 BIOS EPROM 36 可使用闪烁存储器。存储控制器 34 可包括总线接口 8 以允许存储器读写数据在系统总线 6 上向总线代理（bus agent）传送和从总线代理传送。存储控制器 34 还通过高性能图形接口 39 与高性能图形电路 38 连接。在某些实施例中，高性能图形接口 39 可以是先进图形端口 AGP 接口。存储控制器 34 可以将来自系统存储器 10 的数据通过高性能图形接口 39 引导至高性能图形电路 38。

图 10B 系统可包括一个或者多个处理器，此处为了清楚仅示出了两个处理器 70、80。处理器 70、80 可包括局部存储控制中心（MCH）72、82 以连接存储器 2、4。处理器 70、80 可以使用点对点接口电路 78、88 通过点对点接口 50 交换数据。每个处理器 70、80 可以使用点对点接口电路 76、94、86、98 通过各个点对点接口 52、54 与芯片组 90 交换数据。芯片组 90 也可以通过高性能图形接口 92 与高性能图形电路 38 交换数据。

在图 10A 系统中，总线桥 32 可以允许系统总线 6 和总线 16 之间的数据交换，该总线在某些实施例中是工业标准架构（ISA）总线或者外围元件互连（PCI）总线。在图 10B 系统中，芯片组 90 可以通过总线接口 96 与总线 16 交换数据。在任一系统中，在总线 16 上可能存在各种输入/输出（I/O）装置 14，在一些实施例中该装置包括低性能图形控制器、视频控制器、以及网络控制器。在某些实施例中，另一总线桥 18 可以用于允许总线 16 和总线 20 之间的数据交换。在一些实施例中，总线 20 可以是小型计算机系统接口（SCSI）总线、集成驱动电子（IDE）总线、或者通用串行总线（USB）总线。附加的 I/O 装置可以与总线 20 连接。这些附加的 I/O 装置包括键盘和光标控制装置 22（包括鼠标）、音频 I/O 24、通信装置 26（包括调制解调器和网络接口）以及数据存储装置 28。软件代码 30 可以存储于数据存储装置 28。在某些实施例中，数据存储装置 28 可以是固定磁盘、软盘驱动器、光盘驱动器、磁光盘驱动器、磁带、或者包括闪烁存储器的非易失性存储器。

在前述说明书中，已经参照具体实施例描述了本发明。然而，在不背离由所附权利要求界定的本发明更宽范围的情况下可以进行各种改进和变化。因此说明书和附图被视为是用于说明而非限制本发明。

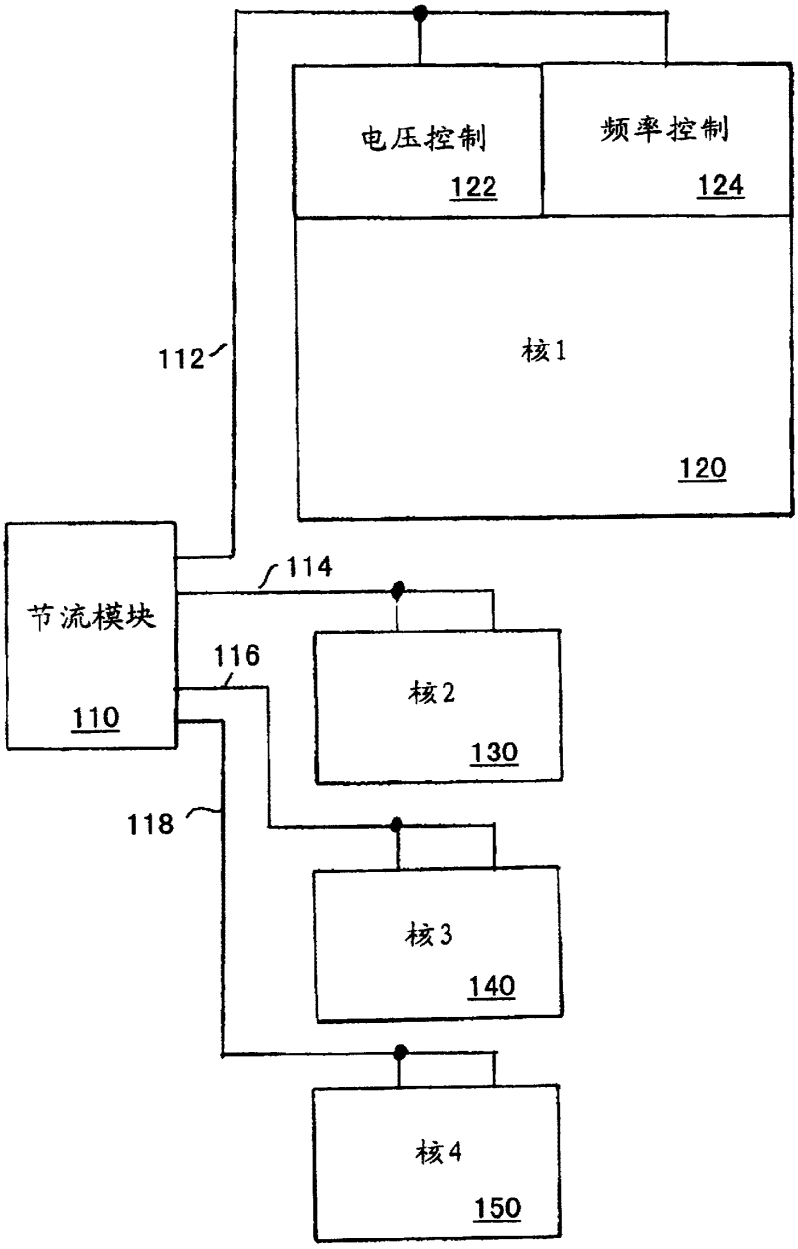


图 1

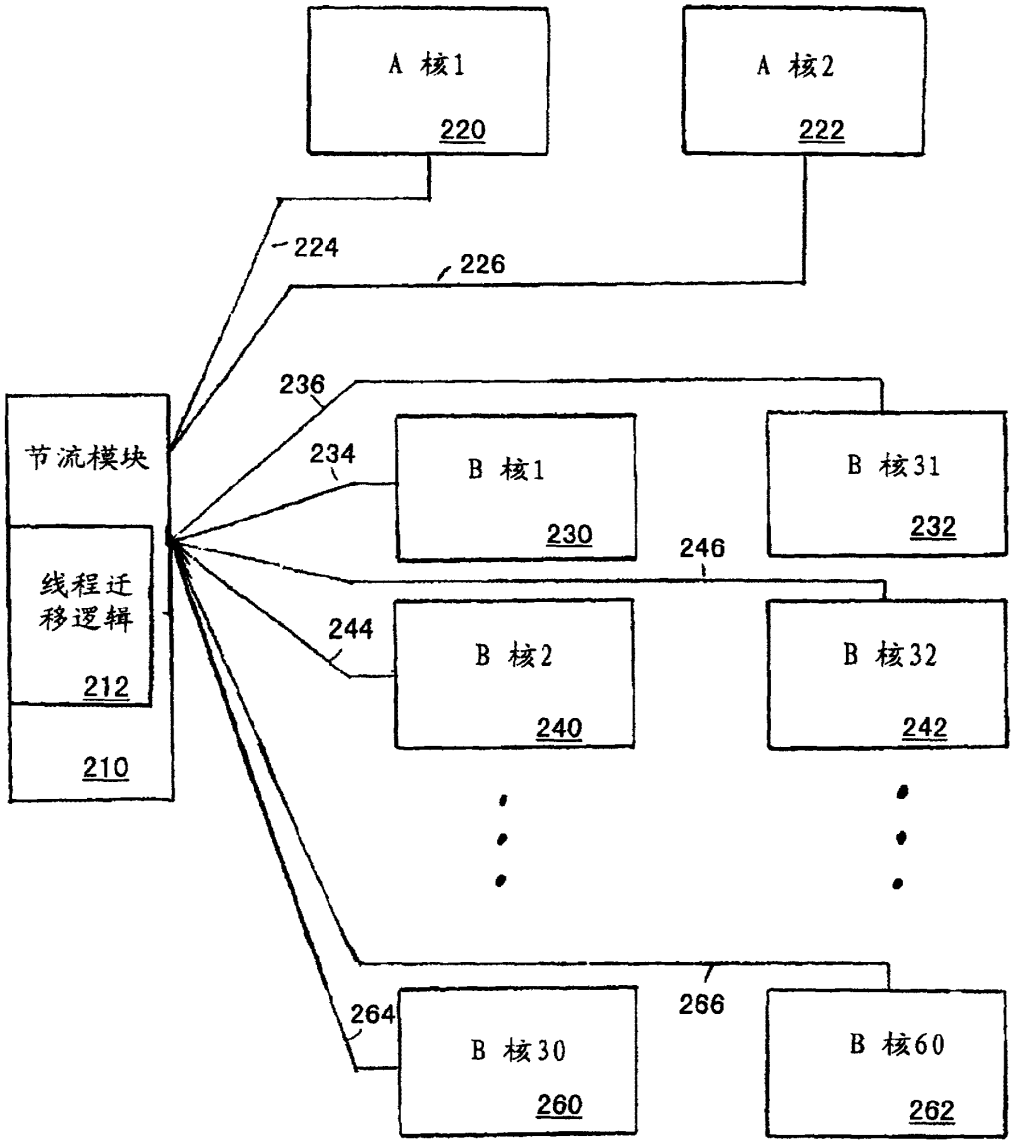


图 2

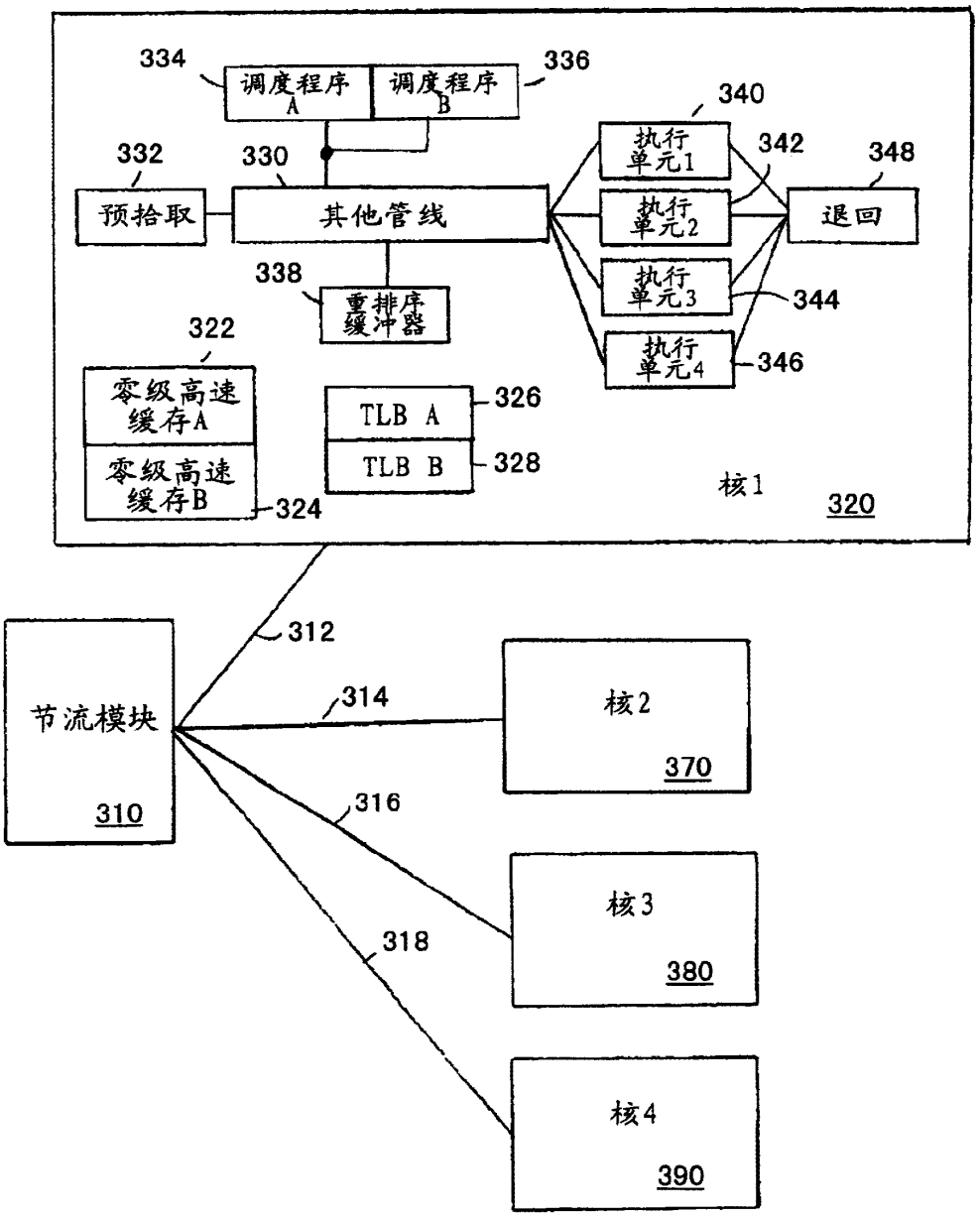


图 3

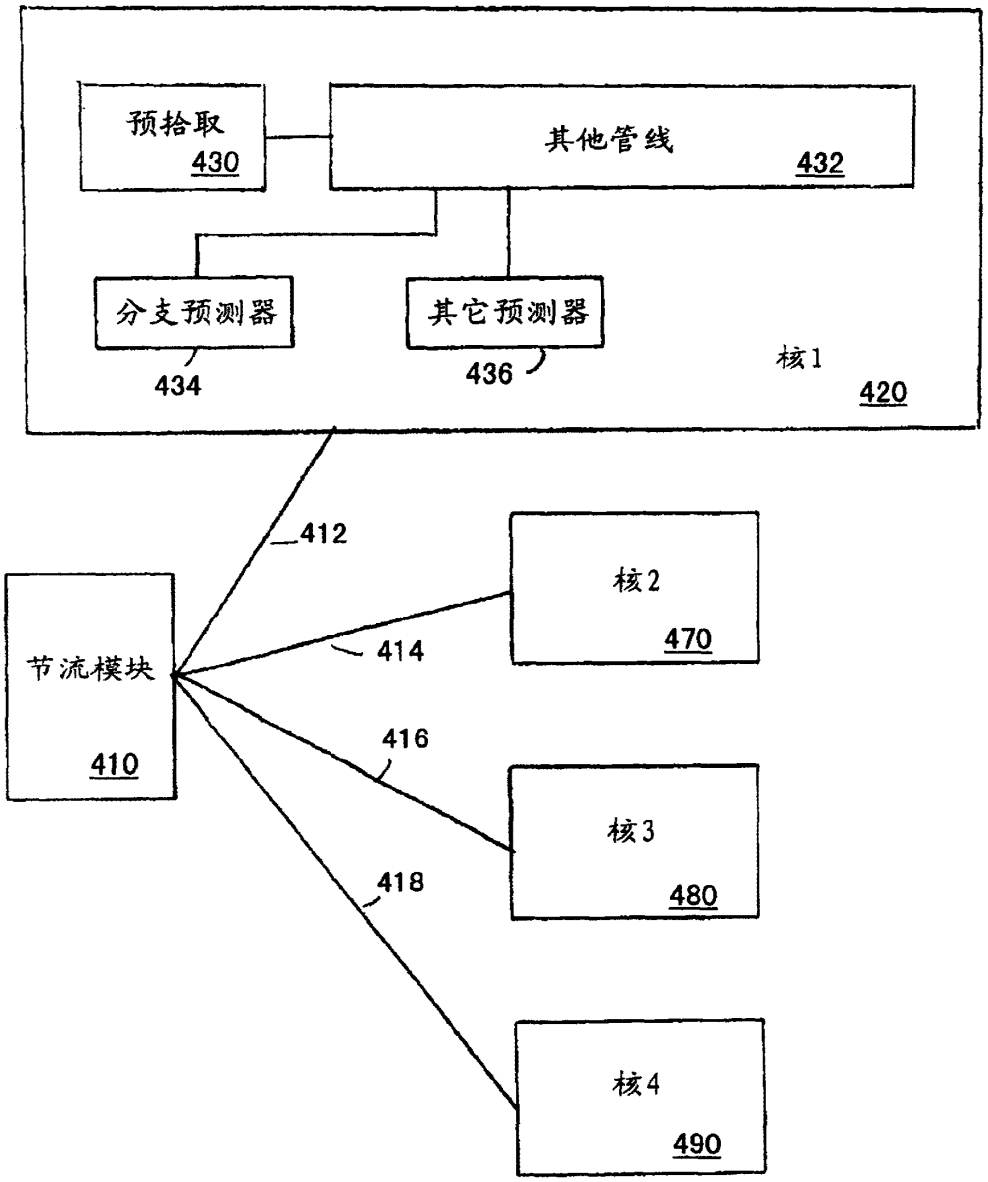


图 4

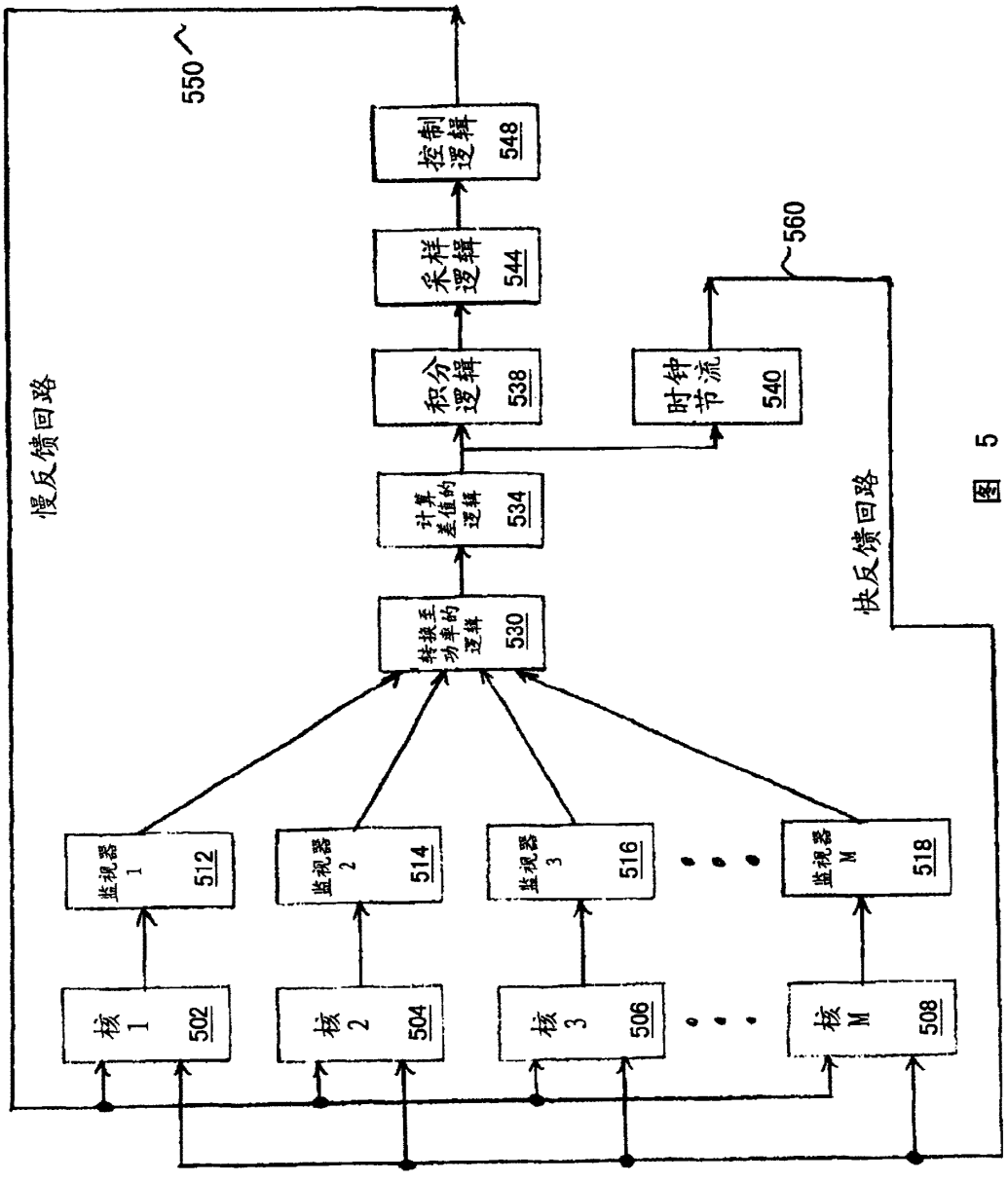


图 5

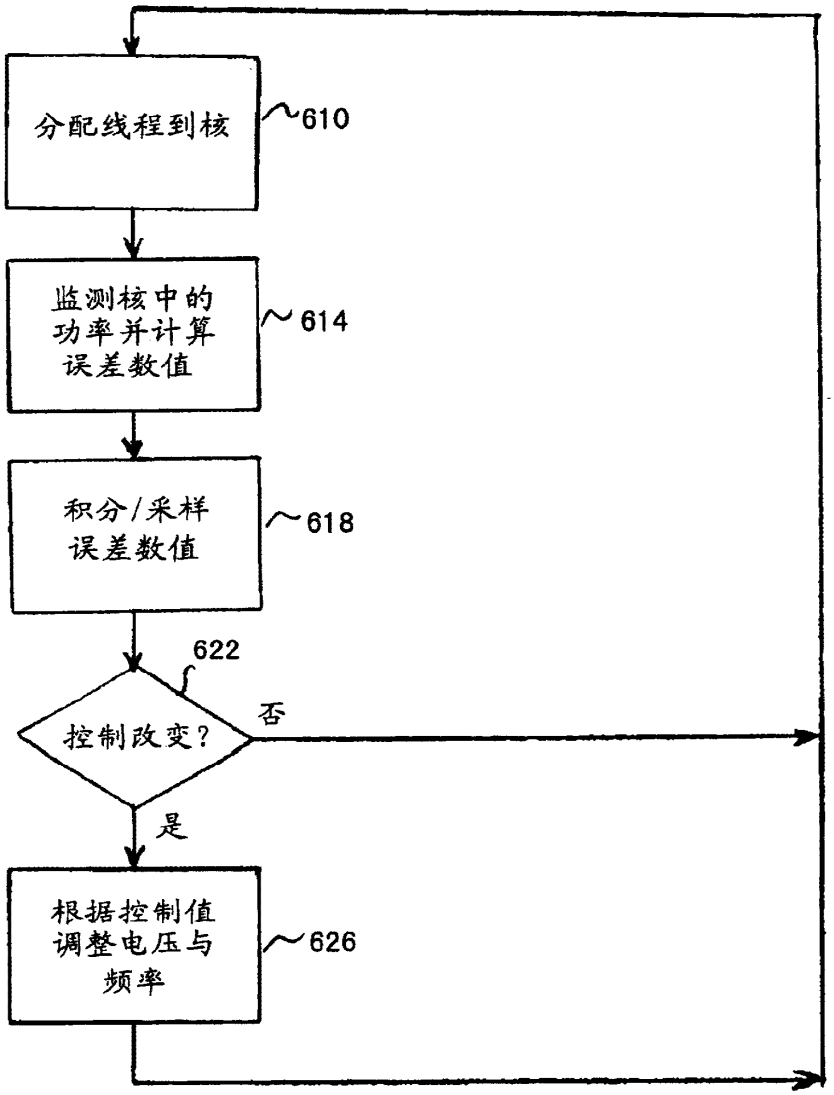


图 6

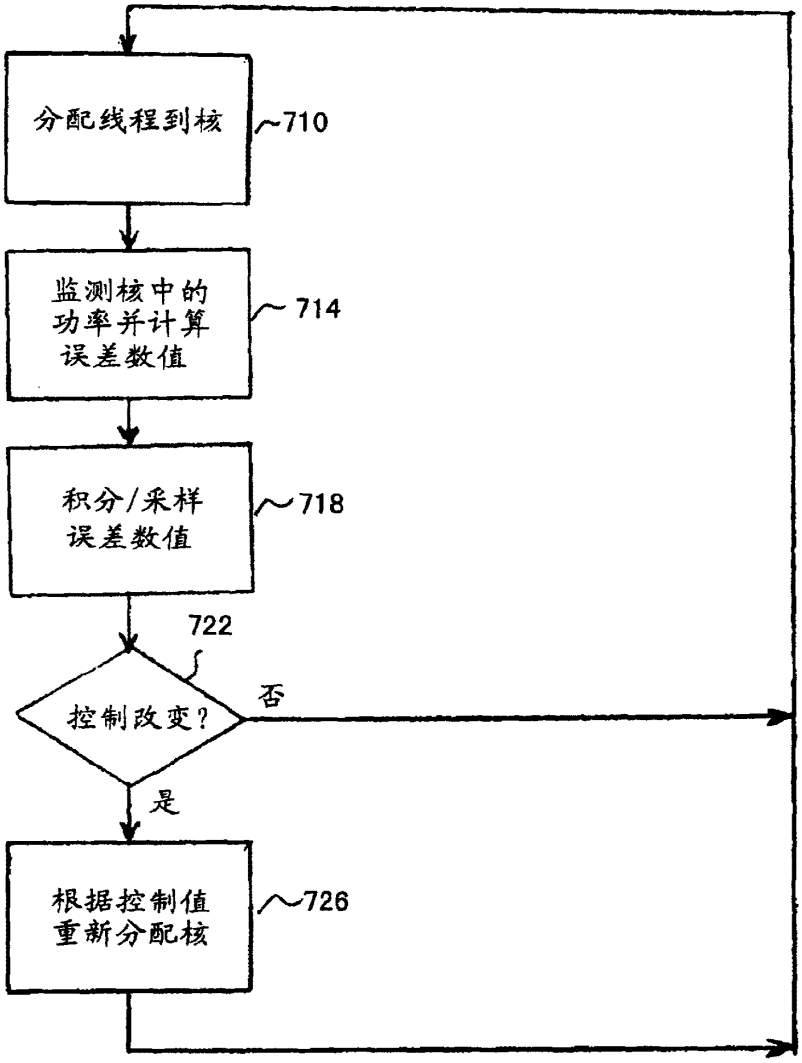


图 7

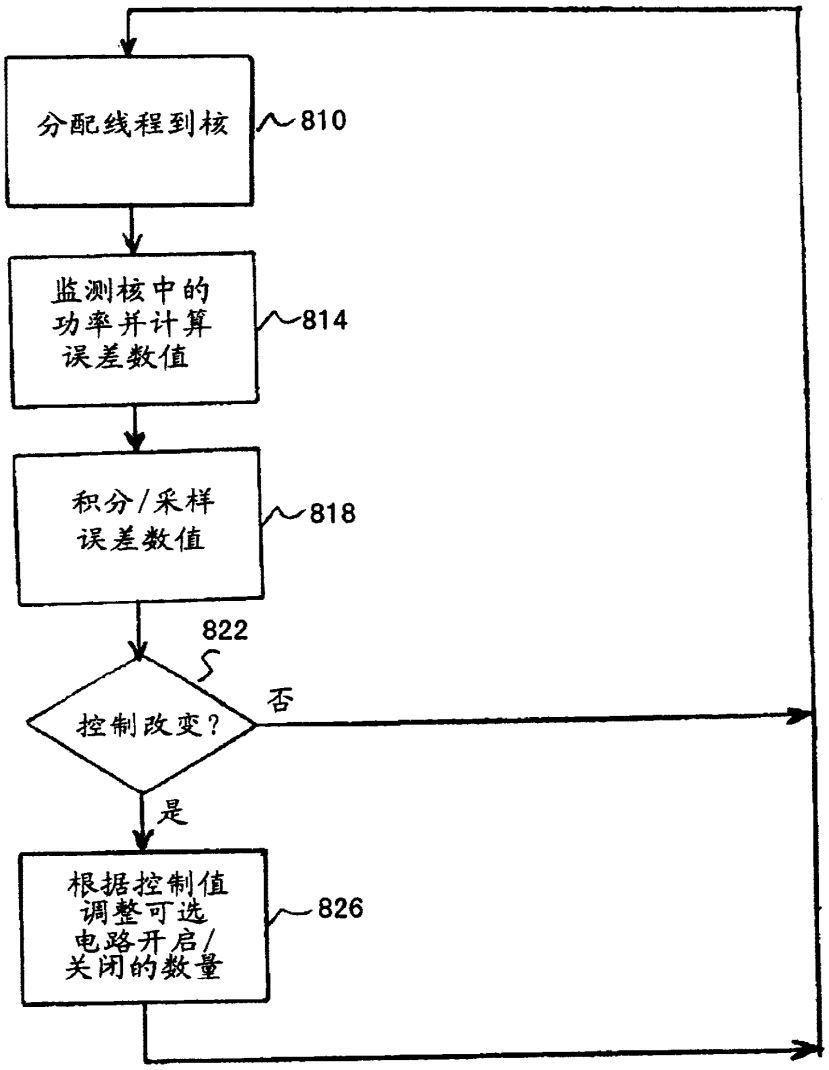


图 8

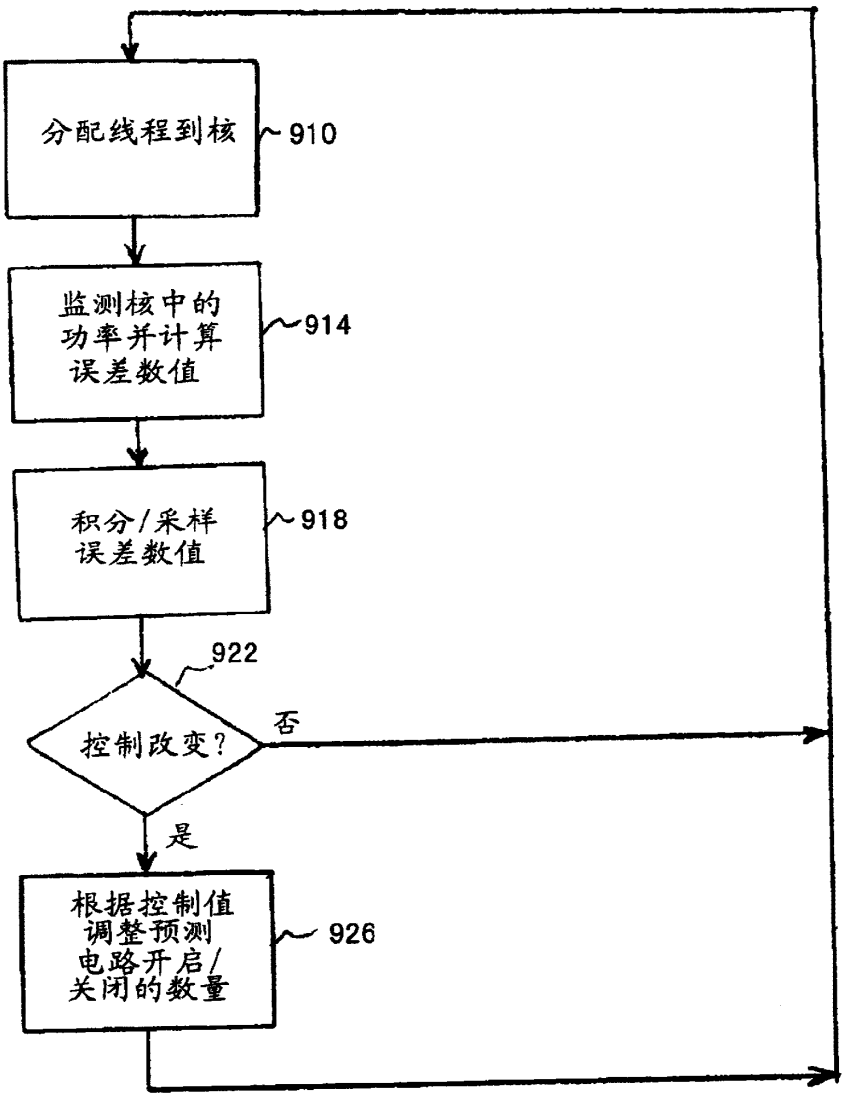


图 9

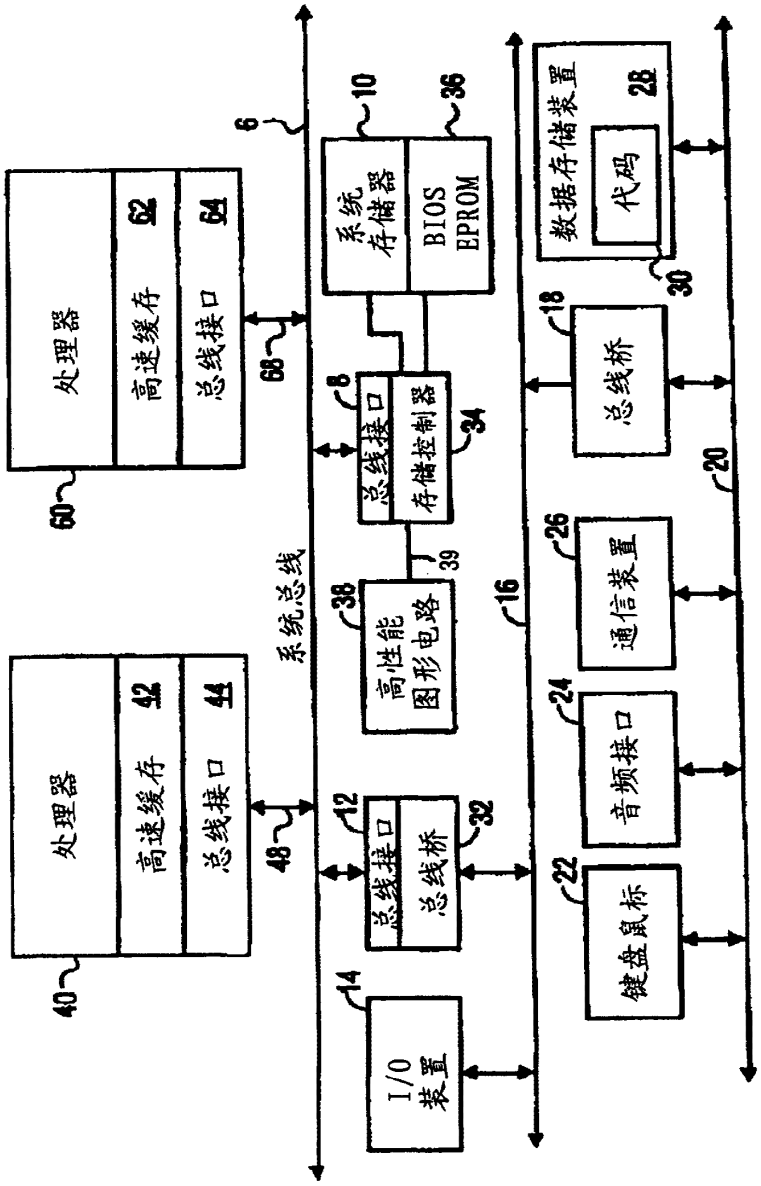


图 10A

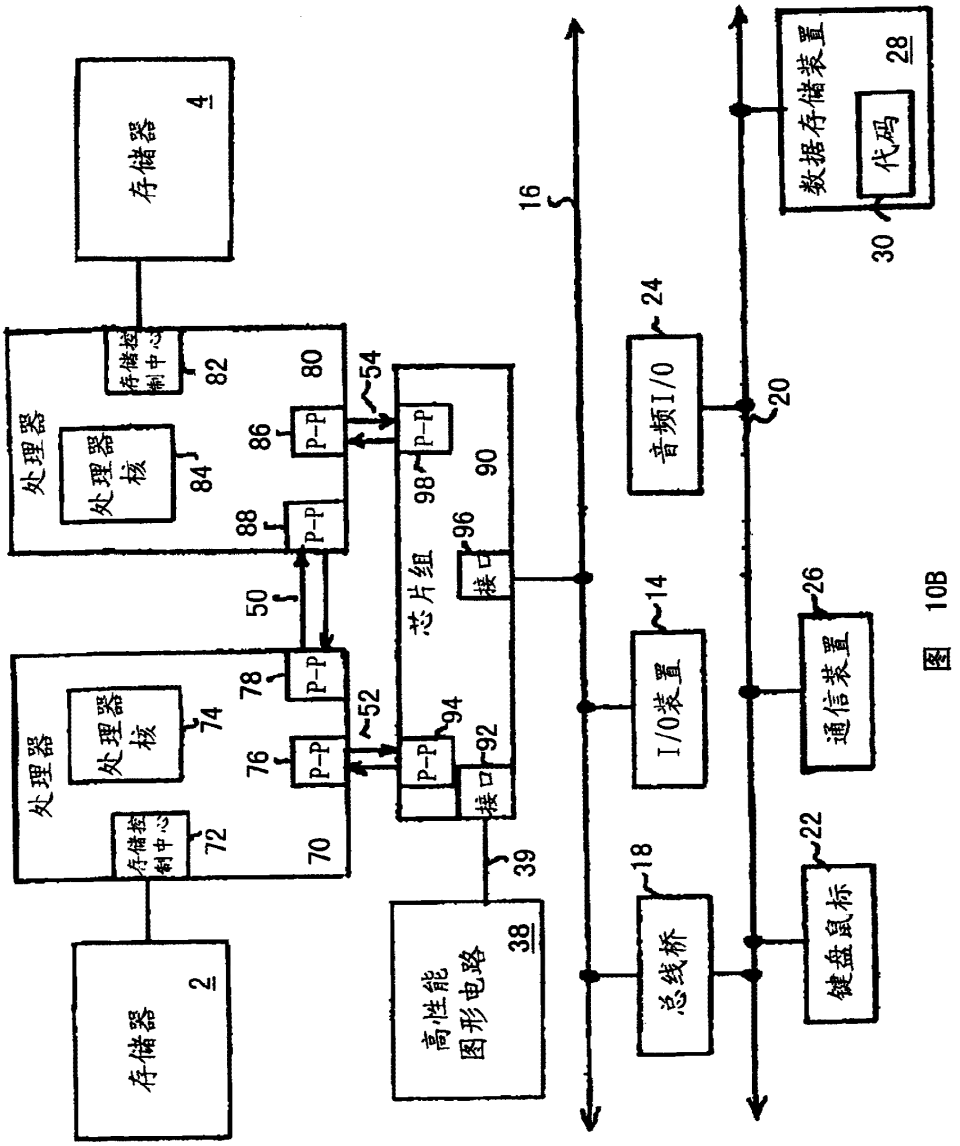


图 10B

Electronic Acknowledgement Receipt

EFS ID:	30049847
Application Number:	15431527
International Application Number:	
Confirmation Number:	4542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Customer Number:	131413
Filer:	Jonathan M Garfinkel/Amarnath S
Filer Authorized By:	Jonathan M Garfinkel
Attorney Docket Number:	42P38886C
Receipt Date:	10-AUG-2017
Filing Date:	13-FEB-2017
Time Stamp:	20:30:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	42P38886C_IDS.PDF	1054221 bc6bc77c465e1e4e7293b2e2256fdf694b079610	no	4

Warnings:

Information:					
2	Foreign Reference	CN101076770A_EFS.PDF	2228522 e1ac3d5fe444e6ce01755874238df543a90c4a4f	no	39
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3	Non Patent Literature	NPL01_FOA_US13335257_05MAY2015_13PGS_EFS.PDF	617820 07b5e94a9ba953ca753303e82c5933f9b01cd8f8	no	13
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5	Non Patent Literature	NPL03_NFOA_US13335257_12JAN2015_15PGS_EFS.PDF	704265 c5e25f69a4a7f88d1d81c49a14865ab64dee4712	no	15
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9	Non Patent Literature	NPL07_THIRD_OA_CN201280063860_15DEC2016_31PGS_EFS.PDF	3902350 5c09c65c14b6d67fe1ea4b635d342a45f06c0fa2	no	31
Warnings:					
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			Total Files Size (in bytes):	15905120	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/431,527	02/13/2017	VARGHESE GEORGE	42P38886C

CONFIRMATION NO. 4542

131413
NDWE LLP/ Intel
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

PUBLICATION NOTICE

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Title:ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

Publication No.US-2017-0154012-A1
Publication Date:06/01/2017

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Varghese George	Examiner: Eric Coleman
Application No.: 15/431,527	Art Unit: 2183
Filed: February 13, 2017	Confirmation No.: 4542
For: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE	

Mail Stop Amendment
Commissioner for Patents
e-Filed via EFS-WEB

PRELIMINARY AMENDMENT

Sir:

Prior to examination of the above-referenced application, Applicant respectfully requests the Examiner to enter the following amendments and to consider the following remarks.

CERTIFICATE OF EFS-Web

I hereby certify that this correspondence is being submitted electronically via EFS-Web on the date shown below to the United States Patent and Trademark Office.

Date of Deposit: May 17, 2017
Name of Person Mailing Correspondence: Allison Madsen
Signature: /Allison Madsen/

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.-19. (Cancelled).

20. (New) A multi-core processor comprising:

a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

21. (New) The multi-core processor of claim 20, wherein the second plurality of cores comprise logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.

22. (New) The multi-core processor of claim 20, wherein the second plurality of cores comprise logic gates that consume less power than corresponding logic gates of the first plurality of cores.

23. (New) The multi-core processor of claim 20, wherein the second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.

24. (New) The multi-core processor of claim 20, wherein the power management hardware is to disable an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lower an operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

25. (New) The multi-core processor of claim 24, wherein the power management hardware is to raise a supply voltage or an operating frequency of said one core in response to higher demand.

26. (New) The multi-core processor of claim 20, wherein the first plurality of cores are at a maximum operating frequency in the state.

27. (New) The multi-core processor of claim 20, wherein the power management hardware is to enable all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

28. (New) A method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set, wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

29. (New) The method of claim 28, wherein the operating of the second plurality of cores comprises driving logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.

30. (New) The method of claim 28, wherein the operating of the second plurality of cores comprises driving logic gates that consume less power than corresponding logic gates of the first plurality of cores.

31. (New) The method of claim 28, wherein the operating comprises operating the second plurality of cores at a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.

32. (New) The method of claim 28, further comprising disabling, with the power management hardware, an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lowering an operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

33. (New) The method of claim 32, further comprising raising, with the power management hardware, a supply voltage or an operating frequency of said one core in response to higher demand, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

34. (New) The method of claim 28, wherein the operating comprises operating the first plurality of cores at a maximum operating frequency in the state.

35. (New) The method of claim 28, further comprising enabling, with the power management hardware, all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

36. (New) A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set, wherein the second plurality of cores consume less

power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

37. (New) The non-transitory machine readable medium of claim 36, wherein the operating of the second plurality of cores comprises driving logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores.

38. (New) The non-transitory machine readable medium of claim 36, wherein the operating of the second plurality of cores comprises driving logic gates that consume less power than corresponding logic gates of the first plurality of cores.

39. (New) The non-transitory machine readable medium of claim 36, wherein the operating comprises operating the second plurality of cores at a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores.

40. (New) The non-transitory machine readable medium of claim 36, further comprising disabling, with the power management hardware, an additional core of the second plurality of cores for each continued drop in demand below a next lower threshold until one core of the second plurality of cores remains enabled, and lowering an operating frequency or a supply voltage of the one core of the second plurality of cores as demand drops below a next lower threshold.

41. (New) The non-transitory machine readable medium of claim 40, further comprising raising, with the power management hardware, a supply voltage or an operating frequency of said one core in response to higher demand, wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand.

42. (New) The non-transitory machine readable medium of claim 36, wherein the operating comprises operating the first plurality of cores at a maximum operating frequency in the state.

43. (New) The non-transitory machine readable medium of claim 36, further comprising enabling, with the power management hardware, all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

REMARKS

Consideration of this application as amended is respectfully requested. The Examiner is invited to call Scott A. Simmons at (408) 675-0441 with any questions or comments. Authorization is hereby given to charge our Deposit Account No. 504238 for any charges that may be due.

Respectfully submitted,
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP

Date: May 17, 2017

/Scott A. Simmons/
Scott A. Simmons
Reg. No.: 60,206

99 Almaden Blvd, Ste 710
San Jose, Ca 95113
408-675-0441

Electronic Patent Application Fee Transmittal

Application Number:	15431527
Filing Date:	13-Feb-2017
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Filer:	Scott Alan Simmons/Allison Madsen
Attorney Docket Number:	42P38886C

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	4	80	320
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**320**

Electronic Acknowledgement Receipt	
EFS ID:	29242285
Application Number:	15431527
International Application Number:	
Confirmation Number:	4542
Title of Invention:	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Customer Number:	131413
Filer:	Scott Alan Simmons/Allison Madsen
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886C
Receipt Date:	17-MAY-2017
Filing Date:	13-FEB-2017
Time Stamp:	20:21:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$320
RAM confirmation Number	051817INTEFSW00007246504238
Deposit Account	504238
Authorized User	Allison Madsen
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38886C_Preliminary_Amendment.pdf	37751 dafd3b9c1268b080bf8e30c1bcc424927f579665	yes	7

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	6
Applicant Arguments/Remarks Made in an Amendment	7	7

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30354 e23e28cf43506b5800e8058b124368000c192b9e	no	2

Warnings:

Information:

Total Files Size (in bytes):	68105

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/431,527	Filing Date 02/13/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	**280**
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	**280**

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	**05/17/2017**	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 20	= 4	X $80 =	320
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**320**

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
GLORIA J. TRAMMELL

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/431,527	02/13/2017		1740	42P38886C	19	3

CONFIRMATION NO. 4542

131413
NDWE LLP/ Intel
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

FILING RECEIPT

OC000000089386347

Date Mailed: 02/23/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

VARGHESE GEORGE, Folsom, CA;
SANJEEV S. JAHAGIRDAR, Folsom, CA;
DEBORAH T. MARR, Portland, OR;

Applicant(s)

Intel Corporation, Santa Clara, CA;

Power of Attorney: The patent practitioners associated with Customer Number 131413

Domestic Priority data as claimed by applicant

This application is a CON of 13/335,257 12/22/2011 PAT 9569278

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/22/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/431,527**

Projected Publication Date: 06/01/2017

Non-Publication Request: No

Early Publication Request: No
Title

ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/431,527	02/13/2017	VARGHESE GEORGE	42P38886C

CONFIRMATION NO. 4542

131413
NDWE LLP/ Intel
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

INFORMAL NOTICE

OC000000089386348

Date Mailed: 02/23/2017

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  VARGHESE GEORGE
  SANJEEV S. JAHAGIRDAR
  DEBORAH T. MARR

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sibrahim/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/431,527

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 131413

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

INTEL CORPORATION

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/Kerry D. Tweet/	Date (Optional)	September 23, 2016
Name	Kerry D. Tweet		
Title	Assistant Director of Patents, Intel Corporation		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Intel Corporation

Application No./Patent No.: To be assigned Filed/Issue Date: Herewith

Titled: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

Intel Corporation, a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 028046, Frame 0420, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Scott A. Simmons/	February 13, 2017
Signature	Date
Scott A. Simmons	60,206
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (03-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Varghese George
Art Unit	
Examiner Name	
Attorney Docket Number	42P38886C

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7992020	B1	2011-08-02	Tuan Tim et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090328055	A1	2009-12-31	Bose et al.	
	2	20080127192	A1	2008-05-29	Capps et al.	
	3	20090271646	A1	2009-10-29	Talwar et al.	
	4	20090307512	A1	2009-12-10	Munjal et al.	
	5	20090055826	A1	2009-02-26	Bernstein et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Varghese George
	Art Unit	
	Examiner Name	
	Attorney Docket Number	42P38886C

	6	20100131781	A1	2010-05-27	Memon et al.	
	7	20110239015	A1	2011-09-29	Boyd et al.	
	8	20110252260	A1	2011-10-13	Flachs et al.	
	9	20120117403	A1	2012-05-10	Bieswanger et al.	
	10	20060095807	A1	2006-05-04	Grochowski et al.	
	11	20080288748	A1	2008-11-20	Sutardja et al.	
	12	20100153954	A1	2010-06-17	Morrow et al.	
	13	20060282692	A1	2006-12-14	Oh	
	14	20100083011	A1	2010-04-01	Onouchi Masafumi et al.	
	15	20100058086	A1	2010-03-04	Lee Wan Yeon	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Varghese George
	Art Unit	
	Examiner Name	
	Attorney Docket Number	42P38886C

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Copy of Notice of Allowance from TW counterpart Application No. 101147200, (Atty. Docket No. 42P38886TW), mailed September 29, 2014, 1 page.	
	2	Aruj, Ori. "Evolution: 20 years of switching Fabric", September 2008. EE Times. Retrieved from http://www.eetimes.com/document.asp?doc_id=1272140.	
	3	PCT International Search Report for PCT Counterpart Application No. PCT/US2012/068274, 5 pgs., (February 22, 2013).	
	4	PCT Written Opinion of the International Searching Authority for PCT Counterpart Application No. PCT/US2012/068274, 6 pgs., (February 22, 2013).	
	5	PCT Notification Concerning Transmittal of Copy of International Preliminary Report on Patentability (Chapter I of the Patent Cooperation Treaty) for PCT Counterpart Application No. PCT/US2012/068274, 8 pgs., (July 03, 2014).	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Varghese George
	Art Unit	
	Examiner Name	
	Attorney Docket Number	42P38886C

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Varghese George
	Art Unit	
	Examiner Name	
	Attorney Docket Number	42P38886C

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott A. Simmons/	Date (YYYY-MM-DD)	2017-02-13
Name/Print	Scott A. Simmons	Registration Number	60,206

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Varghese George et al. Application No. To be assigned Filed: Herewith For: ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE	Examiner: To be assigned Art Unit: To be assigned Confirmation No. To be assigned

Commissioner for Patents
E-FILED VIA EFS-WEB

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicant hereby request consideration of the enclosed Information Disclosure Statement pursuant to 37 C.F.R. § 1.97(c).

Initialed PTO Forms 1449 and Forms 892 from the parent application can be found in U.S. Patent Application No. 13/335,257, filed on December 22, 2011. This previous application is relied upon for an earlier filing date under 35 U.S.C. 120.

Pursuant to C.F.R. 1.98(d), copies of the references are not being provided herewith since they were previously sent to the patent and Trademark Office. Please consider these cited documents in the currently pending 1.53(b) continuation application filed herewith on February 13, 2017.

CERTIFICATE OF EFS Web

I hereby certify that this correspondence is being submitted electronically via EFS-Web on the date shown below to the United States Patent and Trademark Office.

Date of Deposit: February 13, 2017
Name of Person Mailing Correspondence: Allison Madsen
Signature: /Allison Madsen/

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability. If there are any deficiency in fees, please charge Deposit Account No. 504238.

Respectfully submitted,
NICHOLSON, DE VOS, WEBSTER, & ELLIOTT, LLP

Date: February 13, 2017 /Scott A. Simmons/
Scott A. Simmons
Reg. No.: 60,206

217 High Street
Palo Alto, CA 94301
408-675-0441

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Filer:	Scott Alan Simmons/Allison Madsen
Attorney Docket Number:	42P38886C

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	140	140
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1740**

Electronic Acknowledgement Receipt	
EFS ID:	28343293
Application Number:	15431527
International Application Number:	
Confirmation Number:	4542
Title of Invention:	AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE
First Named Inventor/Applicant Name:	VARGHESE GEORGE
Customer Number:	131413
Filer:	Scott Alan Simmons/Allison Madsen
Filer Authorized By:	Scott Alan Simmons
Attorney Docket Number:	42P38886C
Receipt Date:	13-FEB-2017
Filing Date:	
Time Stamp:	18:36:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1740
RAM confirmation Number	021417INTEFSW00005775504238
Deposit Account	504238
Authorized User	Allison Madsen
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	P38886_ADS_FINAL.pdf	1823059 8d8f341147423e37bc25c6d16fb236079ec83d69	no	9
Warnings:					
Information:					
2		P38886C_Appln_FINAL.pdf	83860 53a24e9e242cc8724d838c46ec042ccda5bac7d4	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Abstract	16	16
	Claims	13	15
	Sequence Listing	1	12

Warnings:					
Information:					
3	Drawings-only black and white line drawings	P38886C_Figures_FINAL.pdf	1322201 12f507a8dabe295240b50c3b11b261096c9107ed	no	8
Warnings:					
Information:					
4	Power of Attorney	GENERAL_POA_POST_AIA.pdf	1005483 72613581efca2639e9954365f5e287717265fc29	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					

5	Assignee showing of ownership per 37 CFR 3.73	P38886_373c_aia0096.pdf	118904 b92e530790ee1f5ec1f2cd9c7291db3da5e3385e	no	3
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Form (SB08)	P38886C_IDS_FINAL.pdf	1035943 18e1adc253414c5a1b79a24ebbb4f5a45e233123	no	6
Warnings:					
Information:					
7	Transmittal Letter	P38886C_IDS_Under198d.pdf	18184 d8f19c3157a703394dc235e561446fe5a054165e	no	2
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	36570 20816376474b89ee155d0316b6d14f9ccd5fb462	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	5444204		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	42P38886C
	Application Number	
Title of Invention	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	VARGHESE		GEORGE	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Folsom	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	1113 Halidon way		
Address 2			
City	Folsom	State/Province	CA
Postal Code	95630	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	SANJEEV	S.	JAHAGIRDAR	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Folsom	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	116 Foley Lane		
Address 2			
City	Folsom	State/Province	CA
Postal Code	95630	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	DEBORAH	T.	MARR	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	42P38886C
	Application Number	
Title of Invention	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE	

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	2564 NW Pettygrove St		
Address 2			
City	Portland	State/Province	OR
Postal Code	97210	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	131413		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE		
Attorney Docket Number	42P38886C	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	42P38886C
	Application Number	
Title of Invention	ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE	

Representative Information:

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	13335257	2011-12-22

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

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● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Intel Corporation		
Mailing Address Information For Applicant:			
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Phone Number		Fax Number	
Email Address			

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Assignee Information including Non-Applicant Assignee Information:

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See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Scott A. Simmons/			Date (YYYY-MM-DD)	2017-02-13
First Name	Scott A.	Last Name	Simmons	Registration Number	60,206

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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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ABSTRACT

A method is described that entails operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency.

CLAIMS

What is claimed is:

1. A multi-core processor comprising a plurality of cores that support a same instruction set, where, at least one of the cores is constructed of logic gates that consume less power, for a same applied operating frequency and supply voltage, than the same corresponding logic gates of at least one other of the cores.

2. The multi-core processor of claim 1 wherein the logic gates that consume less power have narrower logic gate driver transistors than the same corresponding logic gates of the at least one other of the cores.

3. The multi-core processor of claim 1 wherein there are at least two cores that are constructed of the logic gates that consume less power.

4. The multi-core processor of claim 1 wherein only one of the cores is constructed of the logic gates that consume less power.

5. The multi-core processor of claim 1 further comprising a switch fabric between the cores and a system memory interface.

6. A method, comprising:

operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency.

7. The method of claim 6 further comprising:

disabling the first core but leaving the second core operable in response to lower demand being offered to the multi-core processor.

8. The method of claim 7 further comprising enabling the first core after it is disabled in response to higher demand being offered to the multi-core processor.

9. The method of claim 8 wherein said method further comprises:

disabling said first core after detecting a first drop in demand offered to said multi-core processor;

enabling said first core after detecting a first rise in demand offered to said multi-core processor, the amount of demand associated with said first drop being greater than the amount of demand associated with said second drop.

10. The method of claim 6 wherein the operating of the first core includes driving load lines with wider transistor widths than corresponding transistor widths in said second core.

11. The method of claim 6 further comprising lowering a supply voltage and/or operating frequency of said first core in response to lower demand being offered to said multi-core processor.

12. The method of claim 6 further comprising raising a supply voltage and/or operating frequency of said first core in response to higher demand being offered to said multi-core processor.

13. The method of claim 6 further comprising:

disabling said first core in response to a drop in demand applied to said multi-core processor; and,

lowering a supply voltage and/or operating frequency of said second core in response to an additional drop in demand applied to said multi-core processor.

14. A machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising:

operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency;

disabling the first core but leaving the second core operable in response to lower demand being offered to the multi-core processor;

15. The machine readable medium of claim 14 wherein said method further comprises enabling the first core after it is disabled in response to higher demand being offered to the multi-core processor.

16. The machine readable medium of claim 15 wherein said method further comprises:

disabling said first core after detecting a first drop in demand offered to said multi-core processor;

enabling said first core after detecting a first rise in demand offered to said multi-core processor, the amount of demand associated with said first drop being greater than the amount of demand associated with said second drop.

17. The machine readable medium of claim 14 wherein said method further comprises lowering a supply voltage and/or operating frequency of said first core in response to lower demand being offered to said multi-core processor.

18. The machine readable medium of claim 14 wherein said method further comprises raising a supply voltage and/or operating frequency of said first core in response to higher demand being offered to said multi-core processor.

19. The machine readable medium of claim 14 wherein said method further comprises:

disabling said first core in response to a drop in demand applied to said multi-core processor; and,

lowering a supply voltage and/or operating frequency of said second core in response to an additional drop in demand applied to said multi-core processor.

UNITED STATES PATENT APPLICATION

For

AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

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Attorney's Docket No. 42P38886C

AN ASYMMETRIC PERFORMANCE MULTICORE ARCHITECTURE WITH SAME INSTRUCTION SET ARCHITECTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present patent application is a continuation application claiming priority from U.S. Patent Application No. 13/335,257, filed December 22, 2011, and titled: "Asymmetric Performance Multicore Architecture with Same Instruction Set Architecture", which is incorporated herein by reference in its entirety.

BACKGROUND

Field of Invention

[0002] The field of invention relates generally to computing system architecture, and, more specifically, to an asymmetric performance multicore architecture with same instruction set architecture (ISA).

Background

[0003] Fig. 1 shows a typical multi-core processor 100_1. As observed in Fig. 1, the multi-core processor 100_1 includes a plurality of processor cores 101_1 to 101_N on a same semiconductor die 100_1. Each of the processor cores typically contain at least one caching layer for caching data and/or instructions. A switch fabric 102 interconnects the processor cores 101_1 to 101_N to one another and to one or more additional caching layers 103_1 to 103_N. According to one approach, the processors 101_1 to 101_N and the one or more caching layers have internal coherency logic to, for example, prevent two different cores from concurrently modifying the same item of data.

[0004] A system memory interface (which may also include additional coherency logic) 104 is also included. Here, if a core requests a specific cache line having a needed instruction or item of data, and, the cache line is not found in any of the caching layers, the request is presented to the system memory interface 104. If the looked for cache line is not in the system memory 105_1 that is directly coupled to interface 104, the request is forwarded through system network interface 106 to another multi-core processor to fetch the desired data/instruction from its local system memory (e.g., system memory 105_X of multi-core processor 100_X). A packet switched network 107 exists between the multi-processor cores 100_1 to 100_X to support these kinds of system memory requests.

[0005] Interfaces to system I/O components 108_1 to 108_Y (e.g., deep non volatile storage such as a hard disk drive, printers, external network interfaces, etc.) are also included on the

multi-processor core. These interfaces may take the form of high speed link interfaces such as high speed Ethernet interfaces and/or high speed PCIe interfaces.

[0006] Some multi core processors may also have a port 105 to the switch fabric 102 to scale upwards the number of processor cores associated with a same (also scaled upward) caching structure. For example, as observed Fig. 1, multi-processor cores 101_1 and 101_2 are coupled through the switch fabric port 105 to effectively form a platform of 2N cores that share a common caching structure (processor 100_2 is coupled to processor 100_1 through a similar port to its switch fabric).

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

[0008] Figure 1 shows a multicore processor and surrounding computer system (prior art);

[0009] Figure 2 shows a power management strategy (prior art);

[0010] Figure 3 shows a logic gate drive circuit;

[0011] Figure 4 shows multi core processor having high power and low power cores that support the same instruction set;

[0012] Figure 5 compares power consumption of a high power core and low power core;

[0013] Figure 6 shows a first power management method;

[0014] Figure 7 shows a second power management method;

[0015] Figure 8 shows a design method.

DETAILED DESCRIPTION

Overview

Detailed Description

[0016] Computing system power consumption is becoming more and more of a concern. As such, a number of different power management schemes are incorporated into modern day computing systems. Typically, the power management component of the system will scale up the processing performance of the system as the system's workload increases, and, scale down the processing performance of the system as the system's workload decreases. Decreasing the processing performance of the system corresponds to power savings as the power consumption of the system is strongly correlated with its performance capabilities.

[0017] A typical way to scale processing performance and power consumption with workload is to enable/disable entire cores and raise/lower their supply voltages and operating frequencies in response to system workload. For example, as observed in Fig. 2, under a maximum performance and power consumption state 201 all cores are enabled and each core is provided with a maximum supply voltage and maximum clock frequency. By contrast, under a minimum performance and power consumption state 202 (at which program code can still be executed), only one core is enabled. The single core is provided with a minimum supply voltage and minimum operating frequency.

[0018] Some basic concepts of electronic circuit power consumption are observed in Fig. 3. Here, the driver circuit 310 portion of a logic gate 311 is observed driving a next one or more logic gate(s) 312. Specifically, the speed of operation of interconnected logic gates 311, 312 rises as the width of its driving transistors 302_1, 302_2 (measured, for each transistor, along the semiconductor surface perpendicular to the direction of current flow) increase and the capacitance 303 of the line 304 (and input capacitance of the load logic gate(s) 312) it is driving decreases. Here, in order to raise the voltage on the line from a logic low level to a logic high level, a sufficiently strong current 305 needs to be driven by the source transistor 302_1 through the line to rapidly apply charge to the capacitance 303 (and thereby raise the voltage on the line). Similarly, in order to lower the voltage on the line from a logic high level to a logic low level, a sufficiently strong current 306 needs to be "sunk" by the sink transistor 302_2 through the line to rapidly draw charge off the capacitance (and thereby lower the voltage on the line).

[0019] Essentially, the amount of current the transistors 302_1, 302_2 will source/sink is a function of their respective widths. That is, the wider the transistors are, the more current they will source/sink. Moreover, the amount of current the transistors 302_1, 302_2 will source/sink

is also a function of the supply voltage VCC that is applied to the driver circuit 310 observed in Fig. 3. Essentially, the higher the supply voltage, the stronger the source/sink currents will be.

[0020] Further still, the rate at which the transistors will be able to apply/draw charge to/from the capacitor is a function of the size of the capacitance 303 of the line 304 being driven. Specifically, the transistors will apply/draw charge slower as the capacitance 304 increases and apply/draw charge faster as the capacitance 304 decreases. The capacitance 304 of the line is based on its physical dimensions. That is, the capacitance 304 increases the longer and wider the line, and by contrast, the capacitance 304 decreases the shorter and narrower the line is. The line itself is of fixed dimensions once the circuit is manufactured. Nevertheless, line width and line length are design parameters that designers must account for. The width of the line cannot be narrowed too much or else it will have the effect of increasing the line's resistance which will also slow down the rate of charge applied/drawn to/from the capacitor.

[0021] A final speed factor is the frequency of the signal itself on the line. Essentially, circuits driven with a faster clock signal will more rapidly switch between applying and drawing charge to/from the line capacitance 304 than circuits with a slower clock signal. Here, more rapid switching corresponds to a circuit that is sending binary information faster.

[0022] All of the factors described above for increasing the rate at which the charge on the capacitor is applied/drawn also lead to a circuit that consumes more power. That is, a circuit that is designed to have relatively wide source/sink transistors, a high supply voltage, short load lines and receive a higher frequency clock signal will operate faster and therefore consume more power than circuits oppositely oriented as to these same parameters.

[0023] Recalling the discussion of Figs. 1 and 2, note that prior art multi core processor power management schemes have been implemented on processors whose constituent cores are identical. That is, referring to Fig. 1, all of cores 101_1 to 101_N are identical in design. In other approaches, the cores are not identical but are radically different. Specifically, one of the cores is a low power core but the lower power characteristic is achieved by stripping out sizable chunks of logic circuitry as compared to the other cores. More specifically, the sizable chunks that are stripped out correspond to the logic that executes the program code instructions. Said another way, the low power core supports a reduced instruction set as compared to the higher performance cores. A problem with this approach, however, is that it is difficult for system software to adjust switch operation between processor cores having different instruction sets.

[0024] Fig. 4 depicts a new approach in which at least one of the cores 401 is designed to be lower performance and therefore consume less power than other cores 402 in the processer. However, the lower power core(s) 401 has a same logic design as the higher power core(s) 402

and therefore supports the same instruction set 403 as the high power core(s) 402. The low power core(s) 401 achieve a lower power design point by having narrower drive transistor widths than the higher power core(s) and/or having other power consumption related design features, such as any of those discussed above with respect to Fig. 3, that are oppositely oriented than the same design features in the higher power cores.

[0025] According to one approach, discussed in more detail below, when the multi-processor core is being designed, the same high level description (e.g., the same VHDL or Verilog description) is used for both the higher performance/power core(s) and the lower performance/power core(s). When the higher level descriptions are synthesized into RTL netlists, however, for the subsequent synthesis from an RTL netlist into a transistor level netlist, different technology libraries are used for the low power core(s) than the high power core(s). As alluded to above, the drive transistors of logic gates associated with the libraries used for the low power core(s) have narrower respective widths than the "same" transistors of the "same" logic gates associated with the libraries used for the high power cores.

[0026] By design of the multiprocessor, referring to Fig. 5, the lower power core(s) exhibit inherently lower power consumption (and processing performance) than the higher power core(s). That is, for a same applied clock or operating frequency, because of its narrower drive transistor widths, for example, a lower power core will consume less power than a higher power core. Because of the narrower drive transistor widths, however, the lower power core has a maximum operating frequency that is less than the maximum operating frequency of the higher power core.

[0027] The import of the lower power core, however, is that the multi-processor is able to entertain a power management strategy that is the same/similar to already existing power management strategies, yet, still achieve an even lower power consumption in the lower/lowest performance/power states. Specifically, recall briefly power state 202 of Fig. 2 in which only one core is left operable (the remaining cores are disabled). Here, if the one remaining operable core is the low power core, the processor will exhibit even lower power consumption than the prior art low power state 202.

[0028] The amount of reduced power savings 503 is directly observable in Fig. 5. Here, recall that all the processors were identical in the multi-processor that was discussed with respect to the prior art low power state 202 of Fig. 2. As such, even if the supply voltage and operating voltage was reduced to a minimum, the power consumption would be that of a higher power processor (e.g., having wider drive transistor widths). This operating point is represented by point 504 of Fig. 5. By contrast, in the lowest power operating state of the improved multi-processor, if the

operable core is a low power core it will consume power represented by point 505 of Fig. 5. As such, the improved processor exhibits comparatively lower power consumption at the lower/lowest performance operating states than the prior art multi-processor, while, at the same time, fully supporting the instruction set architecture the software is designed to operate on.

[0029] Fig. 6 shows a power management process flow that can be executed, for example, with power management software that is running on the multi-processor (or another multi-processor or separate controller, etc.). Conversely, the power management process flow of Fig. 6 can be executed entirely in hardware on the multi-processor or by some combination of such hardware and software.

[0030] According to the process flow of Fig. 6, from an initial state 601 where at least some high power processor cores and the low power core(s) are operating, in response to a continued drop in demand on the multi-processor, another high power core is disabled each time the continued drop in demand falls below some next lower threshold. For example, in a multi-processor core having sixteen cores where fourteen cores are high power cores and two cores are low power cores, the initial state 601 may correspond to a state where seven of the high power cores and both of the low power cores are operational.

[0031] In response to continued lower demand placed on the multi-processor, the seven high power cores will be disabled one by one with each new lower demand threshold 602. For instance, as observed at inset 610, demand level 611 justifies enablement of the seven high power cores and both low power cores. As the demand continually drops to a next lower threshold 612, one of the high power cores is disabled 613 leaving six operable high power cores and two low power cores.

[0032] Before the high power core is disabled, as a matter of designer choice, the core's individual operating frequency, or the operating frequency of all (or some of) the enabled high power cores, or the operating frequency of all (or some of) the enabled high power cores and the low power cores may be lowered to one or more lower operating frequency levels.

[0033] A similar designer choice exists with respect to the supply voltages applied to the cores. That is, before the high power core is disabled, as a matter of designer choice, the core's individual supply voltage, or the supply voltage of all (or some of) the enabled high power cores, or the supply voltage of all (or some of) the enabled high power cores and the low power cores may be lowered to one or more lower supply voltages. Supply voltages may be lowered in conjunction with the lowering of operating frequency, or, just one or none of these parameters may be lowered as described above.

[0034] Eventually, with the continued drop in demand, the last remaining high power core will be disabled 615 after demand falls below some lower threshold 614. This leaves only the low power cores in operation. Operating frequency and/or supply voltage of the low power core(s) may likewise be lowered as demand continues to drop beneath level 614. With continued drop in demand a similar process of disabling cores as demand falls below each next lower demand threshold 604 continues until the multi-processor core is left with only one low power core remaining as its sole operating core 606.

[0035] State 606 is reached of course with the disablement of the last high power core in implementations where the processor only has one lower power core. Again supply voltage and/or operating frequency of the sole remaining low power core may be lowered as demand continues to fall. Importantly, in state 606, as discussed above, the multi-processor will exhibit lower power consumption than other multi-processor cores having an identical power management scheme but whose constituent cores are all high power cores. Even lower power consumption can be provided for in state 606 if the sole operating low power core is provided with a lower supply voltage and/or lower operating frequency that the lowest operating supply voltage and/or operating frequency applied to the high power cores.

[0036] No special adjustment needs to be made by or for application software, virtual machine or virtual machine monitor when the system is running only on the low power core(s) after all the high power cores are disabled. Again, the preservation of the same instruction core across all cores in the system corresponds to transparency from the software's perspective as to the underlying cores. Lower performance may be recognized with lower cores but no special adjustments as to the content of the instruction streams should be necessary. In various alternate implementations: 1) the hardware/machine readable firmware can monitor and control the core mix; or, 2) the hardware can relinquish control to the Operating system and let it monitor the demand and control the core mix.

[0037] Fig. 7 shows essentially a reverse of the processes described above. As observed in Fig. 7, starting from a state in which only a single low power core is operating 701 additional low power cores are enabled (if any more) 702 as demand on the multi-processor continually increases. Eventually, high power cores are enabled 703. Notably, the demand threshold needed to enable a next processor from an operating low power processor may correspond to a lower demand increment than the demand threshold needed to enable to a next processor from an operating high power processor.

[0038] That is, inset 710 shows the increase in demand 711 needed after a low power processor is first enabled to trigger the enablement of a next processor in the face of increased demand.

The increase in demand 712 needed after a high power processer is first enabled to trigger enablement of a next high power processer in the face of increased demand is greater than the aforementioned demand 711. This is so because a high power processor is able to handle more total demand than a low power processor and therefore does not need to have additional "help" as soon as a low power processor does.

[0039] Operating frequency and/or supply voltage may also be increased in conjunction with the enablement of cores in the face of increased demand in a logically inverse manner to that discussed above with respect to the disablement of cores.

[0040] Fig. 8 shows a design process for designing a multi-core processor consistent with the principles discussed above. As part of the design process, high level behavioral descriptions 800 (e.g., VHDL or Verilog descriptions) for each of the processor's cores are synthesized into a Register Transfer Level (RTL) netlist 801. The RTL netlist is synthesized 802 into corresponding higher power core gate level netlist(s) (one for each high power ore) with libraries corresponding to a higher power/performance design (such as logic circuits having wider drive transistors). The RTL netlist is also synthesized 803 into corresponding lower power core gate level netlist(s) (one for each low power core) with libraries corresponding to a lower power/performance design (such as logic circuits having wider drive transistors). Here, the logic designs for the high power and low power cores are the same but the design of their corresponding logic circuits have different performance/power design points.

[0041] The transistor level netlists for the respective cores are then used as a basis for performing a respective place, route and timing analysis 806 and design layout 807. Here, the lower power/performance cores may have more relaxed placement and timing guidelines owing to the larger permissible propagation delay through and between logic circuits. Said another way, recalling from the discussion of Fig. 3 that longer load lines result in slower rise and fall times, the lower performance cores may permit longer load lines between transistors and gates because these cores are designed to have slower operation (of course, if load lines are increased to much along with the inclusion of narrower drive transistors, the drop in performance may be more than desired).

[0042] Upon completion of the layout and timing analysis, the cores are cleared for manufacture upon a clean manufacturing ground rule check 808.

[0043] Processes taught by the discussion above may be performed with program code such as machine-executable instructions that cause a machine that executes these instructions to perform certain functions. In this context, a "machine" may be a machine that converts intermediate form (or "abstract") instructions into processor specific instructions (e.g., an abstract execution

environment such as a "virtual machine" (e.g., a Java Virtual Machine), an interpreter, a Common Language Runtime, a high-level language virtual machine, etc.)), and/or, electronic circuitry disposed on a semiconductor chip (e.g., "logic circuitry" implemented with transistors) designed to execute instructions such as a general-purpose processor and/or a special-purpose processor. Processes taught by the discussion above may also be performed by (in the alternative to a machine or in combination with a machine) electronic circuitry designed to perform the processes (or a portion thereof) without the execution of program code.

[0044] It is believed that processes taught by the discussion above may also be described in source level program code in various object-orientated or non-object-orientated computer programming languages (e.g., Java, C#, VB, Python, C, C++, J#, APL, Cobol, Fortran, Pascal, Perl, etc.) supported by various software development frameworks (e.g., Microsoft Corporation's .NET, Mono, Java, Oracle Corporation's Fusion, etc.). The source level program code may be converted into an intermediate form of program code (such as Java byte code, Microsoft Intermediate Language, etc.) that is understandable to an abstract execution environment (e.g., a Java Virtual Machine, a Common Language Runtime, a high-level language virtual machine, an interpreter, etc.) or may be compiled directly into object code.

[0045] According to various approaches the abstract execution environment may convert the intermediate form program code into processor specific code by, 1) compiling the intermediate form program code (e.g., at run-time (e.g., a JIT compiler)), 2) interpreting the intermediate form program code, or 3) a combination of compiling the intermediate form program code at run-time and interpreting the intermediate form program code. Abstract execution environments may run on various operating systems (such as UNIX, LINUX, Microsoft operating systems including the Windows family, Apple Computers operating systems including MacOS X, Sun/Solaris, OS/2, Novell, etc.).

[0046] An article of manufacture may be used to store program code. An article of manufacture that stores program code may be embodied as, but is not limited to, one or more memories (e.g., one or more flash memories, random access memories (static, dynamic or other)), optical disks, CD-ROMs, DVD ROMs, EPROMs, EEPROMs, magnetic or optical cards or other type of machine-readable media suitable for storing electronic instructions. Program code may also be downloaded from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals embodied in a propagation medium (e.g., via a communication link (e.g., a network connection)).

[0047] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications

and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims.

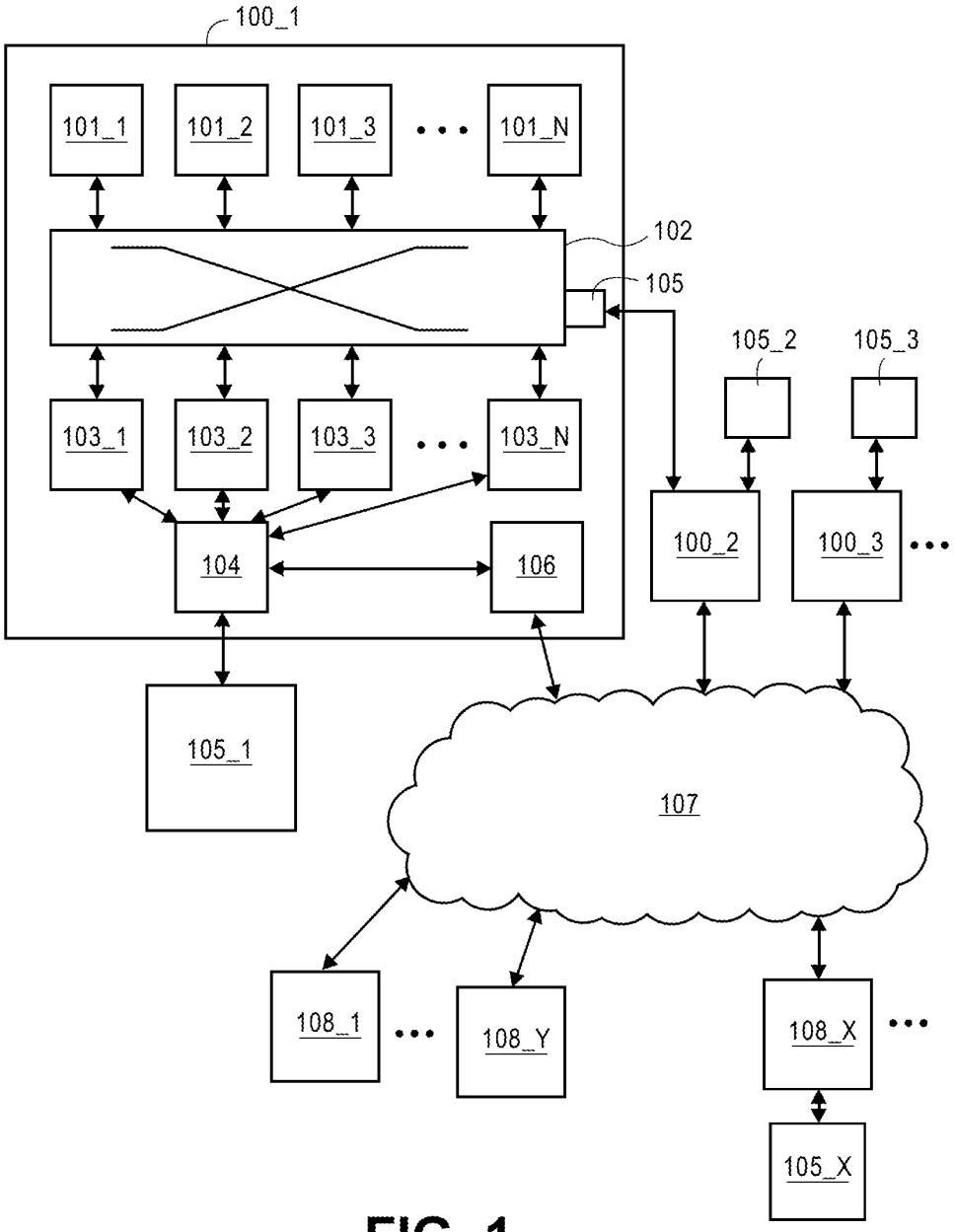
100_1
101_1
101_2
101_3
101_N
102
105
103_1
103_2
103_3
103_N
104
106
105_2
105_3
100_2
100_3
105_1
107
108_1
108_Y
108_X
105_X

FIG. 1

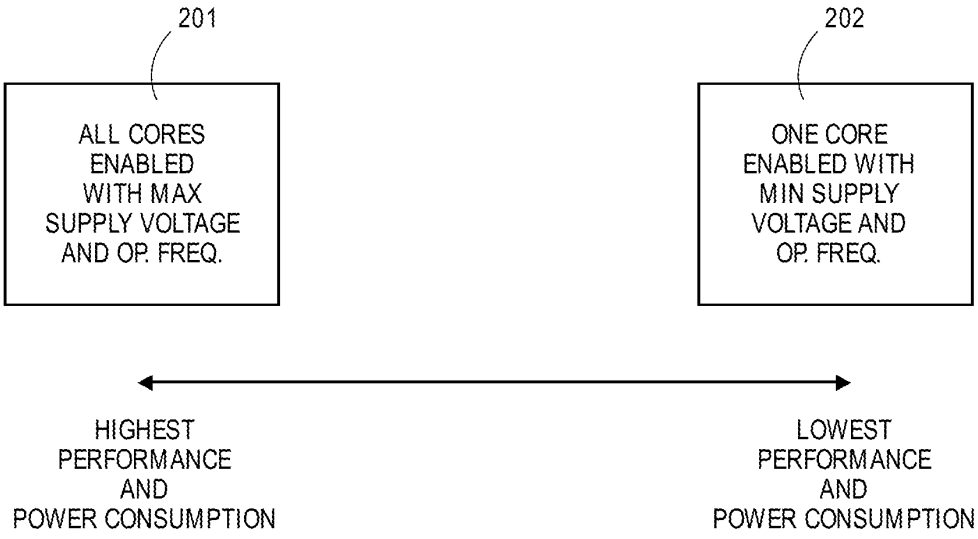
201
ALL CORES ENABLED WITH MAX SUPPLY VOLTAGE AND OP. FREQ.
202
ONE CORE ENABLED WITH MIN SUPPLY VOLTAGE AND OP. FREQ.
HIGHEST PERFORMANCE AND POWER CONSUMPTION
LOWEST PERFORMANCE AND POWER CONSUMPTION

FIG. 2

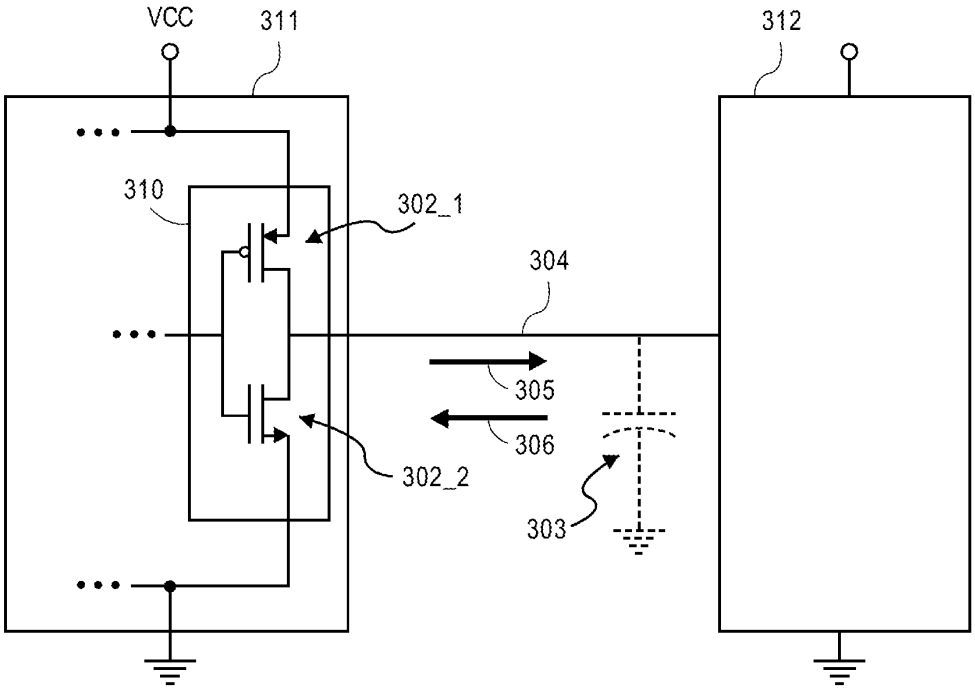

FIG. 3

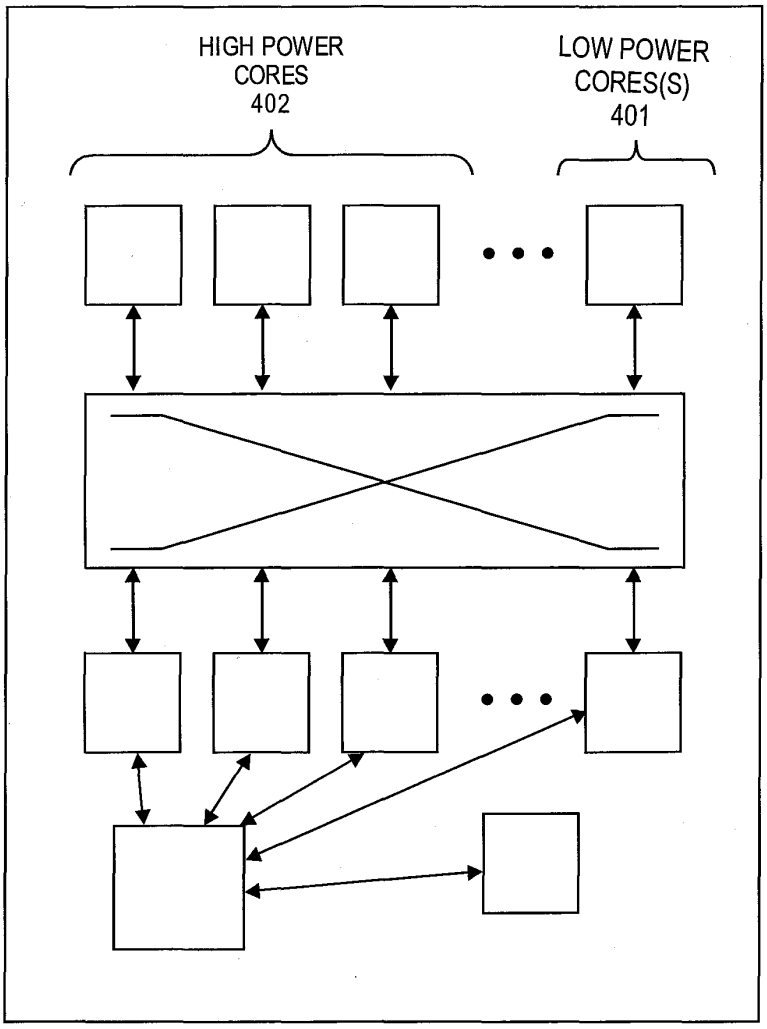

FIG. 4

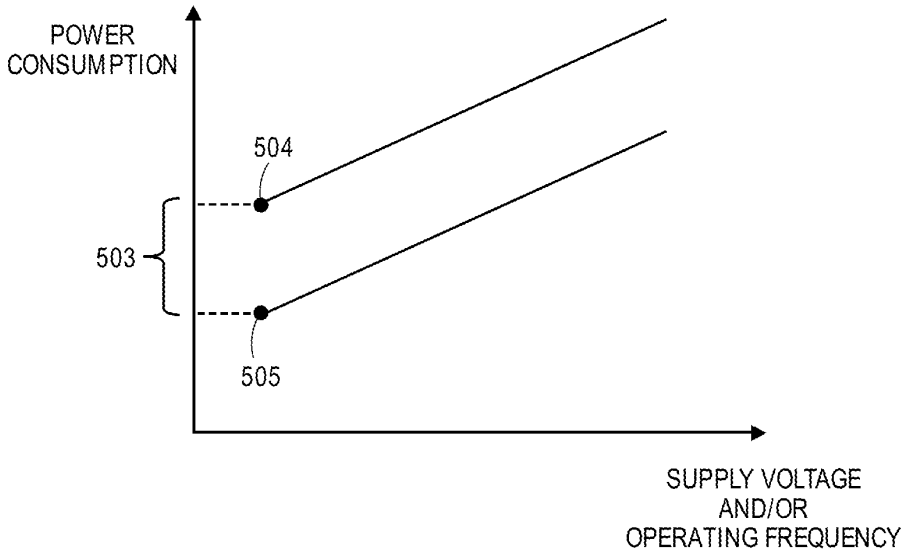
POWER
CONSUMPTION
504
503
505
SUPPLY VOLTAGE
AND/OR
OPERATING FREQUENCY

FIG. 5

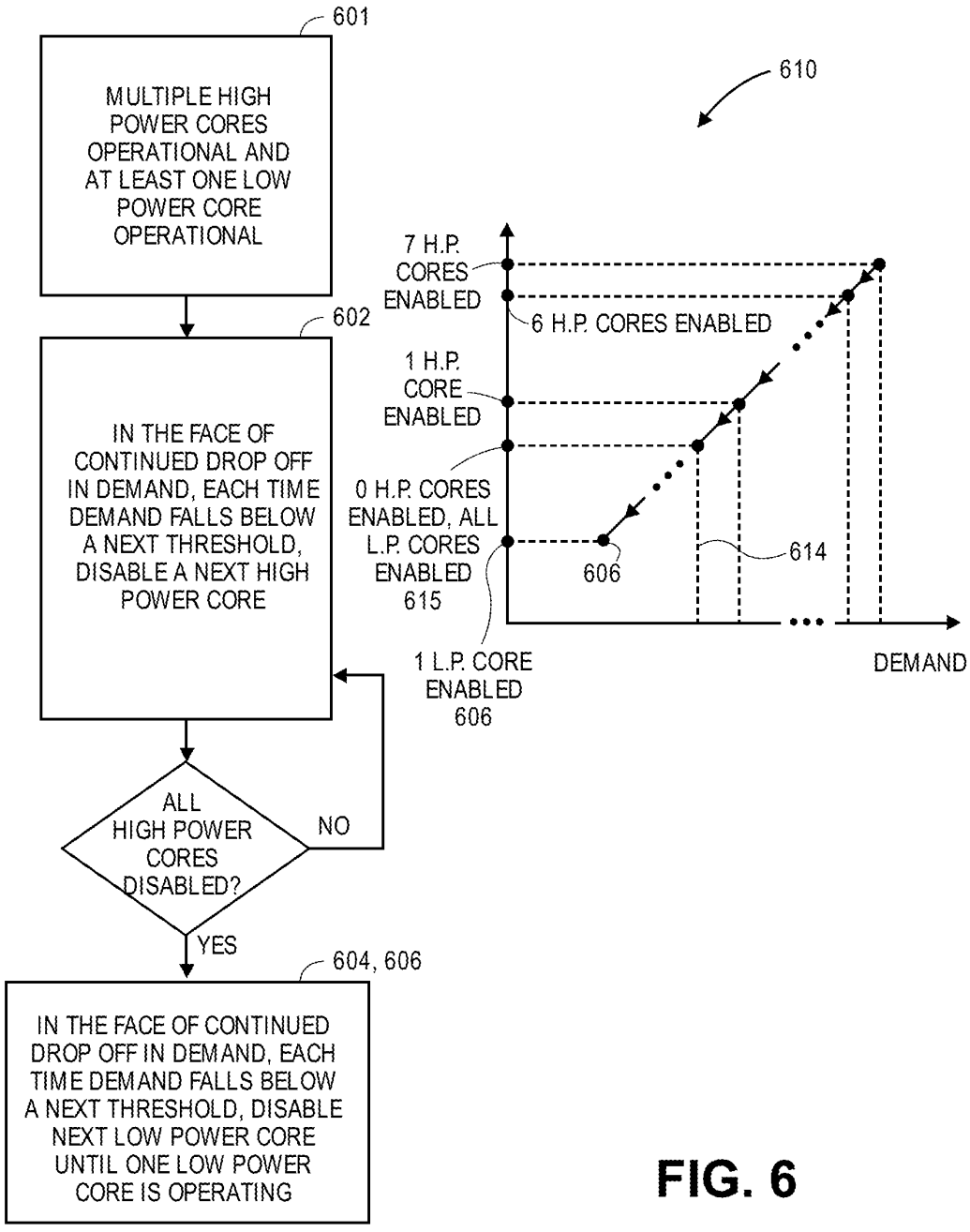
601
MULTIPLE HIGH POWER CORES OPERATIONAL AND AT LEAST ONE LOW POWER CORE OPERATIONAL
602
IN THE FACE OF CONTINUED DROP OFF IN DEMAND, EACH TIME DEMAND FALLS BELOW A NEXT THRESHOLD, DISABLE A NEXT HIGH POWER CORE
ALL HIGH POWER CORES DISABLED?
NO
YES
604, 606
IN THE FACE OF CONTINUED DROP OFF IN DEMAND, EACH TIME DEMAND FALLS BELOW A NEXT THRESHOLD, DISABLE NEXT LOW POWER CORE UNTIL ONE LOW POWER CORE IS OPERATING
610
7 H.P. CORES ENABLED
6 H.P. CORES ENABLED
1 H.P. CORE ENABLED
0 H.P. CORES ENABLED, ALL L.P. CORES ENABLED 615
606
614
1 L.P. CORE ENABLED 606
DEMAND

FIG. 6

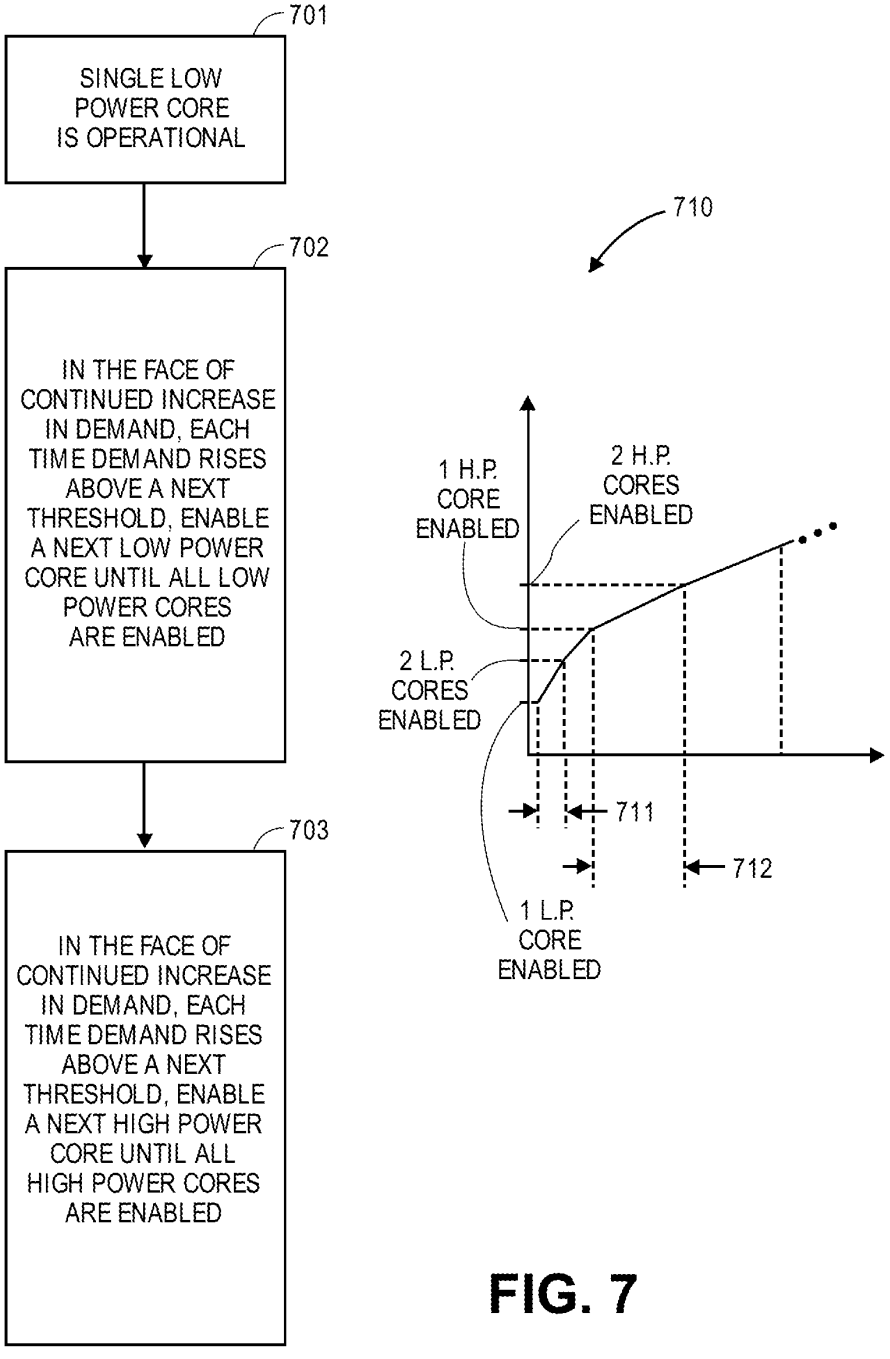
701
SINGLE LOW POWER CORE IS OPERATIONAL
702
IN THE FACE OF CONTINUED INCREASE IN DEMAND, EACH TIME DEMAND RISES ABOVE A NEXT THRESHOLD, ENABLE A NEXT LOW POWER CORE UNTIL ALL LOW POWER CORES ARE ENABLED
703
IN THE FACE OF CONTINUED INCREASE IN DEMAND, EACH TIME DEMAND RISES ABOVE A NEXT THRESHOLD, ENABLE A NEXT HIGH POWER CORE UNTIL ALL HIGH POWER CORES ARE ENABLED
710
1 H.P. CORE ENABLED
2 H.P. CORES ENABLED
2 L.P. CORES ENABLED
1 L.P. CORE ENABLED
711
712

FIG. 7

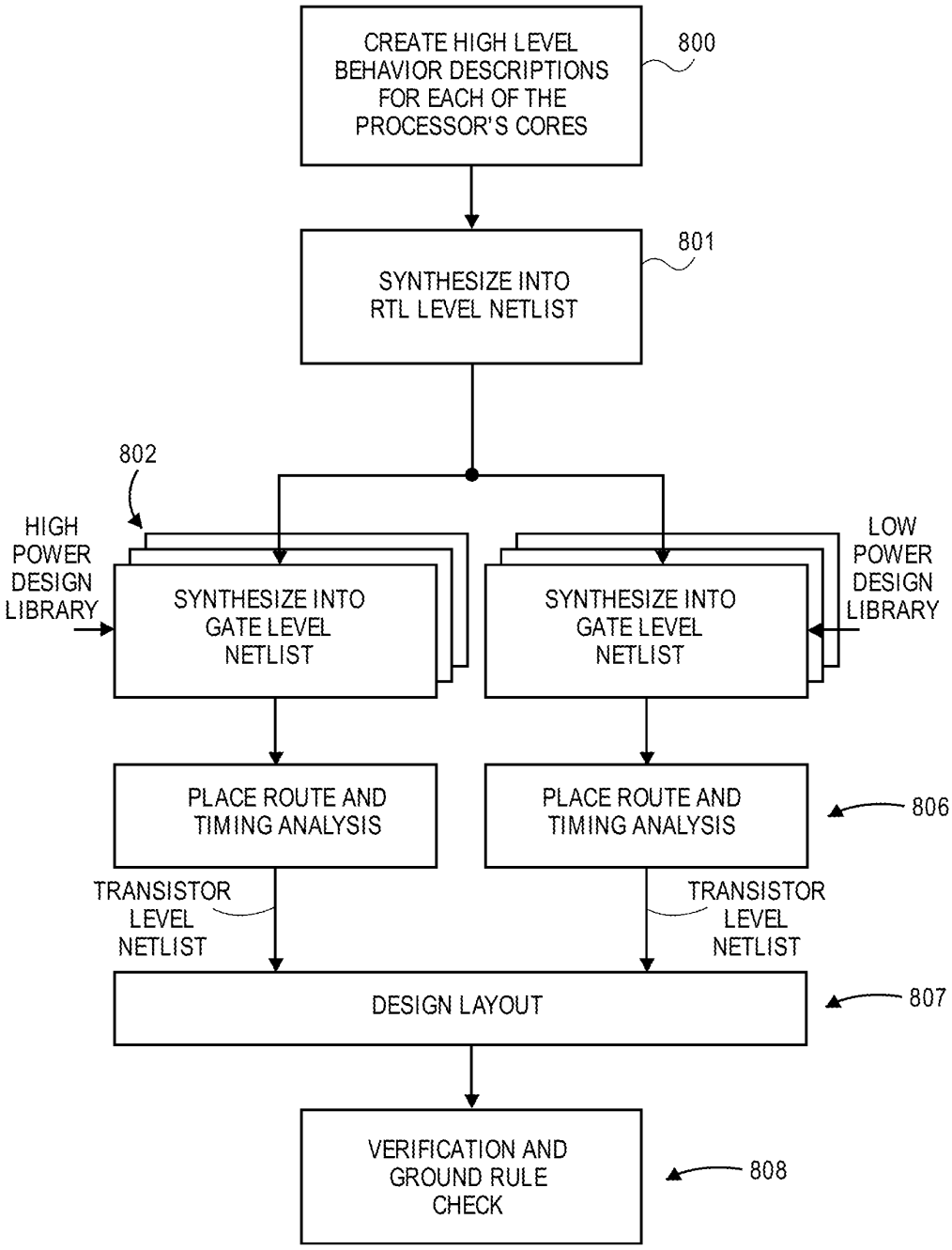
CREATE HIGH LEVEL BEHAVIOR DESCRIPTIONS FOR EACH OF THE PROCESSOR'S CORES
800
SYNTHESIZE INTO RTL LEVEL NETLIST
801
802
HIGH POWER DESIGN LIBRARY
SYNTHESIZE INTO GATE LEVEL NETLIST
SYNTHESIZE INTO GATE LEVEL NETLIST
LOW POWER DESIGN LIBRARY
PLACE ROUTE AND TIMING ANALYSIS
PLACE ROUTE AND TIMING ANALYSIS
806
TRANSISTOR LEVEL NETLIST
TRANSISTOR LEVEL NETLIST
DESIGN LAYOUT
807
VERIFICATION AND GROUND RULE CHECK
808

FIG. 8