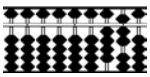
Trevor Mudge
Bredt Family Chair of Computer Science & Engineering



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Education

- Ph.D. Computer Science, University of Illinois, Urbana, Illinois, 1977. Thesis: A Computer Hardware Design Language for Multiprocessor Systems.
- M.S. Computer Science, University of Illinois, Urbana, Illinois, 1973. Thesis: SEMANTRIX: A Semantically Guided Digital Electronic Machine.
- B.Sc. (Hons.) Cybernetics, University of Reading, England, 1969.

Work History

- 2002-present: The Bredt Family Chair of Computer Engineering and Professor Electrical Engineering and Computer Science, Dept. of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1990-2002: Professor Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1992-2002: Director of the Advanced Computer Architecture Lab., The University of Michigan, Ann Arbor
- 1984-1990: Associate Professor Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1977-1983: Assistant Professor Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor
- 1974-1977: Research Assistant, Digital Systems Research Group, Coordinated Science Laboratory, University of Illinois. Research in the areas of digital systems design languages, parallel processing, and fault tolerant computing.
- 1970-1974: Research Assistant, Information Engineering Group, Digital Computer Laboratory, University of Illinois. Design and construction of several digital machines.

Professional Society Membership

- Life Fellow IEEE and member of the IEEE Computer Society
- Fellow of the Association for Computing Machinery
- Member of the IET: The Institution of Engineering and Technology (was Institution of Electrical Engineers)
- Member of the British Computer Society
- Member of Sigma Xi

Awards

- **2021 Test of Time Award** for Razor: A low-power pipeline based on circuit-level timing speculation. 36th Ann. IEEE/ACM Symp. Microarchitecture (MICRO-36), Dec. 2003, pp. 7-18.
- **2021 Best paper** for: Prodigy: Improving the Memory Latency of Data-Indirect Irregular Workloads Using Hardware-Software Co-Design. *Int. Symp. on High Performance Computer Architecture (HPCA)*, Seoul, S. Korea, February 2021.
- **2018 Most Impactful Paper—25 years** Awarded at International Conference on High-Performance Computing (HiPC) Silver Jubilee in December 2018. "Power: A first class design constraint for future architectures." *Proc.*7th Int. Conf. on High Performance Computing - HiPC, (Springer Lecture Notes in Computer Science), Dec. 2000, Bangalore, India, pp. 215-224.
- **2017 ACM SIGARCH/IEEE-CS TCCA Influential ISCA paper award**, for "Dowsy Caches: Simple Techniques for Reducing Leakage Power" (with K. Flautner, N. Kim, S. Martin, D. Blaauw) from the *Proc. of the 29th Ann. Int. Symp. on Computer Architecture*, May 2002. The award recognizes the paper from the ISCA proceedings 15 years earlier that has had the most impact on the field during the intervening years.
- **2017 Fellow of the Association of Computing Machinery**, "For contributions to power aware computer architecture".
- **2015 Top Pick: selected as one of the 12 best papers in computer architecture for 2015** J. Hauswald, M. A. Laurenzano, Y. Zhang, C. Li, A. Rovinski, A. Khurana, R.G. Dreslinski, T. Mudge, V. Petrucci, L. Tang, J. Mars. Sirius: An Open End-to-end Voice and Vision Personal Assistant and Its Implications For Future Warehouse Scale Computers. *IEEE MICRO* May/June 2016, vol. 36, no. 3, pp. 42-53.
- **2014 International Conference on Supercomputing 25th Anniversary Issue 1987-2011 (35 most influential papers)**. For the paper: Improving data cache performance by pre-executing instructions under a cache miss. (James Dundas and Trevor Mudge) Proc. 1997 ACM Int. Conf. on Supercomputing, July 1997. Reprinted in the anniversary issue, U. Banerjee Editor, 2014.
- **2014 Best paper** for: Sources of Error in Full System Simulation. *2014 IEEE Int. Symp. on Performance Analysis of Systems and Software (ISPASS)*, Monterey, CA, March 2014, pp. 13-22.
- **2014 Distinguished Achievement Award** from the University of Illinois Computer Science Department as an "outstanding educator and researcher whose work has advanced the field of low-power computer architecture and its interaction with technology." Given at the Department's CS @ Illinois 50th Anniversary Celebration, October 20th , 2014.
- **2014 ACM/IEEE CS Eckert-Mauchly Award.** For pioneering contributions to low-power computer architecture and its interaction with technology. June 2014.
- **2014 Chartered IT Professional (CTIP),** British Computer Society, c. 2014.
- **2013 Life Fellow of the IEEE**, 2013
- **2012 International Conference on Computer-Aided Design's Ten Year Retrospective Most Influential Paper Award in 2012**. For the paper: Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads. (S. Martin, K. Flautner, D. Blaauw, and T. Mudge.) Appeared in *Proc. Int. Conf. of Computer Aided Design (ICCAD-2002)*, San Jose, CA, Nov. 2002, pp. 721-725.
- **2011 Winner in the 11th Annual International VLSI Symposium Low Power Design Contest.** For the paper: SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric. (S. Satpathy, R. Dreslinski, T. Ou, D. Sylvester, T. Mudge, D. Blaauw.) Appeared in the *Symposium on VLSI Technology and Circuits*. Kyoto, Japan, June 2011, pp.138-139.
- **2011 Winners of the DAC/ISSCC Student Design Contest for 2011** Mentor for (With David Blaauw and Dennis Sylvester) their project "Design and Implementation of Centip3De, a 7-layer Many-Core

System", D. Fick, R. Dreslinski, B. Giridhar, G. Kim, S. Seo, M. Fojtik, S. Satpathy, Y. Lee, D. Kim, N. Liu, M. Wiekowski, G. Chen, T. Mudge, D. Sylvester, and D. Blaauw. Proc. of the ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, June, 2011.

- **2009 Top Pick: selected as one of the 12 best papers in computer architecture for 2009** M. Woh, S. Seo, S. Mahlke, T. Mudge, C. Chakrabarti, and K. Flautner. AnySP: Anytime Anywhere Anyway Signal Processing. *36th Int. Symp. on Computer Architecture*, Austin, TX, June, 2009, pp. 128-139.
- **2009 Ted Kennedy Family Team Excellence Award** for 2008-9 from the College of Engineering, University of Michigan, April 2009.
- **2008 Top Pick: selected as one of the 12 best papers in computer architecture for 2008** K. Lim, P. Ranganathan, J. Chang, C. Patel, T. Mudge, S. Reinhardt. Understanding and designing new server architectures for emerging warehouse-computing environments. *35th Int. Symp. on Computer Architecture*, Beijing, China, June, 2008, pp. 315-326.
- **2008 Best paper** for: From SODA to Scotch: The Evolution of a Wireless Baseband Processor. *41st IEEE/ACM Int. Symp. on Microarchitecture (MICRO*), Lake Como, Italy, Nov. 2008, pp. 152-163.
- **2007 Best Paper Nomination** for: B. Zhai, R. Dreslinski, D. Blaauw, T. Mudge, and D. Sylvester. Energy Efficient Near-threshold Chip Multi-processing. Int. Symp. on Low Power Electronics and Design - 2007 (ISLPED), Aug. 2007, pp. 32-37.
- **2007 Best paper** for: Next Generation Challenge for Software Defined Radio. M. Woh, S. Seo, H. Lee, Y. Lin, S. Mahlke, T. Mudge, C. Chakrabarti, and K. Flautner. *SAMOS VII,* Greece, April 2007, pp. 343-354.
- **2006 Top pick paper selected as one of the 12 best papers in computer architecture for 2006,** for: Y. Lin, H. Lee, M. Woh, Y. Harel, S. Mahlke, T. Mudge, C. Chakrabarti, K Flautner. SODA: A low-power architecture for software radio. *Proc. 33rd Ann. Int. Symp. on Computer Architecture*, Boston, MA USA, June 2006, pp. 89-101.
- **2007 Microprocessor Report Innovation Award:** "RAZOR—Error-Tolerant Approach Supports Speculative Correctness" MPR Analysts' Choice Award in the Innovation category – 2/26/07. (Microprocessor Report has been the leading technical publication for the microprocessor industry since 1987.)
- **2003 Top pick paper selected as one of the 12 best papers in computer architecture for 2003**, for: D. Ernst, N. Kim, S. Das, S. Pant, T. Pham, R. Rao, C. Ziesler, D. Blaauw, T. Austin, T. Mudge, and K. Flautner. Razor: A low-power pipeline based on circuit-level timing speculation. *36th Ann. IEEE/ACM Symp. Microarchitecture (MICRO-36)*, Dec. 2003, pp. 7-18.
- **2003 Best paper** for: D. Ernst, N. Kim, S. Das, S. Pant, T. Pham, R. Rao, C. Ziesler, D. Blaauw, T. Austin, T. Mudge, and K. Flautner. Razor: A low-power pipeline based on circuit-level timing speculation. *36th Ann. IEEE/ACM Symp. Microarchitecture (MICRO-36)*, Dec. 2003, pp. 7-18.
- **2003 Bredt Family Chair of Engineering**, conferred by the College of Engineering in 2003.
- **1997 Research Excellence Award** for 1995-96 from the College of Engineering, University of Michigan, Feb. 1997.
- **1996 Heaviside Premium**. Awarded by the Institution of Electrical Engineer for the best paper of the year: A comparison of two common pipeline structures. *Proc. Computers and Digital Techniques*, 1996.
- **1995 Fellow of the Institute of Electrical and Electronics Engineers**, "For contributions to the design and analysis of high performance processors," 1995.
- **1995 Research Excellence Award** for 1994-95 EECS Department , University of Michigan, Feb. 1995.
- **Best paper nomination** for "Analysis and design of latch-controlled synchronous digital circuits," (15 out of 377) at the 27-th Design Automation Conference, June 1990.
- **1986 Best IEEE MICRO article** of 1986 for "A Microprocessor-based Hypercube Supercomputer."

- **1983 Outstanding Teaching** in Engineering. Awarded by the College of Engineering, University of Michigan, Dec.1983.
- **1982 Quest for Technology** Awards (2). Awarded by Control Data Corporation, Oct. 1982.
- **1981 Best paper runner-up**. Honorable mention from the editors of the IEEE Trans. on Education for runner-up best paper published in 1981: "A Course Sequence in Microprocessor-Based Digital Systems Design."
- **1981 John A. Curtis Award**. Awarded by The Computers in Education Division of the American Society of Engineering Educators, June 1981, for the paper: Teaching Assembly Language Using an Assembly Language Interpreter.
- **1981 Best paper**. Awarded by The Instrument Society of America at their 27-th Int. Symposium, Apr. 1981, for the paper: VLSI Implementation of a Numerical Processor for Robotics.

Miscellaneous Recognition

- **International Symposium on Computer Architecture Hall of Fame:** http://pages.cs.wisc.edu/~arch/www/iscabibhall.html
- **MICRO Hall of fame:** https://www.sigmicro.org/micro-hall-of-fame/
- **Erdős number = 3**

Post Docs

1. Xin He, November 2018 – May 2022. Current position: Senior Engineer at Tentorrent
2. Ronald G. Dreslinski Jr., April 2011 - January 2012 Current position: Associate Professor Department of Electrical Engineering and Computer Science, The University of Michigan
3. Reetuparna Das, September 2011- September 2015 Current position: Associate Professor Department of Electrical Engineering and Computer Science, The University of Michigan.
4. Yoonseo Choi, September 2007 – September 2010 Current position: Software Engineer Intel Corporation.

Ph.D. Theses Supervised

1. Optimizing Sparse Linear Algebra on Reconfigurable Architecture, Dong-hyeon Park, The University of Michigan, 2021. Current position: Military service in the Republic of Korea Army.
2. Rethinking Context Management of Data Parallel Processors in an Era of Irregular Computing, Jonathan Beaumont, The University of Michigan, 2019. Current position: Lecturer IV Dept Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor.
3. Architecting Memory System for Emerging Technologies, Byoungchan Oh, The University of Michigan, 2017. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Senior Memory Architect, Intel Federal LLC.
4. Heterogeneous Mobile Platform Characterization and Accelerator Design, Cao Gao, The University of Michigan, 2017. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Software Engineer, Google Inc.

5. Studies in Exascale Computer Architecture: Interconnect, Resiliency, and Checkpointing, Sandunmalee Nilmini Abeyratne, The University of Michigan, 2017. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Performance Architect Intel Corporation.
6. Designing Flexible, Energy Efficient and Secure Wireless Solutions for the Internet of Things, Yajing Chen, The University of Michigan, 2017. (Co-chairman Hun-Seok Kim) Current position: Digital Design Engineer, Intel Corporation.
7. Datacenter Design for Future Cloud Radio Access Network, Qi Zheng, The University of Michigan, 2016. (Co-chairman Ronald G. Dreslinski Jr.) Current position: Software Engineer, Square Inc., San Francisco, California.
8. Dense Server Architectures, Anthony Thomas Gutierrez, The University of Michigan, 2015. Current position: Member of Technical Staff, Design Engineer at AMD Research, Seattle Washington.
9. Scaling High-Performance Interconnect Architectures to Many-Core Systems, Korey LaMar Sewell, The University of Michigan, 2012. Current position: CPU Performance Architect, Apple.
10. Near-Threshold Computing: From Single Core to Many-Core Energy Efficient Architectures, Ronald G. Dreslinski Jr., The University of Michigan, 2011. Current position: Assistant Professor Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor.
11. Energy-efficient Architecture For Mobile Signal Processing, Sangwon Seo, The University of Michigan, 2011. Current position: Qualcomm Inc.
12. Architecture and Analysis For Next Generation Mobile Signal Processing, Mark Woh, The University of Michigan, 2011. Current position: Google Inc.
13. A Hardware/Software Approach for Alleviating Scalability Bottlenecks in Transactional Memory Applications, Geoffrey Wyman Blake, The University of Michigan, 2011. Current position: Senior System Development Engineer, Amazon Web Services.
14. Efficient Data Center Architectures Using Non-Volatile Memory and Reliability Techniques, David Andrew Roberts, The University of Michigan, 2010. Current position: Senior Member of Technical Staff at AMD.
15. Disaggregated Memory Architectures for Blade Servers, Kevin Te-Ming Lim, The University of Michigan, 2010. (Co-chairman Steven Reinhardt) Current position: Google Inc.
16. Cache Resource Allocation in Large Scale Chip Multiprocessors, Lisa Rufeng Hsu, The University of Michigan, 2009. (Co-chairman Steven Reinhardt) Current position: Staff Engineer in Qualcomm Datacenter Technologies.
17. Full-System Critical-Path Analysis and Performance Prediction, Ali Ghassan Saidi, The University of Michigan, 2009. (Co-chairman Steven Reinhardt) Current position: Principal System Development Engineer, Amazon Web Services.
18. Microarchitecture Choices And Tradeoffs For Maximizing Processing Efficiency, Deborah T. Marr, The University of Michigan, 2008. Current position: Senior Principal Engineer and Director of the Accelerator Architecture Research Lab, Intel Corporation.
19. Realizing Software Defined Radio – A Study in Designing Mobile Supercomputers, Yuan Lin, The University of Michigan, 2008. (Co-chairman Scott Mahlke) Current position: Senior Principal Engineer, Compiler Technical Lead, Sambanova Inc.
20. The Fast, Efficient, And Representative Benchmarking Of Future Microarchitectures, Jeffrey Stuart Ringenberg, The University of Michigan, 2008. Current position: Lecturer IV Dept Electrical Engineering and Computer Science, U Michigan, Ann Arbor.
21. Architecting Energy Efficient Servers, Tae Ho Kgil, The University of Michigan, 2007. Current position: Head of Cloud and Security Engineering at MagicCube.

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Litigation and bankruptcy checks for companies and debtors.

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Sync your system to PACER to automate legal marketing.