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(54) **CLUSTERED ARCHITECTURE IN A VLIW PROCESSOR**

(75) Inventors: **Marc Tremblay**, Menlo Park, CA (US); **William Joy**, Aspen, CO (US)

(73) Assignee: **Sun Microsystems, Inc.**, Palo Alto, CA (US)

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(58) Field of Search 712/24, 23, 217

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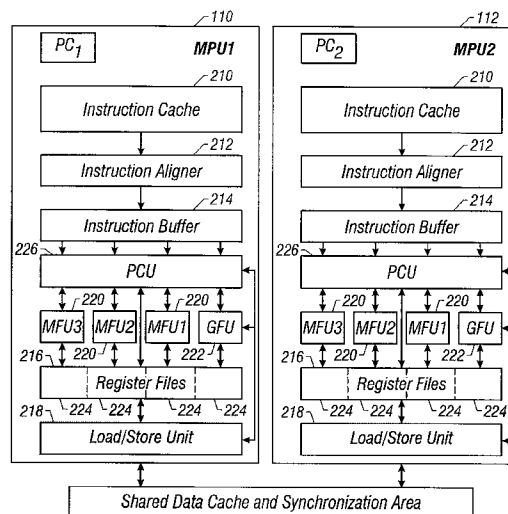
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Primary Examiner—Emanuel Todd Voeltz
(74) *Attorney, Agent, or Firm*—Zagorin, O'Brien & Graham, LLP

(57) **ABSTRACT**

A Very Long Instruction Word (VLIW) processor has a clustered architecture including a plurality of independent functional units and a multi-ported register file that is divided into a plurality of separate register file segments, the register file segments being individually associated with the plurality of independent functional units. The functional units access the respective associated register file segments using read operations that are local to the functional unit/ register file segment pairs. In contrast, the functional units access the register file segments using write operations that are broadcast to a plurality of register file segments. Independence between clusters is attained since the separate clustered functional unit/ register file segment pairs have local (internal) bypassing that allows internal computations to proceed, but have only limited bypassing between different functional unit/ register file segment pair clusters. Thus a particular functional unit/ register segment pair does not bypass to all other functional unit/ register segment pairs.
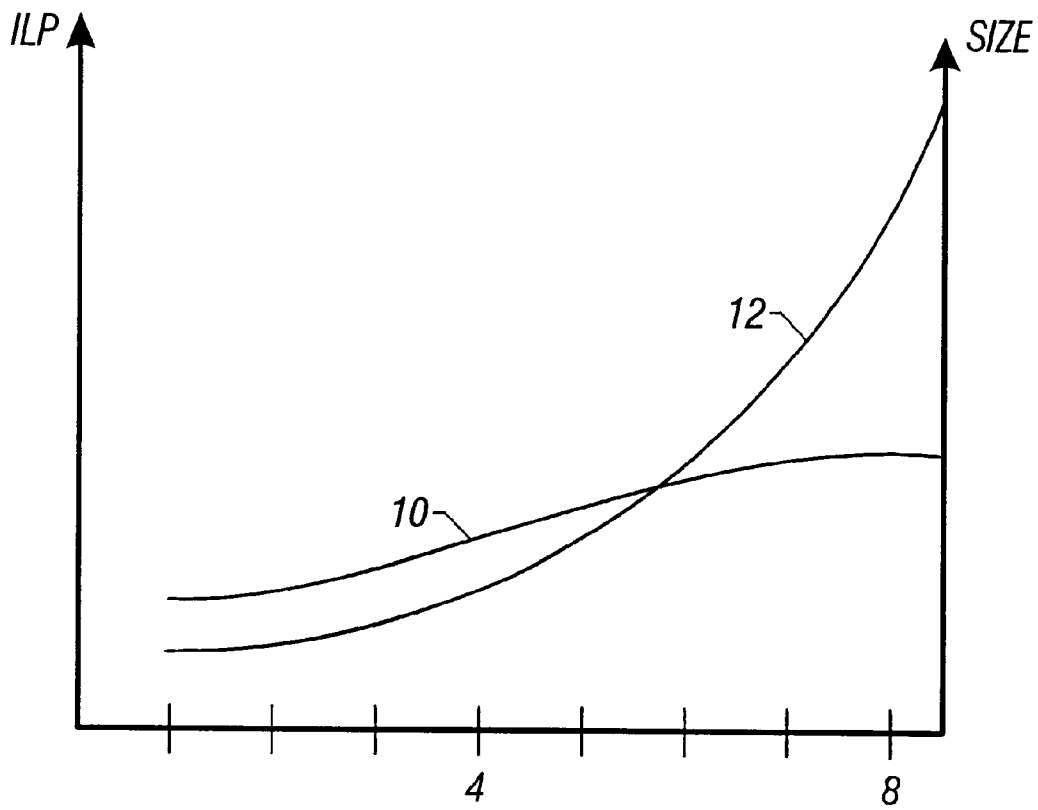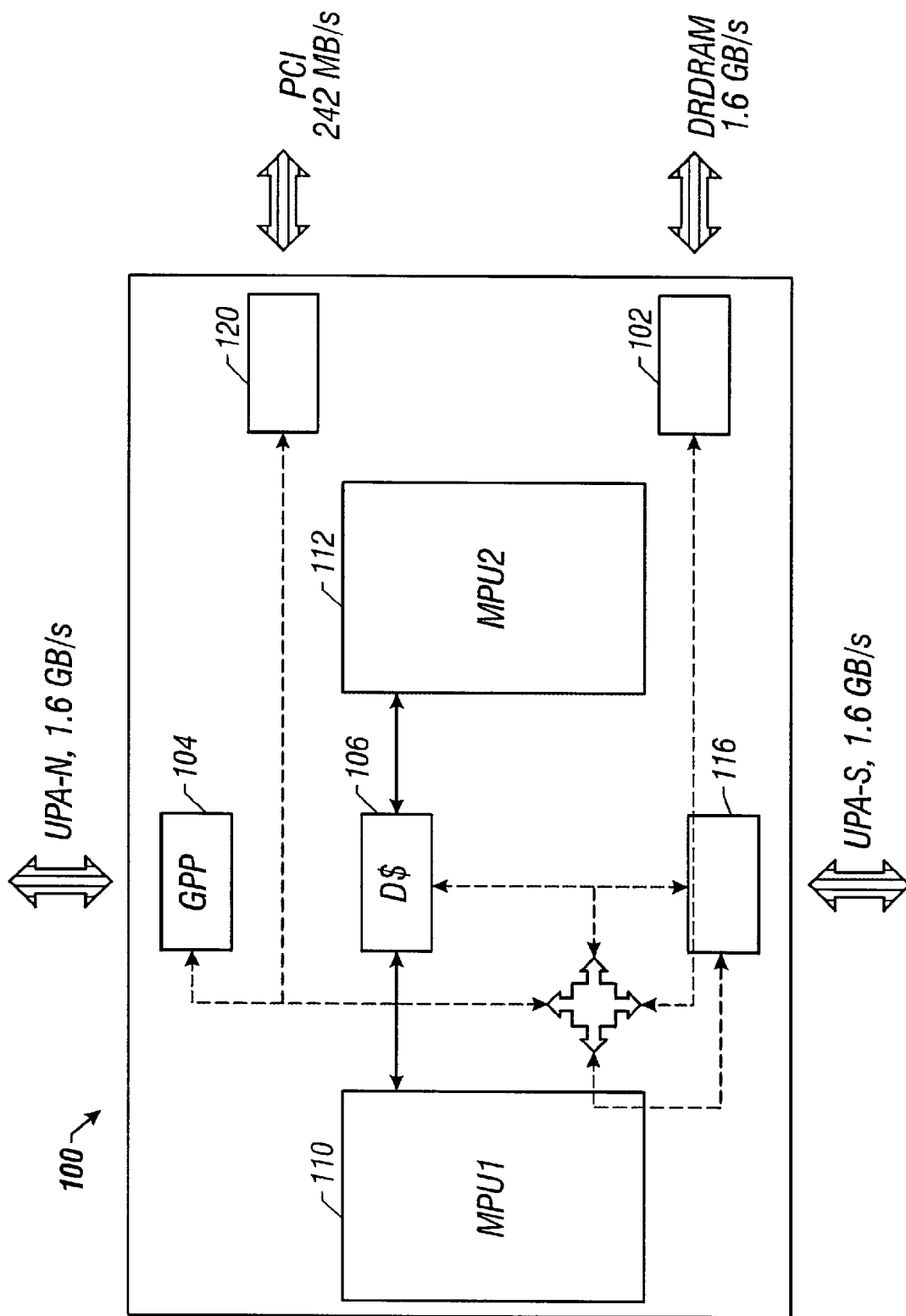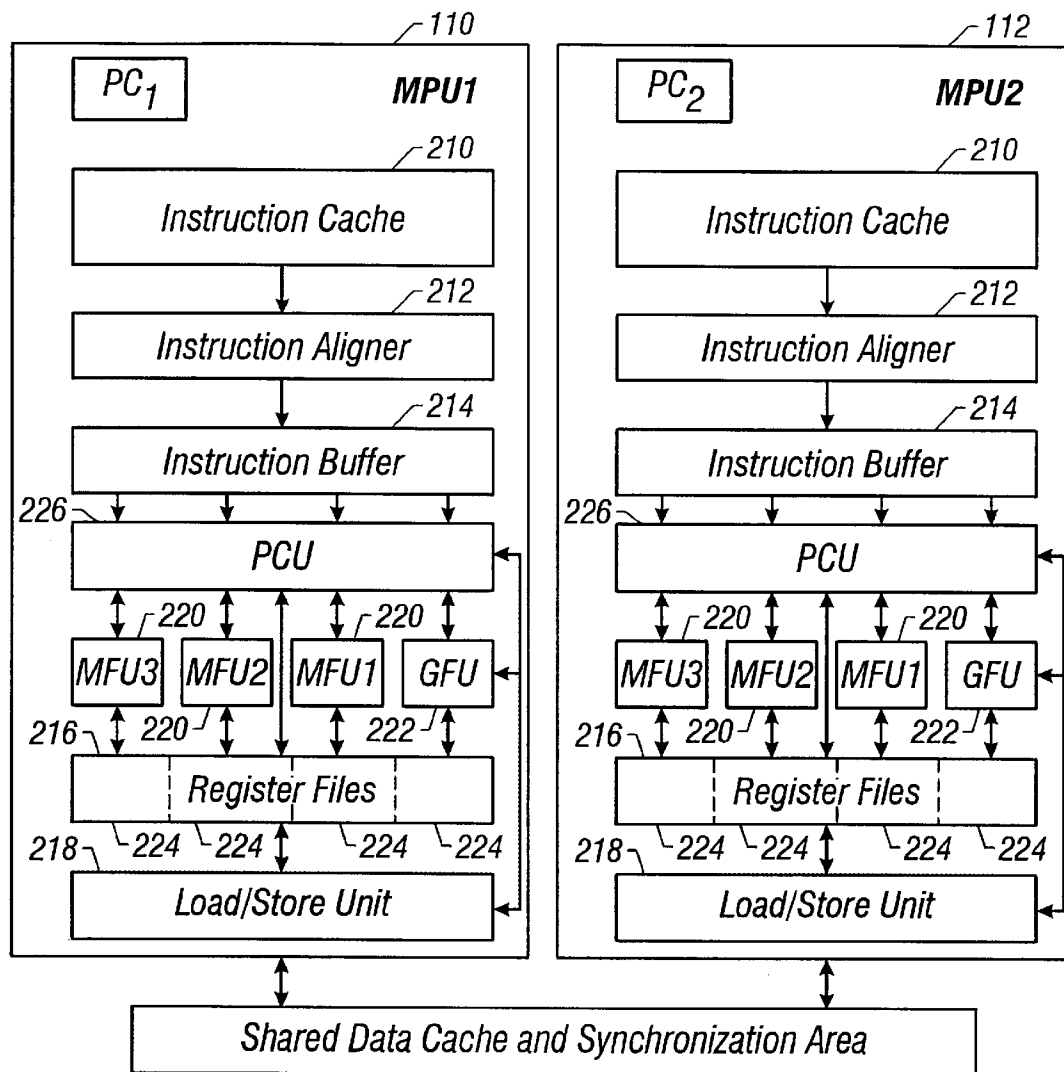
25 Claims, 18 Drawing Sheets

FIG. 1

FIG. 2

FIG. 3

Broadcast Writes (5)

216

316 — RF3

314 — RF2

312 — RF1

310 — RF0

3 Read Ports   _3 Read Ports_   _3 Read Ports_   _3 Read Ports_

FIG. 4

Global Registers 12R/4W or 12R/5W

216 — Register File

MFU₁   MFU₂   MFU₃   GFU
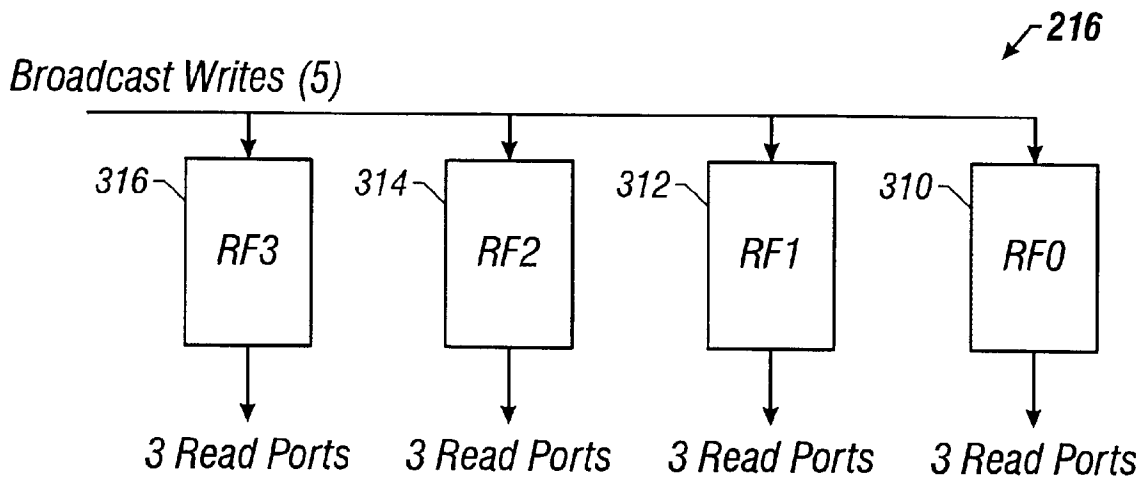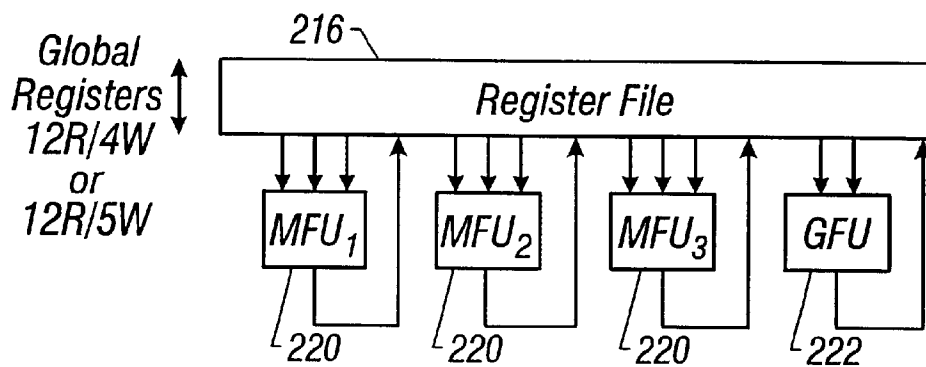
220   220   220   222

FIG. 5

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