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(54) **METHOD OF DATA TRANSFER AND APPARATUS THEREFOR**

(76) Inventor: **Thibault Mougel**, West Lothian (GB)

Correspondence Address:
PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06824 (US)

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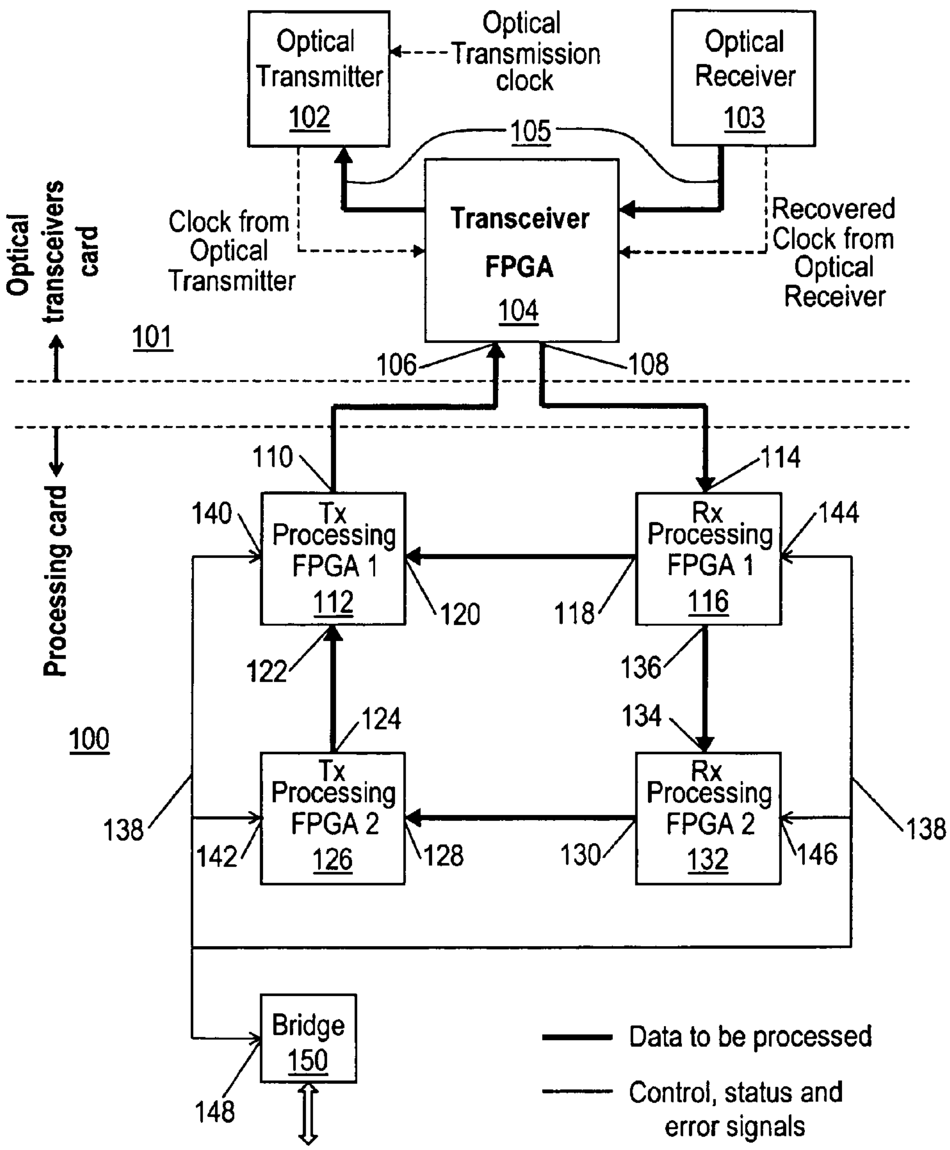
(57) **ABSTRACT**

In the field of programmable devices, such as FPGAs, comprising multi-gigabit transceiver units, it is desirable to communicate a data stream of a first data rate between the programmable devices at a second data rate. In order to achieve this aim, the data stream is read from a first buffer at the second data rate by a first device and communicated to a second device at the second data rate. When the buffer empties, idle bits are inserted in the absence of data. Upon receipt by the second device, the idle bits are identified and removed prior to buffering.



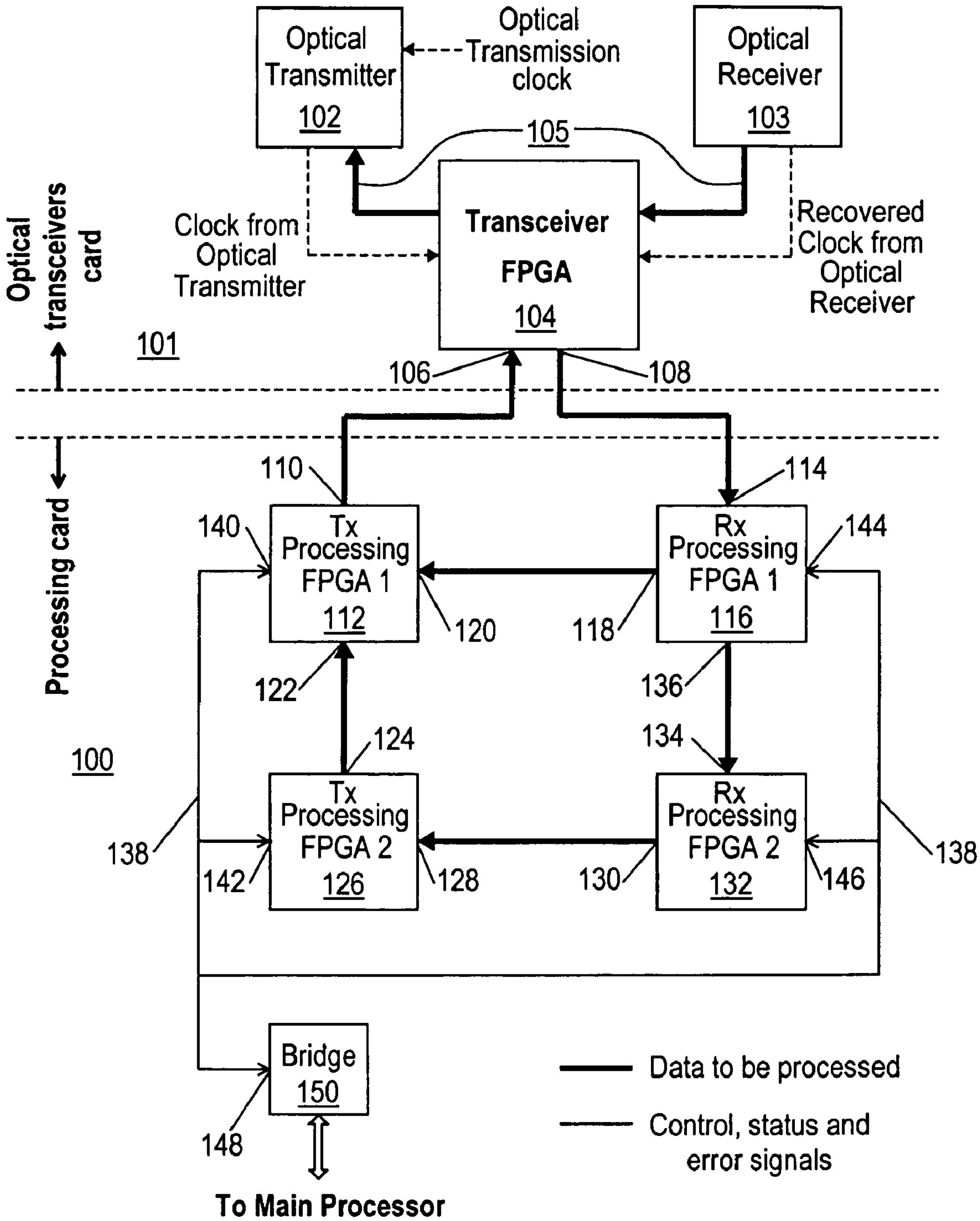

Optical Transmitter 102
Optical Transmission clock
Optical Receiver 103
105
Transceiver FPGA 104
Clock from Optical Transmitter
Recovered Clock from Optical Receiver
Optical transceivers card
101
106
108
Processing card
110
114
140
Tx Processing FPGA 1 112
Rx Processing FPGA 1 116
144
120
118
122
136
124
134
100
138
Tx Processing FPGA 2 126
Rx Processing FPGA 2 132
138
142
128
130
146
Bridge 150
148
To Main Processor
Data to be processed
Control, status and error signals

Fig 1

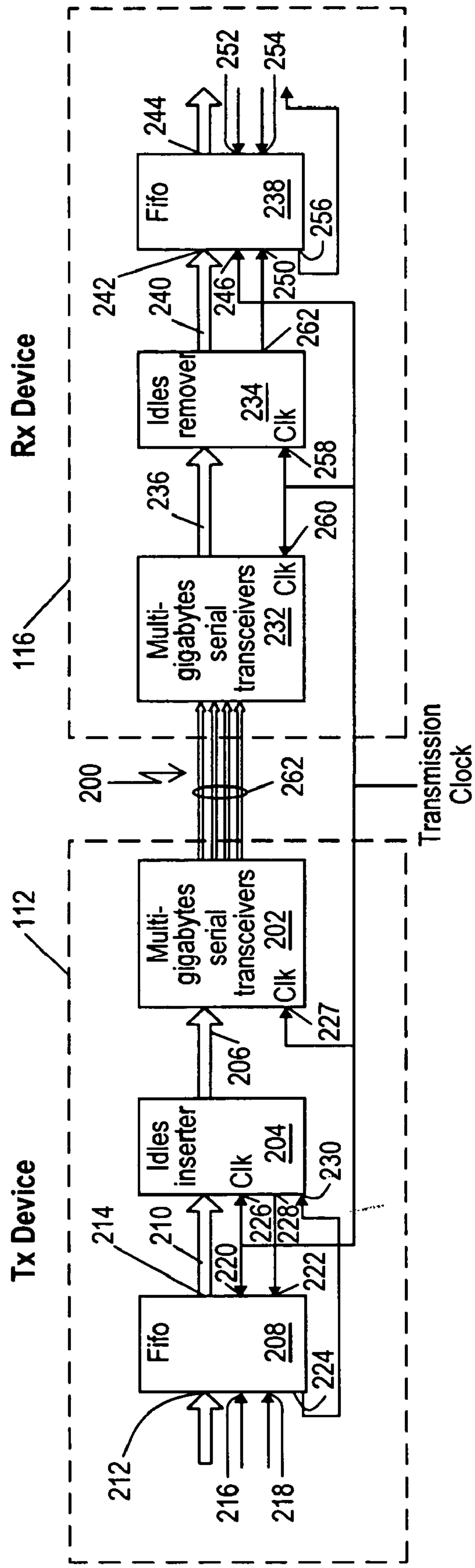

Rx Device
Tx Device
116
112
200
262
Fifo
238
Idles
remover
234
Clk
Multi-
gigabytes
serial
transceivers
232
Clk
Multi-
gigabytes
serial
transceivers
202
Clk
Idles
inserter
Clk
204
Fifo
208
Transmission
Clock
244
252
254
256
242
240
246
250
262
236
258
260
206
227
214
210
220
226
228
230
222
224
212
216
218

Fig. 2

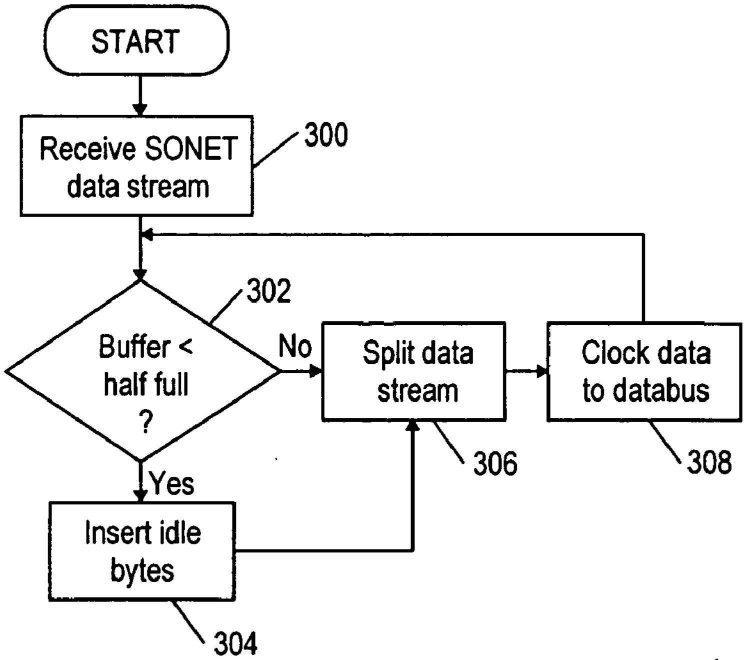

START
Receive SONET data stream
300
302
Buffer < half full ?
No
Split data stream
Clock data to databus
306
308
Yes
Insert idle bytes
304

Fig.3

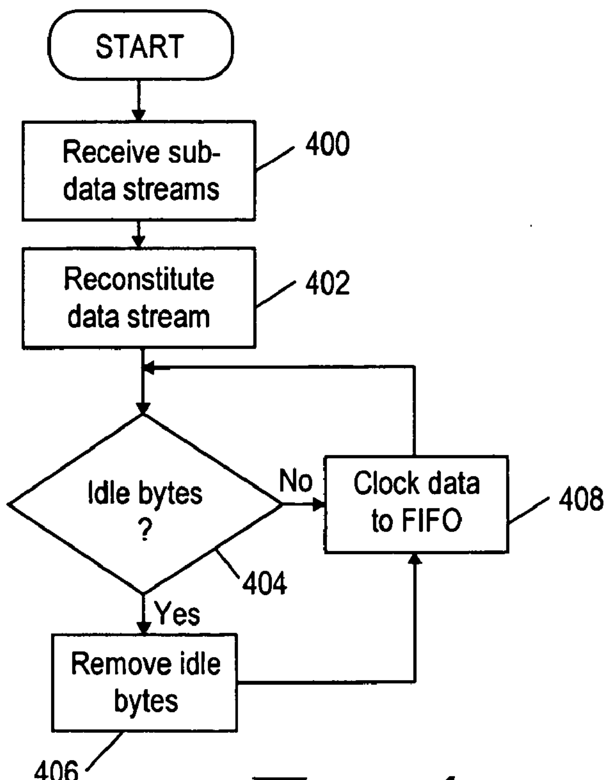

START
Receive sub-data streams
400
Reconstitute data stream
402
Idle bytes ?
No
Clock data to FIFO
408
404
Yes
Remove idle bytes
406

Fig 4

METHOD OF DATA TRANSFER AND APPARATUS THEREFOR

FIELD OF THE INVENTION

[0001] The present invention relates, in general, to a method of transferring a data stream of a first data rate over a data link at a second data rate. The present invention also relates, in general, to an apparatus for transferring a data stream of a first data rate over a data link at a second data rate.

DESCRIPTION OF THE BACKGROUND ART

[0002] In the field of optical communications, an optical communications network is formed from a large number of different hardware and software components. Clearly, there is therefore a need for test equipment in order to measure the integrity of signals generated in the network. Such test equipment is able to transmit test signals comprising test frames representative of actual signals communicated in the network. The test equipment may also receive the test frames, and detect and record any errors.

[0003] Certain test equipment comprises a number of Field Programmable Gate Arrays (FPGAS) and/or Application Specific Integrated Circuits (ASICs) in order to complete certain high-speed computational tasks associated with the tests to be performed. For example, it is known for some test equipment to generate a so-called Bit-Error-Ratio Test (BERT) set, and/or error performance data. However, such tests are processing power intensive due to the amount of data that needs to be processed by a single FPGA at high speed.

[0004] Of recent, manufacturers of FPGAs have begun to design the FPGAs with multi-gigabit serial transceivers that support a communications protocol, such as a so-called XAUIs (pronounced "Zowies"; X Attachment Unit Interfaces; the "X" representing the Roman numeral for ten) protocol to enable communication of data between FPGAs at high speed, thereby allowing the computational burden to be shared between the FPGAs. The XAUI is a low pin count, self-clocked, serial bus protocol directly evolved from the Gigabit Ethernet (GbE). The XAUI protocol supports data rates 2.5 times that of GbE, and by supporting communications over four serial "lanes" a 10 GbE communications link is achieved.

[0005] As mentioned above, for certain tests, it is desirable to communicate data between FPGAs in order to share a computational process, and multi-gigabit serial transceivers provide a mechanism to achieve the desired data transfer via a relatively small number of differential tracks constituting a communications link coupling the transceivers. Also, at least one known test requires data received by the test equipment from a network under test to be sent back to the network under test. Therefore, another application exists for an FPGA, that is part of a receiver unit of the test equipment, to comprise a first multi-gigabit serial transceiver so as to permit communication of received data to another FPGA, that is part of a transmitter unit of the test equipment, the another FPGA comprising a second multi-gigabit serial transceiver.

example, the American National Standards Institute (ANSI) Synchronous Optical NETwork (SONET) standard. Of course, data conforming to other standards, such as the Synchronous Digital Hierarchy (SDH) standard can also be processed. Indeed, in the case of a network analyser unit capable of testing both 10 GbE signals and SONET/SDH signals, the communications link between the FPGAs should be able to support the respective data rates associated with the signal types to be tested, for example 10 Gbps for the GbE packets, or 9.953280 Gbps for SONET OC-192 frames.

[0007] One known multi-gigabit serial communications specification for communicating data between FPGAs supports data communications at a rate of 10 Gbps. As mentioned above, one of the various data rates supported by the SONET standard is 9.953280 Gbps for OC-192 frames. A data rate mismatch therefore clearly exists if an inter-FPGA multi-gigabit serial communications link is used to communicate SONET OC-192 frames, which if not removed, will result in discrete-time jitter and data loss.

[0008] In order to facilitate the transfer of an incoming data stream, between FPGAs using the multi-gigabit serial transceivers, when the data rate of the incoming data stream and the data rate of the multi-gigabit serial transceivers are different, it is known to provide an apparatus which adapts a clocking frequency of the multi-gigabit serial transceivers to match the clock frequency of the incoming data stream. The frequency matching is performed, for example, by coupling FPGAs to external components such as a Phase Locked Loop (PLL) based clock generator, or a Voltage Controlled X Oscillator based clock generator, both of which are described in the XILINX Application Note entitled "SONET Rate Conversation in Virtex-II Pro Devices" (Application Note: Virtex-II Pro Family, XA pp649 (v1.1), May 14, 2002).

[0009] However, such known apparatus disadvantageously use external components, thereby increasing manufacturing overheads. Also, maintaining accuracy of clock synchronization is difficult and complex to achieve. Furthermore, once the apparatus is programmed to be adaptive to a specific incoming data stream dock frequency, the apparatus must be reprogrammed should a data stream of a different frequency be received.

[0010] According to a first aspect of the present invention, there is provided a method of communicating a data stream from a first communications unit of a first programmable logic device to a second communications unit of a second programmable logic device at a first data rate, the data stream comprising a plurality of data units and having a second data rate associated therewith, the method comprising the steps of: the first communications unit receiving the data stream; generating idle units and transmitting the idle units to the second communications unit when data is unavailable to be transmitted to the second communications unit; and wherein the first data rate is greater than or substantially equal to the second data rate.

[0011] In the context of communication of a data stream, an idle unit is a bit pattern indicative of an absence of bits constituting the communication of at least part of the data stream.

[0012] The method may further comprise the step of: temporarily storing the data constituting the data stream

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