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Curd et al.

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(54) **PARTIAL RECONFIGURATION OF A PROGRAMMABLE LOGIC DEVICE USING AN ON-CHIP PROCESSOR**

(75) Inventors: **Derek R. Curd**, Woodside, CA (US); **Punit S. Kalra**, Superior, CO (US); **Richard J. LeBlanc**, Longmont, CO (US); **Vincent P. Eck**, Loveland, CO (US); **Stephen W. Trynosky**, Boulder, CO (US); **Jeffrey V. Lindholm**, Longmont, CO (US); **Trevor J. Bauer**, Boulder, CO (US)

(73) Assignee: **Xilinx, Inc.**, San Jose, CA (US)

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(52) **U.S. Cl.** **716/16**; 716/17; 716/18; 326/39; 326/41
(58) **Field of Search** 716/1–2, 7–8, 716/12, 16–18, 20; 326/40, 41, 38

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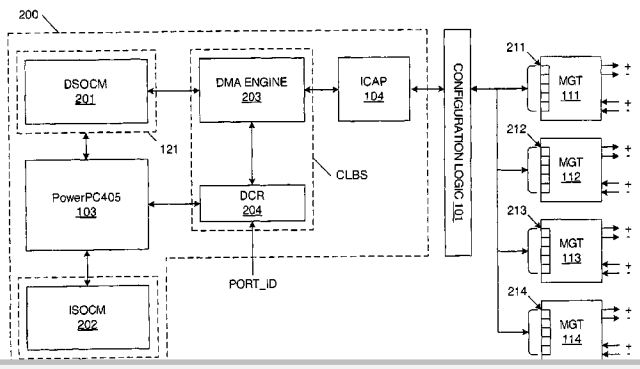
Primary Examiner—Vuthe Siek
Assistant Examiner—Binh Tat
(74) *Attorney, Agent, or Firm*—E. Eric Hoffman; B. Hoffman

(57) **ABSTRACT**

A programmable logic device, such as a field programmable gate array, is partially reconfigured using a read-modify-write scheme that is controlled by a processor. The partial reconfiguration includes (1) loading a base set of configuration data values into a configuration memory array of the programmable logic device, thereby configuring the programmable logic device; (2) reading a first frame of configuration data values from the configuration memory array; (3) modifying a subset of the configuration data values in the first frame of configuration data values, thereby creating a first modified frame of configuration data values; and (4) overwriting the first frame of configuration data values in the configuration memory array with the first modified frame of configuration data values, thereby partially reconfiguring the programmable logic device. The steps of reading, modifying and overwriting are performed under the control of a processor.

19 Claims, 5 Drawing Sheets



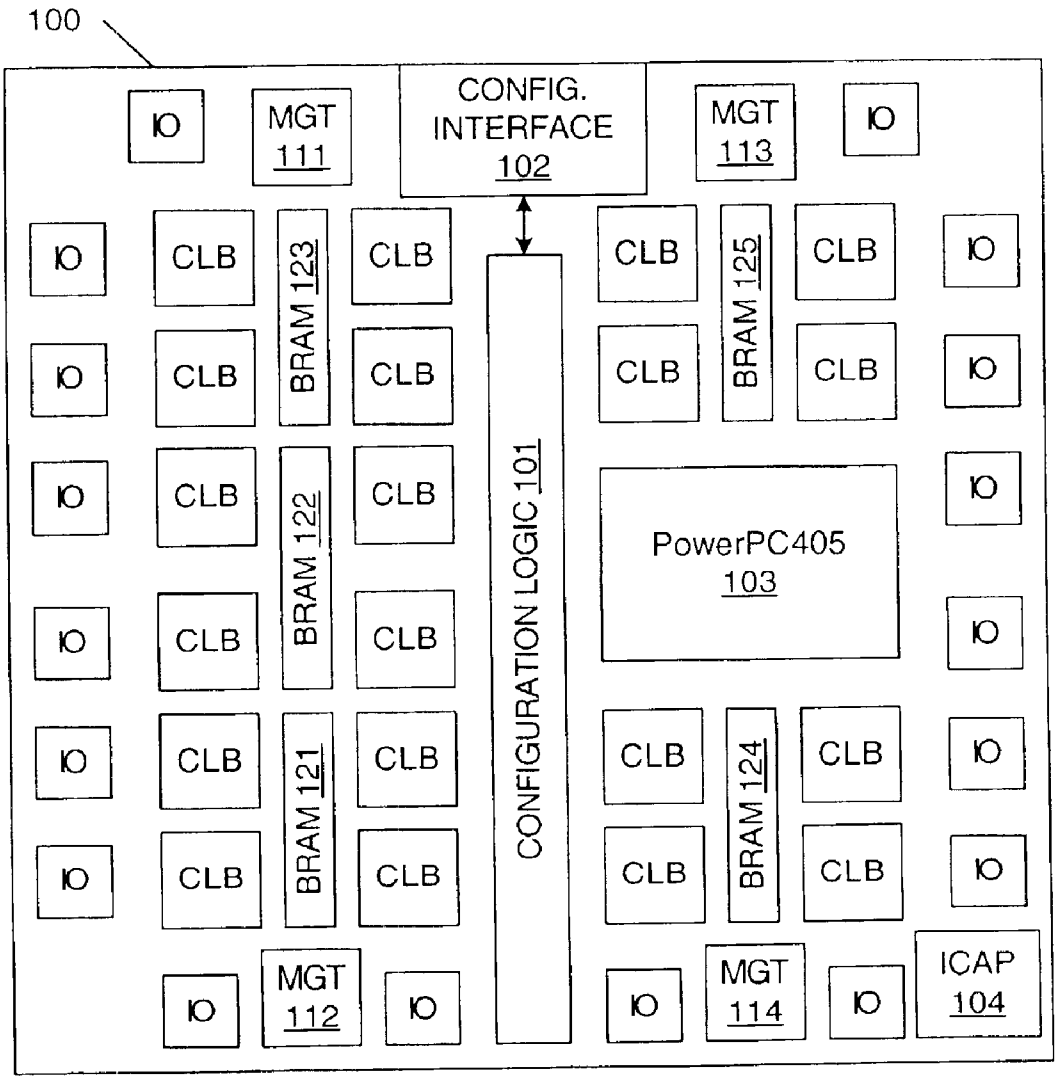


FIG. 1
(PRIOR ART)

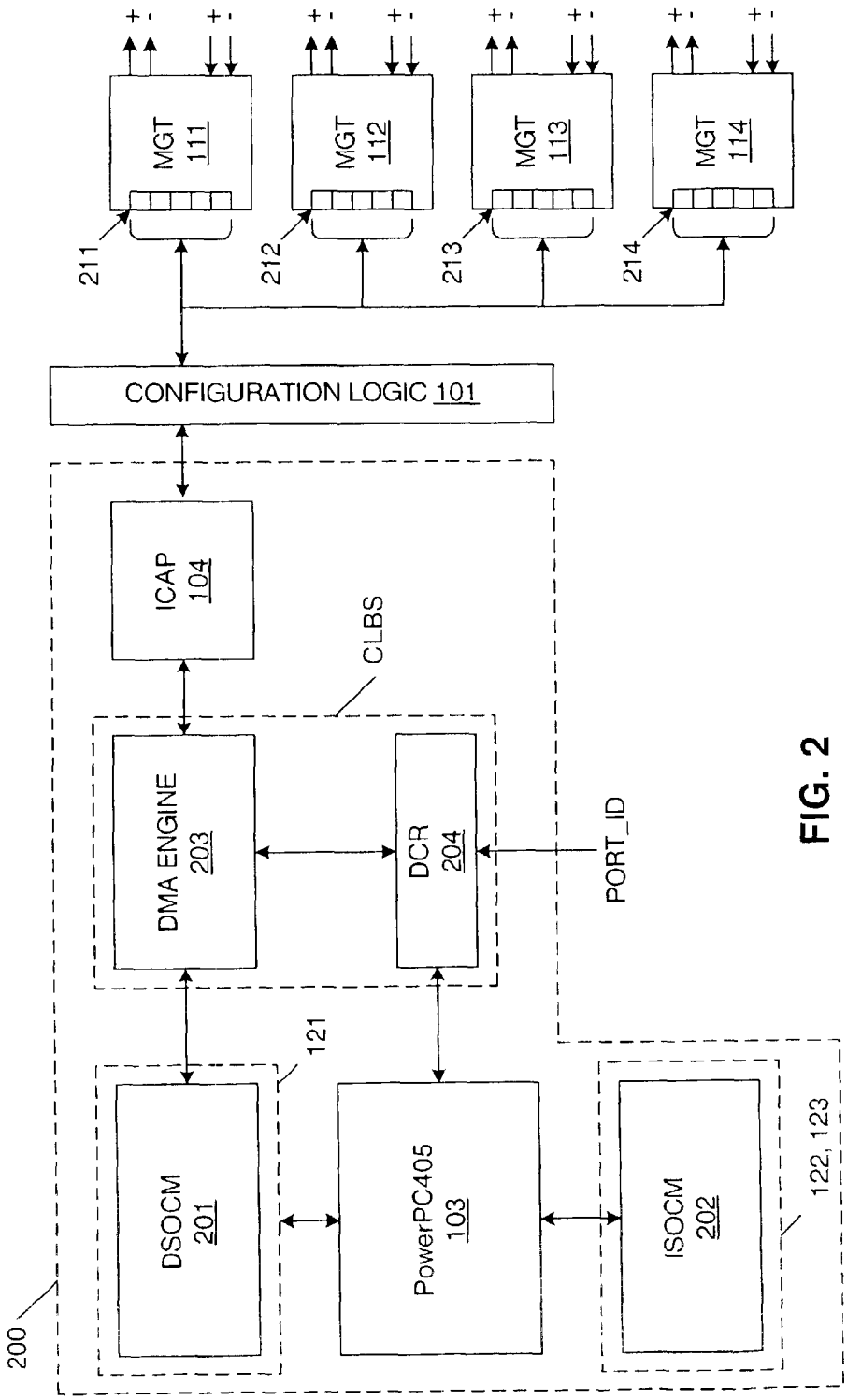


FIG. 2

FIG. 3

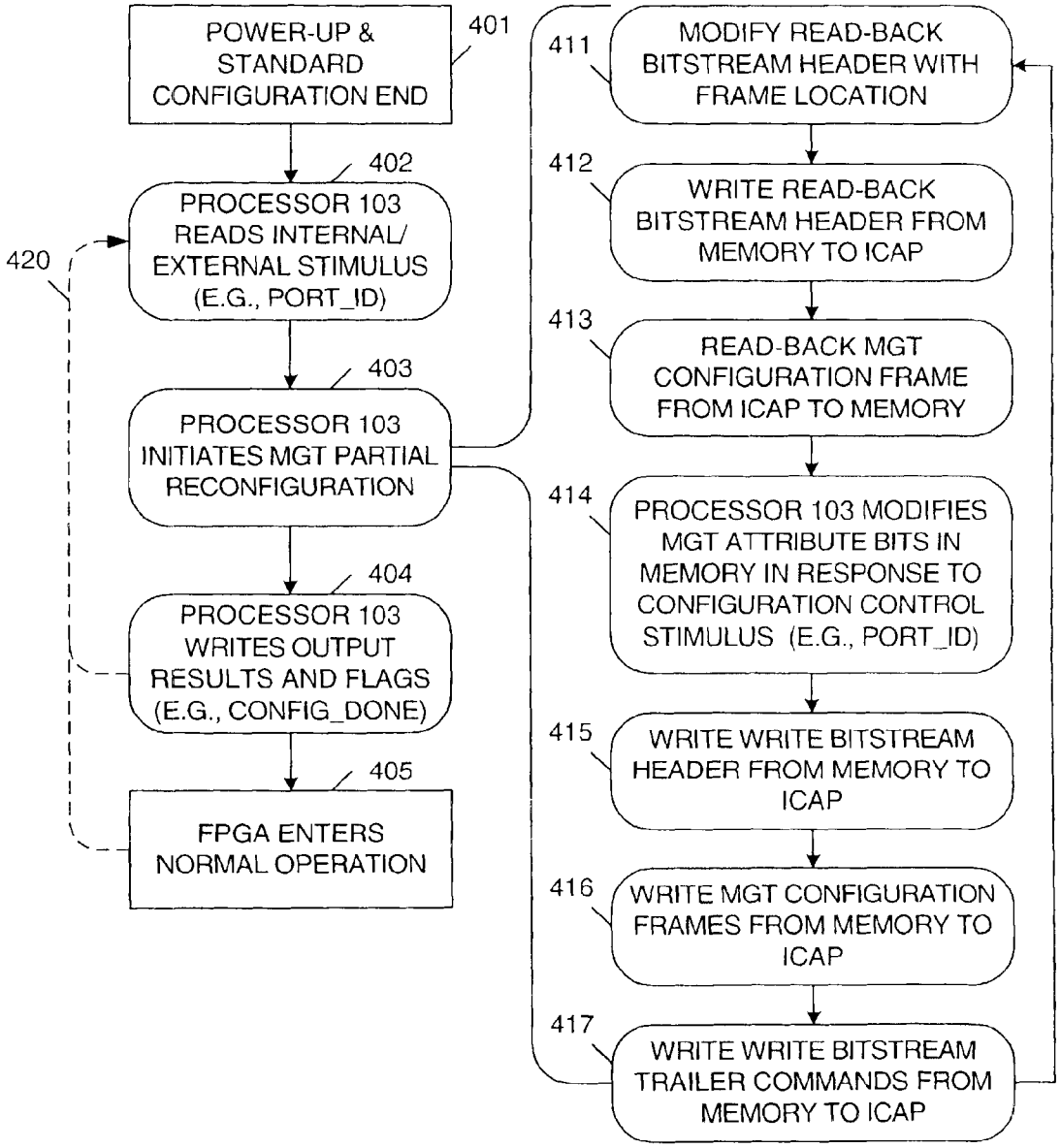


FIG. 4

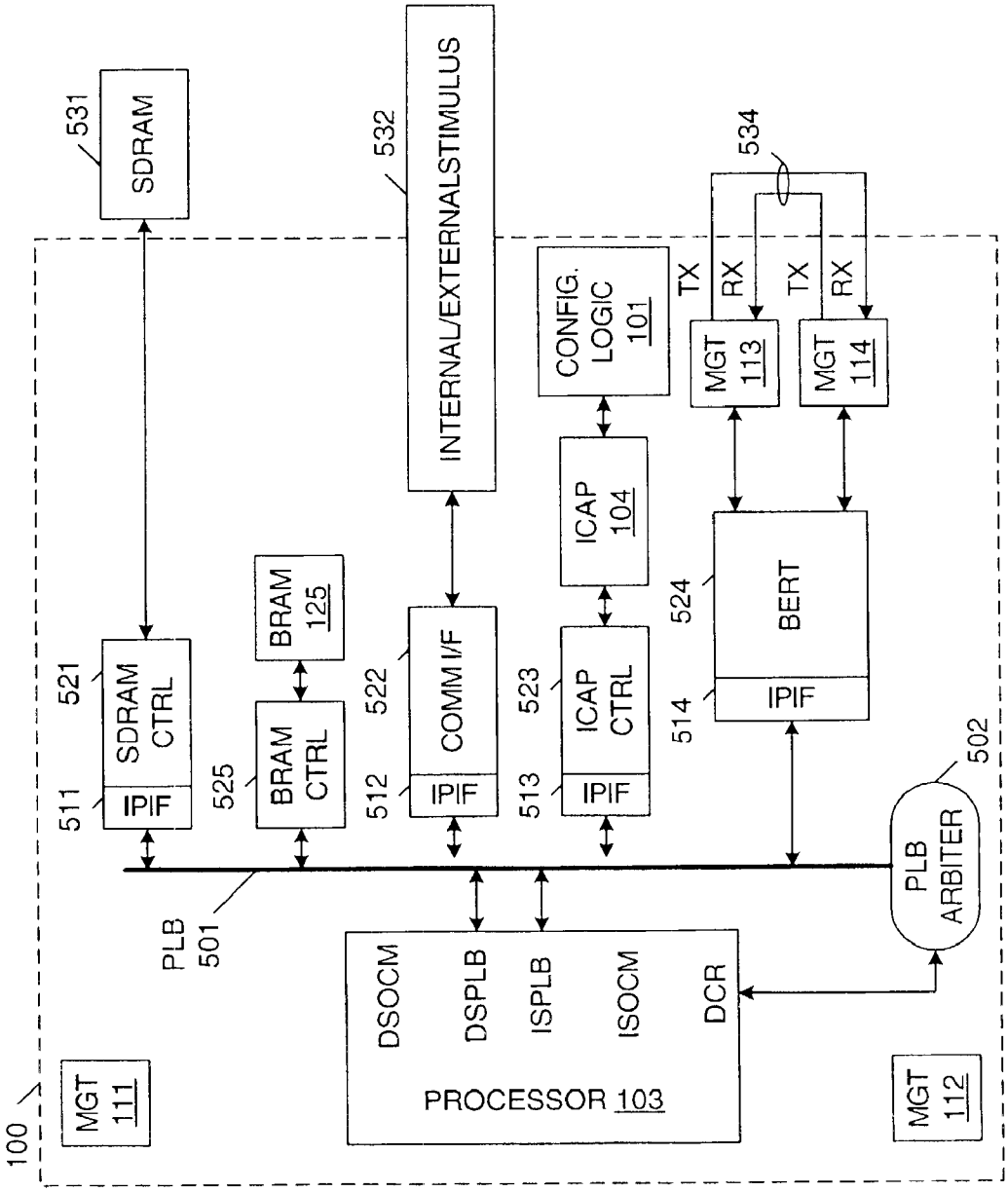


FIG. 5

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