UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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CISCO SYSTEMS, INC.,
Petitioner

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IPR2023-01047
U.S. Patent No. 7,921,323

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DECLARATION OF DANIEL BLUMENTHAL UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW

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I, Daniel Blumenthal, do hereby declare as follows:

I. INTRODUCTION

1. I am making this declaration at the request of Cisco Systems, Inc. in the matter of the *Inter Partes* Review of U.S. Patent No. 7,921,323 ("the '323 Patent") to Yancey et al.

2. I am being compensated for my work in this matter at my standard hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this proceeding. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

3. I have been asked to provide my opinions regarding whether the subject matter of claims 27-28, 31, and 33 ("the Challenged Claims") of the '323 patent would have been obvious to a person having ordinary skill in the art ("POSITA") at the time of the alleged invention, in light of the prior art. It is my opinion that the Challenged Claims would have been obvious to a POSITA.

4. In the preparation of this declaration, I have relied on:

- the '323 patent, Ex. 1001;
- the prosecution history of the '323 patent ("'323 File History"), Ex. 1002;
- U.S. Patent Publication No. 2002/0059274 to Hartsell et al. ("Hartsell"), Ex. 1005;

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- U.S. Patent No. 6,496,291 to Raj et al. ("Raj"), Ex. 1007; and
- Scott Hauck, "The Roles of FPGA's in Reprogrammable Systems," Proceedings of the IEEE, vol. 86, no. 4 (April 1998).

5. In forming the opinions expressed below, I have considered the documents listed above; the relevant legal standards, including the standard for obviousness; and my own knowledge and experience based upon my work in the field of field of communication networks as described below, as well as portions of the following additional materials:

- U.S. Patent No. 6,907,595 to Curd et al., Ex. 1006;
- Microsoft Press, *Computer Dictionary*, Third Edition, 1997, Ex. 1009;
- "Virtex-II Pro™ Platform FPGAs: Introduction and Overview," Xilinx, March 24, 2003, Ex. 1010;
- "Virtex-II Pro™ Platform FPGA User Guide," Xilinx, June 30, 2003, Ex. 1011;
- U.S. Patent No. 7,680,054 to Acharya, Ex. 1013;
- U.S. Patent No. 7,039,057 to Acharya et al., Ex. 1014;
- U.S. Patent No. 7,382,787 to Barnes et al., Ex. 1015;

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