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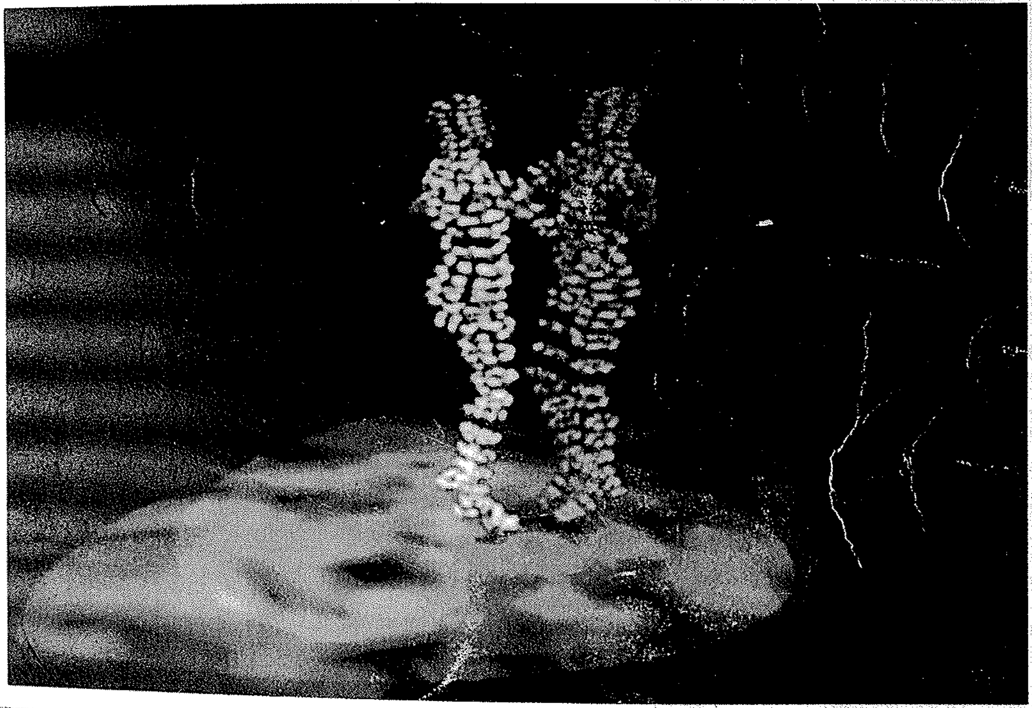

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A frame from an animation created by Michaela Zambrans of the Graphics Research Lab, Simon Fraser University, using LifeForms and Vertigo software.

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Couverture
Un image d'une animation, créé par Michaela Zambrans du laboratoire d'infographie de l'université Simon Fraser, utilisant LifeForms et Vertigo.

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A Simple, Flexible, Parallel Graphics Architecture

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ABSTRACT

Traditional graphics hardware architectures, with their emphasis on the graphics pipeline, are becoming less useful. As graphics algorithms evolve and grow more capable, it becomes much harder to implement them in silicon. By using general-purpose hardware technology effectively, one can build powerful graphics hardware that is very flexible, yet inexpensive. In this paper we would like to discuss one such architecture that allows for both traditional interactive graphics (polygon scan conversion) as well as more advanced graphics (ray tracing and radiosity).

KEYWORDS

computer graphics hardware

INTRODUCTION

The graphics pipeline has had a long history in computer graphics [1]. Consisting of a front end that performs simple, repetitive floating point calculations on short vectors (for transformations, clipping, perspective) and a back end that scan converts primitives into pixels and determines visibility, it easily became a candidate for hardware acceleration [2, 3, 4]. However, as graphics algorithms evolve and become more capable the utility of this specialized hardware is reduced. The required functionality can no longer be incorporated easily in hardware and instead must increasingly be performed in software on the host system.

VLSI technology is squeezing more and more onto a chip. However, designing a special-purpose chip is getting harder as more functionality is added. This is especially true of custom graphics chips. Most effort in semiconductor houses is now being put into creating more powerful microprocessors and ever larger DRAMs and VRAMs.

In this paper we want to explore an architecture that tries to take advantage of the growing power of VLSI by concentrating on these general-purpose products and using them effectively. We wanted an architecture that minimized graphics hardware. The result, we believe, is an inexpensive, powerful and flexible system.

As well, we will describe a design that utilizes this architecture. The origin of this design came from our experiences with the AT&T Pixel Machine. We wanted to produce a low-cost next-generation machine. Let us first review architecture of the Pixel Machine.

THE PIXEL MACHINE

The Pixel Machine (PXM) was designed as a programmable computer subsystem with pipeline and parallel processing closely coupled to a display system [5]. Built by Pixel Machines Corp, a subsidiary of AT&T, it was launched in 1987. An important design goal was flexibility. Graphics algorithms were not hardwired into the design. Instead, digital signal processors (DSP32) were the basic building blocks (nodes) of the PXM. This allowed for a lot of flexibility as new functionality could be programmed in afterwards. In fact, most of the algorithms were written in C with only the critical sections written in assembler. This resulted in a product that was ideal for research and development.

The PXM consisted of a large box (containing up to 20 VME boards) which was connected to the host computer via a series of registers in the memory address space of the host computer. Data and commands reaching the PXM would first be sent through a pipeline board consisting of nine DSP32 *pipe nodes*. For interactive graphics, the pipe nodes would do transformations, clipping and lighting calculations for the various graphics primitives. A second pipeline board could be added to the PXM to increase performance.

Next, the primitives would be broadcast to 16-64 (depend-

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