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Morein et al.

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(54) **GRAPHICS PROCESSING ARCHITECTURE EMPLOYING A UNIFIED SHADER**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

(63) Continuation of application No. 12/791,597, filed on Jun. 1, 2010, now abandoned, which is a continuation of application No. 11/842,256, filed on Aug. 21, 2007, now abandoned, which is a continuation of application No. 11/117,863, filed on Apr. 29, 2005, now Pat. No. 7,327,369, which is a continuation of application No. 10/718,318, filed on Nov. 20, 2003, now Pat. No. 6,897,871.

(51) **Int. Cl.**
G06F 15/00 (2006.01)

(52) **U.S. Cl.**
USPC **345/501**

(58) **Field of Classification Search**
CPC G06T 15/005; G06T 15/80; G06T 1/20; G06T 1/60; G09G 5/363; G06F 3/14
USPC 345/501
See application file for complete search history.

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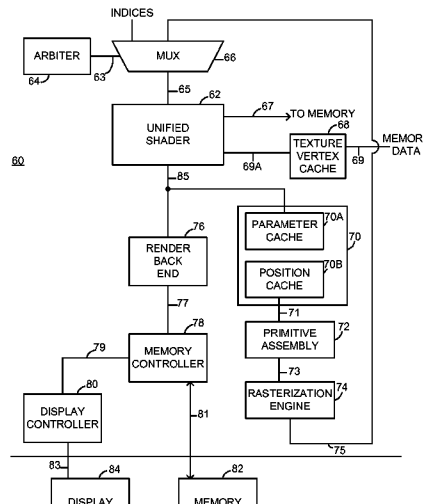*Primary Examiner* — Kee M Tung
Assistant Examiner — Frank Chen
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(57) **ABSTRACT**

A graphics processing architecture in one example performs vertex manipulation operations and pixel manipulation operations by transmitting vertex data to a general purpose register block, and performing vertex operations on the vertex data b a processor unless the general purpose register block does not have enough available space therein to store incoming vertex data; and continues pixel calculation operations that are to be or are currently being performed the processor based on instructions maintained in an instruction store until enough registers within the general purpose register block become available.

11 Claims, 5 Drawing Sheets
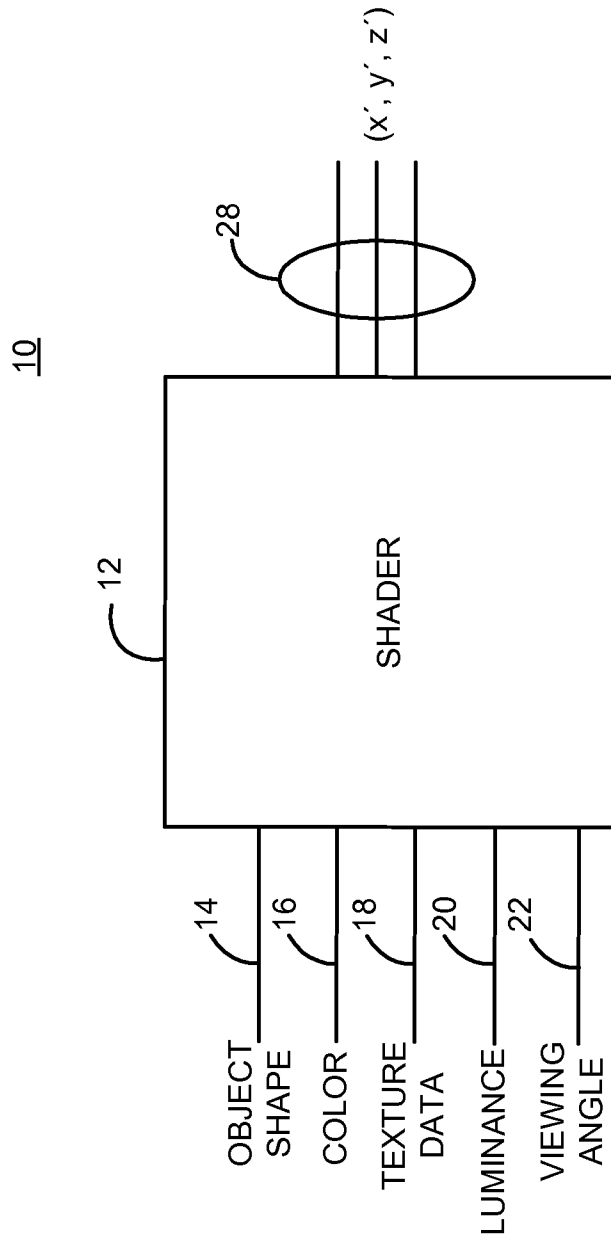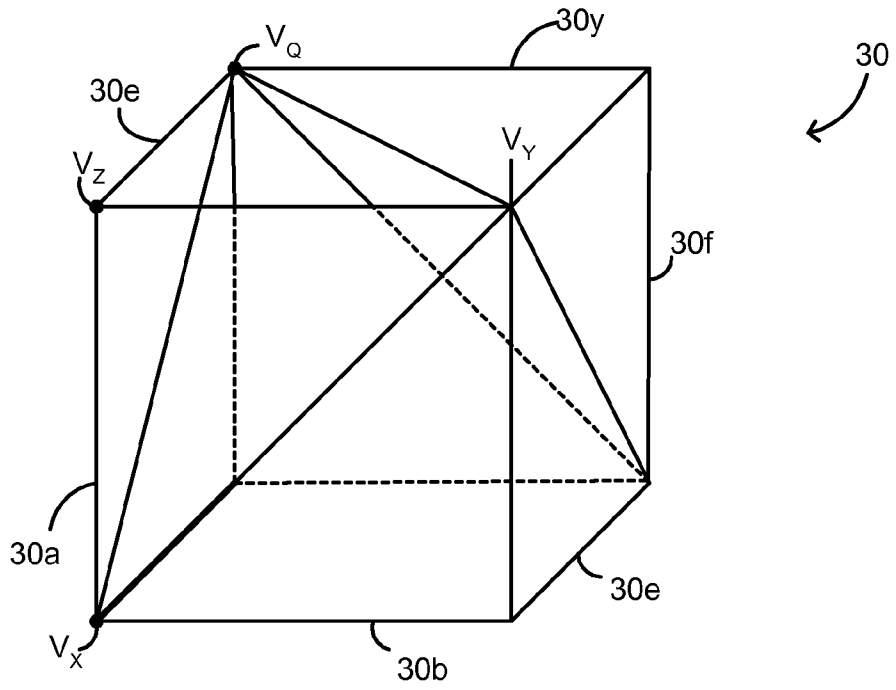
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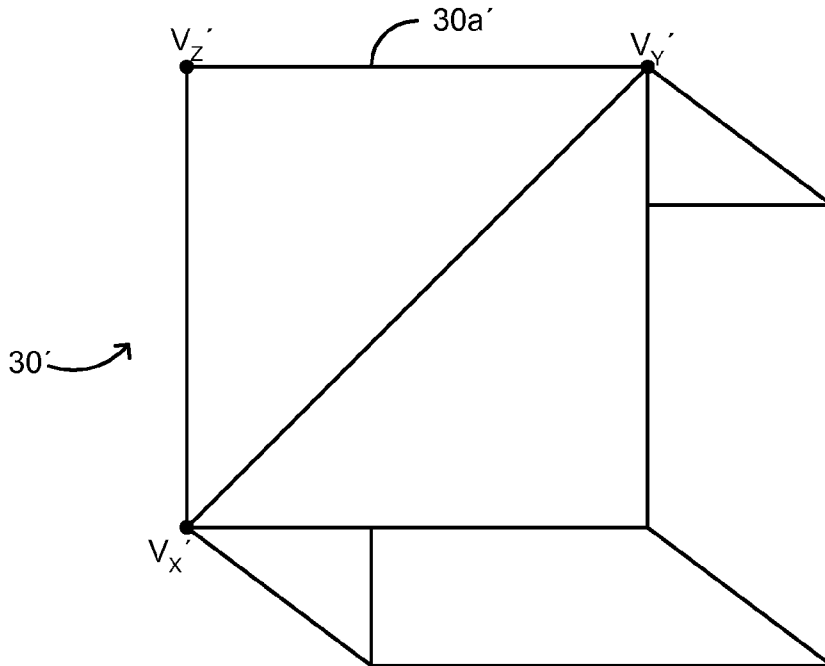Chinese Office Action; Chinese Application No. 2004800405708; dated Sep. 2010.

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OBJECT
SHAPE

COLOR

TEXTURE
DATA

LUMINANCE

VIEWING
ANGLE

SHADER

(x′, y′, z′)

**FIG. 1
(PRIOR ART)**

FIG. 2A
(PRIOR ART)

FIG. 2B
(PRIOR ART)

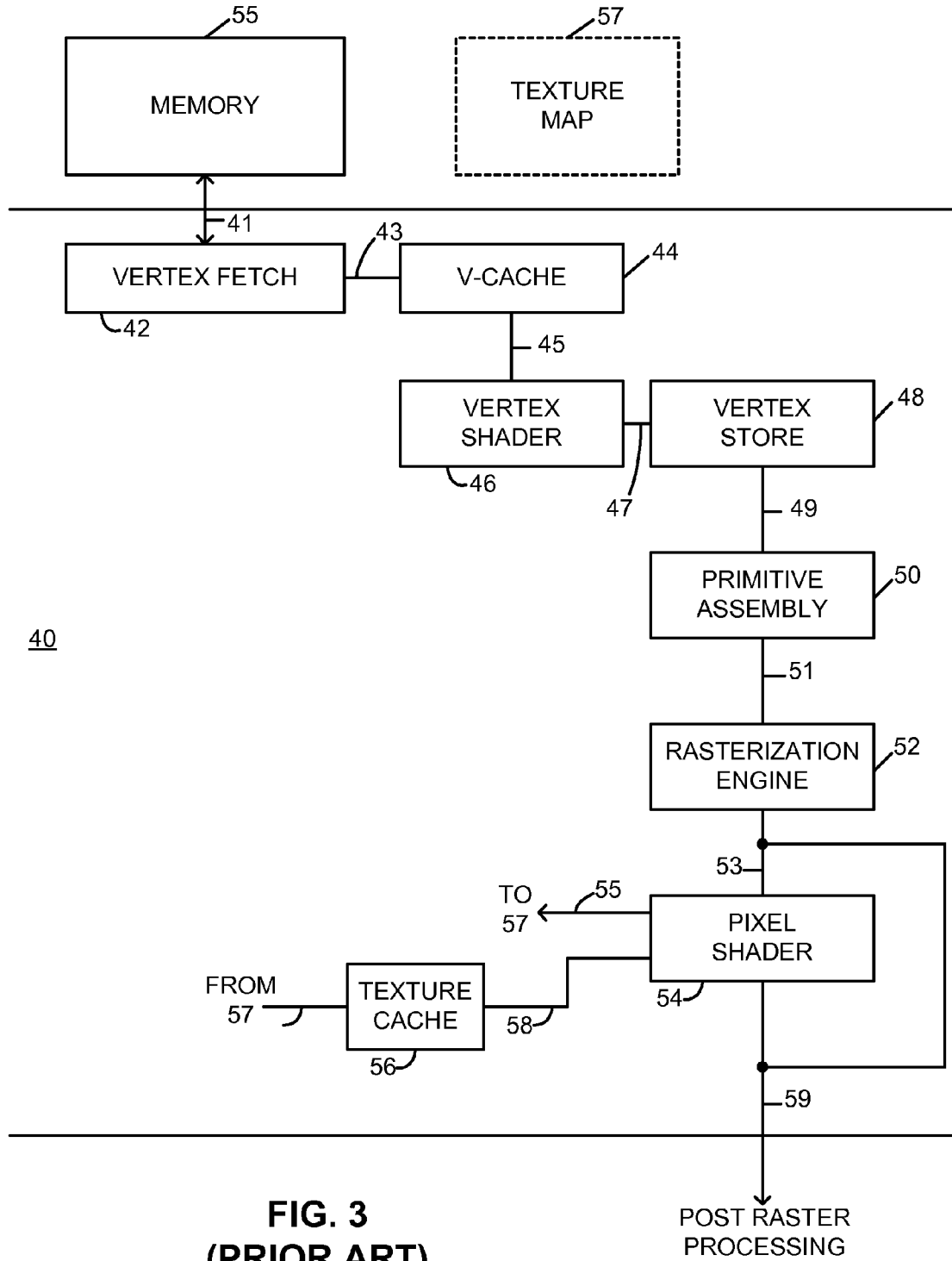**FIG. 3**
(PRIOR ART)

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