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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.,
Petitioner,

v.

ATI TECHNOLOGIES ULC,
Patent Owner.

Case IPR2015-00326
Patent 6,897,871

DECLARATION OF INVENTOR LAURENT LEFEBVRE
REGARDING THE INVENTION DATE OF U.S. PATENT NO. 6,897,871

Mail Stop "Patent Board"
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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LG Ex. 1037
LG v. ATI
IPR2015-00330

ATI 2006
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I, Laurent Lefebvre, declare as follows:

I. BACKGROUND

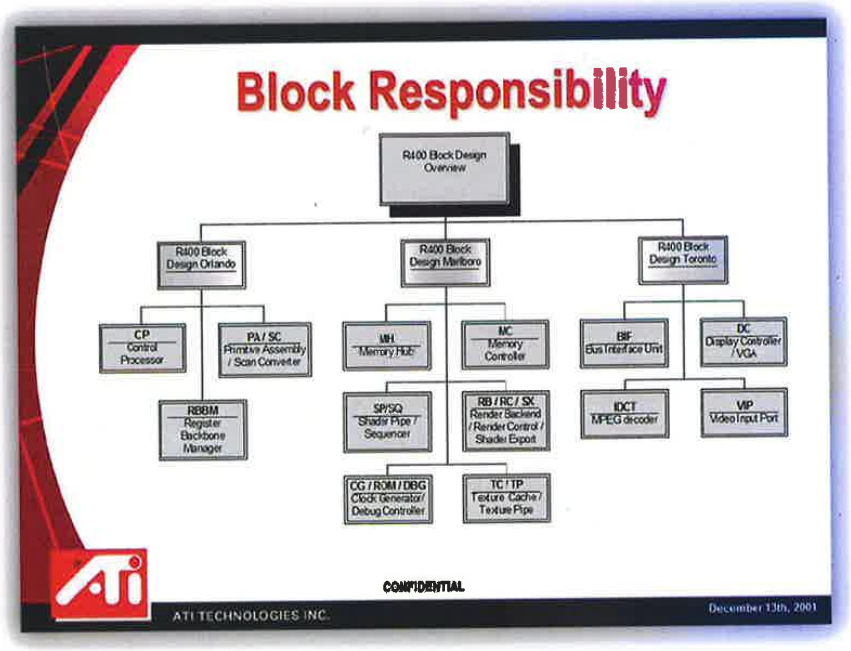
1. I am a computer-graphics hardware architect at AMD Inc. I have been designing computer-graphics processors for the past fifteen years. I specialize in sequencers, shaders, 3D-computer graphics, and integrated-circuit design.

2. From September 2000 to November 2006, I worked as an engineer and hardware architect for ATI Technologies Inc. ("ATI"). It is my understanding that ATI hired me to develop technologies for the R400, which is a graphics processor. Information relating to ATI's development of the R400 is confidential and proprietary. If this information became public, it would put ATI/AMD at a competitive disadvantage because it would give ATI/AMD's competitors access to proprietary algorithms, implementation details, and development schedules for the R400 design.

3. Unlike conventional graphics processors at the time, the R400 used a unified shader for both pixel commands and vertex commands—two types of commands required to produce an image. Conventional graphics processors had separate shaders for pixel commands and vertex commands. But a unified shader, like the R400's unified shader, enhances functionality and efficiency by allowing the same shader complex to be used for both pixel commands and vertex

commands. The R400's unified-shader architecture was later included in a chip called the Xenos chip. The Xenos chip was in the Microsoft® Xbox 360®.

4. The R400 includes many different functional blocks (e.g., the sequencer, shader pipe, primitive assembly, texture cache, texture pipe, raster engine, display, etc.). *See, e.g.*, Ex. 2053, p. 6. The PowerPoint slide titled Block Responsibility (reproduced below) shows the ATI office responsible for designing each block.



Id.

[redacted]

5. For the R400 project, I was responsible for the sequencer block, which is the block that manages the execution of pixel commands and vertex commands for the unified shader. In particular, I drafted the high-level specification that describes the sequencer block's functionality, and I wrote emulator code for the sequencer block. In addition, I was also co-responsible for emulating the shader pipe block and the export block.

6. I am one of the named inventors of U.S. Patent No. 6,897,871 ("the '871 patent"). The other named inventors are Steve Morein, Andy Gruber, and Andi Skende. We collectively conceived of the graphics-processing system claimed in the '871 patent no later than early 2002, while working on the R400. *See infra* Part II. A team of my colleagues and I, which totaled about one hundred engineers, worked on the R400 nearly every business day from no later than early 2002 to November 20, 2003. *See infra* Parts III, V. No later than the third quarter of 2002, we made a GPU in register-transfer-language ("RTL") code that worked to process a first triangle. *See infra* Part IV.

II. CONCEPTION

7. No later than early 2002, Steve Morein, Andy Gruber, Andi Skende, and I collectively conceived of the graphics-processing system in the '871 patent. We each contributed different aspects to this system. Steve Morein came up with the idea for a unified shader. This is shown, for example, in documents titled

[redacted]

"R400 Architecture Proposal" and "R400 Top Level Specification." Ex. 2040, p. 1; Ex. 2041, p. 1. Andy Gruber was the lead architect for the shader pipe. Andy Gruber worked with Andi Skende to come up with ideas for implementing the shader pipe and author the shader processor specification. This is shown, for example, in a document titled "Shader Processor." Ex. 2042, p. 1. And I was the lead for the sequencer block. This is shown, for example, in a document titled "R400 Sequencer Specification." *E.g.,* Ex. 2007, p. 1. I explain each of these documents in turn below.

A. R400 Architecture Proposal

8. Steve Morein authored the "R400 Architecture Proposal." Ex. 2040, p. 1. In this proposal, the R400 includes a unified shader that performs both pixel operations and vertex operations. *See id.* at 9. The R400 also includes a unified processing pipe (i.e., a single programmable pipeline for 2D video, 3D vertex, and 3D pixel operations). *See id.* at 6 ("The most ambitious feature in this design is the 'truly unified pipe': a single programmable pipeline."). With a single pipeline for both pixel commands and vertex commands, the graphics processor had higher color precision and the ability to support more registers, compared with a conventional graphics pipeline. *See id.*

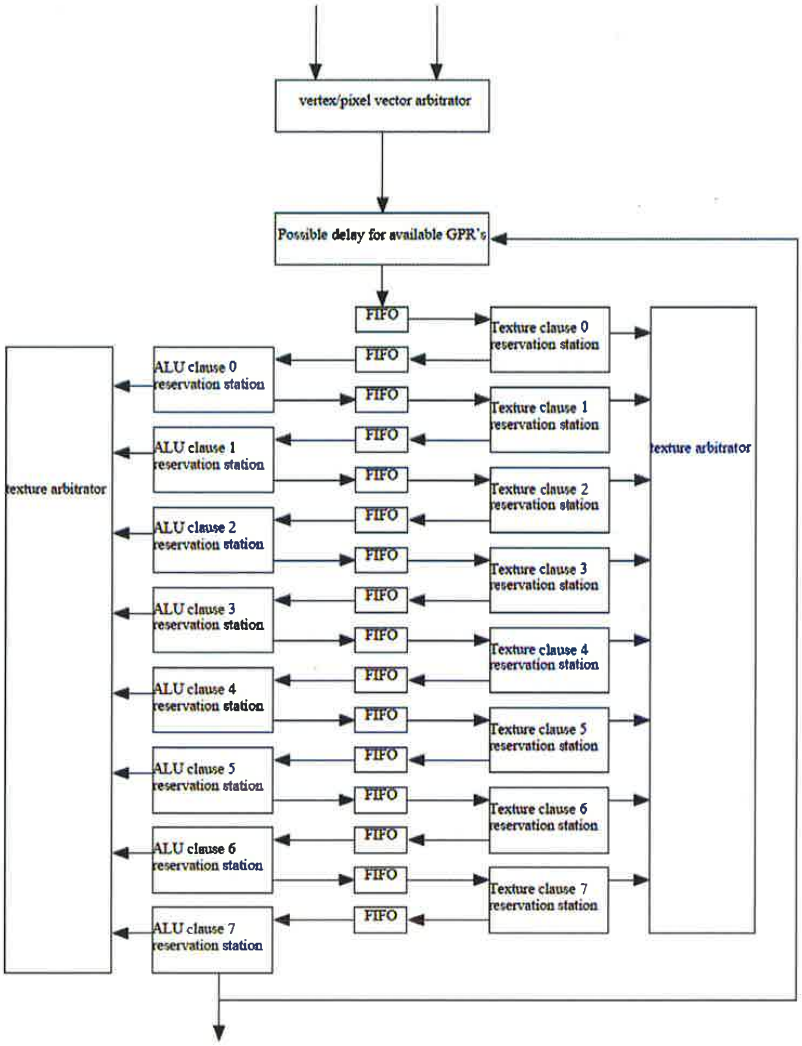
[redacted]

B. R400 Top Level Specification

9. Steve Morein also authored the "R400 Top Level Specification," which sets forth the high-level architecture for the R400. Ex. 2041, p. 1. As shown in this document, the R400 Top Level Specification includes a sequencer. *See e.g., id.* at 27-28, 30. The sequencer manages the instructions for the unified shader. *See id.* at 11 ("Before starting the processing . . . the rasterizer (which includes the sequencer for the shader pipeline) checks to make sure that there are enough free registers in the shader pipeline for the pixel shader program."), 27 ("The raster engine . . . contains the sequencer for the shader pipe.").

10. The R400 Top Level Specification includes a block diagram of the sequencer's control flow (reproduced below for reference).

[redacted]



Id. at 30.

[redacted]

11. This block diagram includes three arbitrators[1]: (1) a "vertex/pixel vector arbitrator" at the top of the diagram; (2) a "texture arbitrator" on the left side of the diagram; and (3) a "texture arbitrator" on the right side of the diagram. *See id.* The "texture arbitrator" on the left side is mislabeled. This arbitrator should be labeled "ALU arbitrator" to correspond to the ALU reservation stations. I describe the control flow for this block diagram in Part II.D.1 of this declaration.

C. R400 Shader Processor

12. Andy Gruber and Andi Skende authored the "Shader Processor," which describes the shader architecture, interfaces, partitioning, and timing of the shader. Ex. 2042, p. 1. The shader processor had four identical Shader pipelines in the R400 architecture, each pipe capable of operating on ALU instructions for vertex parameters and pixel values. *See id.* at 5

D. R400 Sequencer Specification

13. I authored the "R400 Sequencer Specification," which is the architectural specification for the R400 sequencer block. Ex. 2007, p. 1. There are

[1] The term "arbitrator" is interchangeable with the term "arbiter." *See, e.g.*, Ex. 2023, pp. 9-10 (identifying the control flow diagram as: "Figure 2: Reservation stations and arbiters").

[redacted]

at least thirty three revisions of this specification. *See* Ex. 2039, pp. 4-5; Exs. 2007-38. Each revision updates the specification.

14. I developed two versions of the sequencer's control flow. *See* Ex. 2010; Ex. 2028. When I filed the patent application that led to the '871 patent, I intended this patent application to cover both versions of the sequencer's control flow.

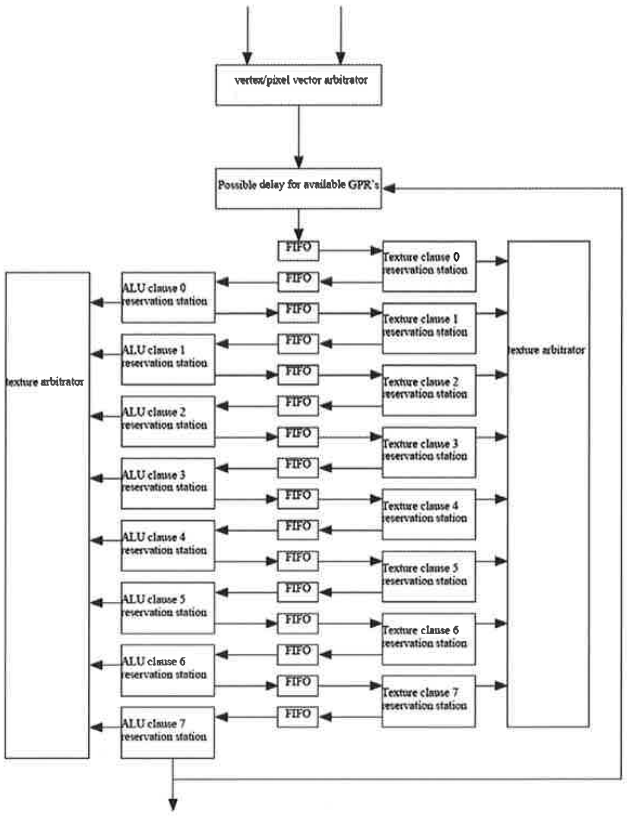
15. The first version, described in Version 0.4 of the R400 Sequencer Specification, was designed for sixteen vertex clauses and sixteen pixel clauses. *See* Ex. 2010, pp. 5, 14-15. ATI presented this version to Microsoft to see whether the R400 was compatible with the application-programming interface ("API") that Microsoft was developing, called DX10. Microsoft rejected this version because Microsoft's API required a sequencer that could process an unlimited number of clauses. To be compatible with this requirement, I developed a second version of the sequencer control flow. This second version is described in Version 2.0 of the R400 Sequencer Specification. *See* Ex. 2028. I explain these versions in turn below.

1. R400 Sequencer Specification (Version 0.4): August 24, 2001

16. Version 0.4 of the R400 Sequencer Specification is dated August 24, 2001. *See* Ex. 2010, p. 3; *see also* Ex. 2043 (for the log entry on August 24, 2001).

[redacted]

This version includes the same sequencer-block diagram as the sequencer-block diagram in the R400 Top Level Specification (reproduced again below for convenience). *Compare* Ex. 2010, p. 5 *with* Ex. 2041, p. 30. Version 0.4 also includes an example of the flow of pixels and vertices through the system. *See* Ex. 2010, pp. 3, 17-19.

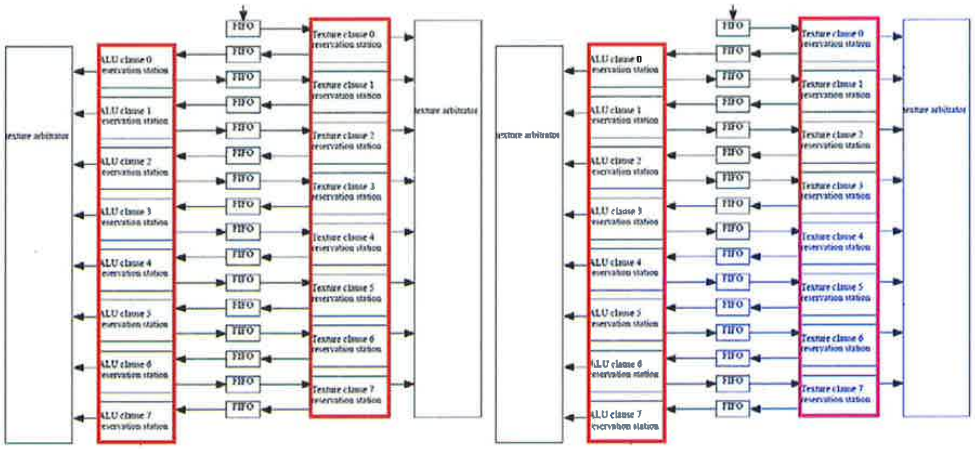


Ex. 2010, p. 5.

[redacted]

17. The sequencer has two sets of reservation stations, one for pixels and one for vertices. *Id.* at 4-5. A representation of the two sets of reservation stations is shown below. Each set has eight ALU reservation stations and eight texture reservation stations. *Id.* Each reservation station stores clauses. *Id.* These clauses contain a sequence of instructions. *Id.* at 4 ("[the sequencer] . . . executes all of the instructions in a clause"); *see also* Ex. 2042, p. 7 ("instructions in a clause will be executed sequentially").

Pixel Reservation Stations Vertex Reservation Stations



18. Clauses flow down each set of reservation stations. *See* Ex. 2010, pp. 4-5. Pixel clauses flow down the set of pixel reservation stations, and vertex clauses flow down the vertex reservation stations. *See id.* Reservation stations touch the arbiter, so the ALU arbiters and the texture arbiters can select clauses traveling down the reservation stations. *See id.* at 17 ("the control packet continues

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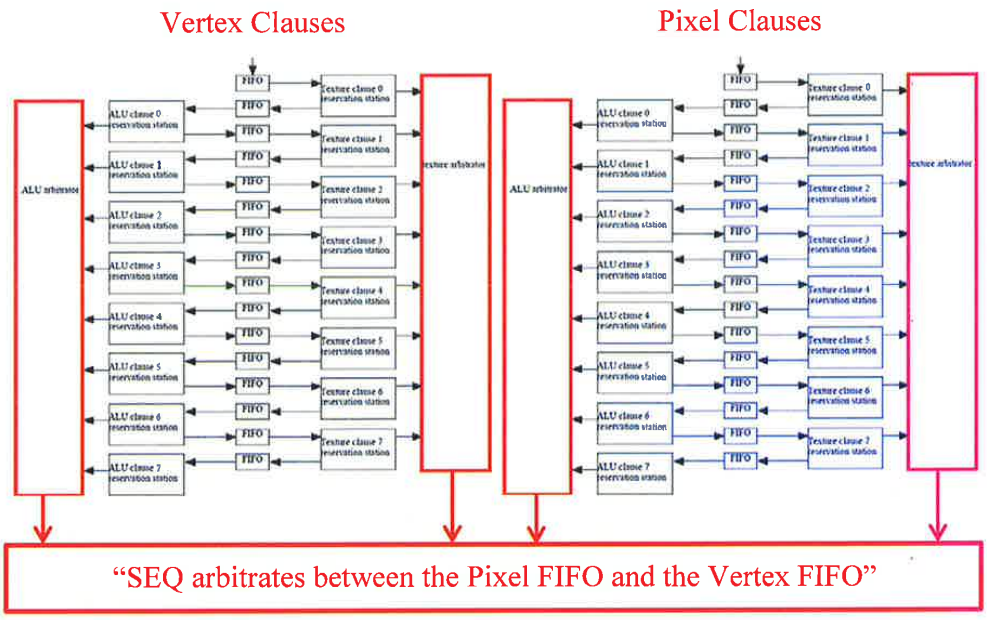
to travel down the path of reservation stations until all clauses have been executed").

19. The arbiter/arbitration logic has two levels of arbitration, collectively shown in red on the figure below.



20. The first level of arbitration is between ALU clauses and texture clauses for both the vertex set of reservation stations and the pixel set of reservation stations. This first level of arbitration is represented by the ALU arbitrators and texture arbitrators labeled in the figure above. ALU arbitration logic

[redacted]

chooses one of the eight potentially pending ALU clauses stored within the ALU reservation stations. *See id.* at 14-15. Texture arbitration logic chooses one of the eight potentially pending texture clauses stored within the texture reservation stations. *See id.* at 14.

21. For the second level of arbitration, the arbitration logic selects between the pixel and the vertex. *See id.* at 17 (2) ("SEQ arbitrates between the Pixel FIFO and the Vertex FIFO"), 18 (4) ("SEQ arbitrates between Pixel FIFO and Vertex FIFO"). So, not only does the arbiter select which clauses to execute, the arbiter also selects which order to execute pixels and vertices. *See id.* at 4 ("a pixel can pass a vertex and a vertex can pass a pixel").

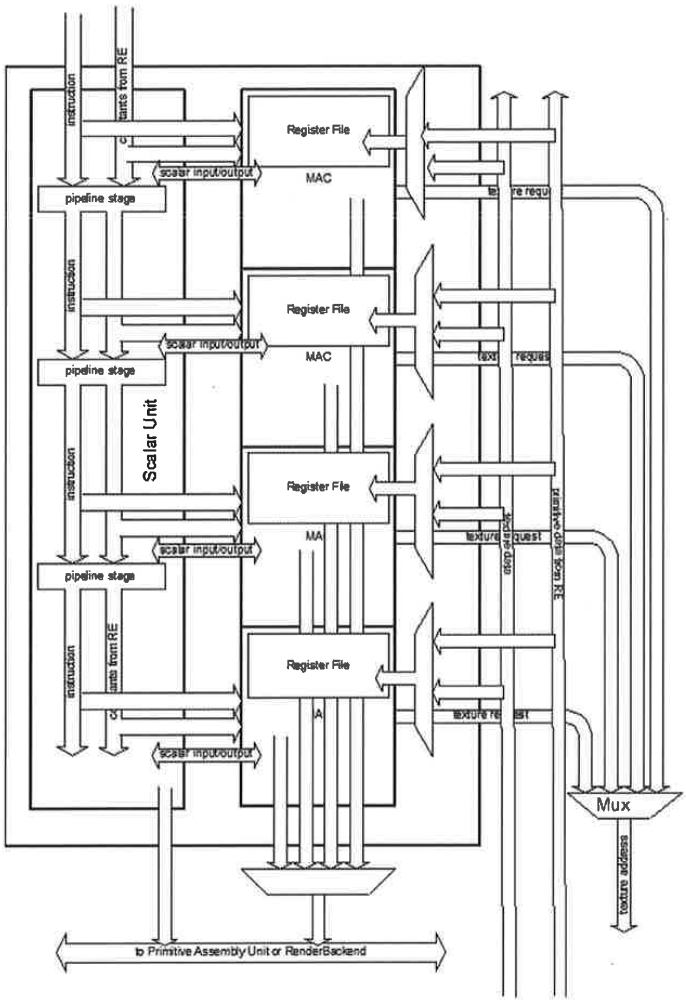
22. The ALU arbitration and the texture arbitration give priority to reservation stations/clauses closer to the bottom of the pipeline. *See id.* After this arbitration selects winning pixel and vertex clauses, the pixel/vertex arbitration logic selects between the pixel and the vertex. *Id.* at 17 (2), 18 (4). Vertices generally have priority. *Id.* at 17 (2). When a vertex is not pending or the register files do not have open space for a vertex, the arbiter selects a pixel. *Id.* at 18 (4).

23. Once arbitration logic selects the pixel/vertex clauses, the sequencer's arbitration logic provides the clauses to a register file in the shader pipe. *See id.* at pp. 17 (5) ("SEQ constructs a control packet for the vector and sends it to the first

[redacted]

reservation station (the FIFO in front of texture state machine 0, or TSM0 FIFO) the control packet contains the state pointer, the tag to the position cache and a register file base pointer."), 17 (9) ("ASM0 accepts the control packet (after being selected by the ASM arbiter) and gets the instructions for ALU clause 0 from the global instruction store").

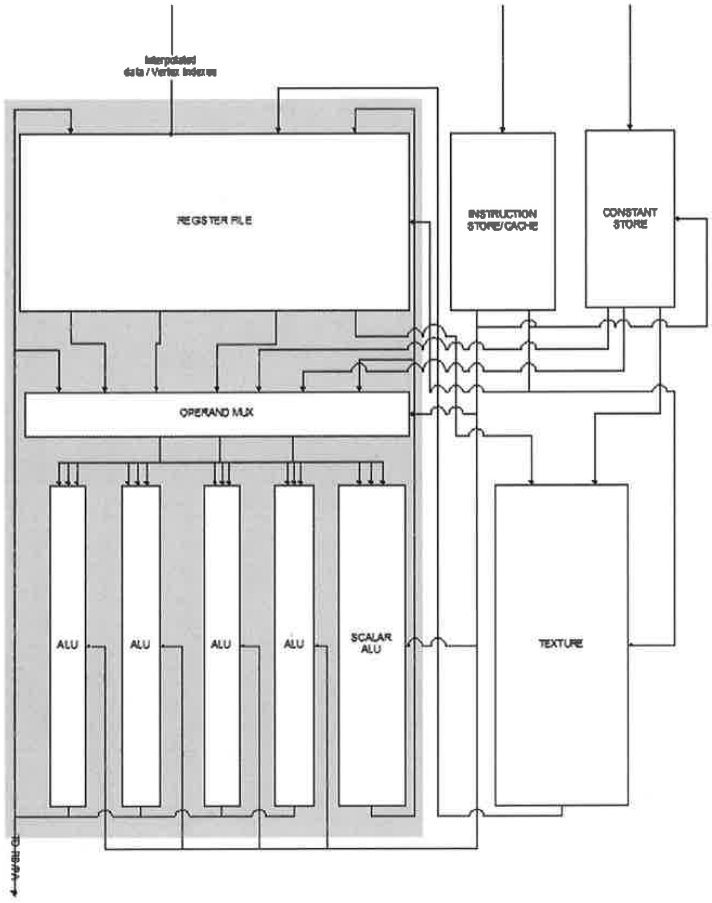
24. The shader pipe, as of Version 0.4 of the R400 Sequencer Specification (reproduced below for reference), has four physical register file memories per shader pipeline. *Id.* at 10.



Id.

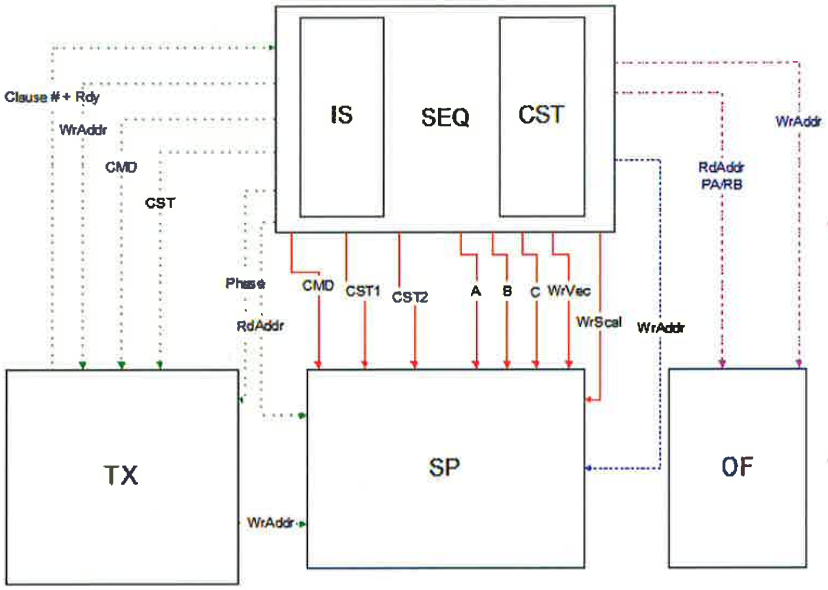
25. Each register file is coupled to a bank of ALUs. *See id.* at 11. The gray area of the Figure reproduced below shows the logical view of the four register files within the shader pipe as software would see it. *Id.* The Figure also

shows an ALU bank, a texture unit, an instruction store/cache, and a constant store. *See id.*



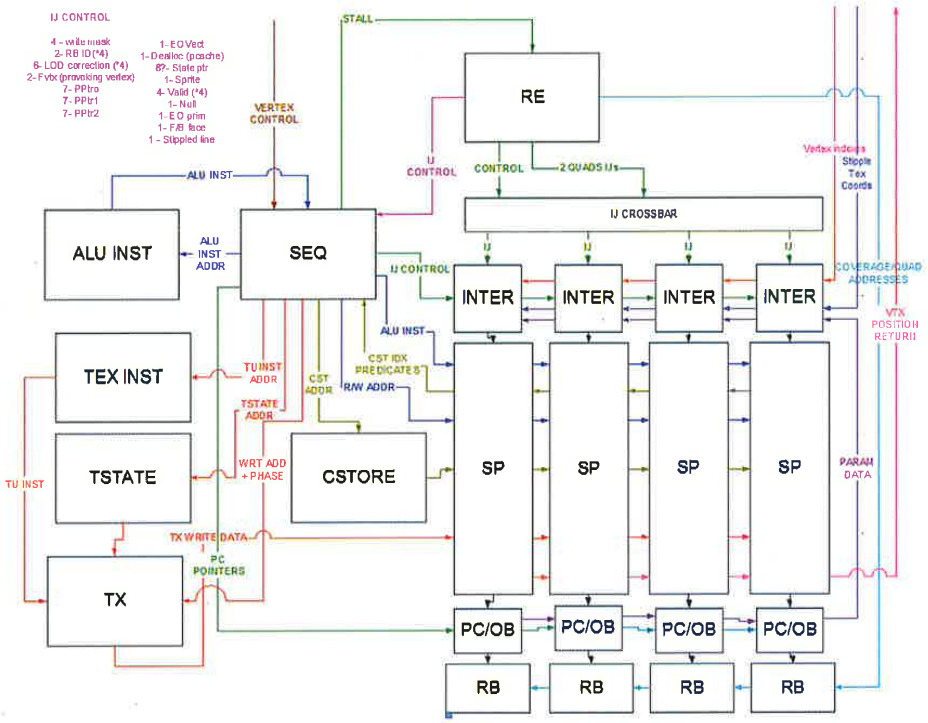
Id.

26. In the Figure reproduced above, the sequencer block comprises the instruction store and the constant store. In a different representation, reproduced below, the instruction store and the constant store are within the sequencer block.



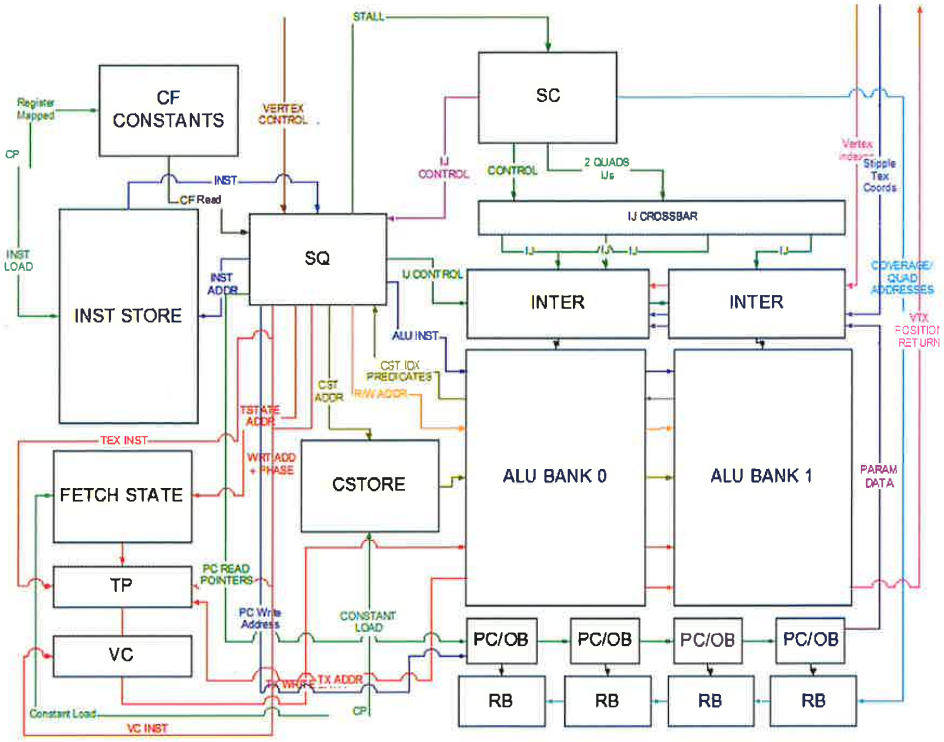
Id. at 12.

27. Later versions of the R400 Sequencer Specification show the sequencer and the shader pipe within the R400 architecture. *See, e.g.*, Ex. 2012, pp. 3, 5. The architecture in Version 0.6 of the R400 Sequencer Specification is reproduced below.



Id. at 5.

28. Following Version 0.6, the R400 architecture was kept in the R400 Sequencer Specification. *See, e.g.*, Ex. 2039, p. 7. A version of the R400 Sequencer Specification dated May 1, 2003 includes the R400 architecture reproduced below. The general role of the sequencer within this architecture did not change. And most inputs/outputs to/from the sequencer stay consistent.



Id.

2. *R400 Sequencer Specification (Version 2.0): April 19, 2002*

29. The sequencer's control flow changed in Version 2.0 of the R400 Sequencer Specification. *See* Ex. 2028, pp. 5, 6, 10. Version 2.0 is dated April 19, 2002. *See id.* at 5; *see also* Ex. 2044 (for the log entry on April 19, 2002).

30. Again, the reason for the change was to meet the requirements of Microsoft's API, called DX10. In particular, Microsoft wanted the sequencer to be able to run shaders with an unlimited number of clauses/instructions. The first

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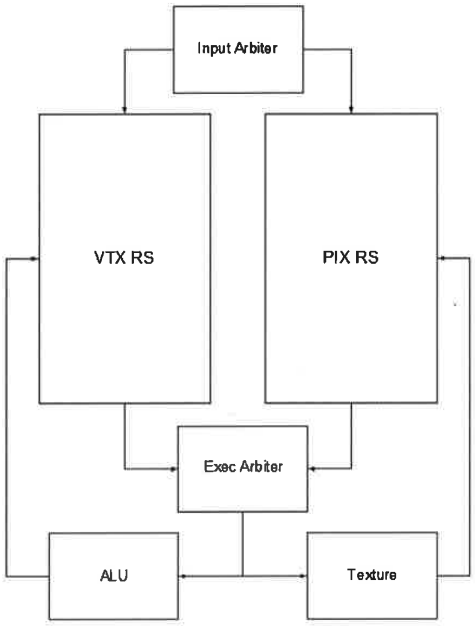
control flow selected from sixteen vertex clauses and sixteen pixel clauses. *See* Ex. 2010, pp. 5, 14-15. To meet Microsoft's specifications, I changed the sequencer's control flow. The new control flow is shown below.



Ex. 2028, p. 10.

31. In this version, there is an input arbiter. *See id.* The input arbiter arbitrates between vectors of vertices that arrive from a primitive assembly and pixel vectors that are generated in a scan converter. *Id.* at 6 ("The sequencer first arbitrates between vectors of 64 vertices that arrive directly from primitive assembly and vectors of 16 quads (64 pixels) that are generated in the scan converter."). This version also has two reservation stations, one reservation station

[redacted]

for vertices (VTX RS) and one reservation station for pixels (PIX RS). *See id.* at 10. The texture threads and the ALU threads are not separated. *See id.* at 23 ("[W]ithout separate 'texture clauses' and 'ALU clauses' we need to know which instructions to dispatch to the Texture Unit and which to the ALU unit."); *see also id.* at 6 (using the term thread). Each reservation station stores threads at specified locations with status bits indicating which engine is needed for execution. *See id.* at 25 ("A thread lives in a given location in the buffer during its entire life."), 26 ("'Status Bits' needed include: . . . [a] Texture/ALU engine [identifier]").

32. An arbiter, labeled as "Exec Arbiter," selects threads for an ALU engine and a texture engine. *See id.* at 25. The arbiter selects a thread based on FIFO. *See id.* at pp. 6 ("The arbitrator will give priority to older threads."), 25 ("[T]he buffer has FIFO qualities in that the threads leave in the order that they enter."). The thread is then read out of a reservation station. *See id.* at 26. Once the texture engine or the ALU engine executes the thread, the respective engine returns the thread to the location from which the thread originated. *See id.* ("[The thread] is returned to the buffer (at the same place) with its status updated once all possible sequential instructions have been executed.").

33. This version is present in later revisions of the Sequencer Specification. *See, e.g.*, Ex. 2039, p. 9.

[redacted]

III. DILIGENCE

34. After conceiving of the design for the R400, my colleagues and I worked to implement it. This work is shown by at least two things: (1) I periodically updated the R400 Sequencer Specification; and (2) my colleagues and I continuously developed, tested, and debugged emulation code and RTL code for the R400, including the other components that supported and interacted with the sequencer.

A. I Periodically Updated the R400 Sequencer Specification

35. During development, the architectural leads for each block wrote specifications to describe the structure and function of the blocks. *See* Ex. 2042, p. 1 (showing that specifications were used by designers). I was the architectural lead for the sequencer block, so I developed the R400 Sequencer Specification.

36. I updated the R400 Sequencer Specification approximately every two to three weeks. *See* Ex. 2039, pp. 4-5 (outlining edits to the document). There are at least thirty three revisions of this document. *See id.*; *see also* Exs. 2007-38. The revisions span from at least May 25, 2001 to August 29, 2003. *See* Ex. 2043, p. 2 (first log entry May 25, 2001); Ex. 2044, p. 1 (last log entry August 29, 2003); Ex. 2039, pp. 4-5 (showing 33 versions from May 7, 2001 to May 1, 2003).

[redacted]

37. Having multiple revisions during development is typical. Each revision showed progress during the previous week(s). During interim periods, the project team worked on outstanding issues. *See e.g.*, Ex. 2018, p. 35 (ending the document with a section labeled "Open Issues").

B. My Colleagues and I Continuously Developed and Debugged Emulation Code and RTL Code for the R400

38. In the beginning of development, only a handful of engineers were assigned to the R400 project. But by late 2001 or early 2002, ATI assigned over one hundred project managers/designers to implement and test the R400. During these two years, many project managers/designers transitioned from other projects and were assigned to solely work on the R400 project. These project managers/designers, including me, diligently worked on the R400. In particular, we used the specifications to write emulation code and RTL code for the R400's functional blocks. We then tested the R400's functional blocks.

39. Everyone assigned to the R400 project saved their work in a revision-control system, called Perforce. I understand that Perforce maintains metadata (i.e., document logs and folder histories). This metadata includes information such as the date each file was revised and the user that made each revision.

40. I understand that this metadata identifies the following users as the users that worked on the R400 design. These users worked from three of ATI's

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offices: (1) Marlboro, Massachusetts, USA; (2) Orlando, Florida, USA; and (3) Toronto, Ontario, Canada. *See* Ex. 2053, p. 6. I recall that periodic meetings occurred to coordinate efforts between the three offices.

Address Prefix	Exhibits
aashkar	2050
abeaudin	2050, 2052
alleng	2050, 2051
amys	2049, 2052
ashishs	2049, 2050, 2052
askende	2048, 2049, 2050, 2051, 2052, 2072
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bhankins	2049, 2050, 2052
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bryans	2050
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chwang	2050
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ctaylor	2048, 2049, 2050, 2051, 2052
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dclifton	2048, 2049, 2050, 2051, 2052
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dglen	2050, 2051
donaldl	2048, 2049, 2050, 2052
dougd	2049, 2050, 2052
dwong	2050, 2051
efong	2049, 2050, 2052
enewman	2050
fghodrat	2050
fhsien	2049, 2050, 2052

[redacted]

Address Prefix	Exhibits
fliljero	2050, 2052
frising	2048, 2050
frivas	2050, 2052
gabarca	2050
georgev	2050, 2052
grayc	2048, 2049, 2050, 2052
gregs	2050
hartogs	2048, 2049, 2050, 2051, 2052
hdong	2050
hwise	2048, 2052
imuskatb	2050
jacarey	2050, 2051
jasif	2050
jasony	2051
jayw	2050, 2051, 2052
jbrady	2050
jcox	2050
jennho	2050
jhoule	2048, 2049, 2050, 2051, 2052

Address Prefix	Exhibits
jiezhou	2050
jimmylau	2050
jling	2050
jmarsano	2050
jowang	2050, 2051
jyarasca	2050, 2052
kcorrell	2050, 2051
keli	2050
kevino	2050, 2052
khabbari	2050
kmahler	2048, 2050, 2052
kmeekins	2049, 2052
koyu	2050
kryan	2050, 2052
lchen	2050
lkang	2050, 2051
llefebvr	2048, 2049, 2050, 2051, 2052
lseiler	2048, 2050, 2051, 2052
markf	2049, 2050, 2051, 2052

[redacted]

Address Prefix	Exhibits
marklee	2050
mdesai	2050, 2052
mdoggett	2050, 2051, 2052
mearl	2048, 2049, 2050, 2052
mkelly	2048, 2050, 2052
moev	2049, 2050
mpersaud	2050
mmang	2048, 2049, 2050, 2052
mmantor	2048, 2049, 2050, 2052
mzhu	2050
mzini	2048, 2049, 2052
nbarbier	2050
nkociuk	2050
nluu	2050
omesh	2050, 2052
paulv	2050, 2051, 2052
pmitchel	2049, 2050, 2051, 2052, 2072
peterp	2050
prunstad	2050

Address Prefix	Exhibits
rbagley	2050, 2051
rbeaudin	2048, 2050, 2051, 2052
rbell	2049, 2050
rfevreau	2050
rfisette	2050
rherrick	2050
rramsey	2048, 2049, 2050, 2052
rthambim	2050
rvelez	2050
sallen	2048, 2049, 2050, 2051, 2052
sbagshaw	2050
scamlin	2049, 2050
scroce	2050
semara	2050
smburu	2050, 2052
smorein	2050, 2051
smoss	2049, 2050, 2052
snezana	2050
tho	2050, 2052

[redacted]

Address Prefix	Exhibits
tien	2049, 2050, 2052
tmartin	2050, 2052
tshah	2050
vbhatia	2050, 2052
vgoel	2050, 2052
viviana	2049, 2052
vliu	2048, 2050

Address Prefix	Exhibits
vromaker	2048, 2049, 2050, 2052
whui	2050
wlawless	2050, 2051
ygiang	2048, 2049, 2050, 2052
yvalcour	2050

[redacted]

41. In Part V, I analyze this metadata. My analysis shows that at least one person on the R400 project team worked on the R400 design every non-holiday business day from early 2002 (when we conceived of the invention) until November 20, 2003 (the effective filing date of the '871 patent). *See infra* Part V.

42. This metadata is not exhaustive of all sequencer/shader-pipe files that were edited during this timeframe. But this metadata shows work that was necessary for implementing the R400 design. Specifically, this metadata shows the design, development, and testing of the R400 sequencer and graphics blocks. *See* Exs. 2048, 2049. This metadata also shows work on the design and development of the R400 generally. *See* Exs. 2050, 2051, 2052, 2072. The design and development of the R400 was necessary to make progress on the sequencer block and the shader pipe block; we could not work on or test the sequencer block or the shader pipe block in isolation.

43. This analysis is also consistent with my memory of the work that we did on the R400. For me and many of the other project managers/designers, the R400 was the only project that most of us were assigned to—it was our full-time responsibility. That means, any time that we did work for ATI between late 2001 and the end of 2003, that work would have been on the R400.

[redacted]

IV. TESTING SHOWED THAT THE RTL IMPLEMENTATION WORKED FOR ITS INTENDED PURPOSE

44. We ran many tests on the R400 during its development. One test in particular, the first triangle, showed that a snapshot of the emulation code and the RTL code worked for its intended purpose—i.e., performing conventional graphics processing using a unified shader.

45. For the R400 project, block-level specifications, block-level diagrams, and interface descriptions provided overarching development concepts. Project managers/designers on the R400 team used these documents to develop C++ code (emulation code) and RTL code for the various blocks of the R400. This code was tested extensively during the development process. Tests could be run on both the emulation code and the RTL code, and these tests could be run on individual blocks or the entire graphics core.

46. Circuit designers extensively use circuit simulation to test the GPU design. After the design has passed extensive testing, the chip design can be cleared for fabrication. Before sending out the design for fabrication, the RTL code is converted to a tape-out file, and that tape-out file is sent to a fabrication facility for fabrication.

47. A product such as the R400 must pass thousands of tests before it is taped out. Many tests were directed to specific commercial specifications. Other

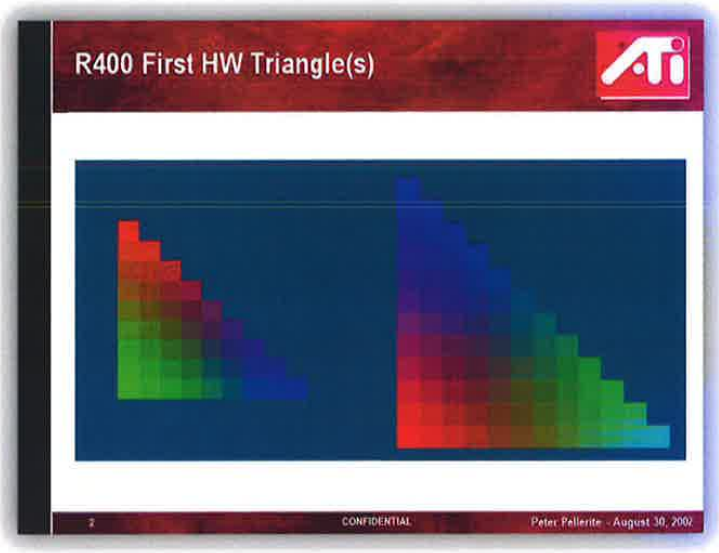
[redacted]

tests were more generic, such as tests for validation and proof of concept. One generic test was the first triangle.

48. The first triangle tested whether the RTL implementation of the GPU could process a Gouraud shaded triangle. At this stage of development, this test involved many different blocks—including the sequencer, the shader pipe, the shader export, the primitive assembly, and the raster engine blocks. *See* Ex. 2058, p. 1; Ex. 2061, pp. 2-5.

49. I recall the first triangle test being successful approximately mid-way through the R400 project. Consistent with my memory, the PowerPoint slide reproduced below shows that the first triangle was reported during a meeting on August 30, 2002.

[redacted]



Ex. 2066, p. 2. According to this presentation, the first triangle was completed on July 1, 2002. *Id.*, p. 6.

50. For a successful first triangle, the sequencer block and the shader pipe block must work together to process both vertex commands and pixel commands. This is shown, for example, in the RTL code that arbitrates between vertices and pixels. An example of this arbitration as implemented in the RTL code is reproduced below.

[redacted]

```
12          case (tta_current_state)
13          TTA0:
14         begin
15              // - ack is connected to TB State Mem read enable, so have to
16              //  wait until the correct phase to ack
17
18              if ( state_read_phase == arb_type_strap )
19
20               if ( vtx_winner_vld_q )          // simply give verts the priority
21                begin
22               vtx_winner_ack = HI;
23                    tta_next_state = TTA1;
24                end
```

```
1                else if ( pix_winner_vld_q )
2                 begin
3                pix_winner_ack = HI;
4                     tta_next_state = TTA2;
5                 end
```

Ex. 2097, 18:12-19:5.

51. In this example code, the arbitration is implemented as a simple "if-else" statement in which vertices have priority. According to this "if-else" statement, "if" a vertex is ready for execution, the sequencer selects the vertex;

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"else" (i.e., otherwise) the sequencer selects the pixel. That is it. The first triangle touched both paths because the vertex processing worked for the "if" path and the pixel processing worked for the "else" path. Other levels of arbitration in the RTL code worked like this example, and these other levels of arbitration would have been touched by the first triangle. So, following the first triangle, we knew the RTL code worked.

52. Passing the first triangle test did not signal the end of the R400 project; the R400 still had to pass many other tests to be commercializable. After processing a first triangle, however, we knew that we had an implementation of the R400 in RTL code that worked for its intended purpose—i.e., performing graphics processing using a unified shader.

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V. DILIGENCE CALENDAR

Em. (R400 Sequencer Emulator Folder History, Exhibit 2048)
Parts (R400 Sequencer Parts Folder History, Exhibit 2049)
Lib. (R400 Document Library Folder History, Exhibit 2050)
Arch. (R400 Architecture Folder History, Exhibit 2051)
Test (R400 GFX Testing Folder History, Exhibit 2052)
SP Parts (R400 Shader Pipe Parts Folder History, Exhibit 2072)

August 2001						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
			1	**2**	**3**	**4**
5	**6**	**7**	**8**	**9**	**10**	**11**
12	**13**	**14**	**15**	**16**	**17**	**18**
19	**20**	**21**	**22**	**23**	**24** **Sequencer Specification**	**25**
26	**27**	**28** Lib., 434 Arch., 44 Test, 510	**29** Arch., 43-44	**30** Arch., 43	**31** Arch., 43	

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September 2001						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
						1
2	**3**	**4**	**5** Lib., 434	**6**	**7** Arch., 43	**8**
9	**10** Lib., 433-34 Arch., 43	**11** Lib., 433 Arch., 43 Test, 510	**12**	**13** Lib., 433	**14** Lib., 433 Arch., 43	**15**
16	**17** Arch., 43	**18** Test, 509	**19** Test, 509	**20** Lib., 432-33 Arch., 42-43 Test, 509	**21** Lib., 432 Arch., 42 SP Parts, 1	**22**
23	**24** Lib., 432 Arch., 42	**25** Lib., 432 Arch., 42 SP Parts, 1	**26** Lib., 432 Arch., 42	**27** Lib., 431-32 Arch., 41-42	**28** Lib., 431 Arch., 41	**29**
30						

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October 2001						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
	1 Lib., 431 Arch., 41	**2** Lib., 431 Arch., 41	**3** Lib., 431 Arch., 41	**4** Lib., 430-31 Arch., 40-41	**5** Lib., 430 Arch., 40	**6**
7	**8** Lib., 430	**9** Lib., 429 Arch., 39	**10** Lib., 429 Arch., 39 Test, 509	**11** Lib., 429 Arch., 39	**12** Lib., 428-29 Arch., 38-39 Test, 509	**13**
14	**15** Lib., 428 Arch., 38 Test, 509	**16** Lib., 428 Arch., 37-38	**17** Lib., 428 Arch., 37	**18** Lib., 427-28 Arch., 37	**19** Lib., 427 Arch., 37	**20**
21	**22** Lib., 427 Arch., 36	**23** Lib., 426-27 Arch., 35-36 Test, 509	**24** Lib., 426 Arch., 34-35	**25** SP Parts, 1	**26** Lib., 425-26 Arch., 34 Test, 508-09	**27**
28	**29** Arch., 34	**30** Test, 508	**31** Lib., 425 Arch., 34			

November 2001						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
				1 Lib., 425 Arch., 34 Test, 508	**2** Lib., 424-25 Arch., 33 Test, 508	**3**
4	**5** Lib., 424 Arch., 32-33	**6** Lib., 424 Arch., 32 Test, 508	**7** Lib., 424 Arch., 32	**8** Lib., 423-24 Arch., 31-32	**9** Lib., 423 Arch., 31	**10**
11	**12** Lib., 422-23 Arch., 30-31 Test, 508	**13** Lib., 422 Arch., 30	**14** Lib., 421-22 Arch., 29-30 SP Parts, 1	**15** Lib., 420-21 Arch., 28-29	**16** Lib., 420 Arch., 28	**17**
18	**19** Lib., 419 Arch., 27-28	**20** Lib., 419 Arch., 27	**21** Lib., 419 Arch., 26-27 SP Parts, 1	**22**	**23**	**24**
25	**26** Lib., 417-19 Arch., 26	**27** Lib., 415-17 Arch., 25-26	**28** Lib., 415 Arch., 24	**29** Lib., 415	**30** Lib., 414-15 Arch., 24	

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December 2001						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
						1
2	**3** Parts, 136 Lib., 413-14 Arch., 24 SP Parts, 1	**4** Lib., 413	**5** Lib., 413	**6** Lib., 412-13 Arch., 24	**7** Lib., 412	**8**
9	**10** Lib., 411-12	**11** Lib., 411 Arch., 24	**12** Em., 75 Arch., 23-24	**13** Lib., 411 Arch., 23 Test, 508	**14** Em., 74 Lib., 410-11 Arch., 23	**15** Lib., 410
16	**17** Lib., 409-10	**18** Em., 74 Lib., 408-09	**19** Em., 74 Lib., 407-08 Arch., 23	**20** Em., 74 Lib., 406	**21** Em., 74 Lib., 406	**22**
23	**24** Lib., 405-06	**25**	**26**	**27** Lib., 405	**28** Lib., 405	**29**
30	**31** Lib., 405					

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January 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
		1	**2** Lib., 404	**3** Em., 74 Lib., 404	**4** Em., 73-74 Lib., 403	**5**
6	**7** Em., 73 Lib., 402 Arch., 23 Test, 508	**8** Em., 73 Lib., 401-02	**9** Em., 72-73 Lib., 399-401	**10** Em., 72 Lib., 399 Arch., 23	**11** Em., 72 Lib., 398 Arch., 23	**12** Lib., 398
13	**14** Lib., 397-98 Arch., 23	**15** Lib., 396-97 Arch., 22-23	**16** Em., 72 Lib., 396 Arch., 22	**17** Lib., 395-96 Arch., 22	**18** Em., 72 Lib., 394-95 Arch., 22	**19**
20	**21** Em., 72 Lib., 392-94	**22** Lib., 392	**23** Em., 71-72 Lib., 390-92	**24** Em., 71 Lib., 389-90 Arch., 22	**25** Em., 71 Lib., 388-89 Arch., 22	**26**
27	**28** Em., 71 Lib., 387-88 Arch., 22	**29** Lib., 385-87 Arch., 22	**30** Em., 71 Lib., 384-85	**31** Em., 71 Lib., 383-84 Arch., 21		

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February 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
					1 Em., 70 Lib., 382-83 Arch., 21	**2**
3 Lib., 382	**4** Em., 70 Lib., 380-81 Arch., 21	**5** Em., 70 Lib., 378-80	**6** Em., 70 Lib., 378	**7** Lib., 377-78	**8** Em., 69-70 Lib., 376-77	**9**
10	**11** Em., 69 Lib., 373-76	**12** Em., 69 Lib., 372-73	**13** Em., 68 Lib., 371-72	**14** Em., 68 Lib., 370-71	**15** Em., 68 Lib., 369-70	**16** Lib., 369
17	**18** Lib., 368-69	**19** Lib., 367-68	**20** Lib., 366-67 Arch., 21	**21** Em., 68 Lib., 364-66 Arch., 21	**22** Em., 68 Lib., 363-64 Arch., 20-21	**23**
24	**25** Em., 68 Lib., 361-63	**26** Lib., 360-61	**27** Em., 68 Lib., 358-60	**28** Em., 68 Lib., 357-58		

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March 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
					1 Lib., 356-57	**2**
3	**4** Em., 67 Lib., 355-56	**5** Em., 67 Lib., 353-55	**6** Em., 67 Lib., 351-53	**7** Em., 66-67 Lib., 350-51	**8** Parts, 136 Lib., 348-50 Arch., 20	**9** Lib., 348
10 Lib., 348	**11** Em., 66 Lib., 346-48	**12** Lib., 345-46 Arch., 20	**13** Lib., 345 Arch., 20	**14** Em., 66 Lib., 344-45	**15** Lib., 343-44 Arch., 20	**16**
17 Lib., 343	**18** Em., 66 Lib., 341-43 Arch., 20	**19** Em., 65-66 Parts, 136 Lib., 341	**20** Parts, 136 Lib., 340-41	**21** Em., 65 Lib., 339-40 Arch., 20	**22** Em., 65 Lib., 337-39	**23**
24 Lib., 337	**25** Lib., 335-37	**26** Em., 65 Lib., 334-35 Arch., 20 Test, 507-08	**27** Em., 65 Parts, 135-36 Lib., 332-33 Arch., 19-20	**28** Lib., 331-32 Test, 507	**29** Parts, 135 Arch., 19 Test, 507	**30**
31 Lib., 331						

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April 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
	1 Em., 65 Lib., 330-31 Arch., 19 Test, 507	**2** Em., 65 Parts, 135 Lib., 328-30 Test, 506-07	**3** Em., 64-65 Parts, 134-35 Lib., 327-28 Arch., 19 Test, 506	**4** Em., 64 Lib., 326-27 Arch., 19	**5** Em., 64 Lib., 324-26 Test, 505-06	**6**
7	**8** Em., 64 Lib., 322-24 Test, 505	**9** Em., 63-64 Lib., 321-22 Test, 505	**10** Lib., 320-21 Arch., 19 Test, 505	**11** Em., 63 Lib., 318-20 Test, 504-05	**12** Em., 62-63 Lib., 317-18 Arch., 19 Test, 504	**13** Lib., 317
14 Lib., 317	**15** Em., 62 Lib., 315-17 Arch., 19 Test, 504	**16** Parts, 134 Lib., 315 Test, 503-04	**17** Em., 62 Lib., 314-15 Test, 503	**18** Em., 62 Lib., 314 Test, 503	**19** Parts, 134 Lib., 312-14 Test, 503	**20**
21	**22** Lib., 311-12	**23** Parts, 134 Lib., 310-11 Test, 503	**24** Parts, 134 Lib., 309-10 Test, 502-03	**25** Em., 62 Lib., 307-09 Arch., 19 Test, 502	**26** Parts, 134 Lib., 306-07 Arch., 19 Test, 502	**27**
28	**29** Lib., 304-06 Test, 501-02	**30** Parts, 134 Lib., 303-04 Test, 501				

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May 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
			1 Parts, 134 Lib., 301-03 Test, 501	**2** Lib., 299-301 Test, 500-01	**3** Em., 62 Parts, 133-34 Lib., 297-98 Test, 499-500	**4**
5	**6** Em., 61-62 Parts, 133 Lib., 294-97 Test, 499	**7** Em., 61 Parts, 133 Lib., 293-94 Arch., 19 Test, 499	**8** Em., 61 Parts, 132-33 Lib., 290-93 Test, 498	**9** Em., 61 Parts, 132 Lib., 289-90 Test, 498	**10** Em., 60-61 Parts, 132 Lib., 286-89 Test, 498	**11**
12	**13** Lib., 284-86 Test, 497	**14** Em., 60 Parts, 131-32 Lib., 281-83 Test, 497	**15** Em., 60 Lib., 280-81 Test, 497	**16** Em., 60 Parts, 131 Lib., 278-80 Arch., 18 Test, 496	**17** Em., 60 Parts, 131 Lib., 277-78 Test, 495-96	**18**
19 Lib., 277	**20** Em., 59-60 Parts, 131 Lib., 276-77 Arch., 18 Test, 495	**21** Em., 59 Parts, 131 Lib., 275-76 Arch., 18 Test, 494-95	**22** Em., 59 Lib., 273-75 Test, 494	**23** Em., 59 Parts, 130-31 Lib., 273 Arch., 18 Test, 494	**24** Em., 59 Parts, 130 Lib., 272-73 Arch., 18 Test, 493-94	**25** Lib., 272
26 Em., 59	**27** Parts, 130 Lib., 271-72	**28** Em., 58 Parts, 129-30 Lib., 270-71 Test, 493	**29** Em., 58 Parts, 129 Lib., 269-70 Test, 492-93	**30** Em., 58 Parts, 129 Lib., 268-69 Arch., 17 Test, 491-92	**31** Em., 58 Parts, 128-29 Lib., 266-68 Test, 490-91	

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June 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
						1
2 Parts, 128	**3** Em., 58 Parts, 128 Lib., 264-66 Arch., 17 Test, 489-90	**4** Em., 57-58 Parts, 127-28 Lib., 263-64 Arch., 17 Test, 489	**5** Em., 57 Parts, 127 Lib., 261-62 Arch., 17 Test, 488-89	**6** Parts, 126-27 Lib., 259-61 Arch., 16 Test, 487-88	**7** Em., 57 Parts, 126 Lib., 257-59 Arch., 16 Test, 487	**8**
9 Lib., 257	**10** Em., 57 Parts, 126 Lib., 255-57 Arch., 16 Test, 486-87	**11** Em., 57 Parts, 125-26 Lib., 254-55 Arch., 16 Test, 485-86	**12** Em., 57 Parts, 125 Lib., 253-54 Arch., 15 Test, 484-85	**13** Em., 57 Parts, 125 Lib., 252-53 Arch., 15 Test, 483-84	**14** Em., 57 Parts, 124-25 Lib., 251-52 Arch., 15 Test, 482	**15** Parts, 124 Test, 482
16 Lib., 251 Test, 482	**17** Em.,56-57 Parts, 124 Lib., 248-51 Arch., 14-15 Test, 480-82	**18** Parts, 123-24 Lib., 247-48 Arch., 14 Test, 479-80	**19** Em., 56 Parts, 123 Lib., 245-47 Test, 479	**20** Em., 56 Parts, 123 Lib., 244-45 Test, 477-79	**21** Em., 56 Lib., 243-44 Test, 476-77	**22**
23	**24** Lib., 241-43 Test, 475-76	**25** Parts, 123 Lib., 239-41 Test, 475	**26** Lib., 238-39 Test, 474-75	**27** Lib., 236-38 Test, 472-74	**28** Lib., 235-36 Test, 471-72	**29**
30 Test, 471						

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July 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
	1 Lib., 235 Arch., 14 Test, 469-471 **1st Triangle**	**2** Lib., 233-35 Arch., 14 Test, 468-69	**3** Em., 56 Lib., 232-33 Arch., 14 Test, 467-68	**4** Lib., 231-32	**5** Em., 56 Lib., 230-31 Test, 467	**6**
7	**8** Em., 56 Lib., 228-30 Arch., 13-14 Test, 467	**9** Em., 55 Parts, 123 Lib., 227-28 Arch., 13 Test, 466-67	**10** Em., 54-55 Lib., 226-27 Arch., 13 Test, 463-66	**11** Parts, 122-23 Lib., 225-26 Arch., 12-13 Test, 461-63	**12** Parts, 122 Lib., 224 Arch., 12 Test, 459-61	**13**
14 Lib., 224 Test, 459	**15** Em., 54 Parts, 122 Lib., 221-24 Arch., 12 Test, 458-59	**16** Em., 54 Parts, 122 Lib., 221 Arch., 12 Test, 456-57	**17** Em., 54 Parts, 122 Lib., 220-21 Arch., 12 Test, 455-56	**18** Parts, 121-22 Lib., 218-20 Arch., 11-12 Test, 454-55	**19** Em., 54 Parts, 121 Lib., 217-18 Arch., 11 Test, 453-54	**20**
21 Test, 453	**22** Em., 53 Parts, 120-21 Lib., 215-17 Arch., 11 Test, 452-53	**23** Em., 53 Parts, 120 Lib., 214-15 Test, 451-52	**24** Parts, 120 Lib., 213-14 Arch., 11 Test, 450-51	**25** Parts, 120 Lib., 213 Test, 449-50	**26** Parts, 120 Lib., 212-13 Arch., 11 Test, 449	**27**
28 Test, 449	**29** Em., 53 Parts, 119-20 Lib., 212 Arch., 11 Test, 448-49	**30** Em., 53 Parts, 119 Lib., 211-12 Arch., 10 Test, 448	**31** Em., 53 Lib., 210-11 Arch., 10 Test, 445-48			

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August 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
				1 Em., 52-53 Lib., 209-10 Arch., 10 Test, 444-45	**2** Em., 52 Parts, 119 Lib., 208-09 Arch., 10 Test, 443-44	**3**
4	**5** Em., 52 Parts, 119 Lib., 207-08 Arch., 9-10 Test, 443	**6** Em., 52 Parts, 118-19 Lib., 206-07 Arch., 9 Test, 442-43	**7** Lib., 206 Arch., 9 Test, 440-41	**8** Em., 52 Parts, 118 Lib., 205-06 Arch., 9 Test, 439-40	**9** Em., 51-52 Parts, 118 Lib., 204-05 Arch., 9 Test, 437-39	**10**
11 Lib., 204 Test, 437	**12** Em., 51 Parts, 118 Lib., 203-04 Test, 433-37	**13** Em., 51 Parts, 118 Lib., 202-03 Arch., 8-9 Test, 432-33	**14** Em., 51 Lib., 201-02 Arch., 8 Test, 432	**15** Em., 50-51 Parts, 118 Lib., 200-01 Test, 431	**16** Em., 50 Parts, 117-18 Lib., 199-200 Test, 430-31	**17**
18 Lib., 199 Test, 430	**19** Em., 50 Parts, 117 Lib., 197-99 Test, 429-30	**20** Parts, 117 Lib., 195-97 Test, 428-29	**21** Lib., 194-95 Test, 426-28	**22** Em., 50 Parts, 117 Lib., 193-94 Test, 425-26	**23** Em., 50 Lib., 192-93 Test, 424-25	**24** Test, 423-24
25 Lib., 191-92 Test, 423	**26** Em., 50 Parts, 116-17 Lib., 189-91 Test, 422-23	**27** Em.,49-50 Parts, 116 Lib., 187-89 Arch., 8 Test, 420-22	**28** Parts, 116 Lib., 186-87 Test, 419-20	**29** Em., 49 Parts, 116 Lib., 184-86 Test, 417-19	**30** Em., 49 Parts, 116 Lib., 183-84 Arch., 8 Test, 415-17	**31** Lib., 183 Test, 415

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September 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
1	**2** Parts, 115-16 Lib., 182-83	**3** Em., 49 Parts, 115 Lib., 181-82 Test, 414-15	**4** Em., 48-49 Lib., 180-81 Test, 413-14	**5** Em., 48 Parts, 115 Lib., 179-80 Test, 411-13	**6** Em., 48 Parts, 115 Lib., 177-79 Test, 410-11	**7**
8	**9** Em., 47-48 Parts, 115 Lib., 176-77 Test, 408-10	**10** Em., 47 Parts, 115 Lib., 174-76 Arch., 8 Test, 407-08	**11** Em., 47 Parts, 114-15 Lib., 173-74 Test, 405-07	**12** Parts, 114 Lib., 172-73 Test, 404-05	**13** Parts, 114 Lib., 171-72 Arch., 8 Test, 403-04	**14**
15 Parts, 114 Lib., 171	**16** Parts, 114 Lib., 170-71 Arch., 8 Test, 402-03	**17** Parts, 113-14 Lib., 169-70 Test, 400-01	**18** Parts, 113 Lib., 167-69 Test, 399-400	**19** Lib., 166-67 Test, 397-99	**20** Parts, 113 Lib., 165-66 Test, 393-97	**21** Test, 393
22 Lib., 165	**23** Parts, 113 Lib., 164-65 Test, 392-93	**24** Parts, 113 Lib., 162-63 Test, 392	**25** Em., 47 Parts, 112-13 Lib., 161-62 Test, 390-92	**26** Em., 47 Parts, 112 Lib., 160-61 Test, 389-90	**27** Em., 46 Parts, 112 Lib., 159-60 Test, 389	**28** Parts, 112
29 Lib., 159 Test, 389	**30** Em., 46 Parts, 112 Lib., 158-59 Test, 388-89					

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October 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
		1 Em., 46 Parts, 111 Lib., 157-58 Test, 386-88	**2** Em., 46 Parts, 111 Lib., 156-57 Test, 385-86	**3** Em., 46 Parts, 111 Lib., 155-56 Test, 384-85	**4** Em., 45 Parts, 111 Lib., 155 Test, 383-84	**5** Lib., 154
6 Lib., 154 Test, 382-383	**7** Parts, 110-11 Lib., 154 Arch., 8 Test, 381-82	**8** Em., 45 Parts, 110 Lib., 152-53 Test, 378-81	**9** Em., 45 Parts, 110 Lib., 151-52 Test, 376-78	**10** Em., 45 Parts, 110 Lib., 150-51 Test, 375-76	**11** Em., 44-45 Lib., 149-50 Test, 373-75	**12**
13 Parts, 110	**14** Em., 44 Parts, 110 Lib., 149 Test, 372-73	**15** Em., 44 Parts, 110 Lib., 147-48 Test, 370-72	**16** Em., 44 Parts, 109-10 Lib., 146-47 Test, 369-70	**17** Em., 44 Parts, 109 Lib., 146 Test, 368-69	**18** Em., 44 Parts, 109 Lib., 144-46 Test, 365-68	**19** Lib., 144
20 Lib., 144	**21** Em., 43 Lib., 143-44 Test, 362-65	**22** Em., 43 Lib., 142-43 Test, 361-62	**23** Em., 43 Lib., 141-42 Arch., 7 Test, 360-61	**24** Em., 43 Parts, 109 Lib., 140-41 Test, 358-60	**25** Em., 42-43 Parts, 109 Lib., 139-40 Test, 357-58	**26** Parts, 108-09
27 Lib., 139 Test, 357	**28** Em., 42 Lib., 138-39 Test, 356-57	**29** Em., 42 Parts, 108 Lib., 137-38 Test, 354-56	**30** Em., 42 Parts, 108 Lib., 136-37 Test, 354	**31** Em., 42 Parts, 108 Lib., 134-36 Test, 352-53		

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November 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
					1 Em., 41-42 Parts, 108 Lib., 133-34 Test, 351-52	**2** Test, 350-51
3 Parts, 108	**4** Lib., 131-33 Test, 350	**5** Parts, 108 Lib., 130-31 Test, 349-50	**6** Em., 41 Parts, 108 Lib., 129-30 Test, 348-49	**7** Em., 41 Parts, 107-08 Lib., 129 Test, 347-48	**8** Em., 41 Parts, 107 Lib., 127-29 Test, 346-47	**9** Lib., 127
10	**11** Em., 40-41 Parts, 107 Lib., 126-27 Test, 344-46	**12** Parts, 107 Lib., 125-26 Test, 343-44	**13** Em., 40 Parts, 106-07 Lib., 123-25 Test, 342-43	**14** Em., 40 Parts, 105-06 Lib., 123 Test, 340-42	**15** Em., 40 Parts, 105 Lib., 122-23 Test, 338-40	**16** Lib., 121-22 Test, 338
17	**18** Em., 40 Parts, 105 Lib., 121 Arch., 7 Test, 337-38	**19** Em., 39-40 Parts, 105 Lib., 119-21 Test, 335-37	**20** Em., 39 Parts, 105 Lib., 118-19 Test, 334-35	**21** Em., 39 Parts, 104-05 Lib., 117-18 Test, 332-34	**22** Em., 39 Parts, 104 Lib., 116-17 Test, 331-32	**23** Parts, 104 Test, 331
24 Lib., 116 Test, 331	**25** Parts, 104 Lib., 116 Test, 330-31	**26** Em., 39 Parts, 104 Lib., 114-16 Arch., 7 Test, 329-30	**27** Parts, 103-04 Lib., 114 Test, 328-29	**28** Lib., 114	**29** Lib., 113-14 Test, 328	**30** Lib., 113

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December 2002						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
1 Test, 328	**2** Parts, 103 Lib., 112-13 Test, 326-28	**3** Em., 39 Parts, 103 Lib., 111-12 Test, 326	**4** Em., 38-39 Parts, 103 Lib., 110-11 Test, 324-25	**5** Em., 38 Lib., 109-10 Test, 321-24	**6** Em., 38 Parts, 103 Lib., 109 Test, 320-21	**7** Lib., 109
8 Lib., 108-09	**9** Em., 38 Parts, 103 Lib., 108 Test, 319-20	**10** Em., 38 Parts, 102-03 Lib., 107-08 Arch., 7 Test, 318-19	**11** Em., 38 Parts, 102 Lib., 106-07 Test, 317-18	**12** Lib., 106 Test, 316-17	**13** Em., 38 Parts, 102 Lib., 105-06 Arch., 7 Test, 315-16	**14**
15 Lib., 105	**16** Em., 37-38 Parts, 102 Lib., 104-05 Test, 313-15	**17** Em., 37 Parts, 102 Lib., 104 Arch., 7 Test, 311-13	**18** Parts, 102 Lib., 103-04 Test, 309-11	**19** Parts, 102 Lib., 102-03 Test, 308-09	**20** Parts, 101-02 Lib., 101-02 Arch., 7 Test, 307-08	**21** Test, 307
22	**23** Parts, 101 Lib., 101 Test, 306-07	**24** Lib., 101	**25**	**26** Lib., 101 Arch., 7 Test, 306	**27** Em., 37 Lib., 101 Test, 306	**28**
29 Lib., 101	**30** Test, 303-06	**31** Em., 37 Lib., 101 Test, 302-03				

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January 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
			1 Parts, 101 Lib., 101	**2** Em., 37 Parts, 101 Lib., 99-101 Test, 301-02	**3** Em., 37 Parts, 101 Lib., 99 Test, 300-01	**4** Parts, 101 Lib., 99
5	**6** Em., 36-37 Parts, 100-01 Lib., 98-99 Test, 299-300	**7** Em., 36 Parts, 100 Lib., 98 Arch., 7 Test, 297-98	**8** Em., 36 Parts, 100 Lib., 97-98 Test, 296-97	**9** Em., 36 Parts, 99-100 Lib., 97 Test, 295-96	**10** Em., 36 Parts, 99 Lib., 96-97 Arch., 6 Test, 287-95	**11** Parts, 99 Test, 287
12 Parts, 99 Lib., 96	**13** Parts, 99 Lib., 94-96 Test, 286-87	**14** Parts, 99 Lib., 94 Test, 285-86	**15** Em., 36 Parts, 98-99 Lib., 92-93 Test, 284-85	**16** Em., 35-36 Parts, 98 Lib., 92 Test, 283-84	**17** Em., 35 Parts, 97-98 Lib., 91-92 Test, 282-83	**18** Parts, 97 Test, 281-82
19 Parts, 97	**20** Em., 35 Parts, 97 Lib., 90-91 Test, 280-81	**21** Em., 35 Parts, 96-97 Lib., 89-90 Test, 280	**22** Em., 35 Parts, 96 Lib., 89 Test, 279-80	**23** Em., 34-35 Parts, 95-96 Lib., 88 Test, 278-79	**24** Em., 34 Parts, 95 Lib., 87-88 Arch., 6 Test, 276-78	**25** Parts, 95 Test, 276
26 Parts, 95 Lib., 87	**27** Em., 34 Parts, 95 Lib., 86 Test, 275-76	**28** Em., 34 Parts, 94-95 Lib., 85-86 Test, 274-75	**29** Em., 34 Parts, 94 Lib., 85 Test, 273-74	**30** Parts, 94 Lib., 84-85 Test, 271-73	**31** Em., 33-34 Parts, 94 Lib., 83-84 Arch., 6 Test, 270-71	

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February 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
						1 Em., 33 Parts, 93-94 Lib., 83
2 Lib., 83	**3** Em., 33 Parts, 93 Lib., 82-83 Test, 269-70	**4** Em., 33 Parts, 93 Lib., 82 Test, 268-69	**5** Em., 33 Parts, 92-93 Lib., 81-82 Arch., 6 Test, 267-68	**6** Em., 33 Parts, 92 Lib., 80-81 Arch., 6 Test, 265-67	**7** Em., 33 Parts, 92 Lib., 80 Test, 263-65	**8** Parts, 92 Lib., 80
9 Parts, 92 Lib., 79	**10** Em., 32 Parts, 91-92 Lib., 79 Test, 263	**11** Em., 32 Parts, 91 Lib., 78-79 Test, 261-63	**12** Lib., 78 Test, 259-61	**13** Em., 32 Parts, 91 Lib., 77-78 Test, 257-59	**14** Em., 32 Parts, 90 Lib., 77 Test, 256-57	**15** Parts, 90
16 Parts, 90	**17** Em., 32 Lib., 76-77	**18** Em., 31-32 Parts, 90 Lib., 76 Test, 255-56	**19** Em., 31 Parts, 89-90 Lib., 74-76 Test, 254-55	**20** Parts, 88-89 Lib., 73-74 Test, 252-54	**21** Em., 31 Parts, 88 Lib., 73 Test, 250-52	**22** Em., 31
23 Lib., 73	**24** Em., 31 Parts, 88 Lib., 71-73 Arch., 6 Test, 249-50	**25** Em., 31 Parts, 88 Lib., 70-71 Test, 248-49	**26** Em., 31 Parts, 87 Lib., 70 Test, 247-48	**27** Em.,30-31 Parts, 87 Lib., 69-70 Arch., 6 Test, 246-47	**28** Parts, 86-87 Lib., 69 Arch., 6 Test, 245-46	

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March 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
						1 Em., 30 Lib., 69
2	**3** Em., 30 Parts, 86 Lib., 68-69 Test, 244-45	**4** Parts, 86 Lib., 68 Arch., 6 Test, 243-44	**5** Em., 30 Parts, 85-86 Lib., 67-68 Test, 241-43	**6** Em., 30 Parts, 85 Lib., 67 Test, 240-41	**7** Em., 29-30 Parts, 85 Lib., 66-67 Test, 238-40	**8**
9	**10** Em., 29 Parts, 85 Lib., 66 Test, 237-38	**11** Parts, 84-85 Lib., 65 Test, 236-37	**12** Em., 29 Parts, 84 Lib., 64-65 Test, 235-36	**13** Em., 29 Parts, 84 Lib., 63-64 Test, 234-35	**14** Parts, 84 Lib., 63 Test, 233-34	**15** Test, 233
16	**17** Parts, 84 Lib., 63 Test, 233	**18** Parts, 83-84 Lib., 62 Test, 232-33	**19** Parts, 83 Lib., 61-62 Test, 231-32	**20** Em., 29 Parts, 83 Lib., 60-61 Test, 230-31	**21** Em., 29 Parts, 83 Lib., 59-60 Test, 229-30	**22**
23	**24** Parts, 83 Lib., 59 Test, 229	**25** Parts, 82-83 Lib., 59 Test, 228-29	**26** Em., 28-29 Parts, 82 Lib., 58-59 Test, 228	**27** Em., 28 Parts, 82 Lib., 57-58 Test, 227-28	**28** Em., 28 Parts, 81-82 Lib., 57 Test, 226-27	**29**
30	**31** Em., 28 Parts, 81 Lib., 57 Test, 225-26					

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April 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
		1 Parts, 81 Lib., 56-57 Test, 225	**2** Em., 27-28 Parts, 81 Lib., 56 Arch., 6 Test, 224	**3** Em., 27 Parts, 80-81 Lib., 55 Test, 223-24	**4** Em., 27 Parts, 80 Lib., 55 Test, 223	**5**
6 Test, 222	**7** Em., 27 Parts, 80 Lib., 55 Test, 222	**8** Parts, 80 Lib., 54-55 Test, 221-22	**9** Em., 27 Parts, 80 Lib., 54 Test, 221	**10** Em., 27 Parts, 79-80 Lib., 54 Test, 220-21	**11** Em., 27 Parts, 79 Lib., 53-54 Test, 219-20	**12**
13	**14** Em., 26 Parts, 79 Lib., 53 Arch., 5 Test, 218-19	**15** Em., 26 Parts, 79 Lib., 52-53 Test, 217-18	**16** Em., 26 Parts, 78-79 Lib., 52 Test, 216-17	**17** Parts, 78 Lib., 51-52 Test, 215-16	**18** Em., 26 Parts, 77-78 Lib., 51 Test, 214-15	**19** Lib., 51 Test, 214
20 Lib., 51	**21** Parts, 77 Lib., 51 Test, 213-14	**22** Em., 26 Parts, 77 Lib., 49-51 Test, 213	**23** Em., 26 Parts, 76-77 Lib., 48-49 Test, 212-13	**24** Em., 25-26 Parts, 76 Lib., 47-48 Test, 211-12	**25** Em., 25 Parts, 76 Lib., 47 Arch., 5 Test, 211	**26**
27	**28** Parts, 75-76 Lib., 47 Test, 211	**29** Parts, 75 Lib., 47 Test, 210-11	**30** Em., 25 Parts, 74-75 Lib., 46 Test, 208-09			

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May 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
				1 Parts, 73-74 Lib., 45-46 Test, 207-08	**2** Parts, 73 Lib., 45 Test, 203-07	**3**
4	**5** Em., 25 Parts, 72-73 Lib., 45 Test, 202-03	**6** Em., 24 Parts, 72 Lib., 44-45 Arch., 5 Test, 201-02	**7** Em., 24 Parts, 72 Lib., 44 Test, 200-01	**8** Em., 24 Parts, 71-72 Lib., 43-44 Arch., 5 Test, 199-200	**9** Em., 24 Parts, 71 Lib., 43 Test, 198-99	**10** Parts, 71
11	**12** Em., 24 Parts, 71 Lib., 42-43 Test, 197	**13** Em., 24 Parts, 70-71 Lib., 42 Test, 196-97	**14** Parts, 69-70 Lib., 41-42 Test, 195-96	**15** Parts, 69 Lib., 40-41 Test, 195	**16** Parts, 69 Lib., 40 Test, 194	**17** Lib., 40
18	**19** Parts, 69 Lib., 39-40 Test, 193-94	**20** Em., 24 Parts, 69 Lib., 39 Test, 192-93	**21** Parts, 68-69 Lib., 38-39 Test, 192	**22** Parts, 67-68 Lib., 38 Test, 190-92	**23** Parts, 67 Lib., 37-38 Test, 189-90	**24**
25	**26** Lib., 37	**27** Lib., 36-37 Test, 189	**28** Parts, 67 Lib., 36 Test, 187-89	**29** Parts, 67 Lib., 35-36 Test, 187	**30** Em., 24 Parts, 66-67 Lib., 35 Test, 186	**31**

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June 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
1	**2** Em., 24 Lib., 34-35 Test, 185-86	**3** Em., 23-24 Parts, 66 Lib., 34 Arch., 5 Test, 184-85	**4** Em., 23 Parts, 65-66 Lib., 34 Test, 183-84	**5** Parts, 65 Lib., 33-34 Arch., 5 Test, 182-83	**6** Parts, 64-65 Lib., 32 Arch., 4 Test, 181-82	**7** Parts, 64
8 Parts, 64	**9** Em., 23 Parts, 64 Lib., 32 Arch., 4 Test, 180-81	**10** Em., 23 Parts, 63-64 Lib., 31-32 Arch., 4 Test, 180	**11** Em., 22 Parts, 63 Lib., 31 Arch., 4 Test, 179	**12** Em., 22 Parts, 62-63 Lib., 30-31 Test, 178-79	**13** Em., 22 Parts, 62 Arch., 3-4 Test, 178	**14** Parts, 62
15	**16** Em., 22 Parts, 61-62 Lib., 29-30 Arch., 3 Test, 177-78	**17** Em.,21-22 Parts, 61 Lib., 28-29 Arch., 3 Test, 176-77	**18** Em., 21 Parts, 61 Lib., 28 Arch., 3 Test, 175-76	**19** Em., 21 Parts, 60-61 Lib., 28 Test, 175	**20** Parts, 60 Lib., 28 Test, 174-75	**21**
22 Parts, 60	**23** Em., 21 Lib., 27-28 Test, 173-74	**24** Em., 21 Parts, 59-60 Lib., 26-27 Arch., 3 Test, 172-73	**25** Em., 21 Parts, 59 Lib., 26 Test, 171-72	**26** Em., 20-21 Parts, 58-59 Lib., 26 Test, 169-71	**27** Em., 20 Parts, 58 Lib., 25-26 Test, 169	**28**
29	**30** Em., 20 Parts, 57-58 Lib., 25 Test, 168-69					

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July 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
		1 Parts, 57 Lib., 24-25 Arch., 3 Test, 167-68	**2** Parts, 57 Lib., 23-24 Test, 166-67	**3** Parts, 57 Lib., 23 Test, 166	**4** Lib., 23	**5** Test, 165
6 Lib., 23	**7** Parts, 56-57 Lib., 23 Test, 165	**8** Em., 20 Parts, 56 Lib., 22-23 Test, 164-65	**9** Parts, 55-56 Lib., 22 Test, 163-64	**10** Em., 20 Parts, 55 Lib., 22 Arch., 2-3 Test, 161-63	**11** Parts, 55 Lib., 22 Test, 159-61	**12** Parts, 54-55 Test, 159
13	**14** Em., 20 Parts, 54 Lib., 21-22 Test, 157-59	**15** Parts, 53-54 Lib., 20-21 Arch., 2 Test, 156-57	**16** Em., 20 Parts, 53 Lib., 20 Test, 154-56	**17** Parts, 52-53 Lib., 20 Test, 153-54	**18** Em., 19 Parts, 52 Lib., 19-20 Test, 153	**19** Parts, 51-52
20	**21** Em., 19 Parts, 51 Lib., 19 Test, 151-53	**22** Em., 19 Parts, 51 Lib., 18-19 Test, 150-51	**23** Em., 19 Parts, 51 Lib., 17-18 Test, 148-50	**24** Parts, 51 Lib., 17 Test, 147-48	**25** Parts, 50-51 Lib., 17 Test, 146-47	**26**
27 Test, 145-46	**28** Em., 19 Parts, 50 Lib., 17 Test, 145	**29** Em., 19 Lib., 16 Test, 144-45	**30** Em., 18-19 Parts, 50 Lib., 16 Arch., 2 Test, 143-44	**31** Em., 18 Parts, 49-50 Lib., 15-16 Test, 142-43		

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August 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
					1 Parts, 49 Lib., 15 Arch., 2 Test, 142	**2**
3	**4** Parts, 49 Lib., 14 Test, 140-42	**5** Em., 18 Parts, 49 Lib., 14 Arch., 2 Test, 140	**6** Parts, 48-49 Lib., 14 Test, 139-40	**7** Em., 18 Parts, 48 Lib., 13-14 Test, 138-39	**8** Em., 18 Parts, 47-48 Lib., 13 Test, 137-38	**9**
10 Parts, 47	**11** Parts, 47 Lib., 13 Arch., 2 Test, 136-37	**12** Lib., 12-13 Arch., 2 Test, 135-36	**13** Em., 18 Parts, 47 Lib., 12 Arch., 2 Test, 134-35	**14** Lib., 12 Test, 133-34	**15** Parts, 46-47 Lib., 11-12 Test, 133	**16**
17	**18** Parts, 46 Lib., 10-11 Test, 133	**19** Em., 18 Test, 132-33	**20** Em., 17-18 Parts, 46 Lib., 10 Test, 130-32	**21** Arch., 2 Em., 17 Parts, 46 Lib., 10 Test, 129-30	**22** Em., 17 Parts, 46 Test, 127-29	**23**
24	**25** Parts, 46 Lib., 9 Test, 127	**26** Em., 17 Parts, 45-46 Test, 125-26	**27** Em.,16-17 Parts, 45 Lib., 9 Arch., 1-2 Test, 124-25	**28** Em., 16 Parts, 44-45 Lib., 8 Arch., 1 Test, 124	**29** Parts, 44 Lib., 8 Test, 123-24	**30** Parts, 44
31						

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September 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
	1	**2** Parts, 44 Test, 122	**3** Parts, 44 Lib., 8-9 Test, 121-22	**4** Parts, 44 Lib., 8 Test, 120-21	**5** Em., 16 Parts, 43-44 Lib., 7-8 Test, 119-20	**6** Parts, 43 Test, 118-19
7 Test, 118	**8** Em., 16 Parts, 43 Lib., 7 Test, 117-18	**9** Em., 16 Parts, 43 Lib., 7 Test, 115-17	**10** Em., 16 Parts, 42-43 Lib., 7 Test, 113-15	**11** Em., 15-16 Parts, 42 Lib., 7 Test, 112-13	**12** Parts, 42 Test, 111-12	**13** Parts, 41-42
14 Parts, 41 Test, 110-11	**15** Parts, 41 Lib., 6-7 Test, 109-10	**16** Em., 15 Parts, 41 Lib., 6 Arch., 1 Test, 107-09	**17** Em., 15 Parts, 41 Lib., 6 Test, 106-07	**18** Lib., 6 Test, 104-05	**19** Test, 102-04	**20** Parts, 40 Test, 102
21 Test, 101	**22** Parts, 39-40 Lib., 6 Test, 99-101	**23** Em., 15 Parts, 39 Lib., 5-6 Test, 97-99	**24** Em., 15 Parts, 39 Lib., 5 Test, 95-97	**25** Em., 14 Parts, 38-39 Lib., 5 Test, 92-95	**26** Em., 14 Parts, 38 Test, 89-92	**27**
28	**29** Em., 14 Parts, 37-38 Lib., 5 Test, 88-89	**30** Em., 14 Parts, 37 Lib., 5 Test, 87-88				

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October 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
			1 Em., 14 Parts, 36-37 Lib., 4-5 Test, 85-87	**2** Em., 14 Parts, 36 Lib., 4 Test, 83-85	**3** Em., 13-14 Parts, 36 Lib., 4 Test, 80-83	**4**
5	**6** Em., 13 Parts, 36 Arch., 1 Test, 80	**7** Em., 13 Parts, 35-36 Test, 77-80	**8** Em., 13 Parts, 35 Lib., 4 Test, 76-77	**9** Em., 13 Parts, 34 Lib., 3-4 Test, 75-76	**10** Parts, 34 Lib., 3 Test, 74-75	**11**
12	**13** Em., 13 Parts, 34 Test, 73-74	**14** Em., 13 Lib., 3 Test, 72-73	**15** Em., 12 Parts, 33 Lib., 3 Test, 70-72	**16** Em., 12 Parts, 33 Test, 69-70	**17** Parts, 33 Test, 68-69	**18**
19 Parts, 33	**20** Parts, 32-33 Test, 67-68	**21** Parts, 32 Lib., 3 Test, 65-66	**22** Em., 12 Parts, 32 Lib., 3 Test, 63-65	**23** Em., 12 Parts, 32 Test, 61-63	**24** Em., 12 Parts, 31 Test, 60-61	**25**
26 Parts, 31	**27** Em., 11 Parts, 30-31 Lib., 3 Test, 59-60	**28** Em., 11 Parts, 30 Test, 57-59	**29** Em., 11 Parts, 30 Test, 56-57	**30** Em., 11 Parts, 30 Lib., 3 Test, 56	**31** Em., 11 Test, 55-56	

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November 2003						
Sunday	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**	**Saturday**
						1 Parts, 29
2	**3** Em., 11 Parts, 29 Test, 53-55	**4** Em., 10-11 Parts, 29 Lib., 2 Test, 51-53	**5** Em., 10 Parts, 29 Test, 50-51	**6** Em., 10 Parts, 29 Test, 49-50	**7** Em., 10 Parts, 28-29 Test, 48-49	**8**
9	**10** Em., 10 Parts, 28 Lib., 2 Test, 47-48	**11** Parts, 28 Test, 46-47	**12** Parts, 28 Test, 45-46	**13** Parts, 27-28 Lib., 2 Test, 44-45	**14** Parts, 27 Test, 43-44	**15**
16 Parts, 27	**17** Em., 10 Test, 41-43	**18** Parts, 27 Test, 40-41	**19** Parts, 26-27 Lib., 2 Test, 39-40	**20** **Priority Application Filed**	**21**	**22**
23	**24**	**25**	**26**	**27**	**28**	**29**
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VI. EXHIBITS

53. The following Exhibits are relevant for this Declaration.

Exhibit Number	Reference
1001	U.S. Patent No. 6,897,871
2007	R400 Sequencer Specification (Version 0.1)
2009	R400 Sequencer Specification (Version 0.3)
2010	R400 Sequencer Specification (Version 0.4)
2011	R400 Sequencer Specification (Version 0.5)
2012	R400 Sequencer Specification (Version 0.6)
2013	R400 Sequencer Specification (Version 0.7)
2014	R400 Sequencer Specification (Version 0.8)
2015	R400 Sequencer Specification (Version 0.9)
2016	R400 Sequencer Specification (Version 1.0)
2017	R400 Sequencer Specification (Version 1.1)
2018	R400 Sequencer Specification (Version 1.2)
2020	R400 Sequencer Specification (Version 1.4)
2021	R400 Sequencer Specification (Version 1.5)
2022	R400 Sequencer Specification (Version 1.6)
2023	R400 Sequencer Specification (Version 1.7)
2024	R400 Sequencer Specification (Version 1.8)
2025	R400 Sequencer Specification (Version 1.9)
2026	R400 Sequencer Specification (Version 1.10)
2027	R400 Sequencer Specification (Version 1.11)
2028	R400 Sequencer Specification (Version 2.0)
2029	R400 Sequencer Specification (Version 2.1)

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2030	R400 Sequencer Specification (Version 2.2)
2031	R400 Sequencer Specification (Version 2.3)
2032	R400 Sequencer Specification (Version 2.4)
2033	R400 Sequencer Specification (Version 2.5)
2034	R400 Sequencer Specification (Version 2.6)
2035	R400 Sequencer Specification (Version 2.7)
2036	R400 Sequencer Specification (Version 2.8)
2037	R400 Sequencer Specification (Version 2.9)
2038	R400 Sequencer Specification (Version 2.10)
2039	R400 Sequencer Specification (Version 2.11)
2040	R400 Architecture Proposal (Version 0.1)
2041	R400 Top Level Specification (Version 0.2)
2042	R400 Shader Processor (Version 1.2)
2043	R400 Sequencer Specification Log (Versions 0.1 to 1.2)
2044	R400 Sequencer Specification Log (Versions 1.4 to 2.11)
2045	R400 Architecture Proposal Log
2046	R400 Top Level Specification Log
2047	R400 Shader Processor Log
2048	R400 Sequencer Emulator Folder History
2049	R400 Sequencer Parts Folder History
2050	R400 Document Library Folder History
2051	R400 Architecture Folder History
2052	R400 GFX Testing Folder History
2053	Peter Pellerite Program Review Slides (12/13/01)
2058	Mark Fowler Program Review Slides (3/22/02)
2061	Mark Fowler Program Review Slides (5/30/02)

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2066	Peter Pellerite Program Review Slides (8/30/02)
2072	R400 Shader Pipe Parts Folder History
2097	RTL Code File: sq_thread_arb.v

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. The statements in this declaration were made with the knowledge that willful false statements and the like are made punishable by fine or imprisonment under Section 1001 of Title 18 of the United States Code and that willful false statements may jeopardize the validity of the '871 patent.

Executed this 9th day of October 2015 in Montreal, Quebec, Canada.

Respectfully submitted,

____/Laurent Lefebvre/____

Laurent Lefebvre