Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 10478 on 2001/11/21 by askende@andi_r400

further update of the I/O definition

Change 9918 on 2001/11/14 by askende@andi_r400

first time check-in

Change 8480 on 2001/10/25 by askende@andi_r400

inserted into source control by Andi S.

Change 6887 on 2001/09/25 by askende@andi_r400_devel

more changes

Change 6810 on 2001/09/21 by askende@andi_r400_devel

newly added files

Change 5440 on 2001/08/16 by askende@andi_r400_devel

adding source code into source control

Change 5002 on 2001/08/02 by pmitchel@pmitchel_test_client

directory creation

```
//depot/r400/devel/parts_lib/src/gfx/sq/ais/sq_alu_instr_seq.v
... #83 change 132649 edit on 2003/11/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- alu_instr_seq timing fixes for constant store read: first the register stage
  on the offset was moved after the sum2 adder; then the init_done_bits signal
  was changed from a combinational ACS state machine output to a registered
  one-bit state machine output to help the path to the new sum2 register
- thread buff status read timing fix - moved the status read back one cycle by
  sending the unregistered, rotated request vector to the arbiter and registering
  the winner out of the arbiter; the output of the status read mux was
  then registered

... #82 change 130763 edit on 2003/11/07 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Reverting timing fix that broke r400sq_const_index_04.cpp test.

... #81 change 129723 edit on 2003/11/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed pix ctl output buffer overwrite bug
- backed timing fix out of status reg and pix thread buff

... #80 change 129066 edit on 2003/10/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added vtx input optimization for autocount on and continued off
- fixed initialization problem for vtx autocount
- made pix thread buff timing fixes: reduced load on status read
         data bit 19, which is the event bit, and also tried to reduce
         the load on pop_thread (part of the same path) in the status register
- backed out a timing fix in alu_instr_seq that was causing a mova
         test to fail
- fixed the AUTO_COUNT_SIZE definition

... #79 change 128209 edit on 2003/10/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fixes for constant store read address

... #78 change 126234 edit on 2003/10/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added export arbiter module that will limit the number of color buffer export
         threads to one every 4 clocks
- hooked up the export blocker outputs and commented out the previous export
         blocking code
```

```
- added export alloc arbiter inputs to exp_alloc_ctl module so that the buf_avail
         counter will be updated by the export allocs
- added logic to support the export arbiter to the vertex and pixel thread buffers
- added logic to support the export arbiter to the thread arbiter
- separated the export alloc request out of the alu request logic in the status
register,
         and added an output for the export alloc request

... #77 change 122520 edit on 2003/09/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

timing fixes - added registers for vs and ps base and size after the
       context register read mux

... #76 change 118589 edit on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for loop index clamping and constant address generation (both index and offset
relative)
- changed the connection of the real time bit such that it now goes directly from the
AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass

... #75 change 115595 edit on 2003/08/08 by dougd@dougd_r400_linux_marlboro (ktext)

fixed the path for the real time bit down the alu pipeline
to reach the constant and instruction stores.

... #74 change 115159 edit on 2003/08/06 by rramsey@rramsey_crayola_linux_orl (ktext)

Change sq_alu_instr_seq so gpr_rd_en is not asserted when reading constants
Changes to thread_arb, ctl_flow_seq, and status_reg to get mem exports flowing

... #73 change 111736 edit on 2003/07/17 by mmang@mmang_crayola_linux_orl (ktext)

Added sp->sx export arbitration between multiple simd engines.
Added register after instr_start OR of multiple simd engines by
taking unregistered signal out of sq_ais_output.

... #72 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
```

```
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #71 change 109679 edit on 2003/07/08 by llefebvr@llefebvr_r400_emu_montreal (ktext)

Fixed r400sp_mova_tests.cpp TEST_CASE=mova512.

The PVPS detection was rightly disabled during the waterfall but wasn't re-enabled for
the following instructions of the clause. I used the waterfall_done signal to re-enable
the PVPS detection after the waterfalling.

... #70 change 109466 edit on 2003/07/07 by dougd@dougd_r400_linux_marlboro (ktext)

fixed error in bit width of ais_real_time

... #69 change 109126 edit on 2003/07/03 by dougd@dougd_r400_linux_marlboro (ktext)

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

... #68 change 108760 edit on 2003/07/01 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Fixed r400sq_const_index_03.cpp. Now works on the SQSP testbench. Still has issues on
the GC because of bad ferret/cp ring buffer synchronization.

Fixed:

1) Bad clamping of the address register in the SP
2) Bad error handling of an out of range address in the SQ.

... #67 change 108222 edit on 2003/06/27 by smoss@smoss_crayola_linux_orl_regress
(ktext)

   I have too many i's

... #66 change 108188 edit on 2003/06/26 by mmang@mmang_crayola_linux_orl (ktext)

For pixel quads, enable all pixels of a quad when any pixel is hit
for gpr write enables and constant address waterfalling sequencing.
Another update will fix constant address register writing.
```

```
... #65 change 107757 edit on 2003/06/25 by mmantor@mmantor_crayola_linux_orl (ktext)

< 1. sq_alu_instr_seq.v  - Use the Queue pop signal to qualify last_in_clause
        and last_in_shader out of the queue.
     2. sq_target_instr_fetch.v  - Fixed a buf in the the target_instruct_fetch
        write to the queue to prevent dropping last_in_shader and last_in_clause
        if the queue is full when first trying to send instruction.  >

... #64 change 107389 edit on 2003/06/22 by mmang@mmang_crayola_linux_orl (ktext)

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

... #63 change 105592 edit on 2003/06/11 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Added storage element in the SQ to store the valid addresses of the mova so that they
```

```
can de restored at any instruction that uses the address register. The way it was
currently would only work if the use of the address was directly following the MOVA
instruction. This fixes r400sq_const_index_02.cpp.

... #62 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

... #61 change 101908 edit on 2003/05/21 by mmang@mmang_crayola_linux_orl (ktext)

Fixed bug in waterfalling by grabbing register input of done_bits
instead of registered value when performing init_done_bits operation.

... #60 change 99346 edit on 2003/05/06 by mmang@mmang_crayola_linux_orl (ktext)

Fixed bug (I created) related to initializing the constant address
register valids at the beginning of a clause.  I used ais_init_pred
which in some cases was too late.  Created new ais_init_const_addr
that is 3 clocks sooner.

... #59 change 98773 edit on 2003/05/02 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added constant address register valids to validate the
    address register data.  The valid is set when address register
    is written.  If valid is not set, sequencer will not waterfall
    those vertices or pixels.  This disables waterfalling for
    predicated off writes and improperly initialized contant
    address registers.
2.  Fixed bug in sqs_alu_instr_seq for phase 3 snooping of
    constant address registers bus.  Previously, this snooping
    did not account for predication of those registers.
3.  Fixed bug where ais_load_done_bits was not hooked up.  This
    signal disables previous vector/scalar management which needs
    to be turned off during constant waterfalling.  With bug,
    pvps logic went unknown which caused unknowns to eventually
    propagate in and out of the gprs.
4.  Fixed bug where non-optimized offset was not being determined
    properly.  non_opt_offset is determined by a priority encoder
    of p0_done, p1_done, p2_done, and p3_done.
5.  With advent of constant address register valids, created
    waterfall_active_q to properly init and avoid re-initing of
    different pixel and vertex done bits.
```

```
... #58 change 96946 edit on 2003/04/22 by viviana@viviana_crayola2_syn (ktext)

Added done_vector to sensitivity list at line 902.
   Removed `SQ_SRCB_PHASE from sensitivity list at line 1018.
   Added isr_thread_type_q to sensitivity list at line 1233.
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/sq.v
... #311 change 132649 edit on 2003/11/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- alu_instr_seq timing fixes for constant store read: first the register stage
  on the offset was moved after the sum2 adder; then the init_done_bits signal
  was changed from a combinational ACS state machine output to a registered
  one-bit state machine output to help the path to the new sum2 register
- thread buff status read timing fix - moved the status read back one cycle by
  sending the unregistered, rotated request vector to the arbiter and registering
  the winner out of the arbiter; the output of the status read mux was
  then registered

... #310 change 130421 edit on 2003/11/06 by bhankins@bhankins_xenos_linux_orl (ktext)

- sq-sx thread id added to sq output and into and through the sx
   - updated sx-rb trackers to use sq-sx thread id
   - removed obsolete code from sx
   - fixed sx bug where an ea from one export to memory was resetting the valid bits
for the other export to memory

... #309 change 129444 edit on 2003/10/30 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Fixing dangling wires in the sq related to performance module.
Fixing shader due to Kill opcode assembler change.
Fixing trakcer problem in the TB_SQSP when autocount vtx is on.

... #308 change 129259 edit on 2003/10/29 by danh@danh_xenos_linux_orl (ktext)

- spi_interp_ctl IJ buffer changed from one 16x200 memory to two 16x100 memories.
       - added additional SQ_SP_interp_qd[0:1]_prim_sela signals to improve spi input
timing.

... #307 change 129213 edit on 2003/10/29 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Added VC_PERF_ACTUAL_STARVED performance counter in the SQ.

... #306 change 129066 edit on 2003/10/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added vtx input optimization for autocount on and continued off
- fixed initialization problem for vtx autocount
- made pix thread buff timing fixes: reduced load on status read
         data bit 19, which is the event bit, and also tried to reduce
         the load on pop_thread (part of the same path) in the status register
- backed out a timing fix in alu_instr_seq that was causing a mova
```

```
         test to fail
- fixed the AUTO_COUNT_SIZE definition

... #305 change 128816 edit on 2003/10/27 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Adding VC performance counters in the SQ.
Removed the SX->RB warnings on non-initialized GPR channels.

... #304 change 128647 edit on 2003/10/27 by rramsey@rramsey_xenos_linux_orl (ktext)

Change ais so PS src sel gets priority over PV
Add predicated jumps and calls to cfs
Fix fetch_type connection in sq and tex_instr_seq

... #303 change 128601 edit on 2003/10/27 by mmantor@mmantor_xenos_linux_orl (ktext)

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

... #302 change 128393 edit on 2003/10/24 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

This should fix the instruction count being off. The bad machine (cfs) was used to
determine the thread type and hence some pixel shader instructions were counted as
vertex ones and vice versa.

... #301 change 128365 edit on 2003/10/24 by mearl@mearl_xenos_linux_orl (ktext)

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed
synthesis
       bugs in SC.

... #300 change 127895 edit on 2003/10/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fixes for gpr alloc

... #299 change 126823 edit on 2003/10/15 by rramsey@rramsey_xenos_linux_orl (ktext)

Add sqvc tracker to gc testbench when running with orlando trackers
Rework some of the alu/tex constant logic to get rid of the bug that
was allowing threads to start processing before all of the constants for
their context had been loaded.

... #298 change 126796 edit on 2003/10/15 by vromaker@vromaker_r400_linux_marlboro
```

```
(ktext)

- hooked up the new alu_arb_policy and tx_cache_sel register bits (but
         temporarily tied the tx_cache_sel input to the vtx thread buff low
         since it is being incorrectly set to 1 by Primlib)

... #297 change 126450 edit on 2003/10/13 by donaldl@donaldl_xenos_linux_orl (ktext)

Delayed SQ_SX_sp_simd_id an extra clock to line up for reduduncy use.

... #296 change 126234 edit on 2003/10/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added export arbiter module that will limit the number of color buffer export
         threads to one every 4 clocks
- hooked up the export blocker outputs and commented out the previous export
         blocking code
- added export alloc arbiter inputs to exp_alloc_ctl module so that the buf_avail
         counter will be updated by the export allocs
- added logic to support the export arbiter to the vertex and pixel thread buffers
- added logic to support the export arbiter to the thread arbiter
- separated the export alloc request out of the alu request logic in the status
register,
         and added an output for the export alloc request

... #295 change 125660 edit on 2003/10/08 by rramsey@rramsey_xenos_linux_orl (ktext)

Fix compile warnings for sq (several missing ports)
Fix compile warning in sx_parameter_caches
Fix SQ_SP_fetch_simd_sel so it lines up with the data coming out of the GPRs

... #294 change 125278 edit on 2003/10/07 by dougd@dougd_r400_linux_marlboro (ktext)

Added a new state register, vc_fifo_depths_l1_req_fifo_depth to
sq_rbbm_interface.v and wired it up to the compare logic for
vc_mini_count_q in sq_fetch_arb.v.

Corrected a typo in sq_vtx_ctl.v that affected synthesis.

... #293 change 124792 edit on 2003/10/03 by dougd@dougd_r400_linux_marlboro (ktext)

Removed all references to SIMD1_DISABLE in sq.v and sq_rbbm_interface.v.

Added 32 new performance counters: many are for SIMD2 and SIMD3 but
other existing counters were expanded to differentiate between vertex
and pixel counts. There are now 95 performance counters in the sq.

... #292 change 124203 edit on 2003/10/01 by dougd@dougd_r400_linux_marlboro (ktext)
```

```
The four existing SYNC_STALL counters were separated into
(8) pix and vtx stall counters.
The two ALU INSTRUCTION ISSUED counters were made to increment
by 1,2,3 or 4.
The two CF INSTRUCTION ISSUED counters were made to increment
by 1,2,3,4,5 or 6.

Added `ifdef's to sq_perfmon_wrapper for SIMD1, SIMD2, SIMD3.

perfmon event window:
An enable for the performance counters is generated by events received
from the VGT and/or SC which create a window of time when the counters
will be active. All of the perf counters are now controlled by this enable.

... #291 change 123952 edit on 2003/09/30 by mmantor@mmantor_xenos_linux_orl (ktext)

<added changes for 2 prim interpolation to the spi and sq and all top level
interconnects, and sq_sx_sp_simd_id for redundancy control, and all changes to test
bench as well as some ncverilog error messages.  Some other misc top level clean up>

... #290 change 123918 edit on 2003/09/29 by rramsey@rramsey_xenos_linux_orl (ktext)

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

... #289 change 123260 edit on 2003/09/25 by mmang@mmang_xenos_linux_orl (ktext)

1.  For Vivian E., added new simd memories and star patch in/out wires.
2.  In vertex thread buffer, fixed bug in simd3 alu state registers.
3.  In pixel thread buffer, fixed bug in simd2/3 cf state read data.
4.  Adjusted simd id bus width for sq to tp tracker.
5.  In sq.v, added vertex shader and pixel shader constant base and
    size connections to simd2/3 alu instruction sequencers.

... #288 change 123113 edit on 2003/09/24 by llefebvr@llefebvr_r400_linux_marlboro
```

(ktext)

Fixed the autocount pixel timing by removing 5 pipeline registers in the SQ control path. Also fixed the counter's with back to 17 bits (from 19) int both the vertex and pixel path such that when it hits the SP it is of the correct 23 bits width (17 bits count + 2 bits phase + 4 bits index). This fixes r400vgt_multi_pass_pix_shader_01 at the sqspsx testbench level.

... #287 change 123076 edit on 2003/09/24 by donaldl@donaldl_xenos_linux_orl (ktext)

Connected ROM block redundancy signals.
Added sq export address buffer support.

... #286 change 122683 edit on 2003/09/23 by mearl@mearl_crayola_linux_orl (ktext)

One primitieve per clock changes in the back of the SC and front of the SQ. Right now, the ONE_PRIM_PER_CLOCK define in
header.v and SC_SQ_interface.v are needed for this change. Will update this to ONEPPC, since this already exists in
header.v. Also, the sim.cfg file does not have an ifdef, so is hardcoded to one prim per clock.

... #285 change 122402 edit on 2003/09/20 by mmang@mmang_crayola_linux_orl (ktext)

1. Added simd2 and simd3 to code.
2. Added simd2 to synthesized code.
3. In sq.blk and sq_rbbm_interface, added DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3 to SQ_MISC_DEBUG register.
4. In header.v, turned on SIMD2_PRESENT.
5. In sc_packer.v, turned on SIMD2 but don't use it with SIMD2_PRESENT_TEMP.
6. In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v, and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2 and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7. In sq_export_alloc.v, handle position/main export id and parameter cache thread base for simd2/3. Be able to handle one type down simd0/1 and a different type down simd2/3 on the same clock.
8. In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd gpr_alloc blocks return different acks, gpr bases, and gpr maxes.
9. In sq_exp_alloc_ctrl.v, handle position/main export buffer management. Be able handle one type down simd0/1 and a different type down simd2/3 on the same clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v, added muxing and memories to handle status bits, cfs

```
    state, and alu state.  Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

... #284 change 121348 edit on 2003/09/15 by dougd@dougd_r400_linux_marlboro (ktext)

1. corrected the trigger events for VTX_SWAP_IN, VTX_SWAP_OUT,
   PIX_SWAP_IN, PIX_SWAP_OUT, CONSTANTS_USED_SIMD0 and  CONSTANTS_USED_SIMD0.
2. made event counters for these used multibit increment values
3. added  "+incdir+$PARTS_LIB/src/gfx/sp" to vcs_top.ini to pick up
   sp_defines.v included in sq_ais_output.v

... #283 change 121065 edit on 2003/09/12 by donaldl@donaldl_crayola_linux_orl (ktext)

Registered ROM_EN_RSP and ROM_PIPE_SEL[3:0].

... #282 change 120910 edit on 2003/09/12 by donaldl@donaldl_crayola_linux_orl (ktext)

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

... #281 change 120592 edit on 2003/09/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

changed SQ_hs_bclk, TST_SQ_rf_star_wrck, TST_SQ_hs_star_wrck so they
       are defined without the [0:0] range

... #280 change 120510 edit on 2003/09/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for SQ_VC_simd_id typo

... #279 change 120426 edit on 2003/09/10 by donaldl@donaldl_crayola_linux_orl (ktext)
```

```
Added redundancy logic.

... #278 change 120190 edit on 2003/09/09 by dougd@dougd_r400_linux_marlboro (ktext)

changed SQ_RB_event to SQ_RB_event_pulse and declared as output from sq.v

... #277 change 120087 edit on 2003/09/08 by dougd@dougd_r400_linux_marlboro (ktext)

Fixed 2 bugs in Real Time address logic in aluconst.
Added correct default value for INST_BASE_VTX in sq_rbbm_interface.v
Fixed bug in Real Time write data buffer in sq_instruction_store.v
Added missing input/output declarations for SIMD2 & SIMD3 signals to sq_aluconst_top.v
Clean up missing SIMD2, SIMD3 wire declarations in sq.v for the aluconst, is and cfc

... #276 change 119736 edit on 2003/09/05 by danh@danh_crayola1_linux_orl (ktext)

removed SQ_SP_interp_mode, SQ_SP_interp_buff_swap, added SQ_SP_interp_simd_id for
Redundant SP

... #275 change 119294 edit on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- instatiation of sq export blocker at sq top level
- thread buffer timing fix related to status read/export count update

... #274 change 119127 edit on 2003/09/02 by dougd@dougd_r400_linux_marlboro (ktext)

Added the extra memories and their support to the instruction and
constant stores to support 4 SIMD's. These memories and their
required wiring and control are instantiated with `ifdef and use
the SIMDn_PRESENT macros defined in header.v
Removed the use of SIMD1 macro.

... #273 change 118589 edit on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for loop index clamping and constant address generation (both index and offset
relative)
- changed the connection of the real time bit such that it now goes directly from the
AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass

... #272 change 118128 edit on 2003/08/26 by dclifton@dclifton_r400 (ktext)

Added definable # of simd's to sp.

... #271 change 117706 edit on 2003/08/22 by mmantor@mmantor_crayola_linux_orl (ktext)
```

```
<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with
modifications to their test benches and added
    ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with
SIMD1_PRESENT macro in the SC files>

... #270 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #269 change 116380 edit on 2003/08/13 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added separate gpr allocation/deallocation
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.

... #268 change 115728 edit on 2003/08/10 by rramsey@rramsey_crayola_linux_orl (ktext)

Change SQ to hold off popping the RBBM skid fifo while map copies are in
progress. This fixes the problem where gfx_copy writes were being missed
if they were less than 8 clks apart.
Get rid of extra write into RBBM skid fifo for reads, and instead zero out
we and re out of fifo if it's empty. The fifo was overflowing if the filling
entry was a read, since one additional entry was getting pushed.
sx_sp_pcdata tracker now ignores 4f5eaddf (unwritten pc locations)
Fix a problem in the sqsp testbench that was causing rbbm writes to be dropped
if the sq exerted back pressure.
```

```
... #267 change 115620 edit on 2003/08/08 by dougd@dougd_r400_linux_marlboro (ktext)

1. change all hs virage memories & files to have subword size in name
2. added diagnostic write enable from rbbm interface register to the modules
   with extra memories to support multiple SIMDs

... #266 change 115241 edit on 2003/08/06 by dougd@dougd_r400_linux_marlboro (ktext)

1. corrected the connections to sq_perfmon_wrapper to enable the
ALU active counters.

2. changed a few 1 bit vector declarations ( [0:0] ) to scalar
on SQ outputs because it caused errors in synthesis.

... #265 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #264 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #263 change 112073 edit on 2003/07/21 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for SQ_VC interface
- TP_SQ_dec was hooked up to the interface counter
- timing fix in vtx thread buffer
- simd_num connected thru ptr buff and pix ctl to pix thread buff
- performance fix in pix ctl

... #262 change 111905 edit on 2003/07/18 by ygiang@ygiang_r400_pv2_marlboro (ktext)

added: new perf counters for sq hardware

... #261 change 111736 edit on 2003/07/17 by mmang@mmang_crayola_linux_orl (ktext)

Added sp->sx export arbitration between multiple simd engines.
Added register after instr_start OR of multiple simd engines by
taking unregistered signal out of sq_ais_output.

... #260 change 111419 edit on 2003/07/16 by rramsey@rramsey_crayola_linux_orl (ktext)
```

```
Connect TST_awt_enable to vc_skid_buf and wire it up to the top level

... #259 change 111008 edit on 2003/07/14 by dougd@dougd_r400_linux_marlboro (ktext)

added logic to support programmable memory size for texconst and
aluconst stores.

... #258 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #257 change 110177 edit on 2003/07/10 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes to get simd_id piped down the vertex side and into the thread
buffer. Also only write the active simd's gprs and mux pipe_disable bits.
The memory in sq_vc_skid_buf increased by 1 bit, so this will require
a new memory to be checked in before running without USE_BEHAVE_MEM.

... #256 change 110083 edit on 2003/07/09 by dougd@dougd_r400_linux_marlboro (ktext)

added data output mux to select between the two memories (SIMD1, SIMD0)
for RBBM diagnostic reads. The mux is controlled by a rbbm register bit
in the SQ_DEBUG_MISC register.

... #255 change 110066 edit on 2003/07/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed a bug in tex instr seq related to back-to-back constant reads

... #254 change 110035 edit on 2003/07/09 by moev@moev2_r400_linux_marlboro (ktext)

Changed the HS Star Processor connections to match the clients. In particular BiraFail
& Err_pip_or

... #253 change 109814 edit on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro
```

```
(ktext)

- contains RT bit connection from pix input ctl to pix thread buff
- added SQ_TP_simd_id output to top level

... #252 change 109679 edit on 2003/07/08 by llefebvr@llefebvr_r400_emu_montreal
(ktext)

Fixed r400sp_mova_tests.cpp TEST_CASE=mova512.

The PVPS detection was rightly disabled during the waterfall but wasn't re-enabled for
the following instructions of the clause. I used the waterfall_done signal to re-enable
the PVPS detection after the waterfalling.

... #251 change 109671 edit on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated tex instr seq to sync to the texconst phase
- changed fetch arb to output both the mega grant and the mini
         grant to the tex instr seq

... #250 change 109126 edit on 2003/07/03 by dougd@dougd_r400_linux_marlboro (ktext)

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

... #249 change 108744 edit on 2003/07/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- registered winner_ack out of thread arb for timing
- connected correct instruction store read output based on SIMD1
  for VC ctl flow instruction reads; now SQ_VC interface appears to
  be driven correctly
- minor change to tb_sqsp (commented out random stall for TP_SQ_fetch
  stall, which no longer exists)

... #248 change 108676 edit on 2003/07/01 by dougd@dougd_r400_linux_marlboro (ktext)

generated trigger signals for SIMD0,SIMD1 perfmon counters

... #247 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (ktext)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
```

```
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #246 change 107579 edit on 2003/06/24 by dougd@dougd_r400_linux_marlboro (ktext)

ncverilog will error with
output [0:0] SQ_SP_instruct_start
wire  SQ_SP_instruct_start
because it considers the 1st declaration a vector and
the 2nd one a scalar.

... #245 change 107389 edit on 2003/06/22 by mmang@mmang_crayola_linux_orl (ktext)

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
```

```
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

... #244 change 106191 edit on 2003/06/14 by viviana@viviana_crayola2_syn (ktext)

48x154 memory changed to 48x155.

... #243 change 105943 edit on 2003/06/12 by dougd@dougd_r400_linux_marlboro (ktext)

Added a 2nd write buffer to aluconst, texconst and instruction store to handle
real time writes from cp mixed with non real time writes. This code passes the
mini-regress on tb_sqsp and cp_lcc_tex, cp_lcc_alu, cp_im_load_basic on the gc
testbench but fails cp_lcc_tex_rt and cp_lcc_alu_rt. It appears work for non-realtime.

Added real time prim bit from pix_ctl to ISM in pix_thread_buff when loading a
pixel thread. This bit will allow reading real time constants from the constant stores.

Added VC_wake_up logic.

... #242 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

... #241 change 105277 edit on 2003/06/10 by dougd@dougd_r400_linux_marlboro (ktext)

added output VC_clk_en to sq_rbbm_interface.v and wired it to
SQ_VC_wake_up in sq.v

... #240 change 104848 edit on 2003/06/08 by grayc@grayc_crayola2_linux_orl (ktext)

   fix simd1_valid -> simd1_const_valid

... #239 change 104797 edit on 2003/06/07 by grayc@grayc_crayola2_linux_orl (ktext)

   add VC ports
   modify SP-SQ port names

... #238 change 103932 edit on 2003/06/03 by mmantor@mmantor_crayola_linux_orl (ktext)
```

```
   update for new pipe disable routing

... #237 change 103365 edit on 2003/05/30 by dougd@dougd_r400_linux_marlboro (ktext)

Added missing wire declaration for param_wrap_0_set

... #236 change 103141 edit on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

... #235 change 102924 edit on 2003/05/28 by viviana@viviana_crayola2_syn (ktext)

Added an additional 48x170 and 16x170 and rebuilt the memories.

... #234 change 102264 edit on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated pix thread buffer for simd1 (and removed ctl sub module and redundant logic)
- renamed state_read_phase to arb_phase
- fixed CFSM serialize detection (had to add case of fetch initiated by current clause)
- removed reference to sq_thread_buff_cntl in tracker

... #233 change 102095 edit on 2003/05/22 by dougd@dougd_r400_linux_marlboro (ktext)

Added the following new fields to control registers in the rbbm interface:
 SQ_CONTEXT_MISC_PERFCOUNTER_REF
 SQ_CONTEXT_MISC_YEILD_OPTIMIZE
 SQ_FLOW_CONTROL_VC_ARBITRATION_POLICY
 SQ_FLOW_CONTROL_SIMD1_DISABLE
 SQ_DEBUG_MISC_DB_READ_MEMORY

... #232 change 102039 edit on 2003/05/22 by dougd@dougd_r400_linux_marlboro (ktext)

restored the missing line ".pb_event_state(pb_event_state)," to the instantiation of
sq_export_alloc in sq.v that somehow was removed when a merge was done in the last
submit

... #231 change 101906 edit on 2003/05/21 by dougd@dougd_r400_linux_marlboro (ktext)

added a 2nd read port for VC to texconst and redesigned sq_texconst_wrt_buff to perform
opportunistic writes because the write access slot was given up for VC reads
```

```
... #230 change 101642 edit on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
  fetch, instr que, and instr seq modules, and ais_output for simd1
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed

... #229 change 101009 edit on 2003/05/14 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes for parameter cache deallocation. Need to multiply dealloc
count by (vs_export_count +1) so the correct number of lines are
freed.

... #228 change 100877 edit on 2003/05/14 by rramsey@rramsey_crayola_linux_orl (ktext)

Fix 3 issues related to parameter cache allocation/deallocation
  1) Move allocate subtract for pc_free_cnt so it happens when
     an allocating vtx thread wins arbitration instead of when
     the thread is sent to the CFS. This puts the arbitration/
     allocate path at four clks (from six) so we can correctly
     allocate every four clocks.
  2) Deallocs were being dropped in sq_ptr_buff on back to back
     row transfers if the first of the pair was the last row
     (end of buffer) and the second of the pair had dealloc.
  3) Deallocs need to be accumulated in sq_ptr_buff since multiple
     row transfers of a pixel vector can be marked with dealloc
     and the deallocs are put in the event fifo at end_of_buffer.

Clean up some duplicate code in tb_sqsp and set the default dump
level back to 1 (instead of 3).

... #227 change 100795 edit on 2003/05/13 by dougd@dougd_r400_linux_marlboro (ktext)

corrected signal names to b1 ports of sq_cfc

... #226 change 100631 edit on 2003/05/13 by dougd@dougd_r400_linux_marlboro (ktext)

Added `define SIMD1 to header.v and corrected connections for SIMD1 in sq.v

... #225 change 100629 edit on 2003/05/13 by rramsey@rramsey_crayola_linux_orl (ktext)

Update tb_sqsp for latest SP top level changes
```

```
Zero out rbbm fifo data when writing for re_dly
Add a couple of missing wire declarations to sq

... #224 change 100468 edit on 2003/05/12 by dougd@dougd_r400_linux_marlboro (ktext)

removed incorrect bit width assignments to eo_rt_aluconst and eo_rt_texconst to prevent
compile errors with ncverilog

... #223 change 100164 edit on 2003/05/09 by dougd@dougd_r400_linux_marlboro (ktext)

ifdef'd connections in sq.v to sq_aluconst_top.v for the extra SIMD1 memory

... #222 change 100118 edit on 2003/05/09 by dougd@dougd_r400_linux_marlboro (ktext)

added 2nd memory to sq_cfc to support SIMD1 and ifdef'd the connections in sq_cfc and
sq.v

... #221 change 99918 edit on 2003/05/08 by dougd@dougd_r400_linux_marlboro (ktext)

fixed typo

... #220 change 99912 edit on 2003/05/08 by dougd@dougd_r400_linux_marlboro (ktext)

doubled the instruction store memory, changed the access allocation to accomdate SIMD1
and VC, and `ifdef'd the connections for SIMD1 in sq.v

... #219 change 99346 edit on 2003/05/06 by mmang@mmang_crayola_linux_orl (ktext)

Fixed bug (I created) related to initializing the constant address
register valids at the beginning of a clause.  I used ais_init_pred
which in some cases was too late.  Created new ais_init_const_addr
that is 3 clocks sooner.

... #218 change 99043 edit on 2003/05/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added VC ctl flow seq, instr fetch, instr que and instr seq, and top level IOs
- made some leda fixes
- added non time multiplexed gpr write address output to VC and TP (gpr_dst_addr[6:0])

... #217 change 98773 edit on 2003/05/02 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added constant address register valids to validate the
    address register data.  The valid is set when address register
    is written.  If valid is not set, sequencer will not waterfall
    those vertices or pixels.  This disables waterfalling for
    predicated off writes and improperly initialized contant
    address registers.
```

```
2.  Fixed bug in sqs_alu_instr_seq for phase 3 snooping of
    constant address registers bus.  Previously, this snooping
    did not account for predication of those registers.
3.  Fixed bug where ais_load_done_bits was not hooked up.  This
    signal disables previous vector/scalar management which needs
    to be turned off during constant waterfalling.  With bug,
    pvps logic went unknown which caused unknowns to eventually
    propagate in and out of the gprs.
4.  Fixed bug where non-optimized offset was not being determined
    properly.  non_opt_offset is determined by a priority encoder
    of p0_done, p1_done, p2_done, and p3_done.
5.  With advent of constant address register valids, created
    waterfall_active_q to properly init and avoid re-initing of
    different pixel and vertex done bits.

... #216 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v

... #215 change 97538 edit on 2003/04/24 by ygiang@ygiang_r400_pv2_marlboro (ktext)

added: more sq perf counters

... #214 change 97152 edit on 2003/04/23 by dougd@dougd_r400_linux_marlboro (ktext)

added logic to control vtx perf counters to sq_vtx_ctl.v and sq.v; fixed bug in write
logic in sq_aluconst_wrt_buf.v

... #213 change 96981 edit on 2003/04/22 by viviana@viviana_crayola2_syn (ktext)

Added TST_awt_enable to the interfaces with ss/sq_pix_thread_buff.v and
   ss/sq_vtx_thread_buff.v.
   Replaced the 16x155 and 48x155 memories with 16x170 and 48x170 respectively.
   Replaced the memory to be compiled in buildtb from the 155 to the 170.
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ais/sq_alu_instr_queue.v
... #72 change 130079 edit on 2003/11/04 by rramsey@rramsey_xenos_linux_orl (ktext)

Couple of timing fixes for aiq and cfs
Fix a bug in the rbbm if that was allowing map copies to happen before
memory writes
Fix a problem in the testbench that was causing some incompletes

... #71 change 128647 edit on 2003/10/27 by rramsey@rramsey_xenos_linux_orl (ktext)

Change ais so PS src sel gets priority over PV
Add predicated jumps and calls to cfs
Fix fetch_type connection in sq and tex_instr_seq

... #70 change 124850 edit on 2003/10/03 by rramsey@rramsey_xenos_linux_orl (ktext)

move an adder in front of a register and change to a fifo with registered
outputs to help timing

... #69 change 124792 edit on 2003/10/03 by dougd@dougd_r400_linux_marlboro (ktext)

Removed all references to SIMD1_DISABLE in sq.v and sq_rbbm_interface.v.

Added 32 new performance counters: many are for SIMD2 and SIMD3 but
other existing counters were expanded to differentiate between vertex
and pixel counts. There are now 95 performance counters in the sq.

... #68 change 123918 edit on 2003/09/29 by rramsey@rramsey_xenos_linux_orl (ktext)

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

... #67 change 122520 edit on 2003/09/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

timing fixes - added registers for vs and ps base and size after the
```

```
       context register read mux

... #66 change 118589 edit on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for loop index clamping and constant address generation (both index and offset
relative)
- changed the connection of the real time bit such that it now goes directly from the
AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass

... #65 change 117704 edit on 2003/08/22 by mmantor@mmantor_crayola_linux_orl (ktext)

<Fixed conflict between vec_3op_no_swap and scalar_const_op to control swizzle
correctly for the scalar engine and deliever the special gpr read  address  created in
the sq_ais_output block>

... #64 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #63 change 113039 edit on 2003/07/24 by danh@danh_crayola1_linux_orl (ktext)

Changed src_c_const_addr_rel generation so it matches the emulator code.

... #62 change 112899 edit on 2003/07/24 by danh@danh_crayola1_linux_orl (ktext)

Changed src_c_const_addr_rel generation.

... #61 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >
```

```
... #60 change 109951 edit on 2003/07/09 by llefebvr@llefebvr_r400_emu_montreal (ktext)

Fixing yet another mova problem when the mova is not back to back with it's use and
there is only one waterfall pass, PVPS detection wasn't re-enabled correctly. Fixes
mova_tests.cpp TEST_CASE=mova512_nop_check

... #59 change 109679 edit on 2003/07/08 by llefebvr@llefebvr_r400_emu_montreal (ktext)

Fixed r400sp_mova_tests.cpp TEST_CASE=mova512.

The PVPS detection was rightly disabled during the waterfall but wasn't re-enabled for
the following instructions of the clause. I used the waterfall_done signal to re-enable
the PVPS detection after the waterfalling.

... #58 change 109126 edit on 2003/07/03 by dougd@dougd_r400_linux_marlboro (ktext)

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

... #57 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (ktext)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #56 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
```

```
- recoded a few lines in gpr alloc to see if it will help timing

... #55 change 104616 edit on 2003/06/06 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

HW was clamping to 0 on a GPR addressing error. It should clamp to GPR_base of the
shader.

... #54 change 103141 edit on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

... #53 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/tis/sq_tex_instr_seq.v
... #45 change 132894 edit on 2003/11/19 by rramsey@rramsey_xenos_linux_orl (ktext)

Fix SQ_VC dec signals in tb_sqsp.
Change tbtrk_sqvc so it does not compare fetch addr for mini fetches.
Fix problem in tex_instr_seq that was allowing mini fetches to start
out of phase.
Add more info to msgs from pcdata tracker to tell which set of pc data
is mismatching. Also turn off sx1 compare since it is redundant now that
all the sx data comes from usx_0.

... #44 change 128647 edit on 2003/10/27 by rramsey@rramsey_xenos_linux_orl (ktext)

Change ais so PS src sel gets priority over PV
Add predicated jumps and calls to cfs
Fix fetch_type connection in sq and tex_instr_seq

... #43 change 126823 edit on 2003/10/15 by rramsey@rramsey_xenos_linux_orl (ktext)

Add sqvc tracker to gc testbench when running with orlando trackers
Rework some of the alu/tex constant logic to get rid of the bug that
was allowing threads to start processing before all of the constants for
their context had been loaded.

... #42 change 125660 edit on 2003/10/08 by rramsey@rramsey_xenos_linux_orl (ktext)

Fix compile warnings for sq (several missing ports)
Fix compile warning in sx_parameter_caches
Fix SQ_SP_fetch_simd_sel so it lines up with the data coming out of the GPRs

... #41 change 123918 edit on 2003/09/29 by rramsey@rramsey_xenos_linux_orl (ktext)

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

... #40 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)
```

```
1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #39 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #38 change 112073 edit on 2003/07/21 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for SQ_VC interface
- TP_SQ_dec was hooked up to the interface counter
- timing fix in vtx thread buffer
- simd_num connected thru ptr buff and pix ctl to pix thread buff
- performance fix in pix ctl

... #37 change 110177 edit on 2003/07/10 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes to get simd_id piped down the vertex side and into the thread
buffer. Also only write the active simd's gprs and mux pipe_disable bits.
The memory in sq_vc_skid_buf increased by 1 bit, so this will require
a new memory to be checked in before running without USE_BEHAVE_MEM.

... #36 change 110066 edit on 2003/07/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed a bug in tex instr seq related to back-to-back constant reads

... #35 change 109777 edit on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro
(ktext)


... #34 change 109671 edit on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated tex instr seq to sync to the texconst phase
- changed fetch arb to output both the mega grant and the mini
         grant to the tex instr seq

... #33 change 108744 edit on 2003/07/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- registered winner_ack out of thread arb for timing
```

```
- connected correct instruction store read output based on SIMD1
  for VC ctl flow instruction reads; now SQ_VC interface appears to
  be driven correctly
- minor change to tb_sqsp (commented out random stall for TP_SQ_fetch
  stall, which no longer exists)

... #32 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (ktext)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #31 change 106357 edit on 2003/06/16 by rramsey@rramsey_crayola_linux_orl (ktext)

fix latency of tp/sp signals in tb_sqsp after tp_formatter change
clean up the fetch swizzle warning msg in tb_sqsp
add new memory to sq/tb.f
fix fech_swizzle signal width in tex_instr_seq

... #30 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

... #29 change 101642 edit on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
  fetch, instr que, and instr seq modules, and ais_output for simd1
```

```
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed

... #28 change 99043 edit on 2003/05/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added VC ctl flow seq, instr fetch, instr que and instr seq, and top level IOs
- made some leda fixes
- added non time multiplexed gpr write address output to VC and TP (gpr_dst_addr[6:0])

... #27 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ss/sq_vtx_thread_buff.v
... #80 change 132649 edit on 2003/11/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- alu_instr_seq timing fixes for constant store read: first the register stage
  on the offset was moved after the sum2 adder; then the init_done_bits signal
  was changed from a combinational ACS state machine output to a registered
  one-bit state machine output to help the path to the new sum2 register
- thread buff status read timing fix - moved the status read back one cycle by
  sending the unregistered, rotated request vector to the arbiter and registering
  the winner out of the arbiter; the output of the status read mux was
  then registered

... #79 change 128601 edit on 2003/10/27 by mmantor@mmantor_xenos_linux_orl (ktext)

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

... #78 change 127861 edit on 2003/10/22 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Fixing TP and VC sync stalls for both pixel and vertex threads.

... #77 change 127269 edit on 2003/10/19 by rramsey@rramsey_xenos_linux_orl (ktext)

Change behave mem_model in spi so its read dly matches the real mem
Send interp_valid and ij_line 1clk early to account for 2clk read dly
Fix spi_sp tracker so it works with early valid
Change thread_buf and cfs machines so only fetches can modify the
fetch pending bit. The alu machines only read the value out of the buffer.
Get rid of a bunch of extra 'else' clauses

... #76 change 126796 edit on 2003/10/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- hooked up the new alu_arb_policy and tx_cache_sel register bits (but
         temporarily tied the tx_cache_sel input to the vtx thread buff low
         since it is being incorrectly set to 1 by Primlib)

... #75 change 126234 edit on 2003/10/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added export arbiter module that will limit the number of color buffer export
         threads to one every 4 clocks
- hooked up the export blocker outputs and commented out the previous export
         blocking code
```

```
- added export alloc arbiter inputs to exp_alloc_ctl module so that the buf_avail
         counter will be updated by the export allocs
- added logic to support the export arbiter to the vertex and pixel thread buffers
- added logic to support the export arbiter to the thread arbiter
- separated the export alloc request out of the alu request logic in the status
register,
         and added an output for the export alloc request

... #74 change 125697 edit on 2003/10/08 by dougd@dougd_r400_linux_marlboro (ktext)

fixed bug in eqn for *sync_alu_stall

... #73 change 124792 edit on 2003/10/03 by dougd@dougd_r400_linux_marlboro (ktext)

Removed all references to SIMD1_DISABLE in sq.v and sq_rbbm_interface.v.

Added 32 new performance counters: many are for SIMD2 and SIMD3 but
other existing counters were expanded to differentiate between vertex
and pixel counts. There are now 95 performance counters in the sq.

... #72 change 124203 edit on 2003/10/01 by dougd@dougd_r400_linux_marlboro (ktext)

The four existing SYNC_STALL counters were separated into
(8) pix and vtx stall counters.
The two ALU INSTRUCTION ISSUED counters were made to increment
by 1,2,3 or 4.
The two CF INSTRUCTION ISSUED counters were made to increment
by 1,2,3,4,5 or 6.

Added `ifdef's to sq_perfmon_wrapper for SIMD1, SIMD2, SIMD3.

perfmon event window:
An enable for the performance counters is generated by events received
from the VGT and/or SC which create a window of time when the counters
will be active. All of the perf counters are now controlled by this enable.

... #71 change 123331 edit on 2003/09/25 by dougd@dougd_r400_linux_marlboro (ktext)

usq_alu01_state_mem is used twice as the instance name so I changed
the 2nd one to usq_alu23_state_mem.

... #70 change 123260 edit on 2003/09/25 by mmang@mmang_xenos_linux_orl (ktext)

1.  For Vivian E., added new simd memories and star patch in/out wires.
2.  In vertex thread buffer, fixed bug in simd3 alu state registers.
3.  In pixel thread buffer, fixed bug in simd2/3 cf state read data.
4.  Adjusted simd id bus width for sq to tp tracker.
5.  In sq.v, added vertex shader and pixel shader constant base and
```

```
    size connections to simd2/3 alu instruction sequencers.

... #69 change 123076 edit on 2003/09/24 by donaldl@donaldl_xenos_linux_orl (ktext)

Connected ROM block redundancy signals.
Added sq export address buffer support.

... #68 change 122402 edit on 2003/09/20 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7.  In sq_export_alloc.v, handle position/main export id
    and parameter cache thread base for simd2/3.  Be able
    to handle one type down simd0/1 and a different type
    down simd2/3 on the same clock.
8.  In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
    gpr_alloc blocks return different acks, gpr bases,
    and gpr maxes.
9.  In sq_exp_alloc_ctrl.v, handle position/main export
    buffer management.  Be able handle one type down
    simd0/1 and a different type down simd2/3 on the same
    clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
    added muxing and memories to handle status bits, cfs
    state, and alu state.  Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
```

```
    simd data.<enter description here>

... #67 change 121348 edit on 2003/09/15 by dougd@dougd_r400_linux_marlboro (ktext)

1. corrected the trigger events for VTX_SWAP_IN, VTX_SWAP_OUT,
   PIX_SWAP_IN, PIX_SWAP_OUT, CONSTANTS_USED_SIMD0 and  CONSTANTS_USED_SIMD0.
2. made event counters for these used multibit increment values
3. added  "+incdir+$PARTS_LIB/src/gfx/sp" to vcs_top.ini to pick up
   sp_defines.v included in sq_ais_output.v

... #66 change 120190 edit on 2003/09/09 by dougd@dougd_r400_linux_marlboro (ktext)

changed SQ_RB_event to SQ_RB_event_pulse and declared as output from sq.v

... #65 change 119294 edit on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- instatiation of sq export blocker at sq top level
- thread buffer timing fix related to status read/export count update

... #64 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #63 change 116380 edit on 2003/08/13 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added separate gpr allocation/deallocation
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
```

```
    based on simd id.

... #62 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #61 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #60 change 112073 edit on 2003/07/21 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for SQ_VC interface
- TP_SQ_dec was hooked up to the interface counter
- timing fix in vtx thread buffer
- simd_num connected thru ptr buff and pix ctl to pix thread buff
- performance fix in pix ctl

... #59 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #58 change 108744 edit on 2003/07/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- registered winner_ack out of thread arb for timing
- connected correct instruction store read output based on SIMD1
  for VC ctl flow instruction reads; now SQ_VC interface appears to
  be driven correctly
```

```
- minor change to tb_sqsp (commented out random stall for TP_SQ_fetch
  stall, which no longer exists)

... #57 change 108676 edit on 2003/07/01 by dougd@dougd_r400_linux_marlboro (ktext)

generated trigger signals for SIMD0,SIMD1 perfmon counters

... #56 change 107389 edit on 2003/06/22 by mmang@mmang_crayola_linux_orl (ktext)

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

... #55 change 107266 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

reverted a change that was made for VC testing (and that did not work correctly)

... #54 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
```

```
(ktext)

- swapped PS and ID gpr write phases

... #53 change 103369 edit on 2003/05/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for width mismatch on thread_id input of vtx TB status regs
- initial pass of VC/TP fetch arbiter (not instantiated in sq.v yet)

... #52 change 103141 edit on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

... #51 change 102924 edit on 2003/05/28 by viviana@viviana_crayola2_syn (ktext)

Added an additional 48x170 and 16x170 and rebuilt the memories.

... #50 change 102264 edit on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated pix thread buffer for simd1 (and removed ctl sub module and redundant logic)
- renamed state_read_phase to arb_phase
- fixed CFSM serialize detection (had to add case of fetch initiated by current clause)
- removed reference to sq_thread_buff_cntl in tracker

... #49 change 101642 edit on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
  fetch, instr que, and instr seq modules, and ais_output for simd1
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed

... #48 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
```

```
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v

... #47 change 96981 edit on 2003/04/22 by viviana@viviana_crayola2_syn (ktext)

Added TST_awt_enable to the interfaces with ss/sq_pix_thread_buff.v and
   ss/sq_vtx_thread_buff.v.
   Replaced the 16x155 and 48x155 memories with 16x170 and 48x170 respectively.
   Replaced the memory to be compiled in buildtb from the 155 to the 170.
```

```
//depot/r400/devel/parts_lib/src/gfx/tp/tp.tree
... #71 change 131364 edit on 2003/11/11 by vbhatia@vbhatia_r400_linux_marlboro (ktext)

updated sub-block trackers

... #70 change 130892 edit on 2003/11/07 by vbhatia@vbhatia_r400_linux_marlboro (ktext)

       Initial checkin of Internal Trackers for TP which are controlled by
tp_track_control.cfg
       Still a work in progress, needs thorough validation and emulator updates to be
automatic

... #69 change 130524 edit on 2003/11/06 by tien@tien_r500_emu (ktext)

Added TP perf regs (on to TPC)
Cleaned up some tcf/tpc regs
After cleanup, added TPC_CHICKEN

... #68 change 123530 edit on 2003/09/26 by smburu@smburu_r400_linux_marlboro (ktext)

REQUIRED by changelist 123519.

... #67 change 120715 edit on 2003/09/11 by tien@tien_r500_emu (ktext)

Half of the lod_grad IO shrink change
Aniso control fix

... #66 change 118139 edit on 2003/08/26 by tien@tien_r500_emu (ktext)

MOre pix_mask stuff for predicate handling

... #65 change 118013 edit on 2003/08/25 by tien@tien_r500_emu (ktext)

Partial checkin 2-bit simd and full pix_mask pipelineing
(Not all the way thru yet) :-)

... #64 change 116191 edit on 2003/08/12 by smburu@smburu_r400_linux_marlboro (ktext)

Hicolor and WS changes. Requires new Emulator release from Jocelyn.

... #63 change 116104 edit on 2003/08/12 by tien@tien_r400_devel_marlboro (ktext)

Some changes for predicate tfetch (pix_mask) pipelining

... #62 change 115183 edit on 2003/08/06 by tien@tien_r400_devel_marlboro (ktext)

Unencoded DIM now driven to tp_addresser and tp_fetch
(for cubic mapping, proper face_id generation)
```

```
... #61 change 113623 edit on 2003/07/28 by tien@tien_r400_devel_marlboro (ktext)

Man it's been a long time coming :-)
formatter fix for TP to output to 1 simd only
drive simd signal from TPC to VC (will prolly need to skew it a bit, but that will fall
out from debug)
Clean up get/set logic

... #60 change 107077 edit on 2003/06/19 by smburu@smburu_r400_linux_marlboro (ktext)

Fix to Virage hook-up.

... #59 change 105024 edit on 2003/06/09 by smburu@smburu_r400_sun_marlboro (ktext)

Fixes for test IOs.

... #58 change 104450 edit on 2003/06/05 by nkociuk@nkociuk_r400_linux_marl (ktext)

misc cleanup...

... #57 change 103149 edit on 2003/05/29 by smburu@smburu_r400_linux_marlboro (ktext)

border color logic changes.

... #56 change 102959 edit on 2003/05/28 by tien@tien_r400_devel_marlboro (ktext)

Routed channel id to tp_fetch
Fixed loading of tp_tt

... #55 change 102755 edit on 2003/05/27 by tien@tien_r400_devel_marlboro (ktext)

Cleaned up some bad IO from tp_border until it is connected

... #54 change 100601 edit on 2003/05/12 by tien@tien_r400_devel_marlboro (ktext)

MOved unused bits in FIFOs to MSBs for future removal

... #53 change 100206 edit on 2003/05/09 by nkociuk@nkociuk_r400_linux_marl (ktext)

remove unused block...

... #52 change 99309 edit on 2003/05/06 by smburu@smburu_r400_linux_marlboro (ktext)

New test hook-up and Virage hook-up.
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/cfs/sq_ctl_flow_seq.v
... #126 change 130079 edit on 2003/11/04 by rramsey@rramsey_xenos_linux_orl (ktext)

Couple of timing fixes for aiq and cfs
Fix a bug in the rbbm if that was allowing map copies to happen before
memory writes
Fix a problem in the testbench that was causing some incompletes

... #125 change 129408 edit on 2003/10/30 by rramsey@rramsey_xenos_linux_orl (ktext)

Move some continuous assignments into always blocks to help sim time
Rework cfs_rtr/arb_xfc path to help timing
Fix a problem with detecting serialize for the cf state machine

... #124 change 128647 edit on 2003/10/27 by rramsey@rramsey_xenos_linux_orl (ktext)

Change ais so PS src sel gets priority over PV
Add predicated jumps and calls to cfs
Fix fetch_type connection in sq and tex_instr_seq

... #123 change 128195 edit on 2003/10/23 by rramsey@rramsey_xenos_linux_orl (ktext)

Fix a problem with yield_optimize

... #122 change 127730 edit on 2003/10/22 by rramsey@rramsey_xenos_linux_orl (ktext)

Fix a bug with start_of_clause

... #121 change 127580 edit on 2003/10/21 by danh@danh_xenos_linux_orl (ktext)

Changed any_pred_hi and any_pred_lo generation, now the predicate and valid bits are
now related to the thread that the CFS is working on.

... #120 change 127269 edit on 2003/10/19 by rramsey@rramsey_xenos_linux_orl (ktext)

Change behave mem_model in spi so its read dly matches the real mem
Send interp_valid and ij_line 1clk early to account for 2clk read dly
Fix spi_sp tracker so it works with early valid
Change thread_buf and cfs machines so only fetches can modify the
fetch pending bit. The alu machines only read the value out of the buffer.
Get rid of a bunch of extra 'else' clauses

... #119 change 124634 edit on 2003/10/02 by rramsey@rramsey_xenos_linux_orl (ktext)

adding cond_pred optimize to control flow seq

... #118 change 124203 edit on 2003/10/01 by dougd@dougd_r400_linux_marlboro (ktext)
```

```
The four existing SYNC_STALL counters were separated into
(8) pix and vtx stall counters.
The two ALU INSTRUCTION ISSUED counters were made to increment
by 1,2,3 or 4.
The two CF INSTRUCTION ISSUED counters were made to increment
by 1,2,3,4,5 or 6.

Added `ifdef's to sq_perfmon_wrapper for SIMD1, SIMD2, SIMD3.

perfmon event window:
An enable for the performance counters is generated by events received
from the VGT and/or SC which create a window of time when the counters
will be active. All of the perf counters are now controlled by this enable.

... #117 change 123918 edit on 2003/09/29 by rramsey@rramsey_xenos_linux_orl (ktext)

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

... #116 change 121292 edit on 2003/09/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed incorrect loading of loop indices from the thread buffer into
the ctl flow sequencer; this was causing a problem with the test
r400sq_const_index_07

... #115 change 118589 edit on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for loop index clamping and constant address generation (both index and offset
relative)
- changed the connection of the real time bit such that it now goes directly from the
AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass
```

```
... #114 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #113 change 115159 edit on 2003/08/06 by rramsey@rramsey_crayola_linux_orl (ktext)

Change sq_alu_instr_seq so gpr_rd_en is not asserted when reading constants
Changes to thread_arb, ctl_flow_seq, and status_reg to get mem exports flowing

... #112 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #111 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #110 change 111123 edit on 2003/07/15 by rramsey@rramsey_crayola_linux_orl (ktext)

had a typo in the vc_pending logic

... #109 change 110899 edit on 2003/07/14 by rramsey@rramsey_crayola_linux_orl (ktext)

change tp/vc pending bits so they look at tgt_instr_str_vc_q bits to
determine what type of fetch is being issued

... #108 change 110886 edit on 2003/07/14 by rramsey@rramsey_crayola_linux_orl (ktext)

mask off serial bit for first instruction of a clause.
this change fixes e2blit_src_8888 and probably some other hanging
e2/cp tests

... #107 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
```

```
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #106 change 110467 edit on 2003/07/11 by llefebvr@llefebvr_r400_emu_montreal
(ktext)

Disabling the COND_EXEC_PRED optimization. a COND_EXEC_PRED in the SQ is now threated
like a regular EXEC. We can re-enable this optimization in the future by putting the
thread back to the RS BEFORE making the predicate compare because now we are comapring
a dirty predicate bit set and it causes corruptions. This fixes mova_test.cpp
TEST_CASE=pMova_const.

... #105 change 109126 edit on 2003/07/03 by dougd@dougd_r400_linux_marlboro (ktext)

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

... #104 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- swapped PS and ID gpr write phases

... #103 change 106611 edit on 2003/06/17 by danh@danh_crayola1_linux_orl (ktext)

 Changed the cfs_return_addrs_q[51:0] generation so the correct cfs_return_addr[3:0]_q
order
 will be written into the thread buffer CFS mem when a thread is returned to the thread
buffer.

... #102 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

... #101 change 103141 edit on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)
```

```
- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

... #100 change 102264 edit on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated pix thread buffer for simd1 (and removed ctl sub module and redundant logic)
- renamed state_read_phase to arb_phase
- fixed CFSM serialize detection (had to add case of fetch initiated by current clause)
- removed reference to sq_thread_buff_cntl in tracker

... #99 change 101883 edit on 2003/05/21 by rramsey@rramsey_crayola_linux_orl (ktext)

fix pc write addr generation in ais_output
fix cf state machine so unexecuted conditionals don't cause a thread
to end
turn off cf trackers for now
fix a problem in the test bench related to draw pkts with no draw inits
(some cp tests do this)

... #98 change 100154 edit on 2003/05/09 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes for instruction store addressing (wrapping and absolute)
  Add absolute addressing for cf and exec addresses to cfs
  Add wrapping for jumps and calls to cfs
  Add wrapping for execute addresses to cfs
  Fix wrapping in instr_fetch (vtx wrap at pix_base-1)

These changes fix cp_event_timestamp_instruction_loading_stall at tb_sqsp

... #97 change 99043 edit on 2003/05/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added VC ctl flow seq, instr fetch, instr que and instr seq, and top level IOs
- made some leda fixes
- added non time multiplexed gpr write address output to VC and TP (gpr_dst_addr[6:0])

... #96 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
```

- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v

```
//depot/r400/devel/parts_lib/src/gfx/sq/ia/sq_input_arb.v
... #18 change 118878 edit on 2003/08/30 by rramsey@rramsey_crayola_linux_orl (ktext)

fix a deadlock condition between the input arb and vtx input controller

... #17 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- swapped PS and ID gpr write phases

... #16 change 103849 edit on 2003/06/03 by rramsey@rramsey_crayola_linux_orl (ktext)

Fix a bug in sq_input_arb that was allowing the state machine to go
to IDLE even though a pixel thread was active. This could allow a vtx
and pix thread to try and write into the GPRs at the same time.
Turn tex ctlflow trackers back on in tb_sqsp
Fix TP_SP_data_valid connections in tb_sqsp
Modify alu ctlflow trackers so they can skip over expected instr
with serialize bits set if the rtl does not serialize them

... #15 change 101841 edit on 2003/05/20 by askende@askende_r400_linux_marlboro (ktext)

checking in the interpolator control latency changes in SQ and SP.

... #14 change 101642 edit on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
  fetch, instr que, and instr seq modules, and ais_output for simd1
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_export_buffers.v
... #16 change 105986 delete on 2003/06/13 by bhankins@bhankins_crayola_linux_orl
(ktext)

delete obsolete files

... #15 change 100393 edit on 2003/05/12 by bhankins@bhankins_crayola_win_orl (ktext)

finish making change of mem_we to mem_wen

... #14 change 100382 edit on 2003/05/12 by bhankins@bhankins_crayola_win_orl (ktext)

rename mem_we to mem_wen

... #13 change 100381 edit on 2003/05/12 by bhankins@bhankins_crayola_win_orl (ktext)

fix input data rotate mux

... #12 change 100015 edit on 2003/05/08 by mmantor@mmantor_crayola_linux_orl (ktext)

<sq_ais_output - re-ordered kill_mask going to the sx so bits flow in order msb->lsg
sp2(v3-v0)sp0(v3-v0)) to match exp_mask
                  - removed improper final update of kill mask with predication mask
                  - enable export_mask for all exports
    SX_PA_interfaces.v - fixed checker for back to back transfers
    SX_RB_interfaces.v - hooked up to 7 bit sx_rb_index and rb_sx_index instead of
incorrect 8 bits
    sx.v - changed interfaces for sx_rb and rb_sx interfaces to become 7 bits instead
of 8 bits
    tb_sx.v - changed sx inputs to be 7 bits instead of 8 bits on the above index
interfaces
    tbmod_fake_sp.v - reordered the kill mask and enabled channel mask for exports
    sx_export_buffers.v - moved register after export mems and only load when memory
read, mimized client read muxes added input rotate muxes for export to memory
operations and indivual write address for each memory and set up predication,
kill_mask, alpha kill,and channel mask in the determination of writing data into the
export buffers
    sx_export_control.v - removed dead clock on rb and pa data fetch interface and
client and made arbiter behave as round robin and removed unecessary second input
register, added support for z render targets and multiple render targets and clean up
items
    ex_export_alloc_dealloc.v - enabled channel mask, kill mask, export_mask, and apha
test conditioning of valid bitsa doubled the free rate>
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/tis/sq_tex_instr_queue.v
... #28 change 122402 edit on 2003/09/20 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7.  In sq_export_alloc.v, handle position/main export id
    and parameter cache thread base for simd2/3.  Be able
    to handle one type down simd0/1 and a different type
    down simd2/3 on the same clock.
8.  In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
    gpr_alloc blocks return different acks, gpr bases,
    and gpr maxes.
9.  In sq_exp_alloc_ctrl.v, handle position/main export
    buffer management.  Be able handle one type down
    simd0/1 and a different type down simd2/3 on the same
    clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
    added muxing and memories to handle status bits, cfs
    state, and alu state.  Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

... #27 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
```

```
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #26 change 116380 edit on 2003/08/13 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added separate gpr allocation/deallocation
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.

... #25 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #24 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

... #23 change 103141 edit on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
```

```
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

... #22 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/misc/sq_defs.v
... #37 change 129150 edit on 2003/10/29 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Increasing VC mini count to ll_fifo_size +2.

... #36 change 129066 edit on 2003/10/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added vtx input optimization for autocount on and continued off
- fixed initialization problem for vtx autocount
- made pix thread buff timing fixes: reduced load on status read
         data bit 19, which is the event bit, and also tried to reduce
         the load on pop_thread (part of the same path) in the status register
- backed out a timing fix in alu_instr_seq that was causing a mova
         test to fail
- fixed the AUTO_COUNT_SIZE definition

... #35 change 128645 edit on 2003/10/27 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Incrementing the number of in flight testure requests from 6 to 7.

... #34 change 128365 edit on 2003/10/24 by mearl@mearl_xenos_linux_orl (ktext)

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed
synthesis
       bugs in SC.

... #33 change 126226 integrate on 2003/10/10 by cbrennan@cbrennan_r400_emu (ktext)

Release from my emu branch: texture stacks for TP as well.
Leda rule tweaks
add more .rg files

... ... copy from
//depot/r400/branches/devel_cbrennan/parts_lib/src/gfx/sq/misc/sq_defs.v#3
... #32 change 125806 edit on 2003/10/09 by cbrennan@cbrennan_r400_release (ktext)

Temporarily reduce the num SQ_TP vectors in flight back to 6 until fifo overflows can
be fixed.

... #31 change 125550 edit on 2003/10/08 by rramsey@rramsey_xenos_linux_orl (ktext)

Increase sq_tp_maxcount from 6 to 7
Fix a problem with the simd mux for vtx_alloc_size in export_alloc
Fix a problem with pc_alloc_free_cnt in export_alloc (alloc and dealloc on same clk
was broken)
```

Make alu ctl_flow and instr trackers work with multiple simd's
Also change these trackers to use common code for pix/vtx by selecting the type with
a parameter

... #30 change 123113 edit on 2003/09/24 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Fixed the autocount pixel timing by removing 5 pipeline registers in the SQ control
path. Also fixed the counter's with back to 17 bits (from 19) int both the vertex and
pixel path such that when it hits the SP it is of the correct 23 bits width (17 bits
count + 2 bits phase + 4 bits index). This fixes r400vgt_multi_pass_pix_shader_01 at
the sqspsx testbench level.

... #29 change 122683 edit on 2003/09/23 by mearl@mearl_crayola_linux_orl (ktext)

One primitieve per clock changes in the back of the SC and front of the SQ. Right now,
the ONE_PRIM_PER_CLOCK define in
       header.v and SC_SQ_interface.v are needed for this change. Will update this to
ONEPPC, since this already exists in
       header.v. Also, the sim.cfg file does not have an ifdef, so is hardcoded to one
prim per clock.

... #28 change 118215 edit on 2003/08/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

changed define for SQ_VC_MINI_MAXCOUNT from 16 to 32

... #27 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #26 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #25 change 109126 edit on 2003/07/03 by dougd@dougd_r400_linux_marlboro (ktext)

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

... #24 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

```
- swapped PS and ID gpr write phases

... #23 change 105943 edit on 2003/06/12 by dougd@dougd_r400_linux_marlboro (ktext)

Added a 2nd write buffer to aluconst, texconst and instruction store to handle
real time writes from cp mixed with non real time writes. This code passes the
mini-regress on tb_sqsp and cp_lcc_tex, cp_lcc_alu, cp_im_load_basic on the gc
testbench but fails cp_lcc_tex_rt and cp_lcc_alu_rt. It appears work for non-realtime.

Added real time prim bit from pix_ctl to ISM in pix_thread_buff when loading a
pixel thread. This bit will allow reading real time constants from the constant stores.

Added VC_wake_up logic.

... #22 change 103369 edit on 2003/05/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for width mismatch on thread_id input of vtx TB status regs
- initial pass of VC/TP fetch arbiter (not instantiated in sq.v yet)

... #21 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/is/sq_instruction_store.v
... #43 change 130127 edit on 2003/11/04 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- instruction writes to the different SIMD memories now happen
  independently and no longer wait for all SIMD memories to be
  available

... #42 change 125598 edit on 2003/10/08 by dougd@dougd_r400_linux_marlboro (ktext)

Expanded the read back mux for rbbm diagnostic reads
to include the extra memories for SIMD2 and SIMD3.

... #41 change 122699 edit on 2003/09/23 by dougd@dougd_r400_linux_marlboro (ktext)

fix typo (change blocking to non-blocking assignment)

... #40 change 122558 edit on 2003/09/22 by dougd@dougd_r400_linux_marlboro (ktext)

1. changed sq_stdrfsdks2p8x104cm1sw0 to sq_stdrfsdks2p8x105cm1sw0 in sq_vc_skid_buf.v
2. added timing fixes to sq_aluconst_mem.v, sq_aluconst_rams.v and
sq_instruction_store.v

... #39 change 122402 edit on 2003/09/20 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7.  In sq_export_alloc.v, handle position/main export id
    and parameter cache thread base for simd2/3.  Be able
    to handle one type down simd0/1 and a different type
    down simd2/3 on the same clock.
8.  In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
    gpr_alloc blocks return different acks, gpr bases,
    and gpr maxes.
9.  In sq_exp_alloc_ctrl.v, handle position/main export
    buffer management.  Be able handle one type down
    simd0/1 and a different type down simd2/3 on the same
    clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
```

```
    added muxing and memories to handle status bits, cfs
    state, and alu state.  Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

... #38 change 120087 edit on 2003/09/08 by dougd@dougd_r400_linux_marlboro (ktext)

Fixed 2 bugs in Real Time address logic in aluconst.
Added correct default value for INST_BASE_VTX in sq_rbbm_interface.v
Fixed bug in Real Time write data buffer in sq_instruction_store.v
Added missing input/output declarations for SIMD2 & SIMD3 signals to sq_aluconst_top.v
Clean up missing SIMD2, SIMD3 wire declarations in sq.v for the aluconst, is and cfc

... #37 change 119127 edit on 2003/09/02 by dougd@dougd_r400_linux_marlboro (ktext)

Added the extra memories and their support to the instruction and
constant stores to support 4 SIMD's. These memories and their
required wiring and control are instantiated with `ifdef and use
the SIMDn_PRESENT macros defined in header.v
Removed the use of SIMD1 macro.

... #36 change 116887 edit on 2003/08/18 by dougd@dougd_r400_linux_marlboro (ktext)

restore the `ifdef USE_BEHAVE_MEM that was removed for
testing of virage behavioral models.

... #35 change 115620 edit on 2003/08/08 by dougd@dougd_r400_linux_marlboro (ktext)

1. change all hs virage memories & files to have subword size in name
2. added diagnostic write enable from rbbm interface register to the modules
   with extra memories to support multiple SIMDs

... #34 change 113548 edit on 2003/07/28 by dougd@dougd_r400_linux_marlboro (ktext)

Added missing register stage in memory address path that caused
```

```
memory  failures only with the virage behavoral model.

... #33 change 110083 edit on 2003/07/09 by dougd@dougd_r400_linux_marlboro (ktext)

added data output mux to select between the two memories (SIMD1, SIMD0)
for RBBM diagnostic reads. The mux is controlled by a rbbm register bit
in the SQ_DEBUG_MISC register.

... #32 change 106293 edit on 2003/06/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

code fix to prevent latches

... #31 change 105943 edit on 2003/06/12 by dougd@dougd_r400_linux_marlboro (ktext)

Added a 2nd write buffer to aluconst, texconst and instruction store to handle
real time writes from cp mixed with non real time writes. This code passes the
mini-regress on tb_sqsp and cp_lcc_tex, cp_lcc_alu, cp_im_load_basic on the gc
testbench but fails cp_lcc_tex_rt and cp_lcc_alu_rt. It appears work for non-realtime.

Added real time prim bit from pix_ctl to ISM in pix_thread_buff when loading a
pixel thread. This bit will allow reading real time constants from the constant stores.

Added VC_wake_up logic.

... #30 change 102924 edit on 2003/05/28 by viviana@viviana_crayola2_syn (ktext)

Added an additional 48x170 and 16x170 and rebuilt the memories.

... #29 change 99912 edit on 2003/05/08 by dougd@dougd_r400_linux_marlboro (ktext)

doubled the instruction store memory, changed the access allocation to accomdate SIMD1
and VC, and `ifdef'd the connections for SIMD1 in sq.v

... #28 change 98142 edit on 2003/04/29 by rramsey@rramsey_crayola_linux_orl (ktext)

timing fix for rbi_addr
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/sp.v
... #92 change 132781 edit on 2003/11/19 by dclifton@dclifton_xenos_linux_orl (text)

Duplicated clock gaters in sp.v for test.
Force_m12_zero forces in3_gte_in12 high in sp_macc32 (makes 'x' * 0 consistently 0)
Fixed sensitivity list for pv_SrcCNegate and pv_SrcCAbs in sp_macc.
Created scalar stall for three operand vector ops in sp_macc to preserve previous
scalar.

... #91 change 125258 edit on 2003/10/07 by dclifton@dclifton_xenos_linux_orl (text)

Added a 'u' to instance names of const muxes

... #90 change 125257 edit on 2003/10/07 by dclifton@dclifton_xenos_linux_orl (text)

Fixed latency in pa.  Added mc mux for fanout control on const muxes
for alu constant data in sp.

... #89 change 121057 edit on 2003/09/12 by dclifton@dclifton_crayola_linux_orl (text)

I/O change for VC_SP_data_valid

... #88 change 120910 edit on 2003/09/12 by donaldl@donaldl_crayola_linux_orl (text)

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

... #87 change 120403 edit on 2003/09/10 by dclifton@dclifton_r400 (text)

Conditioned tp_sp_data_valid with gpr_phase for writes to gprs.  Enabled NEGATE signal
to scalar for SC_SUB_CONST_* opcodes

... #86 change 118941 edit on 2003/08/31 by tien@tien_r400_devel_marlboro (text)

One or two more checkins and predicate should be there

... #85 change 118682 edit on 2003/08/29 by dclifton@dclifton_crayola_linux_orl (text)

Connected up upper VC_SP_simd bit

... #84 change 118490 edit on 2003/08/28 by dclifton@dclifton_r400 (text)

Clean up of unused signals, fix of STAR signals in sp.v

... #83 change 118326 edit on 2003/08/27 by tien@tien_r400_devel_marlboro (text)

Final changes for simd expansion to 2 bits
```

```
... #82 change 118128 edit on 2003/08/26 by dclifton@dclifton_r400 (text)

Added definable # of simd's to sp.

... #81 change 112289 edit on 2003/07/22 by dclifton@dclifton_r400 (text)

Updated staging registers in sp_macc.
Revised sp_scalar_lut.
Test signals connected.

... #80 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (text)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #79 change 108942 edit on 2003/07/02 by dclifton@dclifton_r400 (text)

double buffered resets

... #78 change 108543 edit on 2003/06/30 by tien@tien_r400_devel_marlboro (text)

Vector width mismatch fixes

... #77 change 108494 edit on 2003/06/30 by tien@tien_r400_devel_marlboro (text)

Finalized VC_SP IO on the sp side

... #76 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (text)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
```

```
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #75 change 106822 edit on 2003/06/18 by moev@moev2_r400_linux_marlboro (text)

fixed patchbox to reflect proper connectivity of the star system

... #74 change 106572 edit on 2003/06/17 by tien@tien_r400_devel_marlboro (text)

More sp_tp_formatter changes and a port fix on tpc notied by Steve Mburu

... #73 change 106242 edit on 2003/06/15 by tien@tien_r400_devel_marlboro (text)

Added cmask gen code

... #72 change 106092 edit on 2003/06/13 by tien@tien_r400_devel_marlboro (text)

Many updates.

... #71 change 105565 edit on 2003/06/11 by askende@askende_r400_linux_marlboro (text)

top level clean-up

... #70 change 105079 edit on 2003/06/09 by grayc@grayc_crayola2_linux_orl (text)

   adding VC to chip build

... #69 change 104662 edit on 2003/06/06 by grayc@grayc_crayola2_linux_orl (text)

   added VC interfaces

... #68 change 104226 edit on 2003/06/05 by smoss@smoss_crayola_linux_orl (text)

   quick check-in for vc release (code works in release)

... #67 change 101841 edit on 2003/05/20 by askende@askende_r400_linux_marlboro (text)

checking in the interpolator control latency changes in SQ and SP.

... #66 change 101494 edit on 2003/05/18 by tien@tien_r400_devel_marlboro (text)
```

```
sp_tp_formatter fix

... #65 change 101419 edit on 2003/05/16 by tien@tien_r400_devel_marlboro (text)

Moved input flops out of sp_tp_formatter

... #64 change 100961 edit on 2003/05/14 by tien@tien_r400_devel_marlboro (text)

Fixed TP_SP_rf_expand_enable.

... #63 change 100175 edit on 2003/05/09 by askende@askende_r400_linux_marlboro (text)

releasing R500 related IO top level changes for SP/SPI system
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/tis/sq_target_instr_fetch.v
... #46 change 123918 edit on 2003/09/29 by rramsey@rramsey_xenos_linux_orl (ktext)

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

... #45 change 121292 edit on 2003/09/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed incorrect loading of loop indices from the thread buffer into
the ctl flow sequencer; this was causing a problem with the test
r400sq_const_index_07

... #44 change 118589 edit on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for loop index clamping and constant address generation (both index and offset
relative)
- changed the connection of the real time bit such that it now goes directly from the
AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass

... #43 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #42 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
```

```
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #41 change 109126 edit on 2003/07/03 by dougd@dougd_r400_linux_marlboro (ktext)

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

... #40 change 107757 edit on 2003/06/25 by mmantor@mmantor_crayola_linux_orl (ktext)

< 1. sq_alu_instr_seq.v  - Use the Queue pop signal to qualify last_in_clause
        and last_in_shader out of the queue.
     2. sq_target_instr_fetch.v  - Fixed a buf in the the target_instruct_fetch
        write to the queue to prevent dropping last_in_shader and last_in_clause
        if the queue is full when first trying to send instruction.  >

... #39 change 103141 edit on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

... #38 change 100154 edit on 2003/05/09 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes for instruction store addressing (wrapping and absolute)
  Add absolute addressing for cf and exec addresses to cfs
  Add wrapping for jumps and calls to cfs
  Add wrapping for execute addresses to cfs
  Fix wrapping in instr_fetch (vtx wrap at pix_base-1)

These changes fix cp_event_timestamp_instruction_loading_stall at tb_sqsp

... #37 change 99520 edit on 2003/05/07 by mmang@mmang_crayola_linux_orl (ktext)

Bug occurred where first_in_clause was getting lost when instr_queue
was full.  Previously, internal first_in_clause register was cleared
```

```
with tif_rts.  Had to delay clearing to tif_rts & tiq_rtr.

... #36 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_macc32.mc
... #88 change 132781 edit on 2003/11/19 by dclifton@dclifton_xenos_linux_orl (text)

Duplicated clock gaters in sp.v for test.
Force_m12_zero forces in3_gte_in12 high in sp_macc32 (makes 'x' * 0 consistently 0)
Fixed sensitivity list for pv_SrcCNegate and pv_SrcCAbs in sp_macc.
Created scalar stall for three operand vector ops in sp_macc to preserve previous
scalar.

... #87 change 131764 edit on 2003/11/13 by dclifton@dclifton_xenos_linux_orl (text)

Fixed inf feedback on dot product.

... #86 change 130983 edit on 2003/11/10 by dclifton@dclifton_xenos_linux_orl (text)

Disabled Nan detect for comp opcodes.

... #85 change 129423 edit on 2003/10/30 by dclifton@dclifton_xenos_linux_orl (text)

Fixed 0*Nan problem with DST Y result value

... #84 change 129128 edit on 2003/10/29 by dclifton@dclifton_xenos_linux_orl (text)

Fixed PRED_SET result.

... #83 change 127734 edit on 2003/10/22 by dclifton@dclifton_xenos_linux_orl (text)

Fixed recognition of Nans on in3

... #82 change 124330 edit on 2003/10/01 by dclifton@dclifton_xenos_linux_orl (text)

Updated timing parameters for 0.09um technology.

... #81 change 122779 edit on 2003/09/23 by dclifton@dclifton_xenos_linux_orl (text)

more changes for cube opcode

... #80 change 121904 edit on 2003/09/17 by dclifton@dclifton_crayola_linux_orl (text)

Fixes for cube opcode

... #79 change 120401 edit on 2003/09/10 by dclifton@dclifton_crayola_linux_orl (text)

Fixed neg zero plus neg zero.  Conditioned pred_execute output for active opcode.

... #78 change 118490 edit on 2003/08/28 by dclifton@dclifton_r400 (text)

Clean up of unused signals, fix of STAR signals in sp.v
```

```
... #77 change 117026 edit on 2003/08/19 by dclifton@dclifton_r400 (text)

Fixed -0 + -0 case in vector and scalar.
Fixed flip sign timing issue in sp_macc32.
Delayed negate signal to scalar to sync with input b.

... #76 change 115381 edit on 2003/08/07 by dclifton@dclifton_r400 (text)

sp_scalar_lut:  mova reverted to act like max, force_mul_prev2_max_float logic changed,
fixed clamp bug in log, clear sign on force zero, single operand inst for zero for b
input, masked pred_set_execute on anything but kill and pred_set ops.  sp_macc:
force_mul_prev2_max_float logic changed.  sp_macc32: masked inf, nan, or unknown unused
operands for DOT3 and DOT2 ops, disabled flip_sign for adds resolving to zero.
sp_vector:  removed extra register from exported scalar data, fixed mova fixed address
calculation.

... #75 change 114873 edit on 2003/08/04 by askende@askende_r400_linux_marlboro (text)

releasing changes

... #74 change 113214 edit on 2003/07/25 by askende@askende_r400_linux_marlboro (text)

fix related to PRED instructions

... #73 change 112289 edit on 2003/07/22 by dclifton@dclifton_r400 (text)

Updated staging registers in sp_macc.
Revised sp_scalar_lut.
Test signals connected.

... #72 change 110419 edit on 2003/07/11 by llefebvr@llefebvr_r400_emu_montreal (text)

Added MOVA to the list of compare opcodes. The SP instead of doing a simple compare of
the GPRs for mova (as it should do) was doing an Add. This was causing corruptions
whenever MOVA was used to move data from GPR to GPR. This change fixed test
mova_tests.cpp TEST_CASE=mova_reg.

... #71 change 107069 edit on 2003/06/19 by askende@askende_r400_linux_marlboro (text)

checking in changes related to area/timing optimization
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_macc_gpr.v
... #36 change 129408 edit on 2003/10/30 by rramsey@rramsey_xenos_linux_orl (ktext)

Move some continuous assignments into always blocks to help sim time
Rework cfs_rtr/arb_xfc path to help timing
Fix a problem with detecting serialize for the cf state machine

... #35 change 124738 edit on 2003/10/03 by smoss@smoss_crayola_linux_orl_regress
(ktext)

<Orlando Hardware Regression Results >

... #34 change 122989 edit on 2003/09/24 by dclifton@dclifton_xenos_linux_orl (ktext)

Moved output register after phase mux in sp_vector

... #33 change 120910 edit on 2003/09/12 by donaldl@donaldl_crayola_linux_orl (ktext)

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

... #32 change 118490 edit on 2003/08/28 by dclifton@dclifton_r400 (ktext)

Clean up of unused signals, fix of STAR signals in sp.v

... #31 change 112289 edit on 2003/07/22 by dclifton@dclifton_r400 (ktext)

Updated staging registers in sp_macc.
Revised sp_scalar_lut.
Test signals connected.

... #30 change 110836 edit on 2003/07/14 by dclifton@dclifton_r400 (ktext)

Removed DOS carriage returns

... #29 change 110300 edit on 2003/07/10 by viviana@viviana_crayola2_syn (ktext)

STAR_cmdscout should be an output of this module and not an input.

... #28 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (ktext)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
```

```
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #27 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- swapped PS and ID gpr write phases
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa_ccg_sxifsm.v
... #43 change 126888 edit on 2003/10/16 by bhankins@bhankins_xenos_linux_orl (ktext)

Fix perf monitoring signal

... #42 change 125597 edit on 2003/10/08 by bhankins@bhankins_xenos_linux_orl (ktext)

move adders outside of comb. process for timing.  no functional change.

... #41 change 120968 edit on 2003/09/12 by bhankins@bhankins_crayola_linux_orl (ktext)

Updates to simd_id for the sx inteface to use the id sent from the vgt.
   Also, add support for up to four simds.

... #40 change 106341 edit on 2003/06/16 by bhankins@bhankins_crayola_linux_orl (ktext)

fix the generation of nan_kill_flag bits from being reset buy subsequent non-NaN
numbers.

... #39 change 103605 edit on 2003/06/02 by bhankins@fl_bhankins_r400_win (ktext)

changes to accomodate bad pipe signals for 2 simds
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx.v
... #102 change 130421 edit on 2003/11/06 by bhankins@bhankins_xenos_linux_orl (text)

- sq-sx thread id added to sq output and into and through the sx
   - updated sx-rb trackers to use sq-sx thread id
   - removed obsolete code from sx
   - fixed sx bug where an ea from one export to memory was resetting the valid bits
for the other export to memory

... #101 change 129541 edit on 2003/10/31 by bhankins@bhankins_xenos_linux_orl (text)

clean up signal names for consistency.

... #100 change 129120 edit on 2003/10/29 by bhankins@bhankins_xenos_linux_orl (text)

add support for testing memory export data by including a value for the tracker that
   indicates how many bits the pixel quad mask has been shifted.

... #99 change 128319 edit on 2003/10/24 by bhankins@bhankins_xenos_linux_orl (text)

update the creation of the valid pixel table for export to memory

... #98 change 125780 edit on 2003/10/09 by bhankins@bhankins_xenos_linux_orl (text)

update sx test inputs to match the established convention

... #97 change 125637 edit on 2003/10/08 by bhankins@bhankins_xenos_linux_orl (text)

edits made for timing only.  no functional change.

... #96 change 124736 edit on 2003/10/03 by bhankins@bhankins_xenos_linux_orl (text)

1. Add support for second memory test processor
   2. Add updated behavioral code for mc block in sx

... #95 change 124224 edit on 2003/10/01 by bhankins@bhankins_xenos_linux_orl (text)

Changes made to try to improve on timing.  No functional change

... #94 change 123984 edit on 2003/09/30 by bhankins@bhankins_xenos_linux_orl (text)

change names of sx i/o ROM_MCn_disable signals

... #93 change 123795 edit on 2003/09/29 by donaldl@donaldl_xenos_linux_orl (text)

Allow sx parameter caches to accept 3 more pointers so it can
potentially process 2 primitives at once.
```

```
... #92 change 123515 edit on 2003/09/26 by bhankins@bhankins_xenos_linux_orl (text)

- add sx_redundancy.v to hierarchy to try and improve on timing
   - add EXP_BUF_112_DEEP switch.  comment out in sx_defines.v to enable
     all 128 locations of the color export buffer to be used
   - add ONE_STAR_PROCESSOR switch.  comment out in sx_defines.v to use
     two star processors.
   - add support for thread id and thread type for debug.
   - misc changes for timing which don't change the logic.

... #91 change 121325 edit on 2003/09/15 by bhankins@bhankins_crayola_linux_orl (text)

Recode redundancy select to try and improve on timing.

... #90 change 120895 edit on 2003/09/12 by bhankins@bhankins_crayola_linux_orl (text)

remove some debug logic

... #89 change 120887 edit on 2003/09/12 by bhankins@bhankins_crayola_linux_orl (text)

-  Add sx_mem_export.v module to capture pixel addresses and
      calculate rb id values for use in export to memory.
   -  Add support for redundancy logic.  Inputs are currently
      tied low in tb_sqsp.v and chip_sx.tree.
   -  Add non-synthesizable logic to route thread id and thread
      type from sq through sx and out to rb for test.  Allows
      tracker to identify export to memories, and to distinguish
      between them.  Tied low in chip_sx.tree and tb_sqsp.v
      All associated I/O and logic is qualified on `ifdef SIM.
   -  Remove the register in sx_export_control_common.v that was
      requiring some signals on the sq alloc interface to be present
      one clock before the valid.  Now, all sq_sx_exp_ signals are
      expected to be valid only when sq_sx_exp_valid == 1.
   -  Add a register in the generation of the final pixel address
      value for export to memory, to try and improve on timing.

... #88 change 118988 edit on 2003/09/02 by bhankins@bhankins_crayola_linux_orl (text)

- Pull position export buffer out as a separate memory.  Read-side access of pixel
buffer by the
     rb's no longer competes with pa read access of the position buffer.
   - Increase size of pixel buffer memory to 128.
   - Add hooks to control logic to use all 128 locations once the sq logic is ready.
     For now, only first 112 locations are used.
   - Split memory test into two pieces with two test processors.
   - Add hooks to use second memory test processor.  For now, only one is used, and the
sx i/o is
     unchanged from previous checkins.
```

```
   - Add new and remove obsolete memories.

... #87 change 118163 edit on 2003/08/26 by bhankins@bhankins_crayola_linux_orl (text)

   1. Initial checkin of code added to support export-to-memory.  This code is only
partially tested, and not at all optimized yet.
   2. Start to add (dum_mems only) for separate position export memory to split
position and color into two separate memories.
      pos is 16dx128wx16, pix has the full 128dx128wx16, but logic still wraps at 112
for sq compatibility for now.
   3. Split up read-side arbitration to give pa full access to pos buffer, while the
rb's compete only among themselves for the color buffer.

... #86 change 115032 edit on 2003/08/05 by grayc@grayc_crayola2_linux_orl (text)

   added back Laurent changes for sx performance counters
   modified sx.v for new performance register names

... #85 change 112093 edit on 2003/07/21 by bhankins@bhankins_crayola_linux_orl (text)

fix to keep a proper tally of position vectors exported when auxillary vectors are
included

... #84 change 111928 edit on 2003/07/18 by bhankins@bhankins_crayola_linux_orl (text)

misc fixes.  also add support for multiple render targets.  Not fully tested, and
currently disabled by default.

... #83 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (text)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #82 change 108642 edit on 2003/06/30 by donaldl@donaldl_crayola_linux_orl (text)

Added rbiu controls for real-time updates to parameter cache mems (real-time mems)
```

```
... #81 change 107781 edit on 2003/06/25 by bhankins@bhankins_crayola_linux_orl (text)

add register to output of alpha sample mask memory

... #80 change 107442 edit on 2003/06/23 by bhankins@bhankins_crayola_linux_orl (text)

fix memory test wiring error

... #79 change 107193 edit on 2003/06/20 by bhankins@bhankins_crayola_linux_orl (text)

fix scforce warning

... #78 change 105982 edit on 2003/06/13 by bhankins@bhankins_crayola_linux_orl (text)

advance sq-sx control signals by one clock to solve sx timing issues
   add support for updated sx hierarchy

... #77 change 104223 edit on 2003/06/05 by bhankins@bhankins_crayola_linux_orl (text)

fix STAR_cmdscout bus.  Partial hack until sx with new hierarchy is checked in

... #76 change 103932 edit on 2003/06/03 by mmantor@mmantor_crayola_linux_orl (text)

   update for new pipe disable routing

... #75 change 102242 edit on 2003/05/23 by grayc@grayc_crayola2_linux_orl (text)

   change memory name from sc to sx

... #74 change 101741 edit on 2003/05/20 by viviana@viviana_crayola2_syn (text)

Added sx_rf_awt_gate module and connected it.

... #73 change 100015 edit on 2003/05/08 by mmantor@mmantor_crayola_linux_orl (text)

<sq_ais_output - re-ordered kill_mask going to the sx so bits flow in order msb->lsg
sp2(v3-v0)sp0(v3-v0)) to match exp_mask
                  - removed improper final update of kill mask with predication mask
                  - enable export_mask for all exports
    SX_PA_interfaces.v - fixed checker for back to back transfers
    SX_RB_interfaces.v - hooked up to 7 bit sx_rb_index and rb_sx_index instead of
incorrect 8 bits
    sx.v - changed interfaces for sx_rb and rb_sx interfaces to become 7 bits instead
of 8 bits
    tb_sx.v - changed sx inputs to be 7 bits instead of 8 bits on the above index
interfaces
    tbmod_fake_sp.v - reordered the kill mask and enabled channel mask for exports
```

sx_export_buffers.v - moved register after export mems and only load when memory read, mimized client read muxes added input rotate muxes for export to memory operations and indivual write address for each memory and set up predication, kill_mask, alpha kill,and channel mask in the determination of writing data into the export buffers

sx_export_control.v - removed dead clock on rb and pa data fetch interface and client and made arbiter behave as round robin and removed unecessary second input register, added support for z render targets and multiple render targets and clean up items

ex_export_alloc_dealloc.v - enabled channel mask, kill mask, export_mask, and apha test conditioning of valid bitsa doubled the free rate>

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_macc.v
... #78 change 132781 edit on 2003/11/19 by dclifton@dclifton_xenos_linux_orl (ktext)

Duplicated clock gaters in sp.v for test.
Force_m12_zero forces in3_gte_in12 high in sp_macc32 (makes 'x' * 0 consistently 0)
Fixed sensitivity list for pv_SrcCNegate and pv_SrcCAbs in sp_macc.
Created scalar stall for three operand vector ops in sp_macc to preserve previous
scalar.

... #77 change 129408 edit on 2003/10/30 by rramsey@rramsey_xenos_linux_orl (ktext)

Move some continuous assignments into always blocks to help sim time
Rework cfs_rtr/arb_xfc path to help timing
Fix a problem with detecting serialize for the cf state machine

... #76 change 124754 edit on 2003/10/03 by dclifton@dclifton_xenos_linux_orl (ktext)

A few fixes for the mul_prev2 opcode.

... #75 change 120910 edit on 2003/09/12 by donaldl@donaldl_crayola_linux_orl (ktext)

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

... #74 change 120400 edit on 2003/09/10 by dclifton@dclifton_crayola_linux_orl (ktext)

Eliminated sign modifiers from prev opcodes for previous scalar operand

... #73 change 118490 edit on 2003/08/28 by dclifton@dclifton_r400 (ktext)

Clean up of unused signals, fix of STAR signals in sp.v

... #72 change 117446 edit on 2003/08/21 by dclifton@dclifton_r400 (ktext)

Changes for synthesis--removed unused pins from sp_comp_opcodes and sp_macc32_multiply.
Tweaked input delays on spi_hi_prec_int.

... #71 change 115381 edit on 2003/08/07 by dclifton@dclifton_r400 (ktext)

sp_scalar_lut:  mova reverted to act like max, force_mul_prev2_max_float logic changed,
fixed clamp bug in log, clear sign on force zero, single operand inst for zero for b
input, masked pred_set_execute on anything but kill and pred_set ops.  sp_macc:
force_mul_prev2_max_float logic changed.  sp_macc32: masked inf, nan, or unknown unused
operands for DOT3 and DOT2 ops, disabled flip_sign for adds resolving to zero.
sp_vector:  removed extra register from exported scalar data, fixed mova fixed address
calculation.
```

```
... #70 change 114873 edit on 2003/08/04 by askende@askende_r400_linux_marlboro (ktext)

releasing changes

... #69 change 112289 edit on 2003/07/22 by dclifton@dclifton_r400 (ktext)

Updated staging registers in sp_macc.
Revised sp_scalar_lut.
Test signals connected.

... #68 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (ktext)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #67 change 107997 edit on 2003/06/26 by mmantor@mmantor_crayola_linux_orl (ktext)

<remove extra delay stage on scalar_data for scalar_input_red when scalar_opcode_prev
and the creation of force_mul_prev2_max_float to compensate for the stage added back
into the scalar engine>

... #66 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- swapped PS and ID gpr write phases

... #65 change 107066 edit on 2003/06/19 by askende@askende_r400_linux_marlboro (ktext)

area/timing optimization

... #64 change 104895 edit on 2003/06/09 by rramsey@rramsey_crayola_linux_orl (ktext)

Fix a bug with sticky bit used for dot_product nan detection
```

```
... #63 change 97548 edit on 2003/04/25 by askende@askende_r400_linux_marlboro (ktext)

modified the PRED instructions to match the new definition. Src.W channel is now used
instead of Src.X

... #62 change 96874 edit on 2003/04/22 by rramsey@rramsey_crayola_linux_orl (ktext)

fix for pv/ps swizzling
```

```
//depot/r400/devel/parts_lib/src/gfx/sc/sc.v
... #162 change 132842 edit on 2003/11/19 by chammer@chammer_xenos_linux_orl (ktext)

Added changes for Xenos, enabled with `define XENOS
 Includes new rb_id, edram copy mode, zplane changes.

... #161 change 130164 edit on 2003/11/04 by chammer@chammer_xenos_linux_orl (ktext)

Switched SC_RCT(tile) interface to SC_BC(four quad) interface.

... #160 change 127729 edit on 2003/10/22 by rramsey@rramsey_xenos_linux_orl (ktext)

Add window_valid_busy counts to sc and change sc_starved_by_pa to only count busy
cycles

... #159 change 125786 edit on 2003/10/09 by mearl@mearl_xenos_linux_orl (ktext)

Fixed the unused port PA_SC_phase[0] when using ONEPPC

... #158 change 124706 edit on 2003/10/02 by donaldl@donaldl_xenos_linux_orl (ktext)

Changed data width of PA_SC_cntl1 from 30 bits to 29 bits to match
the PA (ie. msb wasn't used).

... #157 change 123755 edit on 2003/09/29 by mearl@mearl_xenos_linux_orl (ktext)

Fix for timing problems, submitting new memories, using real memories for regressions.

... #156 change 122897 edit on 2003/09/23 by ctaylor@ctaylor_xenos_linux_orl (ktext)

Removed 3,6,8 sample MSAA for Xenos.  Cleaned up remnants of render state leftover from
JSS.

... #155 change 122683 edit on 2003/09/23 by mearl@mearl_crayola_linux_orl (ktext)

One primitieve per clock changes in the back of the SC and front of the SQ. Right now,
the ONE_PRIM_PER_CLOCK define in
       header.v and SC_SQ_interface.v are needed for this change. Will update this to
ONEPPC, since this already exists in
       header.v. Also, the sim.cfg file does not have an ifdef, so is hardcoded to one
prim per clock.

... #154 change 120631 edit on 2003/09/11 by chammer@chammer_crayola_linux_orl (ktext)

Added SC_BC ports to chip_sc.tree as UNCONNECTED, tied BC_SC_RTR to 1

... #153 change 119992 edit on 2003/09/08 by rramsey@rramsey_crayola_linux_orl (ktext)
```

```
Add last_pixel logic to SC
Duplicate a bit in the qpp to help fanout

... #152 change 119475 edit on 2003/09/04 by chammer@chammer_crayola_linux_orl (ktext)

Added four quad per clock interface between SC and BC.

... #151 change 117706 edit on 2003/08/22 by mmantor@mmantor_crayola_linux_orl (ktext)

<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with
modifications to their test benches and added
    ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with
SIMD1_PRESENT macro in the SC files>

... #150 change 117311 edit on 2003/08/20 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes to sc for 4 qd/clk picker in KILL_ALL_PIXELS mode
Check in sc memory updates for Vivian
Add some missing connections in sqsp to fix compile warnings
Go to a global define for all trackers to control x vs 0 mismatch/warning
(MISMATCH_X_VS_0)

... #149 change 117140 edit on 2003/08/19 by donaldl@donaldl_crayola_linux_orl (ktext)

Updated for one primitive per clock but ifdef'd currently to work
as one primitive every 2 clocks.

... #148 change 116031 edit on 2003/08/12 by mearl@mearl_crayola_linux_orl (ktext)

added changes for simd id pipe disable logic

... #147 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >
```

```
... #146 change 103932 edit on 2003/06/03 by mmantor@mmantor_crayola_linux_orl (ktext)

   update for new pipe disable routing

... #145 change 99134 edit on 2003/05/05 by viviana@viviana_crayola2_syn (ktext)

Rebuilt the memories with 444 Mhz and Virage/3300 compiler.  Also, added
   sc_rf_awt_gate.v to sc.v for test purposes.

... #144 change 98461 edit on 2003/05/01 by rramsey@RRAMSEY_P4_r400_win (ktext)

fixes for some of the non-context based sc perfcounters
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ais/sq_ais_output.v
... #106 change 131537 edit on 2003/11/12 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

1) added register stage to line up pred_override bits with SP phase
2) made the waterfall/predicated override an or instead of an and.

... #105 change 129066 edit on 2003/10/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added vtx input optimization for autocount on and continued off
- fixed initialization problem for vtx autocount
- made pix thread buff timing fixes: reduced load on status read
         data bit 19, which is the event bit, and also tried to reduce
         the load on pop_thread (part of the same path) in the status register
- backed out a timing fix in alu_instr_seq that was causing a mova
         test to fail
- fixed the AUTO_COUNT_SIZE definition

... #104 change 128659 edit on 2003/10/27 by donaldl@donaldl_xenos_linux_orl (ktext)

Delayed rom_rsp_shift*_* mux shift selects 1 clk to fix synthesis timing.

... #103 change 126908 edit on 2003/10/16 by rramsey@rramsey_xenos_linux_orl (ktext)

absolute modifier for constants should apply to all source constants

... #102 change 123113 edit on 2003/09/24 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Fixed the autocount pixel timing by removing 5 pipeline registers in the SQ control
path. Also fixed the counter's with back to 17 bits (from 19) int both the vertex and
pixel path such that when it hits the SP it is of the correct 23 bits width (17 bits
count + 2 bits phase + 4 bits index). This fixes r400vgt_multi_pass_pix_shader_01 at
the sqspsx testbench level.

... #101 change 123076 edit on 2003/09/24 by donaldl@donaldl_xenos_linux_orl (ktext)

Connected ROM block redundancy signals.
Added sq export address buffer support.

... #100 change 120910 edit on 2003/09/12 by donaldl@donaldl_crayola_linux_orl (ktext)

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

... #99 change 120423 edit on 2003/09/10 by donaldl@donaldl_crayola_linux_orl (ktext)
```

```
Added redundancy logic.

... #98 change 118589 edit on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for loop index clamping and constant address generation (both index and offset
relative)
- changed the connection of the real time bit such that it now goes directly from the
AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass

... #97 change 117704 edit on 2003/08/22 by mmantor@mmantor_crayola_linux_orl (ktext)

<Fixed conflict between vec_3op_no_swap and scalar_const_op to control swizzle
correctly for the scalar engine and deliever the special gpr read  address  created in
the sq_ais_output block>

... #96 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #95 change 116380 edit on 2003/08/13 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added separate gpr allocation/deallocation
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.
```

```
... #94 change 111736 edit on 2003/07/17 by mmang@mmang_crayola_linux_orl (ktext)

Added sp->sx export arbitration between multiple simd engines.
Added register after instr_start OR of multiple simd engines by
taking unregistered signal out of sq_ais_output.

... #93 change 111317 edit on 2003/07/15 by mmang@mmang_crayola_linux_orl (ktext)

Blocking/non-blocking fix found by synthesis.

... #92 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #91 change 110512 edit on 2003/07/11 by mmang@mmang_crayola_linux_orl (ktext)

Fix for Vivian for synthesis in loop i07 and i15.

... #90 change 110177 edit on 2003/07/10 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes to get simd_id piped down the vertex side and into the thread
buffer. Also only write the active simd's gprs and mux pipe_disable bits.
The memory in sq_vc_skid_buf increased by 1 bit, so this will require
a new memory to be checked in before running without USE_BEHAVE_MEM.

... #89 change 109590 edit on 2003/07/07 by viviana@viviana_crayola2_syn (ktext)

Corrected another non-blocking assignment to blocking in a combinational logic block.

... #88 change 109565 edit on 2003/07/07 by viviana@viviana_crayola2_syn (ktext)

Corrected non-blocking assignments to blocking in combinational block.

... #87 change 109126 edit on 2003/07/03 by dougd@dougd_r400_linux_marlboro (ktext)
```

```
pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

... #86 change 109043 edit on 2003/07/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

made all loop counter variables unique for sythesis

... #85 change 108315 edit on 2003/06/27 by mmang@mmang_crayola_linux_orl (ktext)

Qualify constant address register write using constant waterfalling mask

... #84 change 108188 edit on 2003/06/26 by mmang@mmang_crayola_linux_orl (ktext)

For pixel quads, enable all pixels of a quad when any pixel is hit
for gpr write enables and constant address waterfalling sequencing.
Another update will fix constant address register writing.

... #83 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (ktext)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #82 change 107389 edit on 2003/06/22 by mmang@mmang_crayola_linux_orl (ktext)

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
```

```
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

... #81 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- swapped PS and ID gpr write phases

... #80 change 105982 edit on 2003/06/13 by bhankins@bhankins_crayola_linux_orl (ktext)

advance sq-sx control signals by one clock to solve sx timing issues
   add support for updated sx hierarchy

... #79 change 105784 edit on 2003/06/12 by rramsey@rramsey_crayola_linux_orl (ktext)

fix width of num_params_q

... #78 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
```

```
- recoded a few lines in gpr alloc to see if it will help timing

... #77 change 101883 edit on 2003/05/21 by rramsey@rramsey_crayola_linux_orl (ktext)

fix pc write addr generation in ais_output
fix cf state machine so unexecuted conditionals don't cause a thread
to end
turn off cf trackers for now
fix a problem in the test bench related to draw pkts with no draw inits
(some cp tests do this)

... #76 change 101642 edit on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
  fetch, instr que, and instr seq modules, and ais_output for simd1
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed

... #75 change 100015 edit on 2003/05/08 by mmantor@mmantor_crayola_linux_orl (ktext)

<sq_ais_output - re-ordered kill_mask going to the sx so bits flow in order msb->lsg
sp2(v3-v0)sp0(v3-v0)) to match exp_mask
                  - removed improper final update of kill mask with predication mask
                  - enable export_mask for all exports
    SX_PA_interfaces.v - fixed checker for back to back transfers
    SX_RB_interfaces.v - hooked up to 7 bit sx_rb_index and rb_sx_index instead of
incorrect 8 bits
    sx.v - changed interfaces for sx_rb and rb_sx interfaces to become 7 bits instead
of 8 bits
    tb_sx.v - changed sx inputs to be 7 bits instead of 8 bits on the above index
interfaces
    tbmod_fake_sp.v - reordered the kill mask and enabled channel mask for exports
    sx_export_buffers.v - moved register after export mems and only load when memory
read, mimized client read muxes added input rotate muxes for export to memory
operations and indivual write address for each memory and set up predication,
kill_mask, alpha kill,and channel mask in the determination of writing data into the
export buffers
    sx_export_control.v - removed dead clock on rb and pa data fetch interface and
client and made arbiter behave as round robin and removed unecessary second input
register, added support for z render targets and multiple render targets and clean up
items
    ex_export_alloc_dealloc.v - enabled channel mask, kill mask, export_mask, and apha
```

```
test conditioning of valid bitsa doubled the free rate>

... #74 change 99346 edit on 2003/05/06 by mmang@mmang_crayola_linux_orl (ktext)

Fixed bug (I created) related to initializing the constant address
register valids at the beginning of a clause.  I used ais_init_pred
which in some cases was too late.  Created new ais_init_const_addr
that is 3 clocks sooner.

... #73 change 98773 edit on 2003/05/02 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added constant address register valids to validate the
    address register data.  The valid is set when address register
    is written.  If valid is not set, sequencer will not waterfall
    those vertices or pixels.  This disables waterfalling for
    predicated off writes and improperly initialized contant
    address registers.
2.  Fixed bug in sqs_alu_instr_seq for phase 3 snooping of
    constant address registers bus.  Previously, this snooping
    did not account for predication of those registers.
3.  Fixed bug where ais_load_done_bits was not hooked up.  This
    signal disables previous vector/scalar management which needs
    to be turned off during constant waterfalling.  With bug,
    pvps logic went unknown which caused unknowns to eventually
    propagate in and out of the gprs.
4.  Fixed bug where non-optimized offset was not being determined
    properly.  non_opt_offset is determined by a priority encoder
    of p0_done, p1_done, p2_done, and p3_done.
5.  With advent of constant address register valids, created
    waterfall_active_q to properly init and avoid re-initing of
    different pixel and vertex done bits.

... #72 change 96738 edit on 2003/04/21 by mmang@mmang_crayola_linux_orl (ktext)

Fixed bug in sq_ais_output.v related to address register write and
predication.  Fixed a variety of tests to not use uninitialized gpr
or address registers.  2 tests still fail because of previous vector
scalar swizzle bug, 1 test still fails because of MOVA hardware bug, and
1 test still fails because of predicated address register write causes
XXXXXX which causes waterfalling to hang.
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ca/sq_thread_arb.v
... #43 change 132649 edit on 2003/11/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- alu_instr_seq timing fixes for constant store read: first the register stage
  on the offset was moved after the sum2 adder; then the init_done_bits signal
  was changed from a combinational ACS state machine output to a registered
  one-bit state machine output to help the path to the new sum2 register
- thread buff status read timing fix - moved the status read back one cycle by
  sending the unregistered, rotated request vector to the arbiter and registering
  the winner out of the arbiter; the output of the status read mux was
  then registered

... #42 change 128601 edit on 2003/10/27 by mmantor@mmantor_xenos_linux_orl (ktext)

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

... #41 change 126234 edit on 2003/10/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added export arbiter module that will limit the number of color buffer export
         threads to one every 4 clocks
- hooked up the export blocker outputs and commented out the previous export
         blocking code
- added export alloc arbiter inputs to exp_alloc_ctl module so that the buf_avail
         counter will be updated by the export allocs
- added logic to support the export arbiter to the vertex and pixel thread buffers
- added logic to support the export arbiter to the thread arbiter
- separated the export alloc request out of the alu request logic in the status
register,
         and added an output for the export alloc request

... #40 change 121292 edit on 2003/09/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed incorrect loading of loop indices from the thread buffer into
the ctl flow sequencer; this was causing a problem with the test
r400sq_const_index_07

... #39 change 119294 edit on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- instatiation of sq export blocker at sq top level
- thread buffer timing fix related to status read/export count update
```

```
... #38 change 116380 edit on 2003/08/13 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added separate gpr allocation/deallocation
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.

... #37 change 115159 edit on 2003/08/06 by rramsey@rramsey_crayola_linux_orl (ktext)

Change sq_alu_instr_seq so gpr_rd_en is not asserted when reading constants
Changes to thread_arb, ctl_flow_seq, and status_reg to get mem exports flowing

... #36 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #35 change 112073 edit on 2003/07/21 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for SQ_VC interface
- TP_SQ_dec was hooked up to the interface counter
- timing fix in vtx thread buffer
- simd_num connected thru ptr buff and pix ctl to pix thread buff
- performance fix in pix ctl

... #34 change 108744 edit on 2003/07/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- registered winner_ack out of thread arb for timing
```

```
- connected correct instruction store read output based on SIMD1
  for VC ctl flow instruction reads; now SQ_VC interface appears to
  be driven correctly
- minor change to tb_sqsp (commented out random stall for TP_SQ_fetch
  stall, which no longer exists)

... #33 change 102264 edit on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated pix thread buffer for simd1 (and removed ctl sub module and redundant logic)
- renamed state_read_phase to arb_phase
- fixed CFSM serialize detection (had to add case of fetch initiated by current clause)
- removed reference to sq_thread_buff_cntl in tracker

... #32 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v

... #31 change 96947 edit on 2003/04/22 by viviana@viviana_crayola2_syn (ktext)

Removed width from paramenter definitions.
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_vector.v
... #77 change 123973 edit on 2003/09/30 by dclifton@dclifton_xenos_linux_orl (ktext)

Moved output register past scalar fog mux

... #76 change 122991 edit on 2003/09/24 by dclifton@dclifton_xenos_linux_orl (ktext)

Moved output register in sp_macc_gpr past phase mux

... #75 change 120910 edit on 2003/09/12 by donaldl@donaldl_crayola_linux_orl (ktext)

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

... #74 change 120403 edit on 2003/09/10 by dclifton@dclifton_r400 (ktext)

Conditioned tp_sp_data_valid with gpr_phase for writes to gprs.  Enabled NEGATE signal
to scalar for SC_SUB_CONST_* opcodes

... #73 change 118490 edit on 2003/08/28 by dclifton@dclifton_r400 (ktext)

Clean up of unused signals, fix of STAR signals in sp.v

... #72 change 118127 edit on 2003/08/26 by dclifton@dclifton_crayola_linux_orl (ktext)

Fixed max pos clamp on const addr.  Eliminated some registers in export scalar fog
path.

... #71 change 117026 edit on 2003/08/19 by dclifton@dclifton_r400 (ktext)

Fixed -0 + -0 case in vector and scalar.
Fixed flip sign timing issue in sp_macc32.
Delayed negate signal to scalar to sync with input b.

... #70 change 115381 edit on 2003/08/07 by dclifton@dclifton_r400 (ktext)

sp_scalar_lut:  mova reverted to act like max, force_mul_prev2_max_float logic changed,
fixed clamp bug in log, clear sign on force zero, single operand inst for zero for b
input, masked pred_set_execute on anything but kill and pred_set ops.  sp_macc:
force_mul_prev2_max_float logic changed.  sp_macc32: masked inf, nan, or unknown unused
operands for DOT3 and DOT2 ops, disabled flip_sign for adds resolving to zero.
sp_vector:  removed extra register from exported scalar data, fixed mova fixed address
calculation.

... #69 change 112289 edit on 2003/07/22 by dclifton@dclifton_r400 (ktext)

Updated staging registers in sp_macc.
```

```
Revised sp_scalar_lut.
Test signals connected.

... #68 change 108760 edit on 2003/07/01 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Fixed r400sq_const_index_03.cpp. Now works on the SQSP testbench. Still has issues on
the GC because of bad ferret/cp ring buffer synchronization.

Fixed:

1) Bad clamping of the address register in the SP
2) Bad error handling of an out of range address in the SQ.

... #67 change 108140 edit on 2003/06/26 by rramsey@rramsey_crayola_linux_orl (ktext)

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

... #66 change 107389 edit on 2003/06/22 by mmang@mmang_crayola_linux_orl (ktext)

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
```

```
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

... #65 change 107174 edit on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- swapped PS and ID gpr write phases

... #64 change 106817 edit on 2003/06/18 by moev@moev2_r400_linux_marlboro (ktext)

fix port definition of STAR_cmdscout from input to output

... #63 change 100673 edit on 2003/05/13 by askende@askende_r400_linux_marlboro (ktext)

fix a typo related to out-of-range indexing

... #62 change 100175 edit on 2003/05/09 by askende@askende_r400_linux_marlboro (ktext)

releasing R500 related IO top level changes for SP/SPI system
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ss/sq_pix_thread_buff.v
... #77 change 132649 edit on 2003/11/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- alu_instr_seq timing fixes for constant store read: first the register stage
  on the offset was moved after the sum2 adder; then the init_done_bits signal
  was changed from a combinational ACS state machine output to a registered
  one-bit state machine output to help the path to the new sum2 register
- thread buff status read timing fix - moved the status read back one cycle by
  sending the unregistered, rotated request vector to the arbiter and registering
  the winner out of the arbiter; the output of the status read mux was
  then registered

... #76 change 129723 edit on 2003/11/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed pix ctl output buffer overwrite bug
- backed timing fix out of status reg and pix thread buff

... #75 change 129066 edit on 2003/10/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added vtx input optimization for autocount on and continued off
- fixed initialization problem for vtx autocount
- made pix thread buff timing fixes: reduced load on status read
         data bit 19, which is the event bit, and also tried to reduce
         the load on pop_thread (part of the same path) in the status register
- backed out a timing fix in alu_instr_seq that was causing a mova
         test to fail
- fixed the AUTO_COUNT_SIZE definition

... #74 change 128601 edit on 2003/10/27 by mmantor@mmantor_xenos_linux_orl (ktext)

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

... #73 change 127861 edit on 2003/10/22 by llefebvr@llefebvr_r400_linux_marlboro
(ktext)

Fixing TP and VC sync stalls for both pixel and vertex threads.

... #72 change 127269 edit on 2003/10/19 by rramsey@rramsey_xenos_linux_orl (ktext)

Change behave mem_model in spi so its read dly matches the real mem
Send interp_valid and ij_line 1clk early to account for 2clk read dly
Fix spi_sp tracker so it works with early valid
```

```
Change thread_buf and cfs machines so only fetches can modify the
fetch pending bit. The alu machines only read the value out of the buffer.
Get rid of a bunch of extra 'else' clauses

... #71 change 126983 edit on 2003/10/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed code that was causing a latch in synthesis

... #70 change 126234 edit on 2003/10/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added export arbiter module that will limit the number of color buffer export
         threads to one every 4 clocks
- hooked up the export blocker outputs and commented out the previous export
         blocking code
- added export alloc arbiter inputs to exp_alloc_ctl module so that the buf_avail
         counter will be updated by the export allocs
- added logic to support the export arbiter to the vertex and pixel thread buffers
- added logic to support the export arbiter to the thread arbiter
- separated the export alloc request out of the alu request logic in the status
register,
         and added an output for the export alloc request

... #69 change 125697 edit on 2003/10/08 by dougd@dougd_r400_linux_marlboro (ktext)

fixed bug in eqn for *sync_alu_stall

... #68 change 124792 edit on 2003/10/03 by dougd@dougd_r400_linux_marlboro (ktext)

Removed all references to SIMD1_DISABLE in sq.v and sq_rbbm_interface.v.

Added 32 new performance counters: many are for SIMD2 and SIMD3 but
other existing counters were expanded to differentiate between vertex
and pixel counts. There are now 95 performance counters in the sq.

... #67 change 124203 edit on 2003/10/01 by dougd@dougd_r400_linux_marlboro (ktext)

The four existing SYNC_STALL counters were separated into
(8) pix and vtx stall counters.
The two ALU INSTRUCTION ISSUED counters were made to increment
by 1,2,3 or 4.
The two CF INSTRUCTION ISSUED counters were made to increment
by 1,2,3,4,5 or 6.

Added `ifdef's to sq_perfmon_wrapper for SIMD1, SIMD2, SIMD3.

perfmon event window:
```

```
An enable for the performance counters is generated by events received
from the VGT and/or SC which create a window of time when the counters
will be active. All of the perf counters are now controlled by this enable.

... #66 change 123260 edit on 2003/09/25 by mmang@mmang_xenos_linux_orl (ktext)

1.  For Vivian E., added new simd memories and star patch in/out wires.
2.  In vertex thread buffer, fixed bug in simd3 alu state registers.
3.  In pixel thread buffer, fixed bug in simd2/3 cf state read data.
4.  Adjusted simd id bus width for sq to tp tracker.
5.  In sq.v, added vertex shader and pixel shader constant base and
    size connections to simd2/3 alu instruction sequencers.

... #65 change 123076 edit on 2003/09/24 by donaldl@donaldl_xenos_linux_orl (ktext)

Connected ROM block redundancy signals.
Added sq export address buffer support.

... #64 change 122402 edit on 2003/09/20 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7.  In sq_export_alloc.v, handle position/main export id
    and parameter cache thread base for simd2/3.  Be able
    to handle one type down simd0/1 and a different type
    down simd2/3 on the same clock.
8.  In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
    gpr_alloc blocks return different acks, gpr bases,
    and gpr maxes.
9.  In sq_exp_alloc_ctrl.v, handle position/main export
    buffer management.  Be able handle one type down
    simd0/1 and a different type down simd2/3 on the same
    clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
    added muxing and memories to handle status bits, cfs
    state, and alu state.  Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
```

```
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

... #63 change 121348 edit on 2003/09/15 by dougd@dougd_r400_linux_marlboro (ktext)

1. corrected the trigger events for VTX_SWAP_IN, VTX_SWAP_OUT,
   PIX_SWAP_IN, PIX_SWAP_OUT, CONSTANTS_USED_SIMD0 and  CONSTANTS_USED_SIMD0.
2. made event counters for these used multibit increment values
3. added  "+incdir+$PARTS_LIB/src/gfx/sp" to vcs_top.ini to pick up
   sp_defines.v included in sq_ais_output.v

... #62 change 119294 edit on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- instatiation of sq export blocker at sq top level
- thread buffer timing fix related to status read/export count update

... #61 change 117504 edit on 2003/08/21 by mmang@mmang_crayola_linux_orl (ktext)

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

... #60 change 117311 edit on 2003/08/20 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes to sc for 4 qd/clk picker in KILL_ALL_PIXELS mode
Check in sc memory updates for Vivian
Add some missing connections in sqsp to fix compile warnings
Go to a global define for all trackers to control x vs 0 mismatch/warning
(MISMATCH_X_VS_0)

... #59 change 116380 edit on 2003/08/13 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added separate gpr allocation/deallocation
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
```

```
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.

... #58 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #57 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #56 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #55 change 108676 edit on 2003/07/01 by dougd@dougd_r400_linux_marlboro (ktext)
```

```
generated trigger signals for SIMD0,SIMD1 perfmon counters

... #54 change 107389 edit on 2003/06/22 by mmang@mmang_crayola_linux_orl (ktext)

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

... #53 change 106190 edit on 2003/06/14 by viviana@viviana_crayola2_syn (ktext)

Changed the width of the state memory to 155 bits.

... #52 change 105943 edit on 2003/06/12 by dougd@dougd_r400_linux_marlboro (ktext)

Added a 2nd write buffer to aluconst, texconst and instruction store to handle
real time writes from cp mixed with non real time writes. This code passes the
mini-regress on tb_sqsp and cp_lcc_tex, cp_lcc_alu, cp_im_load_basic on the gc
testbench but fails cp_lcc_tex_rt and cp_lcc_alu_rt. It appears work for non-realtime.
```

```
Added real time prim bit from pix_ctl to ISM in pix_thread_buff when loading a
pixel thread. This bit will allow reading real time constants from the constant stores.

Added VC_wake_up logic.

... #51 change 105465 edit on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

... #50 change 103141 edit on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

... #49 change 102924 edit on 2003/05/28 by viviana@viviana_crayola2_syn (ktext)

Added an additional 48x170 and 16x170 and rebuilt the memories.

... #48 change 102365 edit on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

moved wire declaration of sx_exp_buff_full_0 (and others) before the
instantiation of the status registers to fix ncverilog warning

... #47 change 102264 edit on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated pix thread buffer for simd1 (and removed ctl sub module and redundant logic)
- renamed state_read_phase to arb_phase
- fixed CFSM serialize detection (had to add case of fetch initiated by current clause)
- removed reference to sq_thread_buff_cntl in tracker

... #46 change 101642 edit on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
```

```
  fetch, instr que, and instr seq modules, and ais_output for simdl
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed

... #45 change 99315 edit on 2003/05/06 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed typos that were causing cp_e2polyscanlines_simple to fail

... #44 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v

... #43 change 96981 edit on 2003/04/22 by viviana@viviana_crayola2_syn (ktext)

Added TST_awt_enable to the interfaces with ss/sq_pix_thread_buff.v and
   ss/sq_vtx_thread_buff.v.
   Replaced the 16x155 and 48x155 memories with 16x170 and 48x170 respectively.
   Replaced the memory to be compiled in buildtb from the 155 to the 170.
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_parameter_caches.v
... #30 change 128657 edit on 2003/10/27 by donaldl@donaldl_xenos_linux_orl (ktext)

Added muxes to output of real-time parameter cache mems to select the
correct parameter based on bits [8:7] of the ptr selects.

... #29 change 128365 edit on 2003/10/24 by mearl@mearl_xenos_linux_orl (ktext)

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed
synthesis
       bugs in SC.

... #28 change 126859 edit on 2003/10/15 by donaldl@donaldl_xenos_linux_orl (ktext)

Fixed error - need to delay SX_SQ_vtx_data3 an extra clock.

... #27 change 125820 edit on 2003/10/09 by bhankins@bhankins_xenos_linux_orl (ktext)

fix unconnected inputs

... #26 change 125660 edit on 2003/10/08 by rramsey@rramsey_xenos_linux_orl (ktext)

Fix compile warnings for sq (several missing ports)
Fix compile warning in sx_parameter_caches
Fix SQ_SP_fetch_simd_sel so it lines up with the data coming out of the GPRs

... #25 change 123795 edit on 2003/09/29 by donaldl@donaldl_xenos_linux_orl (ktext)

Allow sx parameter caches to accept 3 more pointers so it can
potentially process 2 primitives at once.

... #24 change 118988 edit on 2003/09/02 by bhankins@bhankins_crayola_linux_orl (ktext)

- Pull position export buffer out as a separate memory.  Read-side access of pixel
buffer by the
     rb's no longer competes with pa read access of the position buffer.
   - Increase size of pixel buffer memory to 128.
   - Add hooks to control logic to use all 128 locations once the sq logic is ready.
     For now, only first 112 locations are used.
   - Split memory test into two pieces with two test processors.
   - Add hooks to use second memory test processor.  For now, only one is used, and the
sx i/o is
     unchanged from previous checkins.
   - Add new and remove obsolete memories.

... #23 change 118400 edit on 2003/08/27 by donaldl@donaldl_crayola_linux_orl (ktext)

Pipelined vtx_ptr_valid to qualify wrap control signals.
```

```
... #22 change 110328 edit on 2003/07/10 by donaldl@donaldl_crayola_linux_orl (ktext)

Bug fix - delayed read address in real-time parameter caches & added missing clocks
when instantiating sx_rt_param_cache.

... #21 change 108642 edit on 2003/06/30 by donaldl@donaldl_crayola_linux_orl (ktext)

Added rbiu controls for real-time updates to parameter cache mems (real-time mems)

... #20 change 106810 edit on 2003/06/18 by askende@askende_r400_linux_marlboro (ktext)

checking in a fix to force q2_param_array0_tmp signal to load on  WRAP 1 when
       cylindrical wrap is enabled

... #19 change 104227 edit on 2003/06/05 by donaldl@donaldl_crayola_linux_orl (ktext)

Created separate integers for each process using a for loop.

... #18 change 104223 edit on 2003/06/05 by bhankins@bhankins_crayola_linux_orl (ktext)

fix STAR_cmdscout bus.  Partial hack until sx with new hierarchy is checked in

... #17 change 103932 edit on 2003/06/03 by mmantor@mmantor_crayola_linux_orl (ktext)

   update for new pipe disable routing
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_export_control.v
... #43 change 105986 delete on 2003/06/13 by bhankins@bhankins_crayola_linux_orl
(ktext)

delete obsolete files

... #42 change 100113 edit on 2003/05/09 by bhankins@bhankins_crayola_linux_orl (ktext)

1. bug fix with quad_gen_cnt and quad_pair_base_offset.
   2. replace pa_pos_req_buff (skid_buff_top) with ati_fifo to remove unnecessary
warnings.

... #41 change 100015 edit on 2003/05/08 by mmantor@mmantor_crayola_linux_orl (ktext)

<sq_ais_output - re-ordered kill_mask going to the sx so bits flow in order msb->lsg
sp2(v3-v0)sp0(v3-v0)) to match exp_mask
                  - removed improper final update of kill mask with predication mask
                  - enable export_mask for all exports
    SX_PA_interfaces.v - fixed checker for back to back transfers
    SX_RB_interfaces.v - hooked up to 7 bit sx_rb_index and rb_sx_index instead of
incorrect 8 bits
    sx.v - changed interfaces for sx_rb and rb_sx interfaces to become 7 bits instead
of 8 bits
    tb_sx.v - changed sx inputs to be 7 bits instead of 8 bits on the above index
interfaces
    tbmod_fake_sp.v - reordered the kill mask and enabled channel mask for exports
    sx_export_buffers.v - moved register after export mems and only load when memory
read, mimized client read muxes added input rotate muxes for export to memory
operations and indivual write address for each memory and set up predication,
kill_mask, alpha kill,and channel mask in the determination of writing data into the
export buffers
    sx_export_control.v - removed dead clock on rb and pa data fetch interface and
client and made arbiter behave as round robin and removed unecessary second input
register, added support for z render targets and multiple render targets and clean up
items
    ex_export_alloc_dealloc.v - enabled channel mask, kill mask, export_mask, and apha
test conditioning of valid bitsa doubled the free rate>
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/misc/sq_export_alloc.v
... #42 change 130421 edit on 2003/11/06 by bhankins@bhankins_xenos_linux_orl (ktext)

- sq-sx thread id added to sq output and into and through the sx
   - updated sx-rb trackers to use sq-sx thread id
   - removed obsolete code from sx
   - fixed sx bug where an ea from one export to memory was resetting the valid bits
for the other export to memory

... #41 change 128601 edit on 2003/10/27 by mmantor@mmantor_xenos_linux_orl (ktext)

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

... #40 change 125550 edit on 2003/10/08 by rramsey@rramsey_xenos_linux_orl (ktext)

Increase sq_tp_maxcount from 6 to 7
Fix a problem with the simd mux for vtx_alloc_size in export_alloc
Fix a problem with pc_alloc_free_cnt in export_alloc (alloc and dealloc on same clk
was broken)
Make alu ctl_flow and instr trackers work with multiple simd's
Also change these trackers to use common code for pix/vtx by selecting the type with
a parameter

... #39 change 122683 edit on 2003/09/23 by mearl@mearl_crayola_linux_orl (ktext)

One primitieve per clock changes in the back of the SC and front of the SQ. Right now,
the ONE_PRIM_PER_CLOCK define in
       header.v and SC_SQ_interface.v are needed for this change. Will update this to
ONEPPC, since this already exists in
       header.v. Also, the sim.cfg file does not have an ifdef, so is hardcoded to one
prim per clock.

... #38 change 122402 edit on 2003/09/20 by mmang@mmang_crayola_linux_orl (ktext)

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
```

7. In sq_export_alloc.v, handle position/main export id
   and parameter cache thread base for simd2/3. Be able
   to handle one type down simd0/1 and a different type
   down simd2/3 on the same clock.
8. In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
   gpr_alloc blocks return different acks, gpr bases,
   and gpr maxes.
9. In sq_exp_alloc_ctrl.v, handle position/main export
   buffer management. Be able handle one type down
   simd0/1 and a different type down simd2/3 on the same
   clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
    added muxing and memories to handle status bits, cfs
    state, and alu state. Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

... #37 change 119294 edit on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- instatiation of sq export blocker at sq top level
- thread buffer timing fix related to status read/export count update

... #36 change 116380 edit on 2003/08/13 by mmang@mmang_crayola_linux_orl (ktext)

1. Added separate gpr allocation/deallocation
   management for multiple simds (sq_gpr_alloc,
   sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
   sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2. Made thread_arb poll cfs rtr on a 4 clock
   interval in order to ensure the arbiters
   stayed in phase between simds.
3. Created new interface signal between
   thread_arb and export_alloc to lock export_id
   and parameter cache base for each simd. In

```
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.

... #35 change 114305 edit on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro
(ktext)

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

... #34 change 113286 edit on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

... #33 change 110640 edit on 2003/07/12 by mmantor@mmantor_crayola_linux_orl (ktext)

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

... #32 change 107389 edit on 2003/06/22 by mmang@mmang_crayola_linux_orl (ktext)

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
```

```
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

... #31 change 101168 edit on 2003/05/15 by rramsey@rramsey_crayola_linux_orl (ktext)

fix a problem with my param cache allocate fix and fill the hole
in our spsx tracker that let the problem slip through my regressions
(pc write addr was not being checked)

... #30 change 101009 edit on 2003/05/14 by rramsey@rramsey_crayola_linux_orl (ktext)

Changes for parameter cache deallocation. Need to multiply dealloc
count by (vs_export_count +1) so the correct number of lines are
freed.

... #29 change 100877 edit on 2003/05/14 by rramsey@rramsey_crayola_linux_orl (ktext)

Fix 3 issues related to parameter cache allocation/deallocation
  1) Move allocate subtract for pc_free_cnt so it happens when
     an allocating vtx thread wins arbitration instead of when
     the thread is sent to the CFS. This puts the arbitration/
     allocate path at four clks (from six) so we can correctly
     allocate every four clocks.
```

```
  2) Deallocs were being dropped in sq_ptr_buff on back to back
     row transfers if the first of the pair was the last row
     (end of buffer) and the second of the pair had dealloc.
  3) Deallocs need to be accumulated in sq_ptr_buff since multiple
     row transfers of a pixel vector can be marked with dealloc
     and the deallocs are put in the event fifo at end_of_buffer.

Clean up some duplicate code in tb_sqsp and set the default dump
level back to 1 (instead of 3).

... #28 change 99043 edit on 2003/05/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added VC ctl flow seq, instr fetch, instr que and instr seq, and top level IOs
- made some leda fixes
- added non time multiplexed gpr write address output to VC and TP (gpr_dst_addr[6:0])

... #27 change 98462 edit on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_param_cache_ctl.v
... #15 change 123795 edit on 2003/09/29 by donaldl@donaldl_xenos_linux_orl (ktext)

Allow sx parameter caches to accept 3 more pointers so it can
potentially process 2 primitives at once.

... #14 change 104223 edit on 2003/06/05 by bhankins@bhankins_crayola_linux_orl (ktext)

fix STAR_cmdscout bus.  Partial hack until sx with new hierarchy is checked in

... #13 change 103932 edit on 2003/06/03 by mmantor@mmantor_crayola_linux_orl (ktext)

   update for new pipe disable routing

... #12 change 102246 edit on 2003/05/23 by mearl@mearl_crayola_linux_orl (ktext)

Added mask bits to behavioral parameter cache memories
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa.v
... #171 change 125786 edit on 2003/10/09 by mearl@mearl_xenos_linux_orl (ktext)

Fixed the unused port PA_SC_phase[0] when using ONEPPC

... #170 change 120968 edit on 2003/09/12 by bhankins@bhankins_crayola_linux_orl
(ktext)

Updates to simd_id for the sx inteface to use the id sent from the vgt.
   Also, add support for up to four simds.

... #169 change 117706 edit on 2003/08/22 by mmantor@mmantor_crayola_linux_orl (ktext)

<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with
modifications to their test benches and added
    ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with
SIMD1_PRESENT macro in the SC files>

... #168 change 115386 edit on 2003/08/07 by grayc@grayc_crayola2_linux_orl (ktext)

   partial change for pav and test
   update for mh block file change

... #167 change 111422 edit on 2003/07/16 by grayc@grayc_crayola2_linux_orl (ktext)

   delete KS tile ... add PAV and CP_R tile

... #166 change 104215 edit on 2003/06/05 by smoss@smoss_crayola_linux_orl (ktext)

   pa.v back to new broken state

... #165 change 104210 edit on 2003/06/05 by smoss@smoss_crayola_linux_orl (ktext)

   removed sp disable and simd references to get back to stability

... #164 change 104193 edit on 2003/06/05 by bhankins@FL_BHANKINS_P4 (ktext)

fix wiring error in bad pipe

... #163 change 104124 edit on 2003/06/04 by smoss@smoss_crayola_linux_orl (ktext)

   changed back to #161

... #162 change 104116 edit on 2003/06/04 by smoss@smoss_crayola_linux_orl (ktext)

   old version with pa_sc_phase fix

... #161 change 103971 edit on 2003/06/04 by bhankins@fl_bhankins_r400_win (ktext)
```

```
fixes to support bad pipe for 2 simds

... #160 change 103958 edit on 2003/06/04 by bhankins@fl_bhankins_r400_win (ktext)

minor fix

... #159 change 103932 edit on 2003/06/03 by mmantor@mmantor_crayola_linux_orl (ktext)

   update for new pipe disable routing

... #158 change 103828 edit on 2003/06/03 by dclifton@dclifton_r400 (ktext)

Fixed PA_SC_phase so it works with stub file generator.

... #157 change 103647 edit on 2003/06/02 by moev@moev2_r400_linux_marlboro (ktext)

Made changes to the Virage patchbox to mimic the Virage order (as described in the Data
Sheet).

... #156 change 103611 edit on 2003/06/02 by bhankins@fl_bhankins_r400_win (ktext)

fix syntax error

... #155 change 103610 edit on 2003/06/02 by bhankins@fl_bhankins_r400_win (ktext)

changes to accomodate bad pipes for 2 simd engines.

New I/O is commented out for now for compatibility.

... #154 change 103563 edit on 2003/06/02 by dclifton@dclifton_r400 (ktext)

typo in STAR signals

... #153 change 103373 edit on 2003/05/30 by viviana@viviana_crayola2_syn (ktext)

Added another 12x104 memory for xyz for the ONEPPC ifdef to the pa and reconnected
   the patchin/patchout signals.

... #152 change 101771 edit on 2003/05/20 by dclifton@dclifton_r400 (ktext)

Fixed some typos in STAR signal connections.
Added readback for cl_status.

... #151 change 101696 edit on 2003/05/19 by viviana@viviana_crayola2_syn (ktext)

Added an additional 10x96 memory to be used if ONEPPC is defined.
```

```
... #150 change 101367 edit on 2003/05/16 by dclifton@dclifton_r400 (ktext)

Added one-prim-per-clock mode for setup engine.  Define ONEPPC to get compiler to build
for this mode.

... #149 change 99129 edit on 2003/05/05 by viviana@viviana_crayola2_syn (ktext)

Rebuilt the memories using Virage/3300 compiler and 444 Mhz.  Added pa_rf_awt_gate.v
   instantiated at the pa.v level and used for test purposes.
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa_ag.v
... #43 change 102947 edit on 2003/05/28 by viviana@viviana_crayola2_syn (ktext)

Corrected the STAR_rf_testbus[7] wired to 64x128cm2 memory instead of
STAR_rf_testbus[6].
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa_sxifccg.v
... #40 change 120968 edit on 2003/09/12 by bhankins@bhankins_crayola_linux_orl (ktext)

Updates to simd_id for the sx inteface to use the id sent from the vgt.
   Also, add support for up to four simds.

... #39 change 103602 edit on 2003/06/02 by bhankins@fl_bhankins_r400_win (ktext)

changes to accomodate 2 simd bad pipe signals
```

```
Change 131801 on 2003/11/13 by jayw@jayw_r400_linux_marlboro

Fixes for shader pixel kills and alpha-test pixel kills.

Change 130157 on 2003/11/04 by jayw@jayw_r400_linux_marlboro

Increased 2 FIFOs from R400 size to C1 Xenos size.  Fixes SC 1prim/clk.

Change 129632 on 2003/10/31 by jayw@jayw_r400_linux_marlboro

Memory export support in RB & DB.

Change 128238 on 2003/10/23 by jayw@jayw_r400_linux_marlboro

spacing reverted.

Change 128177 on 2003/10/23 by jayw@jayw_r400_linux_marlboro

Fixes for memory exports.

Change 127401 on 2003/10/20 by jayw@jayw_r400_linux_marlboro

Initial memory export support.

Change 127068 on 2003/10/16 by jayw@jayw_r400_linux_marlboro

some memory export fixes and quad interface ifdef'ed out.

Change 120857 on 2003/09/11 by jayw@jayw_r400_linux_marlboro

MRT changes `ifdefed, plus a blender and depth MS change update and RC for 2pipe

Change 119672 on 2003/09/05 by jayw@jayw_r400_linux_marlboro

Weekly release. need to pull into rb_branch other top level stuff next.

Change 119123 on 2003/09/02 by jayw@jayw_r400_linux_marlboro

Latest depth changes.

Change 118107 on 2003/08/25 by jayw@jayw_r400_linux_marlboro

Some surface sync logic added, untested.  Some code clean up in szmask processing in
RBT. Fix for HiZ.

Change 117605 on 2003/08/21 by jayw@jayw_r400_linux_marlboro

Depth fixes and unknown color (MS?) fixes.
```

Change 117514 on 2003/08/21 by omesh@omesh_r400_linux_marlboro_tott

Added the tracker for chip level RB read/write tests.

Change 117464 on 2003/08/21 by jayw@jayw_r400_linux_marlboro

Latest RB & DB code.

Change 117275 on 2003/08/20 by jayw@jayw_r400_linux_marlboro

removing RB/depth files, all unused, been moved to db/depth. fixed system_dp.vcpp to remove db_depth_slope_to_pixel.v

Change 117110 on 2003/08/19 by jayw@jayw_r400_linux_marlboro

Latest RB & DB code. Tested agains RELEASE_116888

Change 116043 on 2003/08/12 by paulv@paulv_r400_release

Update TOTT with rb_branch.

Change 115662 on 2003/08/08 by paulv@paulv_r400_release

Release rb_branch to TOTT.

Change 114597 on 2003/08/01 by paulv@paulv_r400_release

RB update to TOTT.

Change 114265 on 2003/07/31 by paulv@paulv_r400_release

Release of RB/DB code to TOTT.

Change 113873 on 2003/07/29 by paulv@paulv_r400_release

RB and MH updates to TOTT.

Change 113533 on 2003/07/28 by paulv@paulv_r400_release

Releasing small amount of RB fixes.

Change 113385 on 2003/07/26 by gregs@gregs_r400_linux_marlboro

<removed iTEST_EN ports>

Change 113216 on 2003/07/25 by paulv@paulv_r400_linux_marlboro

Fixed a typo.

Change 113215 on 2003/07/25 by paulv@paulv_r400_linux_marlboro

Ugh! More timing fixes.

Change 113146 on 2003/07/25 by wlawless@wlawless_r400_linux_marlboro

paralled up the addresses into the CAM's for timing... I think this will
help because the buffering was a killer

Change 113017 on 2003/07/24 by paulv@paulv_r400_linux_marlboro

Fixed my horrid timing "fixes" from yesterday.

Change 112833 on 2003/07/23 by paulv@paulv_r400_linux_marlboro

Commented out all dummy memory models and the tile block is now using the macro verilog
models. Also, added logic between the tile cache and quad cache to invalidate a quad
cache cacheline when a tile cache cacheline gets flushed out to make room for new data.

Change 112745 on 2003/07/23 by wlawless@wlawless_r400_linux_marlboro

fixed pitch0 to use flopped version when more quads and some timing
in frag op

Change 112660 on 2003/07/23 by paulv@paulv_r400_linux_marlboro

Timing fix.

Change 112610 on 2003/07/23 by paulv@paulv_r400_linux_marlboro

Few minor signal reassignments to be more consistent with rest of tile.

Change 112425 on 2003/07/22 by wlawless@wlawless_r400_linux_marlboro

gated if_dec2 with num_equal instead of stop_pipe... didn't need all those
conditions

Change 112347 on 2003/07/22 by wlawless@wlawless_r400_linux_marlboro

moved linear128 per ping pong for timing

Change 112341 on 2003/07/22 by paulv@paulv_r400_linux_marlboro

Shrunk total delay by 600ps (from 6000ps to 5400ps total).

Change 112331 on 2003/07/22 by paulv@paulv_r400_linux_marlboro

Fixed tile_fifo_probe_read when surface not enabled.

Change 112312 on 2003/07/22 by jayw@jayw_r400_linux_marlboro

Hooking up register read logic. removed dummy memory from rb_rbt_fragment_fifo.v

Change 112182 on 2003/07/21 by wlawless@wlawless_r400_linux_marlboro

broke up the read muxes for cam outputs for timing

Change 112163 on 2003/07/21 by paulv@paulv_r400_linux_marlboro

Fixed clk domains for a few signals.

Change 112130 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

removed dummy memory.

Change 112109 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

switching to using real rams, some LEDA fixes

Change 112097 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

removed duplicate declaration.

Change 112094 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

Fix for mc disable signals, needed to be registered.

Change 111880 on 2003/07/18 by paulv@paulv_r400_linux_marlboro

Various HiZ related fixes, including the updating of smask and zrange when specific
enable bits (e.g., stencil_enable, etc.) are set.

Change 111776 on 2003/07/17 by jayw@jayw_r400_linux_marlboro

Fixing use of non-registered inputs from DB.

Change 111699 on 2003/07/17 by wlawless@wlawless_r400_linux_marlboro

inc_amount went neg need to be sign extended

Change 111682 on 2003/07/17 by jgibney@jgibney_r400_linux_marlboro

Fix for multiple render targets bug. Connected registered version of
blend_rd_color_sel to buffer_sol0 into urb_c_cache_state, to align properly with

pixel_res.

Change 111626 on 2003/07/17 by wlawless@wlawless_r400_linux_marlboro

broke up the big always block

Change 111480 on 2003/07/16 by wlawless@wlawless_r400_linux_marlboro

needed to set max probe so it doesn't wrap...

Change 111403 on 2003/07/16 by paulv@paulv_r400_linux_marlboro

Needed to use the flopped read data when determining the *queue_vector vector.

Change 111366 on 2003/07/16 by wlawless@wlawless_r400_linux_marlboro

Fixed 128x128 blend 2 samp

Change 111211 on 2003/07/15 by paulv@paulv_r400_linux_marlboro

Forgot to wire up RB_DB_mem_sync_start from the RBM to here. Fixed.

Change 110982 on 2003/07/14 by jayw@jayw_r400_linux_marlboro

fix attempt for RB performance. (fill test)

Change 110959 on 2003/07/14 by wlawless@wlawless_r400_linux_marlboro

A timing fix broke the randoms so fixed it, hope the timing is still good..

Change 110957 on 2003/07/14 by hmonsef@hmonsef

Replace 8x113 with 8x117 and 12x111 with 12x117. Requested by Paul V.

Change 110903 on 2003/07/14 by paulv@paulv_r400_linux_marlboro

Removed some commented out code.

Change 110902 on 2003/07/14 by paulv@paulv_r400_linux_marlboro

Increased both the DB_RB_quaddata_mask and the hiz_qc_quaddata_mask to 8 bits. There
are now 2 bits/quad, with the bits denoting when to update zrange and smask.

Change 110601 on 2003/07/11 by jayw@jayw_r400_linux_marlboro

LEDA and some changes/fixes for 7->8 bits SX index.

Change 110519 on 2003/07/11 by paulv@paulv_r400_linux_marlboro

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Moved logic around in the RBM to fix (hopefully) timing.

Change 110414 on 2003/07/11 by jayw@jayw_r400_linux_marlboro

Fix clean signals.

Change 110340 on 2003/07/10 by paulv@paulv_r400_linux_marlboro

Fixed typo.

Change 110338 on 2003/07/10 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 110107 on 2003/07/09 by paulv@paulv_r400_linux_marlboro

Leda fixes.

Change 110052 on 2003/07/09 by paulv@paulv_r400_linux_marlboro

Timing fix.

Change 109998 on 2003/07/09 by wlawless@wlawless_r400_linux_marlboro

Reorganized how to manage probe more then one tile to avoid locking up
the ops.... hard to explain

Change 109744 on 2003/07/08 by paulv@paulv_r400_linux_marlboro

Hardwired the rb_rc_sync_clean* signals to 1 for Orlando (until color and depth
implement their surface sync logic).

Change 109151 on 2003/07/03 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 109091 on 2003/07/03 by paulv@paulv_r400_linux_marlboro

Yet more timing fixes.

Change 108994 on 2003/07/02 by jayw@jayw_r400_linux_marlboro

couple of missing sx index size fixes and move rb_include.

Change 108960 on 2003/07/02 by paulv@paulv_r400_linux_marlboro

Timing fixes for RBM and RBT.  With both subblocks, I removed the cam_lookup modules
```

and just moved the logic into their respective blocks.

Change 108880 on 2003/07/02 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 108869 on 2003/07/02 by jayw@jayw_r400_linux_marlboro

Moving file to common directory from gfx/rb, no other change.

Change 108786 on 2003/07/01 by paulv@paulv_r400_linux_marlboro

Fixed the probe logic so tiles with no surfaces enabled get probed with out a cycle delay between them (necessary due to the 2-cycle address calculation, which is needed to determine cam hits/misses). This problem was causing a non-surface-enabled test to hang.

Change 108751 on 2003/07/01 by paulv@paulv_r400_linux_marlboro

More minor timing fixes.

Change 108750 on 2003/07/01 by wlawless@wlawless_r400_linux_marlboro

fixed a pesky little bug

Change 108593 on 2003/06/30 by jayw@jayw_r400_linux_marlboro

Adding 16 bit pixel mask through DB. NOTE: db_stdrfsdks2p8x136cm1sw0 is now db_stdrfsdks2p8x152cm1sw0

Change 108552 on 2003/06/30 by paulv@paulv_r400_linux_marlboro

Some minor timing fixes.

Change 108521 on 2003/06/30 by wlawless@wlawless_r400_linux_marlboro

Gated mask_q with load_src_addr

Change 108507 on 2003/06/30 by paulv@paulv_r400_linux_marlboro

Fixed LEDA error.

Change 108417 on 2003/06/27 by paulv@paulv_r400_linux_marlboro

Converted rb_rba_alpha_blend_cntl.v to rb_rba_alpha_blend_cntl_alpha and _color versions. This was done to reduce area (instantiating rb_rba_alpha_blend_cntl.v for 8 channels wasted gates) and to fix some minor timing problems.

Change 108392 on 2003/06/27 by paulv@paulv_r400_linux_marlboro

Timing fixes and logic fix (smask decode of GEQUAL and NOTEQUAL was backwards).

Change 108354 on 2003/06/27 by moev@moev2_r400_linux_marlboro

Added module for needed for Virage AWT mode

Change 108304 on 2003/06/27 by moev@moev2_r400_linux_marlboro

Made changes to fix Virage test signals, added awt_gate.

Change 108303 on 2003/06/27 by moev@moev2_r400_linux_marlboro

recreated control file to correct invalid number of fuses in the fusebox.

Change 108263 on 2003/06/27 by paulv@paulv_r400_linux_marlboro

Forgot to assign the fog and const color flopped values to their respective outputs.
Fixed.

Change 108253 on 2003/06/27 by wlawless@wlawless_r400_linux_marlboro

stuff

Change 108196 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

More agp request fixes and fixed the addresses after determining if a request is using
the external queue.

Change 108195 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 108184 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 108169 on 2003/06/26 by wlawless@wlawless_r400_linux_marlboro

fixed a cache cohearicy bug in ms

Change 108077 on 2003/06/26 by wlawless@wlawless_r400_linux_marlboro

Added toggle_q to dec2

Change 108073 on 2003/06/26 by jayw@jayw_r400_linux_marlboro

Preparing for making SX index 8 bits instead of 7 bits.

Change 108065 on 2003/06/26 by wlawless@wlawless_r400_linux_marlboro

Got the first blend multisample to work,,, changed a few things

Change 108059 on 2003/06/26 by jayw@jayw_r400_linux_marlboro

Preparing for Extending SX index from 7 to 8 bits.

Change 108050 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Fixes for external queue logic.

Change 108049 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Fixes for quad cache stall logic.

Change 108020 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

LEDA fix.

Change 107898 on 2003/06/25 by paulv@paulv_r400_linux_marlboro

Timing fixes and fixed a typo in the quad cache.

Change 107879 on 2003/06/25 by paulv@paulv_r400_linux_marlboro

Put the probe_address mux back in (it must have been deleted by accident when I was doing a timing fix).

Change 107788 on 2003/06/25 by jayw@jayw_r400_linux_marlboro

updated to yesterday

Change 107743 on 2003/06/24 by paulv@paulv_r400_linux_marlboro

Fixed some skid values of some fifos (and in turn had to resize some RBM fifos).

Change 107606 on 2003/06/24 by paulv@paulv_r400_linux_marlboro

Fixed some LEDA warnings.

Change 107603 on 2003/06/24 by wlawless@wlawless_r400_linux_marlboro

move dest_inflight_q to be free flowing flop... wasn't getting updated

Change 107545 on 2003/06/23 by paulv@paulv_r400_linux_marlboro

Timing fixes and LEDA fixes. Also removed a file (moved rb_rba_alpha_blend_preswap logic into rb_rba_blend_bypass).

Change 107488 on 2003/06/23 by wlawless@wlawless_r400_linux_marlboro

sig missing from sensitivity list

Change 107439 on 2003/06/23 by paulv@paulv_r400_linux_marlboro

Connected MC_RB_read_source (need for external queue data read returns and, in the future, TC hw-resolve data) and RB_MH_queuecount (which tells the MH that the RB has received external queue data). NOTE: at this time, RB_MH_queuecount means the RB has received any external queue data, even though clients who made read requests to the external queue already allocate space for the data (therefore, they have no queues). There may be a MH fix forthcoming to negate the use of this signal except for TC hw resolve data to RBC.

Change 107430 on 2003/06/23 by wlawless@wlawless_r400_linux_marlboro

The toggle into ATI-FIFO_CAM was changed for pipelining the data
in... Anyway the toggle inside for testing pixels 01 or 23 need
to be changed also.... oooppps

Change 107424 on 2003/06/23 by jayw@jayw_r400_linux_marlboro

pre move

Change 107173 on 2003/06/20 by wlawless@wlawless_r400_linux_marlboro

Some timing fixes, and added rb_id frops

Change 107014 on 2003/06/19 by hmonsef@hmonsef

Replaced by 12x111

Change 106784 on 2003/06/18 by paulv@paulv_r400_linux_marlboro

Reverted most of the timing fixes from yesterday since Mark S. told me that the problem most likely was a tool problem with optimize_registers.

Change 106744 on 2003/06/18 by wlawless@wlawless_r400_linux_marlboro

removed some levels of delay in the ping pong for rtr_local...

Change 106688 on 2003/06/18 by wlawless@wlawless_r400_linux_marlboro

Flopped the output of the Color Cache RAM's to ati_fifo_cam...

This is through the endian logic

Change 106627 on 2003/06/17 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 106308 on 2003/06/16 by wlawless@wlawless_r400_linux_marlboro

Added rb_regs.v to rb_c_cache.v for Mark S... include.v didn't work ???

Change 106298 on 2003/06/16 by paulv@paulv_r400_linux_marlboro

Just a minor code optimization.

Change 106287 on 2003/06/16 by paulv@paulv_r400_linux_marlboro

Removed the GL_ redefines in rb_include.v (since the emulator has been released with the new names).

Change 106283 on 2003/06/16 by wlawless@wlawless_r400_linux_marlboro

Nothing... removed [0] from a single wire... oops

Change 106126 on 2003/06/13 by paulv@paulv_r400_linux_marlboro

Fix for the generation of external queue (MH) addresses.

Change 106018 on 2003/06/13 by paulv@paulv_r400_linux_marlboro

Fixes for AGP requests.

Change 106016 on 2003/06/13 by wlawless@wlawless_r400_linux_marlboro

timing

Change 106015 on 2003/06/13 by paulv@paulv_r400_linux_marlboro

Renamed all false rts signals to snd signals (e.g., DB_RB_quaddata_rts -> DB_RB_quaddata_snd) in order to maintain consistency and avoid confusion. Also fixed a problem writing the db quaddata fifo in the quad cache.

Change 105890 on 2003/06/12 by paulv@paulv_r400_linux_marlboro

Timing fixes and some functional fixes in the quad_cache (specifically, both the HiZ data and DB quaddata fifos are memory macro fifos and one must be careful about when data is actually available at the top).

Change 105831 on 2003/06/12 by wlawless@wlawless_r400_linux_marlboro

moved expand state from going into the state decode... timing

Change 105780 on 2003/06/12 by wlawless@wlawless_r400_linux_marlboro

used doing_frag_zero for the mux control in probe_mask

Change 105652 on 2003/06/11 by wlawless@wlawless_r400_linux_marlboro

floped inputs to frag probe state machine

Change 105642 on 2003/06/11 by hmonsef@hmonsef

Previous Rev the code was instatiated twice by Virage.

Change 105629 on 2003/06/11 by jayw@jayw_r400_linux_marlboro

removed extra name declaration.

Change 105587 on 2003/06/11 by wlawless@wlawless_r400_linux_marlboro

timing

Change 105519 on 2003/06/11 by paulv@paulv_r400_linux_marlboro

Forgot to add the new signal MC_RB_rank_ba3_location to port list (its declared, though). Fixed.

Change 105399 on 2003/06/10 by wlawless@wlawless_r400_linux_marlboro

fixed linear 32_32_32_32 test... made load_new_pipe

Change 105352 on 2003/06/10 by wlawless@wlawless_r400_linux_marlboro

slight change in read cam valids for timing

Change 105049 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Forgot to declare q_mc_rb_rank_ba3_location.

Change 105043 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Fixed a few typos.

Change 105016 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Removed some unused tst_ signals from the top-level db and added TM1 and TM2 signals to both RB and DB top-level.

Change 105004 on 2003/06/09 by wlawless@wlawless_r400_linux_marlboro

mistake in the 'define size for the linear mul stuff added

Change 105003 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Fixed the TST_bist_reuse_seed signal name (reuse was being spelled as resue).

Change 104976 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Fixed some top-level I/O size mismatches, renamed the MC_RB_queuecount signals and added MC_RB_rank_ba3_location.

Change 104757 on 2003/06/06 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 104667 on 2003/06/06 by paulv@paulv_r400_linux_marlboro

Fixed an oversized memory (to remove Synopsys Lint warnings) and did another LEDA cleanup.

Change 104618 on 2003/06/06 by wlawless@wlawless_r400_linux_marlboro

made mux_ctl the state flops for timing...

Change 104597 on 2003/06/06 by wlawless@wlawless_r400_linux_marlboro

Removed ports on scan and bist... per Mark S.

Change 104585 on 2003/06/06 by hmonsef@hmonsef

16x228 was replaced by 16x225

Change 104580 on 2003/06/06 by wlawless@wlawless_r400_linux_marlboro

changed how the linear offset was done because of timing

Change 104578 on 2003/06/06 by hmonsef@hmonsef

Replaces 16x225

Change 104577 on 2003/06/06 by hmonsef@hmonsef

Replaces 16x228

Change 104358 on 2003/06/05 by paulv@paulv_r400_linux_marlboro

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Timing fixes.

Change 104357 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro

timing

Change 104277 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro

timing

Change 104262 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro

timing

Change 104197 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro

changed the clear if_notzero_q to somthing much easier

Change 104077 on 2003/06/04 by wlawless@wlawless_r400_linux_marlboro

timing in read_dest_miss

Change 104053 on 2003/06/04 by paulv@paulv_r400_linux_marlboro

Temporarirly created new defines in rb_include.v for all GL_*
blendcontrol cases until they are added to
cmn_lib/include/rb_reg.v (all the GL_* defines needed to be
renamed due to a conflict with FireGL).

Change 104035 on 2003/06/04 by wlawless@wlawless_r400_linux_marlboro

changed the inflight count logic, should get some better timing

Change 104012 on 2003/06/04 by paulv@paulv_r400_linux_marlboro

Another fix to the skid of the color write request fifo.

Change 104011 on 2003/06/04 by wlawless@wlawless_r400_linux_marlboro

added reg on data out to rbm

Change 103987 on 2003/06/04 by paulv@paulv_r400_linux_marlboro

Resized color read request fifo and fixed both the color r/w skids.

Change 103872 on 2003/06/03 by wlawless@wlawless_r400_linux_marlboro
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timing

Change 103835 on 2003/06/03 by paulv@paulv_r400_linux_marlboro

Replaced all parameters for memory macro fifos with defines.

Change 103784 on 2003/06/03 by paulv@paulv_r400_linux_marlboro

Fixed skid and depth of RBC color read and write fifos due to timing fix in color.

Change 103763 on 2003/06/03 by wlawless@wlawless_r400_linux_marlboro

timing

Change 103736 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Real fix for determining the state_wr_addr and removed an
unused clock in rb_rbt_hiz_quad_checker.v.

Change 103717 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Timing fixes, lint fixes and finished resizing the 8x111
memory in the quad cache to 12x111.

Change 103704 on 2003/06/02 by hmonsef@hmonsef

8x111 replaced by 12x111

Change 103702 on 2003/06/02 by hmonsef@hmonsef

Replaces 8x111

Change 103701 on 2003/06/02 by hmonsef@hmonsef

Replaces 8x111

Change 103687 on 2003/06/02 by wlawless@wlawless_r400_linux_marlboro

move state look up for timing

Change 103659 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Resized the 11x111 ram inside the quad cache as 12x111 (depth has to be an even
number), fixed the register decode in rb_tile_fifo for the cmask_enable.  Also removed
some unnecessary I/O at the top of RB and connected some DB_RB_mem signals.

Change 103646 on 2003/06/02 by wlawless@wlawless_r400_linux_marlboro
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tied some scan and bist this because they where not connected and
causes lint errors, as per Mark S. request

Change 103625 on 2003/06/02 by wlawless@wlawless_r400_linux_marlboro

timing, added 1 more to ati_fifo_cam skid

Change 103607 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

I accidentally removed a signal that shouldn't have been removed (a test I ran still
passed, though). Strange. Anyway, all is better.

Change 103579 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Some lint (synthesis and simulation) fixes, resized the HiZ data fifo in the quad cache
from 8 to 11 deep and fixed a bug with the reading of the DB data fifo in the quad
cache.

Change 103364 on 2003/05/30 by johnchen@johnchen_r400_linux_marlboro

slope_to_pixel normalize 24bits float fix

Change 103336 on 2003/05/30 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 102943 on 2003/05/28 by wlawless@wlawless_r400_linux_marlboro

timing

Change 102860 on 2003/05/28 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 102732 on 2003/05/27 by wlawless@wlawless_r400_linux_marlboro

Timing fix, removed cam_read_hit from the allocate_case

Change 102723 on 2003/05/27 by ygiang@ygiang_r400_linux_marlboro

added:ppvella's block perf counters

Change 102423 on 2003/05/23 by paulv@paulv_r400_linux_marlboro

Removed the db_data_fifo counter and just used the full signal
from the fifo logic.

Change 102389 on 2003/05/23 by paulv@paulv_r400_linux_marlboro

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Requalified z_surface_enable signal to only include smask and
zrange enable (since it is only used by the quad_cache and the
HiZ blocks, which don't deal with zmask).

Change 102370 on 2003/05/23 by wlawless@wlawless_r400_linux_marlboro

Added the ATI fifo's to sx index interface... and some timing fixes

Change 102341 on 2003/05/23 by paulv@paulv_r400_linux_marlboro

Many fixes, including increasing the fifo depth of DB->RBM writes, STAR memory fixes
and some logic issues.

Change 102301 on 2003/05/23 by hmonsef@hmonsef

2 RAMs moved from RB To DB due to DB break up from RB

Change 102300 on 2003/05/23 by hmonsef@hmonsef

Due to DB break up

Change 102298 on 2003/05/23 by hmonsef@hmonsef

New RAM due to DB break up

Change 102297 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102296 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102295 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102294 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102188 on 2003/05/22 by paulv@paulv_r400_linux_marlboro

Fixes for the DB-RB interfaces (only to/from RBT and RBM).

Change 102187 on 2003/05/22 by paulv@paulv_r400_linux_marlboro
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Fixes for the DB-RB interfaces (only to/from RBT and RBM).

Change 102093 on 2003/05/22 by wlawless@wlawless_r400_linux_marlboro

added this pingpong fifo to color cam for timing

Change 102092 on 2003/05/22 by wlawless@wlawless_r400_linux_marlboro

Added a pingpong fifo in the probe path for timing

Change 101978 on 2003/05/21 by wlawless@wlawless_r400_linux_marlboro

TIMING FIXES

Change 101929 on 2003/05/21 by paulv@paulv_r400_linux_marlboro

Timing experiment/fix.

Change 101756 on 2003/05/20 by paulv@paulv_r400_linux_marlboro

Added more performance counter signals.

Change 101733 on 2003/05/20 by hmonsef@hmonsef

LOG2_NUM_PIPES was defined as a register and a wire. Needs to be a register.

Change 101211 on 2003/05/15 by paulv@paulv_r400_linux_marlboro

Memory export fix.

Change 101200 on 2003/05/15 by wlawless@wlawless_r400_linux_marlboro

timing fixes

Change 101195 on 2003/05/15 by paulv@paulv_r400_linux_marlboro

Added some performance counter signals.

Change 101139 on 2003/05/15 by paulv@paulv_r400_linux_marlboro

Memory Export fixes (not done yet, though...).

Change 100983 on 2003/05/14 by wlawless@wlawless_r400_linux_marlboro

Yet another small fix for 2 sample, now all basic pass......

Change 100952 on 2003/05/14 by jayw@jayw_r400_linux_marlboro
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Fixes for 2-sample

Change 100791 on 2003/05/13 by jayw@jayw_r400_linux_marlboro

Flip128L now does full swap.  for memory exports.

Change 100754 on 2003/05/13 by wlawless@wlawless_r400_linux_marlboro

LEDA fixes only

Change 100705 on 2003/05/13 by jayw@jayw_r400_linux_marlboro

updated for DB split

Change 100694 on 2003/05/13 by wlawless@wlawless_r400_linux_marlboro

Added all the 2 sample stuff..........

Change 100677 on 2003/05/13 by paulv@paulv_r400_linux_marlboro

HiZ/HiS fixes and a fix for back-to-back quad cache
uninitialized tiles.

Change 100518 on 2003/05/12 by paulv@paulv_r400_linux_marlboro

Added signal to denote that the HiZ quad checker will not
update the quad cache (for example, when only z enabled and z
write enabled is false).

Change 100508 on 2003/05/12 by wlawless@wlawless_r400_linux_marlboro

got 2 test passing....

Change 100417 on 2003/05/12 by paulv@paulv_r400_linux_marlboro

Some name changes and HiZ/HiS fixes.

Change 100416 on 2003/05/12 by paulv@paulv_r400_linux_marlboro

LEDA fixes.

Change 100221 on 2003/05/09 by wlawless@wlawless_r400_linux_marlboro

Added some counter so that op would not get ahead of probes inc and dec on tiles

Change 100093 on 2003/05/08 by jayw@jayw_r400_linux_marlboro

removed unused depth files and one color file.  removed from system_db.vcpp too.
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Change 99967 on 2003/05/08 by jayw@jayw_r400_linux_marlboro

Added clock enable pin from rb to db.

Change 99893 on 2003/05/08 by wlawless@wlawless_r400_linux_marlboro

Block probes back to the same tile if there is more then 2 tiles... things were getting plugged up,

Change 99808 on 2003/05/07 by paulv@paulv_r400_linux_marlboro

Fixed toplevel *rfsms_stp instantiations.

Change 99733 on 2003/05/07 by hmonsef@hmonsef

Dpeth removed from Rb

Change 99729 on 2003/05/07 by hmonsef@hmonsef

New version is checked in from a different directory

Change 99722 on 2003/05/07 by hmonsef@hmonsef

removed<enter description here>

Change 99721 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99719 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99718 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99717 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99716 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99714 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99713 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99712 on 2003/05/07 by hmonsef@hmonsef

Removed

Change 99711 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99710 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99709 on 2003/05/07 by hmonsef@hmonsef

Change 99707 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99706 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99701 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99697 on 2003/05/07 by hmonsef@hmonsef

comp new rev

Change 99695 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99694 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99693 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

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Change 99692 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99691 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99690 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99689 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99688 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99687 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99686 on 2003/05/07 by hmonsef@hmonsef

comp new rev

Change 99684 on 2003/05/07 by hmonsef@hmonsef

new com rev

Change 99682 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99681 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99680 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99679 on 2003/05/07 by hmonsef@hmonsef

new comp rev
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Change 99678 on 2003/05/07 by hmonsef@hmonsef

New comp rev

Change 99677 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99676 on 2003/05/07 by hmonsef@hmonsef

New comp rev

Change 99675 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99674 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99673 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99672 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99670 on 2003/05/07 by hmonsef@hmonsef

New comp rev

Change 99668 on 2003/05/07 by hmonsef@hmonsef

New compiler Rev

Change 99667 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99666 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99659 on 2003/05/07 by hmonsef@hmonsef

DB removed from RB

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Change 99657 on 2003/05/07 by hmonsef@hmonsef

DB removed form RB

Change 99656 on 2003/05/07 by hmonsef@hmonsef

DB removed from RB

Change 99655 on 2003/05/07 by hmonsef@hmonsef

DB is removed from RB

Change 99654 on 2003/05/07 by hmonsef@hmonsef

 DB is removed from RB

Change 99650 on 2003/05/07 by hmonsef@hmonsef

Checking in the file form virage directory

Change 99649 on 2003/05/07 by hmonsef@hmonsef

Checking in the file from virage directory

Change 99620 on 2003/05/07 by hmonsef@hmonsef

Remove Depth from RB

Change 99618 on 2003/05/07 by hmonsef@hmonsef

Remove Depth from RB

Change 99615 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB

Change 99614 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB

Change 99612 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB

Change 99611 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB
```

```
Change 99599 on 2003/05/07 by paulv@paulv_r400_linux_marlboro

DB split changes, LEDA fixes, other fixes, yadda, yadda, yadda.

Change 99545 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

Signal renaming.  Paul Mitchell's fix.

Change 99531 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

New DB block Part I.  Still renaming a couple of signals.

Change 99517 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

Old unused file.  renamed 96_128

Change 99516 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

Old unused file.

Change 99515 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

New files, but some signals need to be updated.

Change 99403 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99402 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99400 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99399 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99398 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99397 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.
```

Change 99396 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

put 'u' before instance names.

Change 99378 on 2003/05/06 by ygiang@ygiang_r400_linux_marlboro

added: perf signals

Change 99377 on 2003/05/06 by ygiang@ygiang_r400_linux_marlboro

added: rb perfcounters for depth flushes/fills and color reads/writes

Change 99347 on 2003/05/06 by paulv@paulv_r400_linux_marlboro

Added RBM performance signals.

Change 99311 on 2003/05/06 by paulv@paulv_r400_linux_marlboro

Timing fix. Address calc modules are now 3 cycles long.

Change 99198 on 2003/05/05 by paulv@paulv_r400_linux_marlboro

LEDA fix.

Change 99175 on 2003/05/05 by wlawless@wlawless_r400_linux_marlboro

Blocked ld_p2 from comming on if a freeze_on_ms_allocate, 2 cache line loaded with the same
address.....

Change 99169 on 2003/05/05 by paulv@paulv_r400_linux_marlboro

HiZ/HiS fixes.

Change 99145 on 2003/05/05 by johnchen@johnchen_r400_linux_marlboro

fix for a quaddata synchronization problem when surface is enabled and z and s are enabled

Change 99116 on 2003/05/05 by wlawless@wlawless_r400_linux_marlboro

Change to the fragment cache flush, needed to jump back if nothing to flush

Change 98995 on 2003/05/04 by johnchen@johnchen_r400_linux_marlboro

perf counter stuff

Change 98910 on 2003/05/02 by johnchen@johnchen_r400_linux_marlboro

fix for quaddata update

Change 98867 on 2003/05/02 by johnchen@johnchen_r400_linux_marlboro

fix for subnormal 24 float numbers

Change 98775 on 2003/05/02 by paulv@paulv_r400_linux_marlboro

Fixed decode of hier_stencil_enable.

Change 98768 on 2003/05/02 by paulv@paulv_r400_linux_marlboro

Code optimization.

Change 98671 on 2003/05/01 by paulv@paulv_r400_linux_marlboro

Fixed valids.

Change 98654 on 2003/05/01 by johnchen@johnchen_r400_linux_marlboro

update inflight correctly

Change 98572 on 2003/05/01 by jayw@jayw_r400_linux_marlboro

Timing fix for Hamid.

Change 98495 on 2003/05/01 by wlawless@wlawless_r400_linux_marlboro

Slight change to how the ms_lock probes are calculated...

Change 98470 on 2003/05/01 by johnchen@johnchen_r400_linux_marlboro

some bug fixes

Change 98392 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

Module compiler area reductions and some minor fixes.

Change 98387 on 2003/04/30 by jayw@jayw_r400_linux_marlboro

moved rb_rbd_quad_address_calc from depth into color for DB split.renamed bus for sx index reads

Change 98356 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Chnaged the way number_of_total_access_q was calculated. It replaces 4 cascading adders

Change 98340 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

For data going to tile block, since multisample read data has the same tag, the send back to tile is not active when multisample data is being returned from the MC.

Change 98326 on 2003/04/30 by jayw@jayw_r400_linux_marlboro

fixed makefile

Change 98304 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

LEDA fix.

Change 98297 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

Fixed probe flush logic.

Change 98287 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Replaced 128x96 RAM with 96x128

Change 98260 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Replaced 128x96 (incoorect naming) with 96x128

Change 98256 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Replaces the 128x96 RAM with 96x128 used in rb_rbd_cache_ram.v

Change 98254 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

The RAM in access_fifo was changed from 8x131 to 8x136. Spare RAM bits are provided for future use

Change 98145 on 2003/04/29 by johnchen@johnchen_r400_linux_marlboro

fix for backfacing

Change 98066 on 2003/04/29 by paulv@paulv_r400_linux_marlboro

LEDA fixes, timing fixes and logic fixes (oh my).

Change 98018 on 2003/04/28 by jayw@jayw_r400_linux_marlboro

LEDA fixes and removed 96x96

Change 97989 on 2003/04/28 by johnchen@johnchen_r400_linux_marlboro

```
add reg_state signal

Change 97942 on 2003/04/28 by johnchen@johnchen_r400_linux_marlboro

fix memory return validation problem

Change 97717 on 2003/04/25 by johnchen@johnchen_r400_linux_marlboro_rbrc

no fixes...just make it look better

Change 97685 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

Going back to version 38.

Change 97681 on 2003/04/25 by wlawless@wlawless_r400_linux_marlboro

read pending in frag cache, and 2k crossing..

Change 97664 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

Comments.  Removed unnecessary sx fifo count.

Change 97620 on 2003/04/25 by johnchen@johnchen_r400_linux_marlboro_rbrc

wait for the cacheline to be filled up even when detail_mask is zero

Change 97601 on 2003/04/25 by johnchen@johnchen_r400_linux_marlboro_rbrc

stencil fixes for random

Change 97580 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

LEDA fixes.

Change 97575 on 2003/04/25 by wlawless@wlawless_r400_linux_marlboro

a more "BETTER" way to check for 2k boundary crossing to skip over AB or CD
banks.... nice english!!!

Change 97562 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

More LEDA fixes.

Change 97512 on 2003/04/24 by paulv@paulv_r400_linux_marlboro

The valid, last_quarter_tile and associated cacheline signals
going into the calc_new_tile module were off by a cycle.  Fixed.
```

Change 97458 on 2003/04/24 by johnchen@johnchen_r400_linux_marlboro_rbrc

stall event flush to color block until depth block finishes flushing

Change 97401 on 2003/04/24 by johnchen@johnchen_r400_linux_marlboro_rbrc

LEDA fixes

Change 97395 on 2003/04/24 by wlawless@wlawless_r400_linux_marlboro

Set valid on both 1/2's of the cache line when in multisample...

Change 97368 on 2003/04/24 by jayw@jayw_r400_linux_marlboro

LEDA fixes

Change 97281 on 2003/04/23 by johnchen@johnchen_r400_linux_marlboro_rbrc

stall the tile side if the probe side is not quite ready

Change 97244 on 2003/04/23 by wlawless@wlawless_r400_linux_marlboro

Fixed 1713 with a block quad in fifo if it a event

Change 97218 on 2003/04/23 by jayw@jayw_r400_linux_marlboro

fix include missing, and removed ab

Change 97201 on 2003/04/23 by paulv@paulv_r400_linux_marlboro

Fixed interpretation of x to mean the quad (little endian), not the pixel (big endian).

Change 97170 on 2003/04/23 by johnchen@johnchen_r400_linux_marlboro_rbrc

some random fixes, timing fixes

Change 97144 on 2003/04/23 by wlawless@wlawless_r400_linux_marlboro

small fix for 3 and 6 sample in the cover/overlap logic

Change 97139 on 2003/04/23 by jayw@jayw_r400_linux_marlboro

updates

Change 97113 on 2003/04/23 by jayw@jayw_r400_linux_marlboro

AB removal and LEDA fixes, fix for 3 and 6 sample MSAA.

Change 97078 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97075 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128

Change 97074 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97071 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in Depth

Change 97070 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97069 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97068 on 2003/04/23 by hmonsef@hmonsef

Replaces 128x96 in depth

Change 97067 on 2003/04/23 by hmonsef@hmonsef

Replaces 128x96 in depth

Change 97062 on 2003/04/23 by hmonsef@hmonsef

Replaced 3 RAMs for the tile.

Change 97010 on 2003/04/22 by paulv@paulv_r400_linux_marlboro

Fixed x_sel and y_sel signals.

Change 97008 on 2003/04/22 by paulv@paulv_r400_linux_marlboro

The AB (alpha blender) has been moved back into the RB as a subblock (RBA).

Change 96959 on 2003/04/22 by johnchen@johnchen_r400_linux_marlboro_rbrc

handful od random fixes

```
Change 96949 on 2003/04/22 by jayw@jayw_r400_linux_marlboro

LEDA fixes.

Change 96939 on 2003/04/22 by wlawless@wlawless_r400_linux_marlboro

fixed some LEDA things, and got basic_multisample 128x128_4samp working
This was an addressing bug in reading the fragment bit back from the MC

Change 96901 on 2003/04/22 by jayw@jayw_r400_linux_marlboro

LEDA fixes for RC to run clean.

Change 96778 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x230

Change 96776 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x225

Change 96774 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x225

Change 96773 on 2003/04/21 by hmonsef@hmonsef

Repalced 16x225

Change 96772 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x241

Change 96771 on 2003/04/21 by hmonsef@hmonsef

Replaced 32x230

Change 96766 on 2003/04/21 by hmonsef@hmonsef

Changed 3 tiles RAM width

Change 96764 on 2003/04/21 by hmonsef@hmonsef

Changed 3 tiles RAM width

Change 96763 on 2003/04/21 by hmonsef@hmonsef
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Chaged 3 Tile RAMs width

Change 96761 on 2003/04/21 by hmonsef@hmonsef

Change 3 Tile RAMs width

Change 96758 on 2003/04/21 by hmonsef@hmonsef

Changed Tile 3 RAMs width

Change 96534 on 2003/04/18 by johnchen@johnchen_r400_linux_marlboro_rbrc

make sure hiz kills don't get to color

Change 96532 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Fixed the read signal for the detail_fifo.

Change 96526 on 2003/04/18 by johnchen@johnchen_r400_linux_marlboro_rbrc

hiz kill signal added

Change 96523 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Few bug fixes with the tile_killed signaling.

Change 96503 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Now passing a tile_killed signal on the RBT_RBD_* interface.

Change 96497 on 2003/04/18 by hmonsef@hmonsef

Replaced 4 instance of 96x96 with 3 instance of 128x96

Change 96495 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96494 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96492 on 2003/04/18 by hmonsef@hmonsef

Replaces 96x96 RAM

Change 96491 on 2003/04/18 by hmonsef@hmonsef
```

```
Replaces 96x96 RAM

Change 96490 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96488 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96487 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96484 on 2003/04/18 by wlawless@wlawless_r400_linux_marlboro

Multisample stuff, got 128x128 to pass....

Change 96448 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Added a signal between RBT and RBD to denote killed tiles.

Change 96394 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Renamed the HiZ tilechecker tile killed signal (from hiz_flightcount_tiledone to
hiz_tilecheck_tile_killed) and added hiz_quadcheck_tile_killed (from HiZ quad checker).
```

```
Change 130419 on 2003/11/06 by dclifton@dclifton_xenos_linux_orl

Update to account for module compiler library changes.

Change 130204 on 2003/11/04 by danh@danh_xenos_linux_orl

Removed the ati_delay_chain and SPI_delay_in and SPI_delay_out ports.

Change 129692 on 2003/10/31 by danh@danh_xenos_linux_orl

This changes spi_interp_ctl back to its original state (Changelist 129259)

Change 129689 on 2003/10/31 by danh@danh_xenos_linux_orl

This version is only for IKOS release 2.1 (r500_ikos_rel2.1_spi)

Change 129259 on 2003/10/29 by danh@danh_xenos_linux_orl

- spi_interp_ctl IJ buffer changed from one 16x200 memory to two 16x100 memories.
       - added additional SQ_SP_interp_qd[0:1]_prim_sela signals to improve spi input
timing.

Change 128365 on 2003/10/24 by mearl@mearl_xenos_linux_orl

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed
synthesis
       bugs in SC.

Change 127269 on 2003/10/19 by rramsey@rramsey_xenos_linux_orl

Change behave mem_model in spi so its read dly matches the real mem
Send interp_valid and ij_line 1clk early to account for 2clk read dly
Fix spi_sp tracker so it works with early valid
Change thread_buf and cfs machines so only fetches can modify the
fetch pending bit. The alu machines only read the value out of the buffer.
Get rid of a bunch of extra 'else' clauses

Change 126618 on 2003/10/14 by dclifton@dclifton_xenos_linux_orl

Fixed an lsb precision issue with neg mult result shifted 25 places.

Change 126490 on 2003/10/14 by danh@danh_xenos_linux_orl

registered SQ_SP_interp_qd[0:1]_prim_sel fanout to improve synthesis timing results.

Change 125951 on 2003/10/09 by danh@danh_xenos_linux_orl

dos2unix conversion for proper Synopsys Module Compiler format.
```

Change 125673 on 2003/10/08 by dclifton@dclifton_xenos_linux_orl

Fixed bug with factor-of-two negative results out of adder

Change 125427 on 2003/10/07 by danh@danh_xenos_linux_orl

Timing and XY LSB interpolation changes.

Change 124852 on 2003/10/03 by dclifton@dclifton_xenos_linux_orl

Optimizations for timing that changes precision.

Change 123983 on 2003/09/30 by dclifton@dclifton_xenos_linux_orl

Changed output flops to 'dff_out' variety

Change 123952 on 2003/09/30 by mmantor@mmantor_xenos_linux_orl

<added changes for 2 prim interpolation to the spi and sq and all top level interconnects, and sq_sx_sp_simd_id for redundancy control, and all changes to test bench as well as some ncverilog error messages. Some other misc top level clean up>

Change 122820 on 2003/09/23 by danh@danh_xenos_linux_orl

Added 97 most significant zeros to all auto_count concatenations.

Change 122710 on 2003/09/23 by danh@danh_xenos_linux_orl

Registered all ROM_* inputs (Redundant SP control).

Change 121629 on 2003/09/16 by danh@danh_crayola1_linux_orl

Removed XY pipe delay, XY data is now processed by the interpolators

Change 119746 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed interp_buff_swap

Change 119745 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed sq_spi_interp_mode, sq_spi_buff_swap

Change 119742 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed SQ_SP_interp_mode, SQ_SP_interp_buff_swap, added all Redundant SP ports and logic.

```
Change 117446 on 2003/08/21 by dclifton@dclifton_r400

Changes for synthesis--removed unused pins from sp_comp_opcodes and sp_macc32_multiply.
Tweaked input delays on spi_hi_prec_int.

Change 117046 on 2003/08/19 by viviana@viviana_crayola2_syn

Memory configuration file.

Change 116807 on 2003/08/15 by dclifton@dclifton_r400

Improvement for timing

Change 116586 on 2003/08/14 by dclifton@dclifton_r400

Added sin/cos to scalar engine
Changed spi_hi_prec_int to improve timing--it now clamps at max float instead of
rolling back to zero.

Change 111347 on 2003/07/16 by viviana@viviana_crayola2_syn

SPI memories with registers inside and new version of the compiler.

Change 110640 on 2003/07/12 by mmantor@mmantor_crayola_linux_orl

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

Change 110525 on 2003/07/11 by viviana@viviana_crayola2_syn

Removed the STAR_cmdscout connection from the memories instantiated in spi_vsr_ctl.v.

Change 109058 on 2003/07/03 by dclifton@dclifton_r400

Got rid of warning about bit size mismatch.
```

```
Change 108942 on 2003/07/02 by dclifton@dclifton_r400

double buffered resets

Change 108140 on 2003/06/26 by rramsey@rramsey_crayola_linux_orl

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

Change 107174 on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro

- swapped PS and ID gpr write phases

Change 106804 on 2003/06/18 by moev@moev2_r400_linux_marlboro

fixed syntax errors in some of the entries

Change 106710 on 2003/06/18 by moev@moev2_r400_linux_marlboro

Updated files that reflect the SP/SPI split.

Change 106109 on 2003/06/13 by moev@moev2_r400_linux_marlboro

fixes to eliminate temp area left in by accident.

Change 106030 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_rf_fusebox.ctmc for SPI.

Change 106029 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_rf_fusebox.v for SPI.

Change 106028 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro
```

spi_stdrfsdks2p8x96cm1sw0.v for SPI.

Change 106027 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_stdrfsdks2p16x200cm1sw0.v file for SPI

Change 106026 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_rf.cnt file for SPI.

Change 105853 on 2003/06/12 by moev@moev2_r400_linux_marlboro

Files for testing the Virage system

Change 105788 on 2003/06/12 by moev@moev2_r400_linux_marlboro

Made changes to support the Virage memory systems. These include the rewiring of the patchbox, changes to the width of the SCFORCE bus, addition of the AWT gate the change of port STAR_cmdscout from input to output.

Change 105693 on 2003/06/11 by askende@askende_r400_linux_marlboro

releasing a change in the interpolators to compensate for the bug introduced by SX (hardware and emulator)
	when dealing with NaNs and Infs

Change 105692 on 2003/06/11 by askende@askende_r400_linux_marlboro

releasing a change in the interpolators to compensate for the bug introduced by SX (hardware and emulator)
	when dealing with NaNs and Infs

Change 105375 on 2003/06/10 by asutkows@asutkows_r400_sun_marlboro

spi.cnt file for the SPI block.

Change 104458 on 2003/06/05 by askende@askende_r400_linux_marlboro

added indelay in the sp_hi_prec_int.mc module

Change 101842 on 2003/05/20 by askende@askende_r400_linux_marlboro

releasing the top level change related to adding one set of flops at the interface
	between SPI and SP.

Change 101841 on 2003/05/20 by askende@askende_r400_linux_marlboro

checking in the interpolator control latency changes in SQ and SP.

Change 100242 on 2003/05/09 by danh@danh_crayola_linux_orl

Changed p<3:0>_blue_norm and p<3:0>_screen_y_final MSB generation per C code.

Change 99991 on 2003/05/08 by danh@danh_crayola_linux_orl

Made minor Param*blue, Param*alpha sensitivity list changes.

Change 99784 on 2003/05/07 by danh@danh_crayola_linux_orl

Changed all Param*blue and Param*alpha generation so it matches the C code.

Change 97205 on 2003/04/23 by askende@askende_r400_linux_marlboro

1. fix to allow src (argument a) to be written back to the GPRs when doing a MOVA
2. modified the 4 LSBs of the autocount bus to use the SPI block id as supposed to SP block id + vector unit id

```
Change 132894 on 2003/11/19 by rramsey@rramsey_xenos_linux_orl

Fix SQ_VC dec signals in tb_sqsp.
Change tbtrk_sqvc so it does not compare fetch addr for mini fetches.
Fix problem in tex_instr_seq that was allowing mini fetches to start
out of phase.
Add more info to msgs from pcdata tracker to tell which set of pc data
is mismatching. Also turn off sx1 compare since it is redundant now that
all the sx data comes from usx_0.

Change 132557 on 2003/11/18 by bhankins@bhankins_xenos_linux_orl

Back up to revision #22 to allow non-export-to-memory tests to pass for now.

Change 132236 on 2003/11/17 by bhankins@bhankins_xenos_linux_orl

Increase size of bank_avail_quads_to_free to 8 bits to accomodate a value of 128.

Change 130671 on 2003/11/07 by bhankins@bhankins_xenos_linux_orl

- remove obsolete code in tracker
   - remove obsolete file open/reads in tbmod_fake_rb

Change 130421 on 2003/11/06 by bhankins@bhankins_xenos_linux_orl

- sq-sx thread id added to sq output and into and through the sx
   - updated sx-rb trackers to use sq-sx thread id
   - removed obsolete code from sx
   - fixed sx bug where an ea from one export to memory was resetting the valid bits
for the other export to memory

Change 130407 on 2003/11/06 by donaldl@donaldl_xenos_linux_orl

Adjusted delays again with new 90nm libraries to meet latencies.

Change 129610 on 2003/10/31 by amys@amys_xenos_linux_orl

remove dependency on index_rtr signals for comparison

Change 129541 on 2003/10/31 by bhankins@bhankins_xenos_linux_orl

clean up signal names for consistency.

Change 129135 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl

support adding 2 bits to indicate how quad pixel mask bits are rotated
   for use by the trackers
```

```
Change 129122 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl

fix quad buffer address pointer to support larger depth

Change 129121 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl

   - increase quad fifo depth to 656 (behavioral only for now).
- fix bug in export to memory logic.

Change 129120 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl

add support for testing memory export data by including a value for the tracker that
   indicates how many bits the pixel quad mask has been shifted.

Change 128816 on 2003/10/27 by llefebvr@llefebvr_r400_linux_marlboro

Adding VC performance counters in the SQ.
Removed the SX->RB warnings on non-initialized GPR channels.

Change 128657 on 2003/10/27 by donaldl@donaldl_xenos_linux_orl

Added muxes to output of real-time parameter cache mems to select the
correct parameter based on bits [8:7] of the ptr selects.

Change 128601 on 2003/10/27 by mmantor@mmantor_xenos_linux_orl

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

Change 128365 on 2003/10/24 by mearl@mearl_xenos_linux_orl

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed
synthesis
       bugs in SC.

Change 128319 on 2003/10/24 by bhankins@bhankins_xenos_linux_orl

update the creation of the valid pixel table for export to memory

Change 128070 on 2003/10/23 by bhankins@bhankins_xenos_linux_orl

fix lint warning.  no functional change to logic.

Change 128046 on 2003/10/23 by bhankins@bhankins_xenos_linux_orl

added missing include statement
```

```
Change 127857 on 2003/10/22 by bhankins@bhankins_xenos_linux_orl

fix bug to correct how position aux buffers are freed

Change 127742 on 2003/10/22 by llefebvr@llefebvr_r400_linux_marlboro

Removed the warnings from the sp->sx trackers and sx->sp.
Now emulator is always executing the scalar instruction even in the case of a 3 operand
vector opcode. This is to match with random shaders.

Change 127604 on 2003/10/21 by bhankins@bhankins_xenos_linux_orl

- remove debug code
   - put valid quad identifier bit on lsb of quad pixel mask for memory exports

Change 127348 on 2003/10/20 by bhankins@bhankins_xenos_linux_orl

add register for timing

Change 126890 on 2003/10/16 by bhankins@bhankins_xenos_linux_orl

Add missing signals to sensitivity lists

Change 126859 on 2003/10/15 by donaldl@donaldl_xenos_linux_orl

Fixed error - need to delay SX_SQ_vtx_data3 an extra clock.

Change 126350 on 2003/10/13 by bhankins@bhankins_xenos_linux_orl

Changes made to improve timing.  No functional change.

Change 125821 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

include unused outputs to eliminate compile-time warnings

Change 125820 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

fix unconnected inputs

Change 125818 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

remove unused input

Change 125780 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

update sx test inputs to match the established convention
```

```
Change 125660 on 2003/10/08 by rramsey@rramsey_xenos_linux_orl

Fix compile warnings for sq (several missing ports)
Fix compile warning in sx_parameter_caches
Fix SQ_SP_fetch_simd_sel so it lines up with the data coming out of the GPRs

Change 125637 on 2003/10/08 by bhankins@bhankins_xenos_linux_orl

edits made for timing only.  no functional change.

Change 125382 on 2003/10/07 by jayw@jayw_r400_linux_marlboro3

MULTIPLE_QUAD_COMMANDS enabled.  new MRT protocol SX->RB&DB.

Change 124742 on 2003/10/03 by bhankins@bhankins_xenos_linux_orl

fix test pin name

Change 124736 on 2003/10/03 by bhankins@bhankins_xenos_linux_orl

1. Add support for second memory test processor
   2. Add updated behavioral code for mc block in sx

Change 124553 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Commented out old delays.

Change 124540 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Updated clock, input, & output delays for 90nm technology.

Change 124224 on 2003/10/01 by bhankins@bhankins_xenos_linux_orl

Changes made to try to improve on timing.  No functional change

Change 124193 on 2003/10/01 by bhankins@bhankins_xenos_linux_orl

Undid change made for timing - was not functionally equivalent.

Change 123984 on 2003/09/30 by bhankins@bhankins_xenos_linux_orl

change names of sx i/o ROM_MCn_disable signals

Change 123937 on 2003/09/30 by bhankins@bhankins_xenos_linux_orl

Add the thread id debug bits to the detailed quad fifo when we're
   simulating with real memory.  This only affects simulation; the debug
   bits are not included unless 'SIM' is defined.
```

```
Change 123795 on 2003/09/29 by donaldl@donaldl_xenos_linux_orl

Allow sx parameter caches to accept 3 more pointers so it can
potentially process 2 primitives at once.

Change 123515 on 2003/09/26 by bhankins@bhankins_xenos_linux_orl

- add sx_redundancy.v to hierarchy to try and improve on timing
   - add EXP_BUF_112_DEEP switch.  comment out in sx_defines.v to enable
     all 128 locations of the color export buffer to be used
   - add ONE_STAR_PROCESSOR switch.  comment out in sx_defines.v to use
     two star processors.
   - add support for thread id and thread type for debug.
   - misc changes for timing which don't change the logic.

Change 121784 on 2003/09/17 by bhankins@bhankins_xenos_linux_orl

point to sx files in /proj/xenos

Change 121332 on 2003/09/15 by rramsey@rramsey_crayola_linux_orl

Change pix_ctl so deallocs with real pixel vectors don't free param
cache space until interpolation is almost complete
Wire up the vc_sp valid signals correctly
Fix sx_sp_pcdata tracker

Change 121326 on 2003/09/15 by bhankins@bhankins_crayola_linux_orl

Add a pipeline in the generation of the alignment bits for
   memory exports to improve on timing.

Change 121325 on 2003/09/15 by bhankins@bhankins_crayola_linux_orl

Recode redundancy select to try and improve on timing.

Change 121285 on 2003/09/15 by bhankins@bhankins_crayola_linux_orl

Add thread id and type

Change 121157 on 2003/09/13 by smoss@smoss_crayola_linux_orl_regress

   xenos updates

Change 120895 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

remove some debug logic
```

```
Change 120894 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

Fix typo

Change 120887 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

-  Add sx_mem_export.v module to capture pixel addresses and
       calculate rb id values for use in export to memory.
   -  Add support for redundancy logic.  Inputs are currently
       tied low in tb_sqsp.v and chip_sx.tree.
   -  Add non-synthesizable logic to route thread id and thread
       type from sq through sx and out to rb for test.  Allows
       tracker to identify export to memories, and to distinguish
       between them.  Tied low in chip_sx.tree and tb_sqsp.v
       All associated I/O and logic is qualified on `ifdef SIM.
   -  Remove the register in sx_export_control_common.v that was
       requiring some signals on the sq alloc interface to be present
       one clock before the valid.  Now, all sq_sx_exp_ signals are
       expected to be valid only when sq_sx_exp_valid == 1.
   -  Add a register in the generation of the final pixel address
       value for export to memory, to try and improve on timing.

Change 120722 on 2003/09/11 by bhankins@bhankins_crayola_linux_orl

Put known junk values on SQ_SX_exp_ interface signals when SQ_SX_exp_valid==0

Change 118988 on 2003/09/02 by bhankins@bhankins_crayola_linux_orl

- Pull position export buffer out as a separate memory.  Read-side access of pixel
buffer by the
     rb's no longer competes with pa read access of the position buffer.
   - Increase size of pixel buffer memory to 128.
   - Add hooks to control logic to use all 128 locations once the sq logic is ready.
     For now, only first 112 locations are used.
   - Split memory test into two pieces with two test processors.
   - Add hooks to use second memory test processor.  For now, only one is used, and the
sx i/o is
     unchanged from previous checkins.
   - Add new and remove obsolete memories.

Change 118645 on 2003/08/28 by smoss@smoss_crayola_linux_orl_regress

   increased size of valid to 4 bits

Change 118622 on 2003/08/28 by llefebvr@llefebvr_r400_emu_montreal

Modified the Orlando trackers to only compare valid channels. This replaces the
0xDEADDEAD values we had previously. Note that any uninitialized channel will generate
```

a tracker warning still.
 Modified interfaces are:

1) SX->SP parameter cache data
2) SP->SX
3) SX->RB

I left alone the SX->PA interface as we did not have problems over it. The qualifiers are there however if anyone wants to do it.

Change 118400 on 2003/08/27 by donaldl@donaldl_crayola_linux_orl

Pipelined vtx_ptr_valid to qualify wrap control signals.

Change 118200 on 2003/08/26 by rramsey@rramsey_crayola_linux_orl

Increase number of clks the tp_sq inject routine can loop through input data
Fix a problem with the sx_rb color tracker when the sx sends 0 mask quads, or the rb kills quads

Change 118163 on 2003/08/26 by bhankins@bhankins_crayola_linux_orl

   1. Initial checkin of code added to support export-to-memory. This code is only partially tested, and not at all optimized yet.
   2. Start to add (dum_mems only) for separate position export memory to split position and color into two separate memories.
      pos is 16dx128wx16, pix has the full 128dx128wx16, but logic still wraps at 112 for sq compatibility for now.
   3. Split up read-side arbitration to give pa full access to pos buffer, while the rb's compete only among themselves for the color buffer.

Change 117311 on 2003/08/20 by rramsey@rramsey_crayola_linux_orl

Changes to sc for 4 qd/clk picker in KILL_ALL_PIXELS mode
Check in sc memory updates for Vivian
Add some missing connections in sqsp to fix compile warnings
Go to a global define for all trackers to control x vs 0 mismatch/warning (MISMATCH_X_VS_0)

Change 115863 on 2003/08/11 by rramsey@rramsey_crayola_linux_orl

fix write index into pos export buffer when processing aux vectors

Change 115728 on 2003/08/10 by rramsey@rramsey_crayola_linux_orl

Change SQ to hold off popping the RBBM skid fifo while map copies are in progress. This fixes the problem where gfx_copy writes were being missed if they were less than 8 clks apart.

```
Get rid of extra write into RBBM skid fifo for reads, and instead zero out
we and re out of fifo if it's empty. The fifo was overflowing if the filling
entry was a read, since one additional entry was getting pushed.
sx_sp_pcdata tracker now ignores 4f5eaddf (unwritten pc locations)
Fix a problem in the sqsp testbench that was causing rbbm writes to be dropped
if the sq exerted back pressure.

Change 115114 on 2003/08/06 by rramsey@rramsey_crayola_linux_orl

add some missing dummy dump files

Change 115047 on 2003/08/05 by rramsey@rramsey_crayola_linux_orl

Add register to hold pipe disable bits to tb_sqsp
Hook sx instance up to correct set of RBBM signals in tb_sqsp
Increase depth of sc state avail fifo since some events need
to go through that path
       Change sx pa tracker to always opens its files so it doesn't
       cause hangs when the files are empty
       Add deaddead and a selectable x_vs_0 mismatch disable (reports
       a warning rather than a mismatch) to tbtrk_sx_rb.v

Change 115032 on 2003/08/05 by grayc@grayc_crayola2_linux_orl

   added back Laurent changes for sx performance counters
   modified sx.v for new performance register names

Change 113723 on 2003/07/29 by bhankins@bhankins_crayola_linux_orl

modify to use rb_sx.dmp file to generate indices and index_op bit

Change 112600 on 2003/07/23 by rramsey@rramsey_crayola_linux_orl

Change sx-rb trackers so they always open their files at time 0,
that way they don't cause hangs for tests that don't hit any quads
Hook up the real pixel mask in the sx_rb color tracker

Change 112313 on 2003/07/22 by amys@amys_crayola2_linux_orl

fixed bug so tracker can compile

Change 112129 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

double skid depth of input quad fifo to accomodate decreasing it to 1-quad wide

Change 112093 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

fix to keep a proper tally of position vectors exported when auxillary vectors are
```

```
included

Change 112084 on 2003/07/21 by rramsey@rramsey_crayola_linux_orl

mask fifo was not quite deep enough

Change 112064 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

add missing port

Change 112062 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

add commented line, to be uncommented to enable mrt support

Change 112034 on 2003/07/19 by rramsey@rramsey_crayola_linux_orl

Change vcs build script so cover is off by default
Get rid of some compile warnings in tb_sqsp
Change sx_rb color tracker so it doesn't use the sx_rb_quad dump
to get pixel masks

Change 111928 on 2003/07/18 by bhankins@bhankins_crayola_linux_orl

misc fixes.  also add support for multiple render targets.  Not fully tested, and
currently disabled by default.

Change 111806 on 2003/07/18 by mmantor@mmantor_crayola_linux_orl

<extended rb_sx_index to 8 bits for Orlando trackers with bigger export buffers>

Change 111628 on 2003/07/17 by smoss@smoss_crayola_linux_orl_regress

   changed tbmod_fake_pa for ncsim because all requests weren't occurring this was also
true for vcs but sim was passing.  changed buildt for nc to not run a sim after a
compile

Change 111372 on 2003/07/16 by rramsey@rramsey_crayola_linux_orl

add filename to mismatch message

Change 111091 on 2003/07/15 by bhankins@bhankins_crayola_linux_orl

fix sensitivity list

Change 110818 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

remove obsolete memory
```

```
Change 110817 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

add new memory files

Change 110811 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

remove obsolete memory

Change 110809 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

update memories

Change 110793 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

disable run fast sq for now

Change 110748 on 2003/07/13 by mmantor@mmantor_crayola_linux_orl

<I forgot to add this file>

Change 110640 on 2003/07/12 by mmantor@mmantor_crayola_linux_orl

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

Change 110328 on 2003/07/10 by donaldl@donaldl_crayola_linux_orl

Bug fix - delayed read address in real-time parameter caches & added missing clocks
when instantiating sx_rt_param_cache.

Change 110019 on 2003/07/09 by donaldl@fl_donaldl_p4

Testbench (vsim) for sx_param_sub block.

Change 108683 on 2003/07/01 by bhankins@bhankins_crayola_linux_orl
```

```
edit for timing.  no functional difference

Change 108642 on 2003/06/30 by donaldl@donaldl_crayola_linux_orl

Added rbiu controls for real-time updates to parameter cache mems (real-time mems)

Change 108227 on 2003/06/27 by bhankins@bhankins_crayola_linux_orl

add some debug signals

Change 108175 on 2003/06/26 by mmang@mmang_crayola_linux_orl

Re-put in sx SQ_SX_free_id fix that was lost in merge.

Change 108045 on 2003/06/26 by donaldl@donaldl_crayola_linux_orl

No functional change -- regenerated to remove compare warnings during synthesis

Change 108012 on 2003/06/26 by bhankins@bhankins_crayola_linux_orl

fix some signals used for debug

Change 108011 on 2003/06/26 by bhankins@bhankins_crayola_linux_orl

minor fix

Change 108009 on 2003/06/26 by bhankins@bhankins_crayola_linux_orl

fix logic errors in alpha test

Change 107977 on 2003/06/25 by viviana@viviana_crayola2_syn

Recompiled the sx memories to remove second instantiation of the sx_rf_awt_gate module.

Change 107841 on 2003/06/25 by bhankins@bhankins_crayola_linux_orl

remove enable from memory output register

Change 107781 on 2003/06/25 by bhankins@bhankins_crayola_linux_orl

add register to output of alpha sample mask memory

Change 107442 on 2003/06/23 by bhankins@bhankins_crayola_linux_orl

fix memory test wiring error

Change 107438 on 2003/06/23 by bhankins@bhankins_crayola_linux_orl
```

```
improve on counting param cache exports

Change 107389 on 2003/06/22 by mmang@mmang_crayola_linux_orl

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

Change 107193 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

fix scforce warning

Change 107182 on 2003/06/20 by viviana@viviana_crayola2_syn

Memories for the sx built 6/20/03.

Change 107181 on 2003/06/20 by viviana@viviana_crayola2_syn

The memories that were not bit maskable had the rtl bit maskable.
```

```
   All memories were built from scratch to correct this.

Change 107176 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

remove obsolete files

Change 107175 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

delete memory models from this directory (they don't belong here)

Change 107167 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

updates

Change 107157 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

skip the checking of quads that have no mask bits set

Change 107156 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

fix generation of index_op bit

Change 107151 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

remove dos carriage returns

Change 107053 on 2003/06/19 by bhankins@bhankins_crayola_linux_orl

wiring error on memory test logic

Change 107026 on 2003/06/19 by llefebvr@llefebvr_r400_linux_marlboro

1) Added a guard bit to the parameter sub engine of the SX in both the emulator and HW
this was causing a failure on a WQL test.
2) Fixed zero detection problem in parameter_sub engine of the HW were an explicit 1
was added all the time even when the number was 0.0. This was causing
r400sx_wrapper_01.cpp to fail (this is a test that I wrote to duplicate the WQL test
that was failing in order to run it on HW).

Change 107017 on 2003/06/19 by bhankins@bhankins_crayola_linux_orl

delete obsolete memory file

Change 106825 on 2003/06/18 by llefebvr@llefebvr_r400_linux_marlboro

Changing the cylindrical wrap test from > to >= in order to match MS ref rast and R300
algorithm.
```

```
Change 106810 on 2003/06/18 by askende@askende_r400_linux_marlboro

checking in a fix to force q2_param_array0_tmp signal to load on  WRAP 1 when
       cylindrical wrap is enabled

Change 106721 on 2003/06/18 by llefebvr@llefebvr_r400_emu_montreal

Changed the names of he channels in the tracker so that they are placed correctly
(order was ARGB correct order is ABGR)

Change 106713 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

undo prev change

Change 106697 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

correct fifo width

Change 106695 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

modify tbmod_fake_rb.v to generate op bit only if mask is nonzero

Change 106681 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

fix bug in quad mask generation

Change 106566 on 2003/06/17 by bhankins@bhankins_crayola_linux_orl

bug fix when free done happens outside of an export

Change 106193 on 2003/06/14 by bhankins@bhankins_crayola_linux_orl

enable alpha logic

Change 106044 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

bug fix to allow free done to be generated after the 4 phases of data

Change 105995 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

disable alpha test for now

Change 105986 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

delete obsolete files

Change 105985 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl
```

```
delete obsolete files

Change 105982 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

advance sq-sx control signals by one clock to solve sx timing issues
   add support for updated sx hierarchy

Change 105851 on 2003/06/12 by bhankins@bhankins_crayola_linux_orl

add new files for updated sx hierarchy

Change 104227 on 2003/06/05 by donaldl@donaldl_crayola_linux_orl

Created separate integers for each process using a for loop.

Change 104223 on 2003/06/05 by bhankins@bhankins_crayola_linux_orl

fix STAR_cmdscout bus.  Partial hack until sx with new hierarchy is checked in

Change 103988 on 2003/06/04 by donaldl@donaldl_crayola_linux_orl

Initial

Change 103932 on 2003/06/03 by mmantor@mmantor_crayola_linux_orl

   update for new pipe disable routing

Change 103017 on 2003/05/29 by viviana@viviana_crayola2_syn

Added 16 instances of 80x128 and 16 of 64x8.

Change 103013 on 2003/05/29 by viviana@viviana_crayola2_syn

Changed 80x8 memory to 64x8, changed 80x128 memory to be bit writable.

Change 102246 on 2003/05/23 by mearl@mearl_crayola_linux_orl

Added mask bits to behavioral parameter cache memories

Change 102242 on 2003/05/23 by grayc@grayc_crayola2_linux_orl

   change memory name from sc to sx

Change 101742 on 2003/05/20 by viviana@viviana_crayola2_syn

Added the new module for the virage memories new revision.

Change 101741 on 2003/05/20 by viviana@viviana_crayola2_syn
```

```
Added sx_rf_awt_gate module and connected it.

Change 100855 on 2003/05/13 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 100393 on 2003/05/12 by bhankins@bhankins_crayola_win_orl

finish making change of mem_we to mem_wen

Change 100382 on 2003/05/12 by bhankins@bhankins_crayola_win_orl

rename mem_we to mem_wen

Change 100381 on 2003/05/12 by bhankins@bhankins_crayola_win_orl

fix input data rotate mux

Change 100310 on 2003/05/10 by smoss@smoss_crayola_linux_orl_regress

   ncsim for sqsp and sx

Change 100199 on 2003/05/09 by bhankins@bhankins_crayola_win_orl

try to get rid of wierd carriage returns

Change 100113 on 2003/05/09 by bhankins@bhankins_crayola_linux_orl

1. bug fix with quad_gen_cnt and quad_pair_base_offset.
   2. replace pa_pos_req_buff (skid_buff_top) with ati_fifo to remove unnecessary
warnings.

Change 100111 on 2003/05/09 by bhankins@bhankins_crayola_linux_orl

misc updates

Change 100016 on 2003/05/08 by mmantor@mmantor_crayola_linux_orl

<changed index to 7 bits to get compilation>

Change 100015 on 2003/05/08 by mmantor@mmantor_crayola_linux_orl

<sq_ais_output - re-ordered kill_mask going to the sx so bits flow in order msb->lsg
sp2(v3-v0)sp0(v3-v0)) to match exp_mask
                  - removed improper final update of kill mask with predication mask
                  - enable export_mask for all exports
    SX_PA_interfaces.v - fixed checker for back to back transfers
```

```
    SX_RB_interfaces.v - hooked up to 7 bit sx_rb_index and rb_sx_index instead of
incorrect 8 bits
    sx.v - changed interfaces for sx_rb and rb_sx interfaces to become 7 bits instead
of 8 bits
    tb_sx.v - changed sx inputs to be 7 bits instead of 8 bits on the above index
interfaces
    tbmod_fake_sp.v - reordered the kill mask and enabled channel mask for exports
    sx_export_buffers.v - moved register after export mems and only load when memory
read, mimized client read muxes added input rotate muxes for export to memory
operations and indivual write address for each memory and set up predication,
kill_mask, alpha kill,and channel mask in the determination of writing data into the
export buffers
    sx_export_control.v - removed dead clock on rb and pa data fetch interface and
client and made arbiter behave as round robin and removed unecessary second input
register, added support for z render targets and multiple render targets and clean up
items
    ex_export_alloc_dealloc.v - enabled channel mask, kill mask, export_mask, and apha
test conditioning of valid bitsa doubled the free rate>

Change 99662 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

updates to approach running at full speed

Change 99602 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

speed up resets to pixel scoreboard

Change 99567 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

fix to properly stall on quad rtr == 0 from sx

Change 99499 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

update to support running fast via RUN_MAX_SPEED parameter

Change 99374 on 2003/05/06 by bhankins@bhankins_crayola_linux_orl

Include support to send indices to sx one per clock.  Enabled via parameter.

Change 99370 on 2003/05/06 by bhankins@bhankins_crayola_linux_orl

add check for data send signals going unknown

Change 99089 on 2003/05/05 by bhankins@bhankins_crayola_linux_orl

update

Change 99088 on 2003/05/05 by bhankins@bhankins_crayola_linux_orl
```

```
updates

Change 98997 on 2003/05/04 by smoss@smoss_crayola_linux_orl_regress

   dos2unix

Change 98396 on 2003/04/30 by grayc@grayc_crayola2_linux_orl

   new testbench

Change 98395 on 2003/04/30 by grayc@grayc_crayola2_linux_orl

   new testbench

Change 98091 on 2003/04/29 by bhankins@bhankins_crayola_linux_orl

add mechanism to throttle tbmod_fake_int from initiating reads to parameter cache lines
that have
   not yet been written to.

Change 98041 on 2003/04/29 by bhankins@bhankins_crayola_linux_orl

init file done signal

Change 98034 on 2003/04/29 by bhankins@bhankins_crayola_linux_orl

remove reset of 'done' signal.  the signal should be initialized only
   by the InitVec call.

Change 97861 on 2003/04/28 by bhankins@bhankins_crayola_win_orl

update after junk submit

Change 97860 on 2003/04/28 by bhankins@bhankins_crayola_win_orl

junk submit to get perforce gui in sync after samba put back on line.

Change 97645 on 2003/04/25 by bhankins@bhankins_crayola_linux_orl

misc fixes

Change 97150 on 2003/04/23 by bhankins@bhankins_crayola_linux_orl

Update SX trackers to do a better job of helping to check for incomplete tests.
   File streams are now opened only if they are needed in a particular test.  Each
   file stream that is opened must be fully consumed.  Each tracker also outputs a
   "tracker_done" signal indicating that all opened streams have been consumed.
```

```
Change 97060 on 2003/04/23 by bhankins@bhankins_crayola_linux_orl

fix to more properly handle the counting of position and pixel buffer free signals
       from the SX.

Change 96694 on 2003/04/21 by moev@moev_r400_linux_marlboro

updated files to allow serial test to work.

Change 96639 on 2003/04/21 by viviana@viviana_crayola2_syn

Corrected the clock to the Virage memory.

Change 96633 on 2003/04/21 by bhankins@bhankins_crayola_linux_orl

remove unused include

Change 96388 on 2003/04/18 by grayc@grayc_crayola2_linux_orl

   add new include path

Change 96381 on 2003/04/18 by bhankins@bhankins_crayola_linux_orl

resubmitting changes

Change 96380 on 2003/04/18 by bhankins@bhankins_crayola_linux_orl

changes
```

```
Change 132916 on 2003/11/19 by viviana@viviana_xenos_linux_orl

Memory model submitted for simulation.

Change 132904 on 2003/11/19 by vbhatia@vbhatia_r400_linux_marlboro

       Created a superset of the tp and vc testbenches, to deal with coverage tool
limitation,
       Also created a script to run various tests in parallel rather than in series.

Change 132781 on 2003/11/19 by dclifton@dclifton_xenos_linux_orl

Duplicated clock gaters in sp.v for test.
Force_m12_zero forces in3_gte_in12 high in sp_macc32 (makes 'x' * 0 consistently 0)
Fixed sensitivity list for pv_SrcCNegate and pv_SrcCAbs in sp_macc.
Created scalar stall for three operand vector ops in sp_macc to preserve previous
scalar.

Change 132246 on 2003/11/17 by dclifton@dclifton_xenos_linux_orl

Swapped X and Y terms on cube compare to match rasterizer.  Fixed inf input on scalar
add.  Fixed a_eq_neg_b for denorm adds.

Change 131764 on 2003/11/13 by dclifton@dclifton_xenos_linux_orl

Fixed inf feedback on dot product.

Change 131670 on 2003/11/12 by dclifton@dclifton_xenos_linux_orl

Fixed sign on recip_ff(-0) with clamp.
Fixed ma output on cube with x = -y.
Fixed nan interference with mul_prev2 on max with clamp.

Change 130983 on 2003/11/10 by dclifton@dclifton_xenos_linux_orl

Disabled Nan detect for comp opcodes.

Change 130419 on 2003/11/06 by dclifton@dclifton_xenos_linux_orl

Update to account for module compiler library changes.

Change 130347 on 2003/11/05 by dclifton@dclifton_xenos_linux_orl

Two fixes for SIN/COS--quadrant selection fixed and inf/nan detection fixed.

Change 130216 on 2003/11/04 by mmantor@FL_mmantorLT_r400_win

<changes to enable standalone vector pipe random testbench>
```

```
Change 130126 on 2003/11/04 by dclifton@dclifton_xenos_linux_orl

Fixed problem with clamp-to-one getting enabled falsely on MUL by 0

Change 130068 on 2003/11/04 by dclifton@dclifton_xenos_linux_orl

Fixed quandrant assign of SIN/COS, fixed clamp of SQRT with -0 input,
fixed clamp of SIN/COS input for small values

Change 129527 on 2003/10/30 by vbhatia@vbhatia_r400_linux_marlboro

Aniso updates for addresser tb and fmt based cycle count update for formatter tb

Change 129423 on 2003/10/30 by dclifton@dclifton_xenos_linux_orl

Fixed 0*Nan problem with DST Y result value

Change 129408 on 2003/10/30 by rramsey@rramsey_xenos_linux_orl

Move some continuous assignments into always blocks to help sim time
Rework cfs_rtr/arb_xfc path to help timing
Fix a problem with detecting serialize for the cf state machine

Change 129128 on 2003/10/29 by dclifton@dclifton_xenos_linux_orl

Fixed PRED_SET result.

Change 128708 on 2003/10/27 by tien@tien_r400_devel_marlboro

Fix to vtx RF expand for 3 tfetch formats that use it (need channel format_comps)
Removed 3,6,8 sample multisamp tables from deriv
Hooked up encoded format_comp* in tpc where needed

Change 128705 on 2003/10/27 by vbhatia@vbhatia_r400_linux_marlboro

       added support for format 61 testing, clamps for invalid cases on vertex path
       and other updates to get increased coverage.

Change 128610 on 2003/10/27 by dclifton@dclifton_xenos_linux_orl

Fixed recip/rsq/sqrt of -0, fixed clamp on multiplies

Change 128374 on 2003/10/24 by vbhatia@vbhatia_r400_linux_marlboro

updates

Change 128218 on 2003/10/23 by vbhatia@vbhatia_r400_linux_marlboro
```

```
Added format based restriction on xyzw_parity to be only values upto cycle multiplier

Change 128092 on 2003/10/23 by vbhatia@vbhatia_r400_linux_marlboro

Fixed silly error

Change 127997 on 2003/10/22 by vbhatia@vbhatia_r400_linux_marlboro

More random tests and increased testlength to 1M.
       Should see increased coverage.

Change 127734 on 2003/10/22 by dclifton@dclifton_xenos_linux_orl

Fixed recognition of Nans on in3

Change 127582 on 2003/10/21 by vbhatia@vbhatia_r400_release

       Fix for timing reasons, in the vertex fetch data path.
       Removed the VC_SP_data_format 57 to 38 substitution which was delaying data
format
       being fed to other parts of the logic, and accordingly added it to the requisite

       data format muxes.

Change 127496 on 2003/10/21 by dclifton@dclifton_xenos_linux_orl

Fixed clamp-to-one logic.

Change 127355 on 2003/10/20 by dclifton@dclifton_xenos_linux_orl

Fixed clamp-to-one logic

Change 127041 on 2003/10/16 by vbhatia@vbhatia_r400_release

Optimized cmask generation logic to follow tp_fmt_encode,
       hopefully will clean up timing on the formatter.

Change 126691 on 2003/10/15 by dclifton@dclifton_xenos_linux_orl

Another timing related change.  Changed twos comp to ones comp on log
post-process (effects log of number less than 1.0).  Aligned inputs
to high precision pipeline to reduce muxing.  Improved carrysave add
of multiplier results.  Regenerated math tables to reclaim precision
and fix roll-over mismatches.

Change 126689 on 2003/10/15 by dclifton@dclifton_xenos_linux_orl
```

Fixed cube opcode problem with neg/pos X face_id

Change 126451 on 2003/10/13 by donaldl@donaldl_xenos_linux_orl

Qualified q_tp_data_valid with q_tp_simd[1:0].

Change 126189 on 2003/10/10 by vbhatia@vbhatia_r400_linux_marlboro

	Updated

Change 126168 on 2003/10/10 by dclifton@dclifton_r400

Duplicated internal q_rom_pipe_sel, grouped muxes into new module compiler block to encourage proper fanout in synthesis.

Change 125835 on 2003/10/09 by jhoule@jhoule_r400_linux_marlboro

Fixed FMT_1* formats

EMU:
Were rf-expanded as 4x8 instead of 1x32

RTL:
Were considered as 4 channels in the formatter; changed to be like FMT_32.
Fixed sp_tp_cmask_gen.mc as well as tpc_cmask.v (equivalent glue logic for tp4_tc testbench)
Note: All RTL modifications were done by Tien.

Change 125343 on 2003/10/07 by tien@tien_r400_devel_marlboro

Added FMT_DXT3A_AS_1_1_1_1 and in the process of using the name of
the format as it is in the spec, I think I killed my fingers... Geez.

Change 125258 on 2003/10/07 by dclifton@dclifton_xenos_linux_orl

Added a 'u' to instance names of const muxes

Change 125257 on 2003/10/07 by dclifton@dclifton_xenos_linux_orl

Fixed latency in pa. Added mc mux for fanout control on const muxes
for alu constant data in sp.

Change 125040 on 2003/10/06 by vbhatia@vbhatia_r400_linux_marlboro

Updates for interface changes and format optimizations

Change 124796 on 2003/10/03 by viviana@viviana_xenos_linux_orl

```
Added rsp_rf_stp.v and rsp_rf_awt_gate.v to the system_sp.vcpp.  Also added the memory
   configuration files for the rsp memories (4 128x128).

Change 124754 on 2003/10/03 by dclifton@dclifton_xenos_linux_orl

A few fixes for the mul_prev2 opcode.

Change 124738 on 2003/10/03 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 124330 on 2003/10/01 by dclifton@dclifton_xenos_linux_orl

Updated timing parameters for 0.09um technology.

Change 123979 on 2003/09/30 by dclifton@dclifton_r400

changed instance names for vivian

Change 123975 on 2003/09/30 by dclifton@dclifton_xenos_linux_orl

Added 'COMMON_OUTPUT_REGISTER' to move output register past scalar fog muxes

Change 123973 on 2003/09/30 by dclifton@dclifton_xenos_linux_orl

Moved output register past scalar fog mux

Change 123639 on 2003/09/26 by donaldl@donaldl_xenos_linux_orl

Added redundancy shader pipe and fixed some of the connections
to it.

Change 123378 on 2003/09/25 by vbhatia@vbhatia_r400_release

Added format optimizations (matching tp_fmt_encode) for timing reasons

Change 123223 on 2003/09/25 by dclifton@dclifton_r400

Added PIPE_SEL mux for additional TP_RSP_packed_data, TP_RSP_data_valid, and
SPI_SP_data inputs

Change 122991 on 2003/09/24 by dclifton@dclifton_xenos_linux_orl

Moved output register in sp_macc_gpr past phase mux

Change 122989 on 2003/09/24 by dclifton@dclifton_xenos_linux_orl

Moved output register after phase mux in sp_vector
```

Change 122779 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

more changes for cube opcode

Change 122778 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

More changes for cube opcode

Change 122681 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

More cube opcode fixes

Change 122680 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

More cube opcode fixes

Change 122679 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

Many changes for timing, especially using ones comp instead of twos comp in preparation for exp opcode

Change 122678 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

Many changes for timing, especially using ones comp instead of twos comp at preparation for exp opcode

Change 121991 on 2003/09/18 by dclifton@dclifton_r400

First draft of redundant sp block

Change 121905 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Fixes for cube opcode

Change 121904 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Fixes for cube opcode

Change 121902 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Corrected face id definition for cube opcode

Change 121901 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Lots of fixes for cube opcode

Change 121900 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

```
Lots of fixes for cube opcode

Change 121899 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Change in structure to improve timing

Change 121898 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Change in structure to improve timing

Change 121748 on 2003/09/17 by mmantor@FL_mmantorLT_r400_win

<updates to the tb_vector testbench>

Change 121057 on 2003/09/12 by dclifton@dclifton_crayola_linux_orl

I/O change for VC_SP_data_valid

Change 120910 on 2003/09/12 by donaldl@donaldl_crayola_linux_orl

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

Change 120521 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Added new scalar opcode definitions

Change 120403 on 2003/09/10 by dclifton@dclifton_r400

Conditioned tp_sp_data_valid with gpr_phase for writes to gprs.  Enabled NEGATE signal
to scalar for SC_SUB_CONST_* opcodes

Change 120402 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Fixed neg zero plus neg zero.  Conditioned pred execute with valid ops

Change 120401 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Fixed neg zero plus neg zero.  Conditioned pred_execute output for active opcode.

Change 120400 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Eliminated sign modifiers from prev opcodes for previous scalar operand

Change 120399 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl
```

MOVA and MOVA_FLOOR two operand inst. now

Change 120398 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

MOVA and MOVA_FLOOR now two operand inst.

Change 120047 on 2003/09/08 by dclifton@dclifton_r400

Start of testbench for vector unit

Change 119359 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Carrysave on final mult to improve timing

Change 119358 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Carrysave on final mult to improve timing

Change 119233 on 2003/09/03 by tien@tien_r400_devel_marlboro

Final predicate check-in.
I ran the release_parts_lib.pl scripts TWICE before chekcing this in LOL

Change 119064 on 2003/09/02 by viviana@viviana_crayola2_syn

Changed the memories to include internal register.

Change 118941 on 2003/08/31 by tien@tien_r400_devel_marlboro

One or two more checkins and predicate should be there

Change 118760 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Added registered outputs

Change 118759 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Added registered outputs

Change 118688 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

update for 3 simds

Change 118687 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

update for 3 simds

Change 118686 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

```
update for 3 simds

Change 118685 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

update for 3 simds

Change 118684 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Update for 3 simds

Change 118683 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Update for 3 simds

Change 118682 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Connected up upper VC_SP_simd bit

Change 118681 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Latest virage build

Change 118680 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Latest virage build

Change 118679 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Fixed cube opcode

Change 118678 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Fixed cube opcode

Change 118490 on 2003/08/28 by dclifton@dclifton_r400

Clean up of unused signals, fix of STAR signals in sp.v

Change 118326 on 2003/08/27 by tien@tien_r400_devel_marlboro

Final changes for simd expansion to 2 bits

Change 118129 on 2003/08/26 by dclifton@dclifton_r400

Fixed bug in adder.

Change 118128 on 2003/08/26 by dclifton@dclifton_r400
```

```
Added definable # of simd's to sp.

Change 118127 on 2003/08/26 by dclifton@dclifton_crayola_linux_orl

Fixed max pos clamp on const addr.  Eliminated some registers in export scalar fog
path.

Change 117446 on 2003/08/21 by dclifton@dclifton_r400

Changes for synthesis--removed unused pins from sp_comp_opcodes and sp_macc32_multiply.
Tweaked input delays on spi_hi_prec_int.

Change 117026 on 2003/08/19 by dclifton@dclifton_r400

Fixed -0 + -0 case in vector and scalar.
Fixed flip sign timing issue in sp_macc32.
Delayed negate signal to scalar to sync with input b.

Change 116586 on 2003/08/14 by dclifton@dclifton_r400

Added sin/cos to scalar engine
Changed spi_hi_prec_int to improve timing--it now clamps at max float instead of
rolling back to zero.

Change 115899 on 2003/08/11 by tien@tien_r400_devel_marlboro

Cmask fix for 3-channel *_AS_16_16_16_16 formats

Change 115381 on 2003/08/07 by dclifton@dclifton_r400

sp_scalar_lut:  mova reverted to act like max, force_mul_prev2_max_float logic changed,
fixed clamp bug in log, clear sign on force zero, single operand inst for zero for b
input, masked pred_set_execute on anything but kill and pred_set ops.  sp_macc:
force_mul_prev2_max_float logic changed.  sp_macc32: masked inf, nan, or unknown unused
operands for DOT3 and DOT2 ops, disabled flip_sign for adds resolving to zero.
sp_vector:  removed extra register from exported scalar data, fixed mova fixed address
calculation.

Change 114873 on 2003/08/04 by askende@askende_r400_linux_marlboro

releasing changes

Change 113623 on 2003/07/28 by tien@tien_r400_devel_marlboro

Man it's been a long time coming :-)
formatter fix for TP to output to 1 simd only
drive simd signal from TPC to VC (will prolly need to skew it a bit, but that will fall
```

```
out from debug)
Clean up get/set logic

Change 113214 on 2003/07/25 by askende@askende_r400_linux_marlboro

fix related to PRED instructions

Change 112289 on 2003/07/22 by dclifton@dclifton_r400

Updated staging registers in sp_macc.
Revised sp_scalar_lut.
Test signals connected.

Change 111038 on 2003/07/14 by vbhatia@vbhatia_r400_linux_marlboro

Added -coverage option for line,tgl,fsm and conditional coverage to the scripts
and accordingly updated testbenches for enhanced coverage

Change 110836 on 2003/07/14 by dclifton@dclifton_r400

Removed DOS carriage returns

Change 110640 on 2003/07/12 by mmantor@mmantor_crayola_linux_orl

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

Change 110505 on 2003/07/11 by tien@tien_r400_devel_marlboro

tp_lod_deriv fix (denorms -> 0 in fp_fast_mult_dno)
formatter fix (1.0 detection for 32- and 16- bit channels)

Change 110421 on 2003/07/11 by llefebvr@llefebvr_r400_linux_marlboro

This is the bvrl file I forgot to submit along with the .mc file.
```

```
Change 110419 on 2003/07/11 by llefebvr@llefebvr_r400_emu_montreal

Added MOVA to the list of compare opcodes. The SP instead of doing a simple compare of
the GPRs for mova (as it should do) was doing an Add. This was causing corruptions
whenever MOVA was used to move data from GPR to GPR. This change fixed test
mova_tests.cpp TEST_CASE=mova_reg.

Change 110348 on 2003/07/10 by vbhatia@vbhatia_r400_linux_marlboro

Added test and emu support for fmt_32_32_32 float (fmt number 57)

Change 110300 on 2003/07/10 by viviana@viviana_crayola2_syn

STAR_cmdscout should be an output of this module and not an input.

Change 110266 on 2003/07/10 by tien@tien_r400_devel_marlboro

Cleaned up TP_SQ_dec
More formatter fixes.

Change 110200 on 2003/07/10 by tien@tien_r400_devel_marlboro

formatter clamping fix
driving TP_SQ_dec as it should be

Change 110041 on 2003/07/09 by tien@tien_r400_devel_marlboro

More formatter fixes
Fixed sec pitch calcs

Change 109978 on 2003/07/09 by vbhatia@vbhatia_r400_linux_marlboro

updated gen15 and gen31 to not generate invalid dst_sel

Change 109785 on 2003/07/08 by tien@tien_r400_devel_marlboro

VC mode fixes for formatter

Change 109617 on 2003/07/07 by vbhatia@vbhatia_r400_linux_marlboro

Added few more tests for ease of debug

Change 109467 on 2003/07/07 by vbhatia@vbhatia_r400_linux_marlboro

few formatter emu fixes and testbench updates

Change 109464 on 2003/07/07 by viviana@viviana_crayola2_syn
```

Added the register in the 128x128 memory, rebuilt the Virage system with latest compilers.

Change 109202 on 2003/07/03 by tien@tien_r400_devel_marlboro

Removed cmask
Reduced data_valid to 1 bits

Change 108942 on 2003/07/02 by dclifton@dclifton_r400

double buffered resets

Change 108774 on 2003/07/01 by tien@tien_r400_devel_marlboro

Bug fix in tpc_fifos for pm4ply test
Misc formatter fixes

Change 108760 on 2003/07/01 by llefebvr@llefebvr_r400_linux_marlboro

Fixed r400sq_const_index_03.cpp. Now works on the SQSP testbench. Still has issues on the GC because of bad ferret/cp ring buffer synchronization.

Fixed:

1) Bad clamping of the address register in the SP
2) Bad error handling of an out of range address in the SQ.

Change 108627 on 2003/06/30 by tien@tien_r400_devel_marlboro

More formatter fixes

Change 108543 on 2003/06/30 by tien@tien_r400_devel_marlboro

Vector width mismatch fixes

Change 108494 on 2003/06/30 by tien@tien_r400_devel_marlboro

Finalized VC_SP IO on the sp side

Change 108444 on 2003/06/27 by vbhatia@vbhatia_r400_linux_marlboro

Added extra test vector clamp for vertex rf expand enabled, signed no-zero case

Change 108420 on 2003/06/27 by vbhatia@vbhatia_r400_linux_marlboro

updated vc formatter testbench and added a few tests

Change 108276 on 2003/06/27 by tien@tien_r400_devel_marlboro

```
Fixed runme script yet again :-)
More formatter fixes

Change 108181 on 2003/06/26 by tien@tien_r400_devel_marlboro

Formatter fixes

Change 108140 on 2003/06/26 by rramsey@rramsey_crayola_linux_orl

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

Change 108117 on 2003/06/26 by vbhatia@vbhatia_r400_linux_marlboro

Added +CLAMPOFF option, regularly on with clamping data to only values supported by
hardware and can be turned off by this option to test behavior for other values

Change 108080 on 2003/06/26 by tien@tien_r400_devel_marlboro

Fixed mini-regress script for release_* area usage
Fixed large unnuomed coord handling (for a cp_e2* test) .. for real this time I think )
Misc sp_tp_formatter fixes

Change 107997 on 2003/06/26 by mmantor@mmantor_crayola_linux_orl

<remove extra delay stage on scalar_data for scalar_input_red when scalar_opcode_prev
and the creation of force_mul_prev2_max_float to compensate for the stage added back
into the scalar engine>

Change 107806 on 2003/06/25 by moev@moev2_r400_linux_marlboro

Update file to reflect split between sp and spi
```

```
Change 107804 on 2003/06/25 by moev@moev2_r400_linux_marlboro

done with temp file

Change 107735 on 2003/06/24 by vbhatia@vbhatia_r400_linux_marlboro

Updated test bench to clamp out values that are not possible as input to formatter in
rf_expand_enable mode.

Change 107665 on 2003/06/24 by tien@tien_r400_devel_marlboro

Added >1.0 mag clamp in formatter
A few bug fixes with normalizer mux
Added some features to tp_formatter regression script
Updated tp4_tc  mini regression script

Change 107593 on 2003/06/24 by vbhatia@vbhatia_r400_linux_marlboro

Added new tests and fix for same format_comp_x,y,z,w for rf_expand_enabled mode

Change 107502 on 2003/06/23 by vbhatia@vbhatia_r400_linux_marlboro

Enable rf_expand_enable bypass path in emu and testbench

Change 107477 on 2003/06/23 by vbhatia@vbhatia_r400_linux_marlboro

Added more auto generated directed and randomized tp formatter tests

Change 107389 on 2003/06/22 by mmang@mmang_crayola_linux_orl

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
```

```
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

Change 107290 on 2003/06/20 by vbhatia@vbhatia_r400_linux_marlboro

Tp and Vc formatter standalone testbenches around the unified sp_tp_formatter
along with scripts to regress against emulator

Change 107257 on 2003/06/20 by tien@tien_r400_devel_marlboro

Complewted first pass and vc part of formatter
Made regression script more thorough

Change 107174 on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro

- swapped PS and ID gpr write phases

Change 107069 on 2003/06/19 by askende@askende_r400_linux_marlboro

checking in changes related to area/timing optimization

Change 107066 on 2003/06/19 by askende@askende_r400_linux_marlboro

area/timing optimization

Change 106990 on 2003/06/19 by tien@tien_r400_devel_marlboro

Forgot leading one, expanded channels out one more bits

Change 106897 on 2003/06/18 by tien@tien_r400_devel_marlboro

Added mip_packed output on tpc
More fixed to formatter

Change 106822 on 2003/06/18 by moev@moev2_r400_linux_marlboro
```

```
fixed patchbox to reflect proper connectivity of the star system

Change 106821 on 2003/06/18 by moev@moev2_r400_linux_marlboro

part of new compiler

Change 106819 on 2003/06/18 by moev@moev2_r400_linux_marlboro

updated compilers

Change 106817 on 2003/06/18 by moev@moev2_r400_linux_marlboro

fix port definition of STAR_cmdscout from input to output

Change 106572 on 2003/06/17 by tien@tien_r400_devel_marlboro

More sp_tp_formatter changes and a port fix on tpc notied by Steve Mburu

Change 106242 on 2003/06/15 by tien@tien_r400_devel_marlboro

Added cmask gen code

Change 106117 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

sp_stdrfsdks2p128x128cm2sw1.v for SP.

Change 106110 on 2003/06/13 by moev@moev2_r400_linux_marlboro

MAV's version of cnt file

Change 106092 on 2003/06/13 by tien@tien_r400_devel_marlboro

Many updates.

Change 105680 on 2003/06/11 by tien@tien_r400_devel_marlboro

Recoded sp_tp_formatter in Module Compiler

Change 105565 on 2003/06/11 by askende@askende_r400_linux_marlboro

top level clean-up

Change 105079 on 2003/06/09 by grayc@grayc_crayola2_linux_orl

   adding VC to chip build

Change 104895 on 2003/06/09 by rramsey@rramsey_crayola_linux_orl
```

```
Fix a bug with sticky bit used for dot_product nan detection

Change 104662 on 2003/06/06 by grayc@grayc_crayola2_linux_orl

   added VC interfaces

Change 104226 on 2003/06/05 by smoss@smoss_crayola_linux_orl

   quick check-in for vc release (code works in release)

Change 104075 on 2003/06/04 by dclifton@dclifton_r400

added test controller

Change 101841 on 2003/05/20 by askende@askende_r400_linux_marlboro

checking in the interpolator control latency changes in SQ and SP.

Change 101494 on 2003/05/18 by tien@tien_r400_devel_marlboro

sp_tp_formatter fix

Change 101419 on 2003/05/16 by tien@tien_r400_devel_marlboro

Moved input flops out of sp_tp_formatter

Change 101243 on 2003/05/15 by tien@tien_r400_devel_marlboro

Update makefiles and dependecies
Added border code

Change 101041 on 2003/05/14 by tien@tien_r400_devel_marlboro


Change 100961 on 2003/05/14 by tien@tien_r400_devel_marlboro

Fixed TP_SP_rf_expand_enable.

Change 100673 on 2003/05/13 by askende@askende_r400_linux_marlboro

fix a typo related to out-of-range indexing

Change 100175 on 2003/05/09 by askende@askende_r400_linux_marlboro

releasing R500 related IO top level changes for SP/SPI system

Change 97758 on 2003/04/25 by tien@tien_r400_devel_marlboro
```

LEDA changes

Change 97548 on 2003/04/25 by askende@askende_r400_linux_marlboro

modified the PRED instructions to match the new definition. Src.W channel is now used instead of Src.X

Change 97205 on 2003/04/23 by askende@askende_r400_linux_marlboro

1. fix to allow src (argument a) to be written back to the GPRs when doing a MOVA
       2. modified the 4 LSBs of the autocount bus to use the SPI block id as supposed to SP block id + vector unit id

Change 96874 on 2003/04/22 by rramsey@rramsey_crayola_linux_orl

fix for pv/ps swizzling

```
Change 132894 on 2003/11/19 by rramsey@rramsey_xenos_linux_orl

Fix SQ_VC dec signals in tb_sqsp.
Change tbtrk_sqvc so it does not compare fetch addr for mini fetches.
Fix problem in tex_instr_seq that was allowing mini fetches to start
out of phase.
Add more info to msgs from pcdata tracker to tell which set of pc data
is mismatching. Also turn off sx1 compare since it is redundant now that
all the sx data comes from usx_0.

Change 132675 on 2003/11/18 by danh@danh_xenos_linux_orl

Added the tbtrk_sq_sx_pcaddr tracker.

Change 132667 on 2003/11/18 by danh@danh_xenos_linux_orl

Initial Release.

Change 132649 on 2003/11/18 by vromaker@vromaker_r400_linux_marlboro

- alu_instr_seq timing fixes for constant store read: first the register stage
  on the offset was moved after the sum2 adder; then the init_done_bits signal
  was changed from a combinational ACS state machine output to a registered
  one-bit state machine output to help the path to the new sum2 register
- thread buff status read timing fix - moved the status read back one cycle by
  sending the unregistered, rotated request vector to the arbiter and registering
  the winner out of the arbiter; the output of the status read mux was
  then registered

Change 132516 on 2003/11/18 by rramsey@rramsey_xenos_linux_orl

Add a mova test to the sq regression.
Change no_inc in pix_ctl to use sr version instead of nxt value
out of the ppb.
Fix instr base calc in rbbm_if so rt/nrt determination is correct.
Stop vec_grp tracker from comparing pix auto_count cycles.

Change 132219 on 2003/11/16 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 132123 on 2003/11/14 by rramsey@rramsey_xenos_linux_orl

Fix a bug in aluconst_mem related to rt constant reads.
Fix const_map_cntl so deallocate_cnt gets updated correctly when alloc and
context_done happen on same clk.
tb_sqsp was missing some primitive boundaries in the pkr for RT prims.
```

```
Change 131826 on 2003/11/13 by rramsey@rramsey_xenos_linux_orl

get rid of ifndefs so vcs will compile

Change 131814 on 2003/11/13 by dclifton@dclifton_xenos_linux_orl

Added register for undriven signal

Change 131722 on 2003/11/13 by rramsey@rramsey_xenos_linux_orl

Add capability to dump Cadence shm instead of fsdb. Enabled by defining
DUMP_SHM in tb_sqsp/vcsopts.f file

Change 131537 on 2003/11/12 by llefebvr@llefebvr_r400_linux_marlboro

1) added register stage to line up pred_override bits with SP phase
2) made the waterfall/predicated override an or instead of an and.

Change 131465 on 2003/11/11 by donaldl@donaldl_xenos_linux_orl

When in the VS_EVENT state and going to IDLE, update d_sp_sel[3:0] as a default
based on disable_vtx_3,2,1,0 instead of 0.  This is to fix a bug where the correct
o_sp_vsr_valid bit was not being set because the disable simd flags were not being
considered (when going from VS_EVENT to IDLE).

Change 131241 on 2003/11/11 by kmeekins@kmeekins_xenos_linux_orl

Removed event window from VC counters.

Change 131082 on 2003/11/10 by kmeekins@kmeekins_xenos_linux_orl

tb_vc.v
  ----------
  Fixed instantiation of vc now that delay is removed.

  sq_fetch_arb.v
  --------------
  Changed the bus width of vc_mini_count_q to accomidate the +2 modification.

  vcmi_requestor.v
  -----------------
  Increased the uvcmi_input_fifo FIFO depth to 8.
  Added the FIFO full to the performance monitor.

  tp.blk,
  vc.v,
  vc_perf_config.txt,
  vc_perfmon.v,
```

```
  vcmi.v
  ----------------------
  Added the FIFO full for the vcmi_input_fifo to the performance monitor.

Change 130763 on 2003/11/07 by llefebvr@llefebvr_r400_linux_marlboro

Reverting timing fix that broke r400sq_const_index_04.cpp test.

Change 130661 on 2003/11/07 by rramsey@rramsey_xenos_linux_orl

Another attempt to keep the pc_out_ppb from overflowing

Change 130571 on 2003/11/06 by llefebvr@llefebvr_r400_linux_marlboro

This fixes the bad pix/vtx GPR input arbitration performance counter.

Change 130421 on 2003/11/06 by bhankins@bhankins_xenos_linux_orl

- sq-sx thread id added to sq output and into and through the sx
   - updated sx-rb trackers to use sq-sx thread id
   - removed obsolete code from sx
   - fixed sx bug where an ea from one export to memory was resetting the valid bits
for the other export to memory

Change 130346 on 2003/11/05 by danh@danh_xenos_linux_orl

Removed spi delay_in and delay_out ports.

Change 130127 on 2003/11/04 by vromaker@vromaker_r400_linux_marlboro

- instruction writes to the different SIMD memories now happen
  independently and no longer wait for all SIMD memories to be
  available

Change 130094 on 2003/11/04 by rramsey@rramsey_xenos_linux_orl

Fix scalar tracker so it compares all 128 bits based on write masks
It was only comparing the lower 32 bits based on bit 0 of the write mask

Change 130079 on 2003/11/04 by rramsey@rramsey_xenos_linux_orl

Couple of timing fixes for aiq and cfs
Fix a bug in the rbbm if that was allowing map copies to happen before
memory writes
Fix a problem in the testbench that was causing some incompletes

Change 130072 on 2003/11/04 by rramsey@rramsey_xenos_linux_orl
```

```
Update tracker to work with new sp_sx dump file that has all free-done
entries as unique lines between exports

Change 129980 on 2003/11/03 by smoss@smoss_crayola_linux_orl_regress

   some housekeeping and removed bad path

Change 129723 on 2003/11/01 by vromaker@vromaker_r400_linux_marlboro

- fixed pix ctl output buffer overwrite bug
- backed timing fix out of status reg and pix thread buff

Change 129444 on 2003/10/30 by llefebvr@llefebvr_r400_linux_marlboro

Fixing dangling wires in the sq related to performance module.
Fixing shader due to Kill opcode assembler change.
Fixing trakcer problem in the TB_SQSP when autocount vtx is on.

Change 129408 on 2003/10/30 by rramsey@rramsey_xenos_linux_orl

Move some continuous assignments into always blocks to help sim time
Rework cfs_rtr/arb_xfc path to help timing
Fix a problem with detecting serialize for the cf state machine

Change 129348 on 2003/10/30 by mearl@mearl_xenos_linux_orl

Added two primitive interpolation back in.

Change 129259 on 2003/10/29 by danh@danh_xenos_linux_orl

- spi_interp_ctl IJ buffer changed from one 16x200 memory to two 16x100 memories.
       - added additional SQ_SP_interp_qd[0:1]_prim_sela signals to improve spi input
timing.

Change 129213 on 2003/10/29 by llefebvr@llefebvr_r400_linux_marlboro

Added VC_PERF_ACTUAL_STARVED performance counter in the SQ.

Change 129150 on 2003/10/29 by llefebvr@llefebvr_r400_linux_marlboro

Increasing VC mini count to l1_fifo_size +2.

Change 129066 on 2003/10/28 by vromaker@vromaker_r400_linux_marlboro

- added vtx input optimization for autocount on and continued off
- fixed initialization problem for vtx autocount
- made pix thread buff timing fixes: reduced load on status read
         data bit 19, which is the event bit, and also tried to reduce
```

```
         the load on pop_thread (part of the same path) in the status register
- backed out a timing fix in alu_instr_seq that was causing a mova
         test to fail
- fixed the AUTO_COUNT_SIZE definition

Change 128816 on 2003/10/27 by llefebvr@llefebvr_r400_linux_marlboro

Adding VC performance counters in the SQ.
Removed the SX->RB warnings on non-initialized GPR channels.

Change 128675 on 2003/10/27 by smoss@smoss_xenos_linux_orl

   combined ncverilog and vcs simulators to one build

Change 128659 on 2003/10/27 by donaldl@donaldl_xenos_linux_orl

Delayed rom_rsp_shift*_* mux shift selects 1 clk to fix synthesis timing.

Change 128656 on 2003/10/27 by donaldl@donaldl_xenos_linux_orl

Changed vc_req's and tex_req's dependencies on vc_pending_q and
tp_pending_q.

Change 128647 on 2003/10/27 by rramsey@rramsey_xenos_linux_orl

Change ais so PS src sel gets priority over PV
Add predicated jumps and calls to cfs
Fix fetch_type connection in sq and tex_instr_seq

Change 128645 on 2003/10/27 by llefebvr@llefebvr_r400_linux_marlboro

Incrementing the number of in flight testure requests from 6 to 7.

Change 128601 on 2003/10/27 by mmantor@mmantor_xenos_linux_orl

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

Change 128592 on 2003/10/26 by danh@danh_xenos_linux_orl

Changed sc_rt_valid to fix the condition when end_of_prim and end_of_vector do not
occur at the same time, the sc_packer will send real time fill quads.

Change 128526 on 2003/10/24 by mearl@mearl_xenos_linux_orl

Took out two prim per clock to get regression to pass.
```

Change 128393 on 2003/10/24 by llefebvr@llefebvr_r400_linux_marlboro

This should fix the instruction count being off. The bad machine (cfs) was used to determine the thread type and hence some pixel shader instructions were counted as vertex ones and vice versa.

Change 128365 on 2003/10/24 by mearl@mearl_xenos_linux_orl

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed synthesis
bugs in SC.

Change 128209 on 2003/10/23 by vromaker@vromaker_r400_linux_marlboro

- timing fixes for constant store read address

Change 128195 on 2003/10/23 by rramsey@rramsey_xenos_linux_orl

Fix a problem with yield_optimize

Change 128048 on 2003/10/23 by llefebvr@llefebvr_r400_linux_marlboro

Fixed problem in the active counters when both pixels and vertexes were processing at the same time.

Change 128019 on 2003/10/23 by rramsey@rramsey_xenos_linux_orl

go back to prev version

Change 127895 on 2003/10/22 by vromaker@vromaker_r400_linux_marlboro

- timing fixes for gpr alloc

Change 127872 on 2003/10/22 by rramsey@rramsey_xenos_linux_orl

fixes for MT3 functions

Change 127861 on 2003/10/22 by llefebvr@llefebvr_r400_linux_marlboro

Fixing TP and VC sync stalls for both pixel and vertex threads.

Change 127742 on 2003/10/22 by llefebvr@llefebvr_r400_linux_marlboro

Removed the warnings from the sp->sx trackers and sx->sp.
Now emulator is always executing the scalar instruction even in the case of a 3 operand vector opcode. This is to match with random shaders.

```
Change 127730 on 2003/10/22 by rramsey@rramsey_xenos_linux_orl

Fix a bug with start_of_clause

Change 127580 on 2003/10/21 by danh@danh_xenos_linux_orl

Changed any_pred_hi and any_pred_lo generation, now the predicate and valid bits are
now related to the thread that the CFS is working on.

Change 127397 on 2003/10/20 by llefebvr@llefebvr_r400_linux_marlboro

Added an event window for pixels. There was a problem in the global event window as if
both pixels and vertexes were turned on at the same time, as soon as one went off it
was turning off the whole window. This fixes pixel counters being 0 for some tests.

Change 127325 on 2003/10/20 by vromaker@vromaker_r400_linux_marlboro

- updated VC injector to handle multi-cycle returns (the number of cycles, 1 to 4, is
         read from the vc_rp_sp.dmp file)

Change 127313 on 2003/10/20 by dclifton@dclifton_r400

Updated to testbench changes.

Change 127269 on 2003/10/19 by rramsey@rramsey_xenos_linux_orl

Change behave mem_model in spi so its read dly matches the real mem
Send interp_valid and ij_line 1clk early to account for 2clk read dly
Fix spi_sp tracker so it works with early valid
Change thread_buf and cfs machines so only fetches can modify the
fetch pending bit. The alu machines only read the value out of the buffer.
Get rid of a bunch of extra 'else' clauses

Change 127091 on 2003/10/17 by rramsey@RRAMSEY_P4_r400_win

udpate spreadsheet with 10/17/03 results
modify script so it automatically handles reports with/without runtime

Change 127079 on 2003/10/17 by smoss@smoss_xenos_linux_orl

   initialized memory controller for sc and sx to allow real memories to work in
tb_sqsp

Change 126983 on 2003/10/16 by vromaker@vromaker_r400_linux_marlboro

fixed code that was causing a latch in synthesis

Change 126908 on 2003/10/16 by rramsey@rramsey_xenos_linux_orl
```

```
absolute modifier for constants should apply to all source constants

Change 126823 on 2003/10/15 by rramsey@rramsey_xenos_linux_orl

Add sqvc tracker to gc testbench when running with orlando trackers
Rework some of the alu/tex constant logic to get rid of the bug that
was allowing threads to start processing before all of the constants for
their context had been loaded.

Change 126796 on 2003/10/15 by vromaker@vromaker_r400_linux_marlboro

- hooked up the new alu_arb_policy and tx_cache_sel register bits (but
         temporarily tied the tx_cache_sel input to the vtx thread buff low
         since it is being incorrectly set to 1 by Primlib)

Change 126483 on 2003/10/13 by mearl@mearl_xenos_linux_orl

Fix One Prim Per Clock bug in sq_ptr_buff. Revert changes in sq_pix_ctl to make
       2 prim interp changes easier. Put known primdata data on all quads across packer
       to iterator interface. Fix dumps for no_inc_pix_cnt signal.

Change 126450 on 2003/10/13 by donaldl@donaldl_xenos_linux_orl

Delayed SQ_SX_sp_simd_id an extra clock to line up for reduduncy use.

Change 126362 on 2003/10/13 by rramsey@rramsey_xenos_linux_orl

Change sq_sp_interp dump so it contains all of the pass_count and wrap passes
through the interpolator
Add spi_sp tracker (enabled with ENABLE_SPI_TRACKER define)

Change 126324 on 2003/10/13 by dougd@dougd_r400_linux_marlboro

Added logic to generate read enables for the 4 map rams in sq_aluconst_rams.v
Added SQ_CONTEXT_MISC_YEILD_OPTIMIZE register to sq_rbbm_interface.v

Change 126234 on 2003/10/10 by vromaker@vromaker_r400_linux_marlboro

- added export arbiter module that will limit the number of color buffer export
         threads to one every 4 clocks
- hooked up the export blocker outputs and commented out the previous export
         blocking code
- added export alloc arbiter inputs to exp_alloc_ctl module so that the buf_avail
         counter will be updated by the export allocs
- added logic to support the export arbiter to the vertex and pixel thread buffers
- added logic to support the export arbiter to the thread arbiter
- separated the export alloc request out of the alu request logic in the status
```

```
register,
         and added an output for the export alloc request

Change 126226 on 2003/10/10 by cbrennan@cbrennan_r400_emu

Release from my emu branch: texture stacks for TP as well.
Leda rule tweaks
add more .rg files

Change 125806 on 2003/10/09 by cbrennan@cbrennan_r400_release

Temporarily reduce the num SQ_TP vectors in flight back to 6 until fifo overflows can
be fixed.

Change 125780 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

update sx test inputs to match the established convention

Change 125697 on 2003/10/08 by dougd@dougd_r400_linux_marlboro

fixed bug in eqn for *sync_alu_stall

Change 125660 on 2003/10/08 by rramsey@rramsey_xenos_linux_orl

Fix compile warnings for sq (several missing ports)
Fix compile warning in sx_parameter_caches
Fix SQ_SP_fetch_simd_sel so it lines up with the data coming out of the GPRs

Change 125598 on 2003/10/08 by dougd@dougd_r400_linux_marlboro

Expanded the read back mux for rbbm diagnostic reads
to include the extra memories for SIMD2 and SIMD3.

Change 125550 on 2003/10/08 by rramsey@rramsey_xenos_linux_orl

Increase sq_tp_maxcount from 6 to 7
Fix a problem with the simd mux for vtx_alloc_size in export_alloc
Fix a problem with pc_alloc_free_cnt in export_alloc (alloc and dealloc on same clk
was broken)
Make alu ctl_flow and instr trackers work with multiple simd's
Also change these trackers to use common code for pix/vtx by selecting the type with
a parameter

Change 125540 on 2003/10/08 by dclifton@dclifton_r400

Added needed include files.  Strange how these compiled before this.

Change 125509 on 2003/10/07 by dougd@dougd_r400_linux_marlboro
```

```
change perfcounters alu(0/1)_fifo_empty_simd* to count
alu(0/1)_stall_simd* instead.

Change 125370 on 2003/10/07 by mearl@mearl_xenos_linux_orl

Fixed the SQ bug when bad pipe exists before a good pipe. Also, updated
       the RT trackers in the SC testbench.

Change 125278 on 2003/10/07 by dougd@dougd_r400_linux_marlboro

Added a new state register, vc_fifo_depths_l1_req_fifo_depth to
sq_rbbm_interface.v and wired it up to the compare logic for
vc_mini_count_q in sq_fetch_arb.v.

Corrected a typo in sq_vtx_ctl.v that affected synthesis.

Change 125260 on 2003/10/07 by dclifton@dclifton_r400

Updates for a couple of fifos in sq and new block in sp

Change 125059 on 2003/10/06 by rramsey@rramsey_xenos_linux_orl

Fix sq_sx file read in tb_sqsp
Add new tracker for shader writes to gpr
Add myself to failing regression email list

Change 124864 on 2003/10/03 by rramsey@rramsey_xenos_linux_orl

add some missing wire declarations

Change 124850 on 2003/10/03 by rramsey@rramsey_xenos_linux_orl

move an adder in front of a register and change to a fifo with registered
outputs to help timing

Change 124792 on 2003/10/03 by dougd@dougd_r400_linux_marlboro

Removed all references to SIMD1_DISABLE in sq.v and sq_rbbm_interface.v.

Added 32 new performance counters: many are for SIMD2 and SIMD3 but
other existing counters were expanded to differentiate between vertex
and pixel counts. There are now 95 performance counters in the sq.

Change 124774 on 2003/10/03 by smoss@smoss_crayola_linux_orl_regress

   re-enabled behavioral memories until real memories are working
```

```
Change 124741 on 2003/10/03 by bhankins@bhankins_xenos_linux_orl

fix name on sx test pin

Change 124738 on 2003/10/03 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 124634 on 2003/10/02 by rramsey@rramsey_xenos_linux_orl

adding cond_pred optimize to control flow seq

Change 124434 on 2003/10/01 by mmang@mmang_xenos_linux_orl

1.  Turned on 3 simds in emulator (sc_interp.cpp,
    sq_block_model.cpp, and user_block_model.cpp).
2.  Turned on 3 simds in rtl (sc_packer.v,
    tb_sqsp.v, and vgt.v).
3.  Fixed bug in chip_vc.tree to get SQ_VC_simd_id
    and TC_VC_simd hooked up correctly.
4.  Fixed bug in sc_packer.v related to having a 2
    bit simd_id_sel.

Change 124292 on 2003/10/01 by rramsey@rramsey_xenos_linux_orl

Change sq_vgt_rtr to be driven based on fifo full, rather than by the vsr
load state machine

Change 124203 on 2003/10/01 by dougd@dougd_r400_linux_marlboro

The four existing SYNC_STALL counters were separated into
(8) pix and vtx stall counters.
The two ALU INSTRUCTION ISSUED counters were made to increment
by 1,2,3 or 4.
The two CF INSTRUCTION ISSUED counters were made to increment
by 1,2,3,4,5 or 6.

Added `ifdef's to sq_perfmon_wrapper for SIMD1, SIMD2, SIMD3.

perfmon event window:
An enable for the performance counters is generated by events received
from the VGT and/or SC which create a window of time when the counters
will be active. All of the perf counters are now controlled by this enable.

Change 123984 on 2003/09/30 by bhankins@bhankins_xenos_linux_orl

change names of sx i/o ROM_MCn_disable signals
```

```
Change 123966 on 2003/09/30 by smoss@smoss_xenos_linux_orl

   using real memories for sqsp

Change 123952 on 2003/09/30 by mmantor@mmantor_xenos_linux_orl

<added changes for 2 prim interpolation to the spi and sq and all top level
interconnects, and sq_sx_sp_simd_id for redundancy control, and all changes to test
bench as well as some ncverilog error messages.  Some other misc top level clean up>

Change 123918 on 2003/09/29 by rramsey@rramsey_xenos_linux_orl

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

Change 123798 on 2003/09/29 by donaldl@donaldl_xenos_linux_orl

Temporary hook-up of SQ_SX_interp_2prim to zero going to SX until
SQ changes for 2 prims is complete.

Change 123755 on 2003/09/29 by mearl@mearl_xenos_linux_orl

Fix for timing problems, submitting new memories, using real memories for regressions.

Change 123528 on 2003/09/26 by llefebvr@llefebvr_r400_linux_marlboro

The sp->sx, sq->tp and sq->vc trackers now all use the post steered valid bits to know
what is valid. Thus they are now compatible with the redundant pipe. They should track
correctly in any bad pipe configuration. They however don't compare the RSP data for
now (waits for the HW implementation)

Change 123515 on 2003/09/26 by bhankins@bhankins_xenos_linux_orl

- add sx_redundancy.v to hierarchy to try and improve on timing
   - add EXP_BUF_112_DEEP switch.  comment out in sx_defines.v to enable
     all 128 locations of the color export buffer to be used
```

```
   - add ONE_STAR_PROCESSOR switch.  comment out in sx_defines.v to use
     two star processors.
   - add support for thread id and thread type for debug.
   - misc changes for timing which don't change the logic.

Change 123485 on 2003/09/26 by dougd@dougd_r400_linux_marlboro

I removed these files prematurely.

Change 123462 on 2003/09/26 by dclifton@dclifton_r400

disabled USE_BEHAVE_MEM. Changed 8x104 ram in sq to 8x105.

Change 123343 on 2003/09/25 by dougd@dougd_r400_linux_marlboro

adding the x105 virage memories and deleting the x104 used in the sq_vc_skid_buf

Change 123331 on 2003/09/25 by dougd@dougd_r400_linux_marlboro

usq_alu01_state_mem is used twice as the instance name so I changed
the 2nd one to usq_alu23_state_mem.

Change 123260 on 2003/09/25 by mmang@mmang_xenos_linux_orl

1.  For Vivian E., added new simd memories and star patch in/out wires.
2.  In vertex thread buffer, fixed bug in simd3 alu state registers.
3.  In pixel thread buffer, fixed bug in simd2/3 cf state read data.
4.  Adjusted simd id bus width for sq to tp tracker.
5.  In sq.v, added vertex shader and pixel shader constant base and
    size connections to simd2/3 alu instruction sequencers.

Change 123113 on 2003/09/24 by llefebvr@llefebvr_r400_linux_marlboro

Fixed the autocount pixel timing by removing 5 pipeline registers in the SQ control
path. Also fixed the counter's with back to 17 bits (from 19) int both the vertex and
pixel path such that when it hits the SP it is of the correct 23 bits width (17 bits
count + 2 bits phase + 4 bits index). This fixes r400vgt_multi_pass_pix_shader_01 at
the sqspsx testbench level.

Change 123082 on 2003/09/24 by mearl@mearl_crayola_linux_orl

tb files updated for ONE_PRIM_PER_CLOCK, bug fix in interpolators for
ONE_PRIM_PER_CLOCK

Change 123076 on 2003/09/24 by donaldl@donaldl_xenos_linux_orl

Connected ROM block redundancy signals.
Added sq export address buffer support.
```

```
Change 122865 on 2003/09/23 by dougd@dougd_r400_linux_marlboro

fixed typo

Change 122699 on 2003/09/23 by dougd@dougd_r400_linux_marlboro

fix typo (change blocking to non-blocking assignment)

Change 122683 on 2003/09/23 by mearl@mearl_crayola_linux_orl

One primitieve per clock changes in the back of the SC and front of the SQ. Right now,
the ONE_PRIM_PER_CLOCK define in
       header.v and SC_SQ_interface.v are needed for this change. Will update this to
ONEPPC, since this already exists in
       header.v. Also, the sim.cfg file does not have an ifdef, so is hardcoded to one
prim per clock.

Change 122558 on 2003/09/22 by dougd@dougd_r400_linux_marlboro

1. changed sq_stdrfsdks2p8x104cm1sw0 to sq_stdrfsdks2p8x105cm1sw0 in sq_vc_skid_buf.v
2. added timing fixes to sq_aluconst_mem.v, sq_aluconst_rams.v and
sq_instruction_store.v

Change 122520 on 2003/09/22 by vromaker@vromaker_r400_linux_marlboro

timing fixes - added registers for vs and ps base and size after the
       context register read mux

Change 122402 on 2003/09/20 by mmang@mmang_crayola_linux_orl

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7.  In sq_export_alloc.v, handle position/main export id
    and parameter cache thread base for simd2/3.  Be able
    to handle one type down simd0/1 and a different type
    down simd2/3 on the same clock.
8.  In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
    gpr_alloc blocks return different acks, gpr bases,
```

```
    and gpr maxes.
9.  In sq_exp_alloc_ctrl.v, handle position/main export
    buffer management.  Be able handle one type down
    simd0/1 and a different type down simd2/3 on the same
    clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
    added muxing and memories to handle status bits, cfs
    state, and alu state.  Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

Change 121731 on 2003/09/17 by rramsey@RRAMSEY_P4_r400_win

add runtime to report
update spreadsheet with 9/17/2003 results

Change 121629 on 2003/09/16 by danh@danh_crayola1_linux_orl

Removed XY pipe delay, XY data is now processed by the interpolators

Change 121559 on 2003/09/16 by tien@tien_r500_emu

Reverse order of TP (vfetch and tfetch) const

Change 121537 on 2003/09/16 by smoss@smoss_crayola_linux_orl_regress

   increasing interface idle timeout for randoms

Change 121348 on 2003/09/15 by dougd@dougd_r400_linux_marlboro

1. corrected the trigger events for VTX_SWAP_IN, VTX_SWAP_OUT,
   PIX_SWAP_IN, PIX_SWAP_OUT, CONSTANTS_USED_SIMD0 and  CONSTANTS_USED_SIMD0.
2. made event counters for these used multibit increment values
3. added  "+incdir+$PARTS_LIB/src/gfx/sp" to vcs_top.ini to pick up
   sp_defines.v included in sq_ais_output.v
```

```
Change 121332 on 2003/09/15 by rramsey@rramsey_crayola_linux_orl

Change pix_ctl so deallocs with real pixel vectors don't free param
cache space until interpolation is almost complete
Wire up the vc_sp valid signals correctly
Fix sx_sp_pcdata tracker

Change 121292 on 2003/09/15 by vromaker@vromaker_r400_linux_marlboro

fixed incorrect loading of loop indices from the thread buffer into
the ctl flow sequencer; this was causing a problem with the test
r400sq_const_index_07

Change 121278 on 2003/09/15 by dclifton@dclifton_r400

Added to SQ include directory list

Change 121219 on 2003/09/14 by smoss@smoss_crayola_linux_orl_regress

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Change 121157 on 2003/09/13 by smoss@smoss_crayola_linux_orl_regress

   xenos updates

Change 121065 on 2003/09/12 by donaldl@donaldl_crayola_linux_orl

Registered ROM_EN_RSP and ROM_PIPE_SEL[3:0].

Change 120910 on 2003/09/12 by donaldl@donaldl_crayola_linux_orl

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

Change 120887 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

-  Add sx_mem_export.v module to capture pixel addresses and
      calculate rb id values for use in export to memory.
   -  Add support for redundancy logic.  Inputs are currently
      tied low in tb_sqsp.v and chip_sx.tree.
   -  Add non-synthesizable logic to route thread id and thread
      type from sq through sx and out to rb for test.  Allows
      tracker to identify export to memories, and to distinguish
      between them.  Tied low in chip_sx.tree and tb_sqsp.v
      All associated I/O and logic is qualified on `ifdef SIM.
   -  Remove the register in sx_export_control_common.v that was
```

```
      requiring some signals on the sq alloc interface to be present
      one clock before the valid.  Now, all sq_sx_exp_ signals are
      expected to be valid only when sq_sx_exp_valid == 1.
   -  Add a register in the generation of the final pixel address
      value for export to memory, to try and improve on timing.

Change 120645 on 2003/09/11 by rramsey@rramsey_crayola_linux_orl

Remove some unused defines
Add reset condition for primdata pipe stages in qdpr_proc
Fix a bug with tp_count in fetch_arb when running with the VC
Increase loop_cnt for vc inject in tb_sqsp

Change 120592 on 2003/09/10 by vromaker@vromaker_r400_linux_marlboro

changed SQ_hs_bclk, TST_SQ_rf_star_wrck, TST_SQ_hs_star_wrck so they
       are defined without the [0:0] range

Change 120510 on 2003/09/10 by vromaker@vromaker_r400_linux_marlboro

fix for SQ_VC_simd_id typo

Change 120426 on 2003/09/10 by donaldl@donaldl_crayola_linux_orl

Added redundancy logic.

Change 120423 on 2003/09/10 by donaldl@donaldl_crayola_linux_orl

Added redundancy logic.

Change 120397 on 2003/09/10 by rramsey@rramsey_crayola_linux_orl

Add code to keep the vc and tp inject routines from clobbering each other
Fix vc inject routine so it handles formats that require double returns

Change 120296 on 2003/09/09 by dougd@dougd_r400_linux_marlboro

added `include "register_addr.v"

Change 120270 on 2003/09/09 by llefebvr@llefebvr_r400_linux_marlboro

Now reading the SIMD_ID from the dump in the tracker. Not doing anything with it
however. It is just read in order to get to the valid data after it.

Change 120190 on 2003/09/09 by dougd@dougd_r400_linux_marlboro

changed SQ_RB_event to SQ_RB_event_pulse and declared as output from sq.v
```

```
Change 120087 on 2003/09/08 by dougd@dougd_r400_linux_marlboro

Fixed 2 bugs in Real Time address logic in aluconst.
Added correct default value for INST_BASE_VTX in sq_rbbm_interface.v
Fixed bug in Real Time write data buffer in sq_instruction_store.v
Added missing input/output declarations for SIMD2 & SIMD3 signals to sq_aluconst_top.v
Clean up missing SIMD2, SIMD3 wire declarations in sq.v for the aluconst, is and cfc

Change 119982 on 2003/09/08 by vromaker@vromaker_r400_linux_marlboro

added defaults to case statements

Change 119853 on 2003/09/06 by rramsey@rramsey_crayola_linux_orl

Changes to make quad processing resources programmable

Change 119747 on 2003/09/05 by danh@danh_crayola1_linux_orl

Removed SQ_SP_interp_mode, SQ_SP_interp_buff_swap, added all SPI Redundant SP
ports/connections.

Change 119736 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed SQ_SP_interp_mode, SQ_SP_interp_buff_swap, added SQ_SP_interp_simd_id for
Redundant SP

Change 119733 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed SQ_SP_interp_mode, added SQ_SP_interp_simd_id for Redundant SP capability.

Change 119457 on 2003/09/04 by dclifton@dclifton_r400

added sq_export_blocker to makefile
Fixed TP_SP_data_valid signal

Change 119422 on 2003/09/04 by mmang@mmang_crayola_linux_orl

removed vc_sp for now

Change 119294 on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro

- instatiation of sq export blocker at sq top level
- thread buffer timing fix related to status read/export count update

Change 119195 on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro

new file for arbitrating between exporting threads
```

```
Change 119127 on 2003/09/02 by dougd@dougd_r400_linux_marlboro

Added the extra memories and their support to the instruction and
constant stores to support 4 SIMD's. These memories and their
required wiring and control are instantiated with `ifdef and use
the SIMDn_PRESENT macros defined in header.v
Removed the use of SIMD1 macro.

Change 118878 on 2003/08/30 by rramsey@rramsey_crayola_linux_orl

fix a deadlock condition between the input arb and vtx input controller

Change 118743 on 2003/08/29 by viviana@viviana_crayola2_syn

Configuration file to build the virage memories with a register in the
   320x32 cfc memory.

Change 118694 on 2003/08/29 by rramsey@rramsey_crayola_linux_orl

changes for random backpressure

Change 118622 on 2003/08/28 by llefebvr@llefebvr_r400_emu_montreal

Modified the Orlando trackers to only compare valid channels. This replaces the
0xDEADDEAD values we had previously. Note that any uninitialized channel will generate
a tracker warning still.
 Modified interfaces are:

1) SX->SP parameter cache data
2) SP->SX
3) SX->RB

I left alone the SX->PA interface as we did not have problems over it. The qualifiers
are there however if anyone wants to do it.

Change 118589 on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro

- fix for loop index clamping and constant address generation (both index and offset
relative)
- changed the connection of the real time bit such that it now goes directly from the
AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass

Change 118581 on 2003/08/28 by dclifton@dclifton_r400

tied the upper bit of sq_tp_trk_simd_id low.
```

```
Change 118490 on 2003/08/28 by dclifton@dclifton_r400

Clean up of unused signals, fix of STAR signals in sp.v

Change 118397 on 2003/08/27 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 118215 on 2003/08/26 by vromaker@vromaker_r400_linux_marlboro

changed define for SQ_VC_MINI_MAXCOUNT from 16 to 32

Change 118200 on 2003/08/26 by rramsey@rramsey_crayola_linux_orl

Increase number of clks the tp_sq inject routine can loop through input data
Fix a problem with the sx_rb color tracker when the sx sends 0 mask quads, or
the rb kills quads

Change 118130 on 2003/08/26 by dclifton@dclifton_r400

Added tbtrk_sqvc, fixed vector engine assignments.

Change 118128 on 2003/08/26 by dclifton@dclifton_r400

Added definable # of simd's to sp.

Change 117957 on 2003/08/25 by dougd@dougd_r400_linux_marlboro

Fixed some wiring errors in the wrapper that prevented some counters from working.

Change 117706 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with
modifications to their test benches and added
    ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with
SIMD1_PRESENT macro in the SC files>

Change 117704 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<Fixed conflict between vec_3op_no_swap and scalar_const_op to control swizzle
correctly for the scalar engine and deliever the special gpr read  address  created in
the sq_ais_output block>

Change 117631 on 2003/08/21 by vromaker@vromaker_r400_linux_marlboro

- fix for VC_SQ_data_rdy (this was being asserted too often, but did not
         cause any of the tests to fail...)
```

```
Change 117627 on 2003/08/21 by vromaker@vromaker_r400_linux_marlboro

VC tracker added to tb_sqsp

Change 117504 on 2003/08/21 by mmang@mmang_crayola_linux_orl

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

Change 117311 on 2003/08/20 by rramsey@rramsey_crayola_linux_orl

Changes to sc for 4 qd/clk picker in KILL_ALL_PIXELS mode
Check in sc memory updates for Vivian
Add some missing connections in sqsp to fix compile warnings
Go to a global define for all trackers to control x vs 0 mismatch/warning
(MISMATCH_X_VS_0)

Change 116887 on 2003/08/18 by dougd@dougd_r400_linux_marlboro

restore the `ifdef USE_BEHAVE_MEM that was removed for
testing of virage behavioral models.

Change 116795 on 2003/08/15 by vromaker@vromaker_r400_linux_marlboro

adding sq-vc tracker (not debugged yet - just checking in working copy)

Change 116380 on 2003/08/13 by mmang@mmang_crayola_linux_orl

1.  Added separate gpr allocation/deallocation
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
```

```
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.

Change 116303 on 2003/08/13 by danh@danh_r400_win

Updated failing tests status.

Change 115781 on 2003/08/11 by rramsey@RRAMSEY_P4_r400_win

update sq status
add runtime column to report so it works with the spreadsheet script

Change 115728 on 2003/08/10 by rramsey@rramsey_crayola_linux_orl

Change SQ to hold off popping the RBBM skid fifo while map copies are in
progress. This fixes the problem where gfx_copy writes were being missed
if they were less than 8 clks apart.
Get rid of extra write into RBBM skid fifo for reads, and instead zero out
we and re out of fifo if it's empty. The fifo was overflowing if the filling
entry was a read, since one additional entry was getting pushed.
sx_sp_pcdata tracker now ignores 4f5eaddf (unwritten pc locations)
Fix a problem in the sqsp testbench that was causing rbbm writes to be dropped
if the sq exerted back pressure.

Change 115620 on 2003/08/08 by dougd@dougd_r400_linux_marlboro

1. change all hs virage memories & files to have subword size in name
2. added diagnostic write enable from rbbm interface register to the modules
   with extra memories to support multiple SIMDs

Change 115595 on 2003/08/08 by dougd@dougd_r400_linux_marlboro

fixed the path for the real time bit down the alu pipeline
to reach the constant and instruction stores.

Change 115581 on 2003/08/08 by rramsey@RRAMSEY_P4_r400_win

update sq status

Change 115492 on 2003/08/07 by mmang@mmang_crayola_linux_orl

change order of include paths for register_addr.v

Change 115430 on 2003/08/07 by danh@danh_r400_win

Updated status (lines 271-284).

Change 115426 on 2003/08/07 by dclifton@dclifton_r400
```

```
Added another block

Change 115274 on 2003/08/06 by smoss@smoss_crayola_win

monitor strange ncsim errors

Change 115254 on 2003/08/06 by smoss@smoss_crayola_win

fixing deaddead

Change 115241 on 2003/08/06 by dougd@dougd_r400_linux_marlboro

1. corrected the connections to sq_perfmon_wrapper to enable the
ALU active counters.

2. changed a few 1 bit vector declarations ( [0:0] ) to scalar
on SQ outputs because it caused errors in synthesis.

Change 115159 on 2003/08/06 by rramsey@rramsey_crayola_linux_orl

Change sq_alu_instr_seq so gpr_rd_en is not asserted when reading constants
Changes to thread_arb, ctl_flow_seq, and status_reg to get mem exports flowing

Change 115122 on 2003/08/06 by rramsey@RRAMSEY_P4_r400_win

Update with Aug6 sanity results and add a new worksheet that has failures sorted by
failure type

Change 115115 on 2003/08/06 by smoss@smoss_crayola_linux_orl_regress

   Randy's keeping me honest

Change 115114 on 2003/08/06 by rramsey@rramsey_crayola_linux_orl

add some missing dummy dump files

Change 115049 on 2003/08/05 by rramsey@RRAMSEY_P4_r400_win

Put some comments on all of the failing tests so we can try to bin the issues for
debugging

Change 115047 on 2003/08/05 by rramsey@rramsey_crayola_linux_orl

Add register to hold pipe disable bits to tb_sqsp
Hook sx instance up to correct set of RBBM signals in tb_sqsp
Increase depth of sc state avail fifo since some events need
to go through that path
```

```
        Change sx pa tracker to always opens its files so it doesn't
        cause hangs when the files are empty
        Add deaddead and a selectable x_vs_0 mismatch disable (reports
        a warning rather than a mismatch) to tbtrk_sx_rb.v

Change 114774 on 2003/08/04 by rramsey@RRAMSEY_P4_r400_win

update sqspsx status

Change 114706 on 2003/08/04 by danh@danh_r400_win

Updated r400sq_* status.

Change 114427 on 2003/08/01 by smoss@smoss_crayola_linux_orl_regress

   added rb_sx dump

Change 114404 on 2003/08/01 by amys@amys_r400_regress_linux

changes made to fix running ncsim using Orlando trackers

Change 114305 on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

Change 114167 on 2003/07/31 by danh@danh_r400_win

Updated the r400sq_* status.

Change 114159 on 2003/07/31 by rramsey@RRAMSEY_P4_r400_win

update status. remove some CP tests that don't anything at sqsp.

Change 113990 on 2003/07/30 by rramsey@rramsey_crayola_linux_orl

Changes to support real time prims.
Tests that draw rt only now drive sc inputs
RBBM stream is held off while each rt prim processes so
rt code/const/params are not clobbered

Change 113953 on 2003/07/30 by danh@danh_r400_win

Updated r400sq_* status.

Change 113550 on 2003/07/28 by dougd@dougd_r400_linux_marlboro
```

```
added define+virage_ignore_read_addx to support virage behavoral models

Change 113548 on 2003/07/28 by dougd@dougd_r400_linux_marlboro

Added missing register stage in memory address path that caused
memory  failures only with the virage behavoral model.

Change 113503 on 2003/07/28 by rramsey@RRAMSEY_P4_r400_win

update sq stats

Change 113302 on 2003/07/25 by danh@danh_r400_win

Updated r400sq_* status.

Change 113293 on 2003/07/25 by rramsey@RRAMSEY_P4_r400_win

update sq status

Change 113286 on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

Change 113223 on 2003/07/25 by rramsey@rramsey_crayola_linux_orl

uncomment driver for SQ_SP_interp_xyline

Change 113207 on 2003/07/25 by danh@danh_r400_win

Updated the r400sq_* status.

Change 113039 on 2003/07/24 by danh@danh_crayola1_linux_orl

Changed src_c_const_addr_rel generation so it matches the emulator code.

Change 112899 on 2003/07/24 by danh@danh_crayola1_linux_orl

Changed src_c_const_addr_rel generation.

Change 112882 on 2003/07/24 by rramsey@RRAMSEY_P4_r400_win

update sqspsx status

Change 112600 on 2003/07/23 by rramsey@rramsey_crayola_linux_orl

Change sx-rb trackers so they always open their files at time 0,
that way they don't cause hangs for tests that don't hit any quads
```

```
Hook up the real pixel mask in the sx_rb color tracker

Change 112375 on 2003/07/22 by vromaker@vromaker_r400_linux_marlboro

- fixed VC interface counter

Change 112335 on 2003/07/22 by danh@danh_r400_win

Updated the r400sq* status.

Change 112289 on 2003/07/22 by dclifton@dclifton_r400

Updated staging registers in sp_macc.
Revised sp_scalar_lut.
Test signals connected.

Change 112108 on 2003/07/21 by rramsey@RRAMSEY_P4_r400_win

update with 07/21 status and some comments on the failing tests

Change 112073 on 2003/07/21 by vromaker@vromaker_r400_linux_marlboro

- fix for SQ_VC interface
- TP_SQ_dec was hooked up to the interface counter
- timing fix in vtx thread buffer
- simd_num connected thru ptr buff and pix ctl to pix thread buff
- performance fix in pix ctl

Change 112034 on 2003/07/19 by rramsey@rramsey_crayola_linux_orl

Change vcs build script so cover is off by default
Get rid of some compile warnings in tb_sqsp
Change sx_rb color tracker so it doesn't use the sx_rb_quad dump
to get pixel masks

Change 111986 on 2003/07/18 by dougd@dougd_r400_linux_marlboro

Added dummy mems for all virage memorie that didn't already have them.
Moved memory data output register in sq_cfc.v into the memory and dummy memory.
Replaced all virage memories, etc. to get the memory needed for sq_cfc.v

Change 111905 on 2003/07/18 by ygiang@ygiang_r400_pv2_marlboro

added: new perf counters for sq hardware

Change 111807 on 2003/07/18 by mmantor@mmantor_crayola_linux_orl

<added new dummy file for test cases that needed it>
```

```
Change 111736 on 2003/07/17 by mmang@mmang_crayola_linux_orl

Added sp->sx export arbitration between multiple simd engines.
Added register after instr_start OR of multiple simd engines by
taking unregistered signal out of sq_ais_output.

Change 111732 on 2003/07/17 by rramsey@RRAMSEY_P4_r400_win

Update with regression results, plus a couple of my own

Change 111726 on 2003/07/17 by smoss@smoss_crayola_linux_orl_regress

   modified $value$plusargs to keep cadence happy

Change 111692 on 2003/07/17 by danh@danh_r400_win

Updated the r400sq* status.

Change 111650 on 2003/07/17 by rramsey@rramsey_crayola_linux_orl

Add pasx done to testbench timeout logic

Change 111628 on 2003/07/17 by smoss@smoss_crayola_linux_orl_regress

   changed tbmod_fake_pa for ncsim because all requests weren't occurring this was also
true for vcs but sim was passing.  changed buildt for nc to not run a sim after a
compile

Change 111612 on 2003/07/17 by moev@moev2_r400_linux_marlboro

Clean up files no longer used by the verification flow

Change 111603 on 2003/07/17 by moev@moev2_r400_linux_marlboro

SQ changes to test Virage's HS memories.

Change 111419 on 2003/07/16 by rramsey@rramsey_crayola_linux_orl

Connect TST_awt_enable to vc_skid_buf and wire it up to the top level

Change 111381 on 2003/07/16 by rramsey@rramsey_crayola_linux_orl

Fix compile result check in buildtb
Tie off sx related done signals when the sx is not there
and spit them out if it is there and the tb hangs
Don't source sx_sp_pcdata stimulus when using live sx
Remove extra ifdef
```

Change 111353 on 2003/07/16 by bhankins@bhankins_crayola_linux_orl

when the sx is present, include the sx trackers in on the decision to stop the simulation

Change 111345 on 2003/07/16 by rramsey@RRAMSEY_P4_r400_win

Fix the update script to handle 'run time' being reported
Redo the last status update to the spreadsheet since 'run time'
caused all the fields to get shifted

Change 111342 on 2003/07/16 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 111317 on 2003/07/15 by mmang@mmang_crayola_linux_orl

Blocking/non-blocking fix found by synthesis.

Change 111305 on 2003/07/15 by smoss@smoss_crayola_win

update

Change 111303 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

allow pa/sx requests before the rbbm file is empty

Change 111280 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

need to wait for vc_done if serialize and vc_pending

Change 111275 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

add SX_BLOCK_SIM so the sx trackers know where they are running

Change 111132 on 2003/07/15 by smoss@smoss_crayola_linux_orl

   just copying randy

Change 111123 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

had a typo in the vc_pending logic

Change 111107 on 2003/07/15 by smoss@smoss_crayola_linux_orl

   updated

```
Change 111093 on 2003/07/15 by smoss@smoss_crayola_linux_orl

   decapitating tb_sc

Change 111008 on 2003/07/14 by dougd@dougd_r400_linux_marlboro

added logic to support programmable memory size for texconst and
aluconst stores.

Change 110899 on 2003/07/14 by rramsey@rramsey_crayola_linux_orl

change tp/vc pending bits so they look at tgt_instr_str_vc_q bits to
determine what type of fetch is being issued

Change 110886 on 2003/07/14 by rramsey@rramsey_crayola_linux_orl

mask off serial bit for first instruction of a clause.
this change fixes e2blit_src_8888 and probably some other hanging
e2/cp tests

Change 110884 on 2003/07/14 by rramsey@RRAMSEY_P4_r400_win

update with latest regression results

Change 110880 on 2003/07/14 by rramsey@rramsey_crayola_linux_orl

Add back in a signal declaration to fix the no SX build
Move some signals to the other half of a REMOVE_SX ifdef

Change 110669 on 2003/07/12 by smoss@smoss_crayola_linux_orl_regress

   removed errant else

Change 110640 on 2003/07/12 by mmantor@mmantor_crayola_linux_orl

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
```

```
    >

Change 110512 on 2003/07/11 by mmang@mmang_crayola_linux_orl

Fix for Vivian for synthesis in loop i07 and i15.

Change 110467 on 2003/07/11 by llefebvr@llefebvr_r400_emu_montreal

Disabling the COND_EXEC_PRED optimization. a COND_EXEC_PRED in the SQ is now threated
like a regular EXEC. We can re-enable this optimization in the future by putting the
thread back to the RS BEFORE making the predicate compare because now we are comapring
a dirty predicate bit set and it causes corruptions. This fixes mova_test.cpp
TEST_CASE=pMova_const.

Change 110451 on 2003/07/11 by dclifton@dclifton_r400

Fixed typo for spi ram compile

Change 110401 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed the sq/vc 103 memory to 104.

Change 110310 on 2003/07/10 by viviana@viviana_crayola2_syn

Changed the vc memory to 104 bits wide, deleted the 103 memory and rebuilt all
   memories with latest version of virage.

Change 110177 on 2003/07/10 by rramsey@rramsey_crayola_linux_orl

Changes to get simd_id piped down the vertex side and into the thread
buffer. Also only write the active simd's gprs and mux pipe_disable bits.
The memory in sq_vc_skid_buf increased by 1 bit, so this will require
a new memory to be checked in before running without USE_BEHAVE_MEM.

Change 110083 on 2003/07/09 by dougd@dougd_r400_linux_marlboro

added data output mux to select between the two memories (SIMD1, SIMD0)
for RBBM diagnostic reads. The mux is controlled by a rbbm register bit
in the SQ_DEBUG_MISC register.

Change 110066 on 2003/07/09 by vromaker@vromaker_r400_linux_marlboro

- fixed a bug in tex instr seq related to back-to-back constant reads

Change 110035 on 2003/07/09 by moev@moev2_r400_linux_marlboro

Changed the HS Star Processor connections to match the clients. In particular BiraFail
& Err_pip_or
```

```
Change 109951 on 2003/07/09 by llefebvr@llefebvr_r400_emu_montreal

Fixing yet another mova problem when the mova is not back to back with it's use and
there is only one waterfall pass, PVPS detection wasn't re-enabled correctly. Fixes
mova_tests.cpp TEST_CASE=mova512_nop_check

Change 109814 on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro

- contains RT bit connection from pix input ctl to pix thread buff
- added SQ_TP_simd_id output to top level

Change 109777 on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro


Change 109679 on 2003/07/08 by llefebvr@llefebvr_r400_emu_montreal

Fixed r400sp_mova_tests.cpp TEST_CASE=mova512.

The PVPS detection was rightly disabled during the waterfall but wasn't re-enabled for
the following instructions of the clause. I used the waterfall_done signal to re-enable
the PVPS detection after the waterfalling.

Change 109671 on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro

- updated tex instr seq to sync to the texconst phase
- changed fetch arb to output both the mega grant and the mini
         grant to the tex instr seq

Change 109590 on 2003/07/07 by viviana@viviana_crayola2_syn

Corrected another non-blocking assignment to blocking in a combinational logic block.

Change 109565 on 2003/07/07 by viviana@viviana_crayola2_syn

Corrected non-blocking assignments to blocking in combinational block.

Change 109466 on 2003/07/07 by dougd@dougd_r400_linux_marlboro

fixed error in bit width of ais_real_time

Change 109126 on 2003/07/03 by dougd@dougd_r400_linux_marlboro

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

Change 109043 on 2003/07/03 by vromaker@vromaker_r400_linux_marlboro
```

```
made all loop counter variables unique for sythesis

Change 108947 on 2003/07/02 by dclifton@dclifton_r400

Updated makefile for latest changes.  Fixed testbench test signals into SP and SPI.

Change 108763 on 2003/07/01 by llefebvr@llefebvr_r400_emu_montreal

Updates for r400sq_const_index_0x.cpp

Change 108760 on 2003/07/01 by llefebvr@llefebvr_r400_linux_marlboro

Fixed r400sq_const_index_03.cpp. Now works on the SQSP testbench. Still has issues on
the GC because of bad ferret/cp ring buffer synchronization.

Fixed:

1) Bad clamping of the address register in the SP
2) Bad error handling of an out of range address in the SQ.

Change 108744 on 2003/07/01 by vromaker@vromaker_r400_linux_marlboro

- registered winner_ack out of thread arb for timing
- connected correct instruction store read output based on SIMD1
  for VC ctl flow instruction reads; now SQ_VC interface appears to
  be driven correctly
- minor change to tb_sqsp (commented out random stall for TP_SQ_fetch
  stall, which no longer exists)

Change 108676 on 2003/07/01 by dougd@dougd_r400_linux_marlboro

generated trigger signals for SIMD0,SIMD1 perfmon counters

Change 108585 on 2003/06/30 by rramsey@rramsey_crayola_linux_orl

hook up the sx_rb_quad_mask signals to the fake_rb's
not sure how this was working at all with the live SX

Change 108536 on 2003/06/30 by smoss@smoss_crayola_linux_orl_regress

   removed rand function warning

Change 108524 on 2003/06/30 by dougd@dougd_r400_linux_marlboro

generate read enable for sq_hs_sms_sq_shsd1_320x96cm4 in sq_texconst_mem
and read enable for sq_stdrfsdks2p64x32cm4sw0 in sq_texconst_rams
```

```
Change 108511 on 2003/06/30 by rramsey@rramsey_crayola_linux_orl

changes for new sp top level

Change 108315 on 2003/06/27 by mmang@mmang_crayola_linux_orl

Qualify constant address register write using constant waterfalling mask

Change 108250 on 2003/06/27 by rramsey@rramsey_crayola_linux_orl

left some signals out of a sensitivity list

Change 108222 on 2003/06/27 by smoss@smoss_crayola_linux_orl_regress

   I have too many i's

Change 108208 on 2003/06/26 by dclifton@dclifton_r400

Changes to get the tb_sqsp to work in modelsim

Change 108188 on 2003/06/26 by mmang@mmang_crayola_linux_orl

For pixel quads, enable all pixels of a quad when any pixel is hit
for gpr write enables and constant address waterfalling sequencing.
Another update will fix constant address register writing.

Change 108140 on 2003/06/26 by rramsey@rramsey_crayola_linux_orl

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

Change 108063 on 2003/06/26 by viviana@viviana_crayola2_syn

Regenerated the high speed memories to add two instances of the 1280x128 and two
```

```
instances of the
   4096x96.

Change 108024 on 2003/06/26 by mmantor@FL_mmantorLT_r400_win

remove template file having problems in ncverilog

Change 107822 on 2003/06/25 by rramsey@RRAMSEY_P4_r400_win

and another syntax error

Change 107820 on 2003/06/25 by rramsey@RRAMSEY_P4_r400_win

fix decimal vs hex problem

Change 107817 on 2003/06/25 by fhsien@fhsien_r400_LT

correct syntax error

Change 107801 on 2003/06/25 by grayc@grayc_crayola2_linux_orl

   fix syntax

Change 107757 on 2003/06/25 by mmantor@mmantor_crayola_linux_orl

< 1. sq_alu_instr_seq.v  - Use the Queue pop signal to qualify last_in_clause
        and last_in_shader out of the queue.
     2. sq_target_instr_fetch.v  - Fixed a buf in the the target_instruct_fetch
        write to the queue to prevent dropping last_in_shader and last_in_clause
        if the queue is full when first trying to send instruction.  >

Change 107717 on 2003/06/24 by mmantor@mmantor_crayola_linux_orl

<added new regression test for cyl_wrap and changed vcs for texconst mem and fixed wrap
bug in controller during interpolation and added a dum mem config for the texconst
memory  >

Change 107579 on 2003/06/24 by dougd@dougd_r400_linux_marlboro

ncverilog will error with
output [0:0] SQ_SP_instruct_start
wire  SQ_SP_instruct_start
because it considers the 1st declaration a vector and
the 2nd one a scalar.

Change 107389 on 2003/06/22 by mmang@mmang_crayola_linux_orl

1.  made change sp_vector.v to grab pred/kill results
```

```
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

Change 107266 on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro

reverted a change that was made for VC testing (and that did not work correctly)

Change 107174 on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro

- swapped PS and ID gpr write phases

Change 107015 on 2003/06/19 by viviana@viviana_crayola2_syn

Re-ran cover on the high speed memories to add fuse_box318 files previously deleted.
   Also deleted fuse_box29 files no longer used.

Change 107009 on 2003/06/19 by smoss@smoss_crayola_linux_orl_regress

   update
```

```
Change 106949 on 2003/06/19 by smoss@smoss_crayola_linux_orl_regress

   removed sq_tp_stall signal in anticipation of new sq_tp interface

Change 106751 on 2003/06/18 by danh@danh_r400_win

Updated r400sq_* status.

Change 106611 on 2003/06/17 by danh@danh_crayola1_linux_orl

 Changed the cfs_return_addrs_q[51:0] generation so the correct cfs_return_addr[3:0]_q
order
 will be written into the thread buffer CFS mem when a thread is returned to the thread
buffer.

Change 106597 on 2003/06/17 by rramsey@RRAMSEY_P4_r400_win

more status

Change 106528 on 2003/06/17 by rramsey@rramsey_crayola_linux_orl

hook up iterator_SP_cntx0 so realtime works correctly

Change 106375 on 2003/06/16 by danh@danh_r400_win

Updated the r400sq* status.

Change 106357 on 2003/06/16 by rramsey@rramsey_crayola_linux_orl

fix latency of tp/sp signals in tb_sqsp after tp_formatter change
clean up the fetch swizzle warning msg in tb_sqsp
add new memory to sq/tb.f
fix fech_swizzle signal width in tex_instr_seq

Change 106293 on 2003/06/16 by vromaker@vromaker_r400_linux_marlboro

code fix to prevent latches

Change 106277 on 2003/06/16 by viviana@viviana_crayola2_syn

Extra bit added to pixel state data.

Change 106273 on 2003/06/16 by danh@danh_crayola1_linux_orl

Changed TB_TP_REQ_FIFO_DEPTH (128 to 256) & TB_TP_REQ_FIFO_ADDR_WIDTH (7 to 8) to
resolve fifo overflow.
```

```
Change 106191 on 2003/06/14 by viviana@viviana_crayola2_syn

48x154 memory changed to 48x155.

Change 106190 on 2003/06/14 by viviana@viviana_crayola2_syn

Changed the width of the state memory to 155 bits.

Change 106078 on 2003/06/13 by rramsey@RRAMSEY_P4_r400_win

more status updates

Change 105982 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

advance sq-sx control signals by one clock to solve sx timing issues
   add support for updated sx hierarchy

Change 105943 on 2003/06/12 by dougd@dougd_r400_linux_marlboro

Added a 2nd write buffer to aluconst, texconst and instruction store to handle
real time writes from cp mixed with non real time writes. This code passes the
mini-regress on tb_sqsp and cp_lcc_tex, cp_lcc_alu, cp_im_load_basic on the gc
testbench but fails cp_lcc_tex_rt and cp_lcc_alu_rt. It appears work for non-realtime.

Added real time prim bit from pix_ctl to ISM in pix_thread_buff when loading a
pixel thread. This bit will allow reading real time constants from the constant stores.

Added VC_wake_up logic.

Change 105924 on 2003/06/12 by vromaker@vromaker_r400_linux_marlboro

timing fixes

Change 105914 on 2003/06/12 by danh@danh_r400_win

Updated r400cl* status.

Change 105891 on 2003/06/12 by rramsey@RRAMSEY_P4_r400_win

more status updates

Change 105889 on 2003/06/12 by danh@danh_crayola1_linux_orl

Changed the "pix: check for buf avail and export count < 16" section of the alu_req
generation,
       added parentheses around the alloc_size_q & sx_buf_avail logic.

Change 105811 on 2003/06/12 by rramsey@rramsey_crayola_linux_orl
```

```
update spsx tracker so msg signal names match the rtl signal names
fix a typo in a pix_rs_input msg

Change 105809 on 2003/06/12 by rramsey@rramsey_crayola_linux_orl

some of the compares had not been updated with the new
vc field in the dump file

Change 105784 on 2003/06/12 by rramsey@rramsey_crayola_linux_orl

fix width of num_params_q

Change 105770 on 2003/06/12 by rramsey@RRAMSEY_P4_r400_win

picking more tests, adding comments to tests with known issues

Change 105750 on 2003/06/12 by smoss@smoss_crayola_linux_orl_regress

   removed sq_sp_simdl_instruct_start to coincide with @105565

Change 105592 on 2003/06/11 by llefebvr@llefebvr_r400_linux_marlboro

Added storage element in the SQ to store the valid addresses of the mova so that they
can de restored at any instruction that uses the address register. The way it was
currently would only work if the use of the address was directly following the MOVA
instruction. This fixes r400sq_const_index_02.cpp.

Change 105537 on 2003/06/11 by vromaker@vromaker_r400_linux_marlboro

- added sq_fetch_arb to and removed sq_thread_buff_cntl from system_sq.vcpp
- made a timing fix to gpr alloc

Change 105525 on 2003/06/11 by rramsey@RRAMSEY_P4_r400_win

picking more tests

Change 105465 on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

Change 105457 on 2003/06/10 by danh@danh_r400_win
```

```
Made changes in regards to my simulation results.

Change 105437 on 2003/06/10 by rramsey@RRAMSEY_P4_r400_win

picking some tests to debug

Change 105417 on 2003/06/10 by rramsey@RRAMSEY_P4_r400_win

update status for jun 9 regression

Change 105283 on 2003/06/10 by llefebvr@llefebvr_r400_linux_marlboro

I have added the write enables to qualify the data sent to the SX. This is needed when
doing predicated exports or constant waterfalling on exports. This fixed
r400sq_const_index_01.cpp test.

Change 105277 on 2003/06/10 by dougd@dougd_r400_linux_marlboro

added output VC_clk_en to sq_rbbm_interface.v and wired it to
SQ_VC_wake_up in sq.v

Change 105052 on 2003/06/09 by smoss@smoss_crayola_linux_orl_regress

   a few cadence related changes
   1) moved rbbm_event_type to occur after the read of rbbm_re
   2) temporarily disabled randomization on the clock for the tb_sqsp dump file

Change 104848 on 2003/06/08 by grayc@grayc_crayola2_linux_orl

   fix simd1_valid -> simd1_const_valid

Change 104797 on 2003/06/07 by grayc@grayc_crayola2_linux_orl

   add VC ports
   modify SP-SQ port names

Change 104715 on 2003/06/06 by danh@danh_r400_win

Updated per simulation results.

Change 104661 on 2003/06/06 by dougd@dougd_r400_linux_marlboro

fixed typo

Change 104616 on 2003/06/06 by llefebvr@llefebvr_r400_linux_marlboro

HW was clamping to 0 on a GPR addressing error. It should clamp to GPR_base of the
shader.
```

```
Change 104600 on 2003/06/06 by dougd@dougd_r400_linux_marlboro

added missing case value that was causing synopsys to infer latches

Change 104555 on 2003/06/06 by danh@danh_r400_win

Made changes per simulation results.

Change 104554 on 2003/06/06 by dougd@dougd_r400_linux_marlboro

fixed typo -
d_rd0_addr was assigned in two process blocks
and d_rd1_addr was not being assigned at all.

Change 104302 on 2003/06/05 by ashishs@fl_ashishs_r400_win

upadted the script since it was just fetching data till 4000 rows. Now it will fetch
data till 10000 rows (break after it finds null rows) and then sort them
accordingly....

Change 104261 on 2003/06/05 by rramsey@rramsey_crayola_linux_orl

Fix some wiring issues in tb_sqsp
Add warning msg to tb_sqsp to tell when a test is trying to swizzle
fetch addresses since this is not supported yet in the SP
(didn't make it a failure since some tests are passing with swizzle
-- they must have the same value in all channels)
Fix predicate compare in pix_rs_input tracker
fetch_swizzle bit of instr needed to be muxed based on thread_type
in sqtp tracker

Change 104211 on 2003/06/05 by rramsey@RRAMSEY_P4_r400_win

status from 6_4_2003

Change 104159 on 2003/06/04 by danh@danh_crayola1_linux_orl

Changed count_match[3:0] generation, when param_gen_cycle is high all count_match[3:0]
bits will now go high.

Change 104139 on 2003/06/04 by rramsey@rramsey_crayola_linux_orl

turn off debug print for this one too

Change 104076 on 2003/06/04 by dougd@dougd_r400_linux_marlboro

fixed bug in the loading of the write data buffer.
```

```
Change 104075 on 2003/06/04 by dclifton@dclifton_r400

added test controller

Change 104046 on 2003/06/04 by smoss@smoss_crayola_linux_orl_regress

   removed print statements

Change 104031 on 2003/06/04 by rramsey@rramsey_crayola_linux_orl

Fix trackers so they actually compare, and compare the correct data

Change 104026 on 2003/06/04 by rramsey@RRAMSEY_P4_r400_win

update makefile with spi block, memory changes, etc

Change 103932 on 2003/06/03 by mmantor@mmantor_crayola_linux_orl

   update for new pipe disable routing

Change 103931 on 2003/06/03 by danh@danh_r400_win

Updated per simulation results.

Change 103849 on 2003/06/03 by rramsey@rramsey_crayola_linux_orl

Fix a bug in sq_input_arb that was allowing the state machine to go
to IDLE even though a pixel thread was active. This could allow a vtx
and pix thread to try and write into the GPRs at the same time.
Turn tex ctlflow trackers back on in tb_sqsp
Fix TP_SP_data_valid connections in tb_sqsp
Modify alu ctlflow trackers so they can skip over expected instr
with serialize bits set if the rtl does not serialize them

Change 103379 on 2003/05/30 by danh@danh_r400_win

updated per simulation results.

Change 103369 on 2003/05/30 by vromaker@vromaker_r400_linux_marlboro

- fix for width mismatch on thread_id input of vtx TB status regs
- initial pass of VC/TP fetch arbiter (not instantiated in sq.v yet)

Change 103365 on 2003/05/30 by dougd@dougd_r400_linux_marlboro

Added missing wire declaration for param_wrap_0_set
```

```
Change 103256 on 2003/05/30 by dougd@dougd_r400_linux_marlboro

fixed bug in wrapping logic for rtn_ptr, read_ptr and stop_ptr for addressing the
mapping table address freelist

Change 103204 on 2003/05/29 by dougd@dougd_r400_linux_marlboro

initial submit of a submodule to count and bin pixels for perfmon

Change 103141 on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

Change 103074 on 2003/05/29 by viviana@viviana_crayola2_syn

Added a `include of sq_reg.v for synthesis purposes.

Change 102924 on 2003/05/28 by viviana@viviana_crayola2_syn

Added an additional 48x170 and 16x170 and rebuilt the memories.

Change 102411 on 2003/05/23 by dougd@dougd_r400_linux_marlboro

Simulation only protocol checking logic was moved to a clock process block
to prevent a difference in order of evaluation between vcs and ncverilog
from causing a false error assertion due to a race condition in simulation.

Change 102365 on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro

moved wire declaration of sx_exp_buff_full_0 (and others) before the
instantiation of the status registers to fix ncverilog warning

Change 102264 on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro

- updated pix thread buffer for simd1 (and removed ctl sub module and redundant logic)
- renamed state_read_phase to arb_phase
- fixed CFSM serialize detection (had to add case of fetch initiated by current clause)
- removed reference to sq_thread_buff_cntl in tracker

Change 102193 on 2003/05/22 by danh@danh_r400_win

updated per simulation results.

Change 102154 on 2003/05/22 by rramsey@RRAMSEY_P4_r400_win
```

```
Update with 5/17/03 status

Change 102095 on 2003/05/22 by dougd@dougd_r400_linux_marlboro

Added the following new fields to control registers in the rbbm interface:
 SQ_CONTEXT_MISC_PERFCOUNTER_REF
 SQ_CONTEXT_MISC_YEILD_OPTIMIZE
 SQ_FLOW_CONTROL_VC_ARBITRATION_POLICY
 SQ_FLOW_CONTROL_SIMD1_DISABLE
 SQ_DEBUG_MISC_DB_READ_MEMORY

Change 102052 on 2003/05/22 by danh@danh_crayola1_linux_orl

instr_ptr and instr_ptr_q are now only compared when event_vld_q is low.

Change 102042 on 2003/05/22 by danh@danh_r400_win

updated per simulation results.

Change 102039 on 2003/05/22 by dougd@dougd_r400_linux_marlboro

restored the missing line ".pb_event_state(pb_event_state)," to the instantiation of
sq_export_alloc in sq.v that somehow was removed when a merge was done in the last
submit

Change 102013 on 2003/05/21 by danh@danh_r400_win

Made changes per the simulations I ran today.

Change 101908 on 2003/05/21 by mmang@mmang_crayola_linux_orl

Fixed bug in waterfalling by grabbing register input of done_bits
instead of registered value when performing init_done_bits operation.

Change 101906 on 2003/05/21 by dougd@dougd_r400_linux_marlboro

added a 2nd read port for VC to texconst and redesigned sq_texconst_wrt_buff to perform
opportunistic writes because the write access slot was given up for VC reads

Change 101883 on 2003/05/21 by rramsey@rramsey_crayola_linux_orl

fix pc write addr generation in ais_output
fix cf state machine so unexecuted conditionals don't cause a thread
to end
turn off cf trackers for now
fix a problem in the test bench related to draw pkts with no draw inits
(some cp tests do this)
```

```
Change 101881 on 2003/05/21 by danh@danh_crayola1_linux_orl

Changed PB_READ_3 state, it now uses pi_interp_cnt_q instead of interp_cnt_q.

Change 101841 on 2003/05/20 by askende@askende_r400_linux_marlboro

checking in the interpolator control latency changes in SQ and SP.

Change 101642 on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
  fetch, instr que, and instr seq modules, and ais_output for simd1
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed

Change 101575 on 2003/05/19 by smoss@smoss_crayola_linux_orl_regress

   changed delay on tp_sp signals

Change 101378 on 2003/05/16 by smoss@smoss_crayola_linux_orl_regress

   added field for TP_SP_rf_expand_enable

Change 101314 on 2003/05/16 by moev@moev_r400_linux_marlboro

updates

Change 101168 on 2003/05/15 by rramsey@rramsey_crayola_linux_orl

fix a problem with my param cache allocate fix and fill the hole
in our spsx tracker that let the problem slip through my regressions
(pc write addr was not being checked)

Change 101103 on 2003/05/14 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 101064 on 2003/05/14 by danh@danh_r400_win

Updated fields in regards to my simulation results.

Change 101009 on 2003/05/14 by rramsey@rramsey_crayola_linux_orl
```

```
Changes for parameter cache deallocation. Need to multiply dealloc
count by (vs_export_count +1) so the correct number of lines are
freed.

Change 100885 on 2003/05/14 by rramsey@RRAMSEY_P4_r400_win

update validation report

Change 100881 on 2003/05/14 by danh@danh_r400_win

Changed the lines of the simulations that I have run.

Change 100877 on 2003/05/14 by rramsey@rramsey_crayola_linux_orl

Fix 3 issues related to parameter cache allocation/deallocation
  1) Move allocate subtract for pc_free_cnt so it happens when
     an allocating vtx thread wins arbitration instead of when
     the thread is sent to the CFS. This puts the arbitration/
     allocate path at four clks (from six) so we can correctly
     allocate every four clocks.
  2) Deallocs were being dropped in sq_ptr_buff on back to back
     row transfers if the first of the pair was the last row
     (end of buffer) and the second of the pair had dealloc.
  3) Deallocs need to be accumulated in sq_ptr_buff since multiple
     row transfers of a pixel vector can be marked with dealloc
     and the deallocs are put in the event fifo at end_of_buffer.

Clean up some duplicate code in tb_sqsp and set the default dump
level back to 1 (instead of 3).

Change 100801 on 2003/05/13 by dougd@dougd_r400_linux_marlboro

corrected port width mismatches in sq_aluconst_top; removed unused input and output
from sq_const_map_cntl and in it's instantiations in sq_aluconst_top and
sq_texconst_top

Change 100795 on 2003/05/13 by dougd@dougd_r400_linux_marlboro

corrected signal names to b1 ports of sq_cfc

Change 100748 on 2003/05/13 by danh@danh_crayola1_linux_orl

instr_ptr and instr_ptr_q are now only compared when event_vld_q is low.

Change 100631 on 2003/05/13 by dougd@dougd_r400_linux_marlboro

Added `define SIMD1 to header.v and corrected connections for SIMD1 in sq.v
```

```
Change 100629 on 2003/05/13 by rramsey@rramsey_crayola_linux_orl

Update tb_sqsp for latest SP top level changes
Zero out rbbm fifo data when writing for re_dly
Add a couple of missing wire declarations to sq

Change 100468 on 2003/05/12 by dougd@dougd_r400_linux_marlboro

removed incorrect bit width assignments to eo_rt_aluconst and eo_rt_texconst to prevent
compile errors with ncverilog

Change 100453 on 2003/05/12 by rramsey@rramsey_crayola_linux_orl

Update for top level sp changes

Change 100310 on 2003/05/10 by smoss@smoss_crayola_linux_orl_regress

   ncsim for sqsp and sx

Change 100167 on 2003/05/09 by rramsey@RRAMSEY_P4_r400_win

Updating status

Change 100164 on 2003/05/09 by dougd@dougd_r400_linux_marlboro

ifdef'd connections in sq.v to sq_aluconst_top.v for the extra SIMD1 memory

Change 100154 on 2003/05/09 by rramsey@rramsey_crayola_linux_orl

Changes for instruction store addressing (wrapping and absolute)
  Add absolute addressing for cf and exec addresses to cfs
  Add wrapping for jumps and calls to cfs
  Add wrapping for execute addresses to cfs
  Fix wrapping in instr_fetch (vtx wrap at pix_base-1)

These changes fix cp_event_timestamp_instruction_loading_stall at tb_sqsp

Change 100118 on 2003/05/09 by dougd@dougd_r400_linux_marlboro

added 2nd memory to sq_cfc to support SIMD1 and ifdef'd the connections in sq_cfc and
sq.v

Change 100015 on 2003/05/08 by mmantor@mmantor_crayola_linux_orl

<sq_ais_output - re-ordered kill_mask going to the sx so bits flow in order msb->lsg
sp2(v3-v0)sp0(v3-v0)) to match exp_mask
                  - removed improper final update of kill mask with predication mask
```

```
                - enable export_mask for all exports
    SX_PA_interfaces.v - fixed checker for back to back transfers
    SX_RB_interfaces.v - hooked up to 7 bit sx_rb_index and rb_sx_index instead of
incorrect 8 bits
    sx.v - changed interfaces for sx_rb and rb_sx interfaces to become 7 bits instead
of 8 bits
    tb_sx.v - changed sx inputs to be 7 bits instead of 8 bits on the above index
interfaces
    tbmod_fake_sp.v - reordered the kill mask and enabled channel mask for exports
    sx_export_buffers.v - moved register after export mems and only load when memory
read, mimized client read muxes added input rotate muxes for export to memory
operations and indivual write address for each memory and set up predication,
kill_mask, alpha kill,and channel mask in the determination of writing data into the
export buffers
    sx_export_control.v - removed dead clock on rb and pa data fetch interface and
client and made arbiter behave as round robin and removed unecessary second input
register, added support for z render targets and multiple render targets and clean up
items
    ex_export_alloc_dealloc.v - enabled channel mask, kill mask, export_mask, and apha
test conditioning of valid bitsa doubled the free rate>

Change 99918 on 2003/05/08 by dougd@dougd_r400_linux_marlboro

fixed typo

Change 99912 on 2003/05/08 by dougd@dougd_r400_linux_marlboro

doubled the instruction store memory, changed the access allocation to accomdate SIMD1
and VC, and `ifdef'd the connections for SIMD1 in sq.v

Change 99520 on 2003/05/07 by mmang@mmang_crayola_linux_orl

Bug occurred where first_in_clause was getting lost when instr_queue
was full.  Previously, internal first_in_clause register was cleared
with tif_rts.  Had to delay clearing to tif_rts & tiq_rtr.

Change 99346 on 2003/05/06 by mmang@mmang_crayola_linux_orl

Fixed bug (I created) related to initializing the constant address
register valids at the beginning of a clause.  I used ais_init_pred
which in some cases was too late.  Created new ais_init_const_addr
that is 3 clocks sooner.

Change 99315 on 2003/05/06 by vromaker@vromaker_r400_linux_marlboro

fixed typos that were causing cp_e2polyscanlines_simple to fail

Change 99123 on 2003/05/05 by rramsey@rramsey_crayola_linux_orl
```

```
Add some control to hold off inputs at vs/ps done events
Increase utb_tp_req_fifo depth
Change writes into vtx/pix done fifos so they only happen on the first
draw_init for a context

Change 99043 on 2003/05/05 by vromaker@vromaker_r400_linux_marlboro

- added VC ctl flow seq, instr fetch, instr que and instr seq, and top level IOs
- made some leda fixes
- added non time multiplexed gpr write address output to VC and TP (gpr_dst_addr[6:0])

Change 99041 on 2003/05/05 by rramsey@RRAMSEY_P4_r400_win

Regression results from 5/4/03
3451 tests: 66% Pass, 12% Fail, 23% incomplete

Change 98861 on 2003/05/02 by smoss@smoss_crayola_linux_orl_regress

   more sq stuff

Change 98818 on 2003/05/02 by smoss@smoss_crayola_linux_orl_regress

   added missing dump

Change 98793 on 2003/05/02 by rramsey@rramsey_crayola_linux_orl

Check in Dan's fixes for the control flow trackers
Turn internal trackers back on in tb_sqsp

Change 98773 on 2003/05/02 by mmang@mmang_crayola_linux_orl

1.  Added constant address register valids to validate the
    address register data.  The valid is set when address register
    is written.  If valid is not set, sequencer will not waterfall
    those vertices or pixels.  This disables waterfalling for
    predicated off writes and improperly initialized contant
    address registers.
2.  Fixed bug in sqs_alu_instr_seq for phase 3 snooping of
    constant address registers bus.  Previously, this snooping
    did not account for predication of those registers.
3.  Fixed bug where ais_load_done_bits was not hooked up.  This
    signal disables previous vector/scalar management which needs
    to be turned off during constant waterfalling.  With bug,
    pvps logic went unknown which caused unknowns to eventually
    propagate in and out of the gprs.
4.  Fixed bug where non-optimized offset was not being determined
    properly.  non_opt_offset is determined by a priority encoder
```

```
    of p0_done, p1_done, p2_done, and p3_done.
5.  With advent of constant address register valids, created
    waterfall_active_q to properly init and avoid re-initing of
    different pixel and vertex done bits.

Change 98750 on 2003/05/02 by viviana@viviana_crayola2_syn

Memory increased from 48x155 to 48x170.

Change 98577 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress

   reverting changes due to over-engineered process

Change 98571 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress

   sometime it helps when you save the file first

Change 98569 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress

   added FSDB_DUMP option for VCS

Change 98509 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress

   removed tb_sqsp

Change 98462 on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro

- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v

Change 98398 on 2003/04/30 by smoss@smoss_crayola_linux_orl_regress

   new sq stuff

Change 98397 on 2003/04/30 by grayc@grayc_crayola2_linux_orl

   new tb

Change 98367 on 2003/04/30 by rramsey@rramsey_crayola_linux_orl

these trackers were looking at the wrong register stage to determine
```

thread_id and thread_type

Change 98343 on 2003/04/30 by ashishs@fl_ashishs_r400_win

Correcting an error from script since it wasn't updating the user's comments and locked by user correctly. Also adding an empty XLS file which is used by the script to add and merge data

Change 98307 on 2003/04/30 by ashishs@fl_ashishs_r400_win

fixed a small error in the script because of which it wasnt getting the comments from the report. Also updated some comments.

Change 98283 on 2003/04/30 by viviana@viviana_crayola2_syn

Files no longer used in the SQ.

Change 98274 on 2003/04/30 by rramsey@rramsey_crayola_linux_orl

change if(`DEBUG_PRINT) to `ifdef DEBUG_PRINT so trackers
work at gc level

Change 98261 on 2003/04/30 by ashishs@fl_ashishs_r400_win

added the script for updating the XLS hadware regression data. Can have more enhancements depending on requirements

Change 98144 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

Add internal trackers to tb_sqsp, clean up memory files listed in tb.f
Remove DEBUG_PRINT from tb.f, it should be specified in vcsopts.f

Change 98142 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

timing fix for rbi_addr

Change 98140 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

fix a typo in a signal path

Change 98132 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

update trackers for new fields in dump files and make them
work for events

Change 98079 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

Fix a bug with alu1's trigger

```
Add define control for comment printing

Change 98067 on 2003/04/29 by danh@danh_crayola_linux_orl

Made type_serialize_1 and vc_request_1 changes.

Change 97992 on 2003/04/28 by dougd@dougd_r400_linux_marlboro

fixed some Leda reported problems

Change 97991 on 2003/04/28 by dougd@dougd_r400_linux_marlboro

added R500 dual read ports and extra memories.

Change 97962 on 2003/04/28 by danh@danh_crayola_linux_orl

Made signal changes in regards to .dmp file changes.

Change 97961 on 2003/04/28 by danh@danh_crayola_linux_orl

Made signal name changes in regards to .dmp file changes.

Change 97958 on 2003/04/28 by danh@danh_crayola_linux_orl

Made signal changes in regards to the .dmp file changes.

Change 97956 on 2003/04/28 by danh@danh_crayola_linux_orl

Added jump_call_addr registers.

Change 97892 on 2003/04/28 by danh@danh_crayola_linux_orl

       no changes made.

Change 97732 on 2003/04/25 by danh@danh_crayola_linux_orl

Changed signal names per sq_pix_control_flow_alu.dmp

Change 97708 on 2003/04/25 by rramsey@rramsey_crayola_linux_orl

Move inc for event thread count to front of event fifo
They were still happening on the same clk as real threads

Change 97670 on 2003/04/25 by rramsey@rramsey_crayola_linux_orl

Change buildtb and buildkdb to use tb.f for libraries and compile options
to keep from having to add files in two places
Couple of bug fixes/enhancements for tb_sqsp
```

```
Fix path define for sp_macc tracker when running tb_sqsp

Change 97538 on 2003/04/24 by ygiang@ygiang_r400_pv2_marlboro

added: more sq perf counters

Change 97402 on 2003/04/24 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Tracker used to test the inputs and outputs of all MACC units within the shader
pipes.

Change 97152 on 2003/04/23 by dougd@dougd_r400_linux_marlboro

added logic to control vtx perf counters to sq_vtx_ctl.v and sq.v; fixed bug in write
logic in sq_aluconst_wrt_buf.v

Change 96990 on 2003/04/22 by viviana@viviana_crayola2_syn

Ran cover on the sq_rf.cnt to add the new 16x170 and 48x170 memories.

Change 96981 on 2003/04/22 by viviana@viviana_crayola2_syn

Added TST_awt_enable to the interfaces with ss/sq_pix_thread_buff.v and
   ss/sq_vtx_thread_buff.v.
   Replaced the 16x155 and 48x155 memories with 16x170 and 48x170 respectively.
   Replaced the memory to be compiled in buildtb from the 155 to the 170.

Change 96948 on 2003/04/22 by viviana@viviana_crayola2_syn

Changed the name of the FIFO.

Change 96947 on 2003/04/22 by viviana@viviana_crayola2_syn

Removed width from paramenter definitions.

Change 96946 on 2003/04/22 by viviana@viviana_crayola2_syn

Added done_vector to sensitivity list at line 902.
   Removed `SQ_SRCB_PHASE from sensitivity list at line 1018.
   Added isr_thread_type_q to sensitivity list at line 1233.

Change 96876 on 2003/04/22 by rramsey@rramsey_crayola_linux_orl

only compare if one of the vector unit bits is valid

Change 96738 on 2003/04/21 by mmang@mmang_crayola_linux_orl
```

```
Fixed bug in sq_ais_output.v related to address register write and
predication.  Fixed a variety of tests to not use uninitialized gpr
or address registers.  2 tests still fail because of previous vector
scalar swizzle bug, 1 test still fails because of MOVA hardware bug, and
1 test still fails because of predicated address register write causes
XXXXXX which causes waterfalling to hang.

Change 96623 on 2003/04/21 by bhankins@bhankins_crayola_linux_orl

add support for including SX units into tb_sqsp.v

Change 96455 on 2003/04/18 by bhankins@bhankins_crayola_linux_orl

initial checkin to optionally include (not included by default) two SX units
       with associated support logic and trackers.

Change 96445 on 2003/04/18 by rramsey@rramsey_crayola_linux_orl

Move compares into a task, add a flag
to enable marking x vs 0 compares as warnings

Change 96389 on 2003/04/18 by mzini@mzini_crayola_linux_orl

 Temporarily removed the checking of control bits until the hardware catches up
```

```
Change 132842 on 2003/11/19 by chammer@chammer_xenos_linux_orl

Added changes for Xenos, enabled with `define XENOS
 Includes new rb_id, edram copy mode, zplane changes.

Change 131449 on 2003/11/11 by mearl@mearl_xenos_linux_orl

Bug fixes for 2 primitive interpolation.

Change 131174 on 2003/11/10 by mearl@mearl_xenos_linux_orl

Fixed 2 bugs with two primitive interpolation.

Change 130601 on 2003/11/06 by smoss@smoss_crayola_linux_orl_regress

   housekeeping

Change 130407 on 2003/11/06 by donaldl@donaldl_xenos_linux_orl

Adjusted delays again with new 90nm libraries to meet latencies.

Change 130164 on 2003/11/04 by chammer@chammer_xenos_linux_orl

Switched SC_RCT(tile) interface to SC_BC(four quad) interface.

Change 129450 on 2003/10/30 by viviana@viviana_xenos_linux_orl

Configuration file with the 28x99 and 28x100 memories recently added.

Change 128670 on 2003/10/27 by smoss@smoss_xenos_linux_orl

   combined ncverilog and vcs into one build, removed a few warnings

Change 128652 on 2003/10/27 by smoss@smoss_crayola_linux_orl_regress

   some housekeeping

Change 128365 on 2003/10/24 by mearl@mearl_xenos_linux_orl

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed
synthesis
       bugs in SC.

Change 127878 on 2003/10/22 by donaldl@fl_donaldl_p4

Changed oZ_TC from 28 bit to 27 bits to reflect latest sc_ztc_flt2fix.

Change 127729 on 2003/10/22 by rramsey@rramsey_xenos_linux_orl
```

```
Add window_valid_busy counts to sc and change sc_starved_by_pa to only count busy
cycles

Change 127504 on 2003/10/21 by kmeekins@kmeekins_r400_win

Released work from my test environment.

Change 126566 on 2003/10/14 by mearl@mearl_xenos_linux_orl

Fixed bug in multi-pass logic when persistent event increments counter.

Change 126483 on 2003/10/13 by mearl@mearl_xenos_linux_orl

Fix One Prim Per Clock bug in sq_ptr_buff. Revert changes in sq_pix_ctl to make
       2 prim interp changes easier. Put known primdata data on all quads across packer
       to iterator interface. Fix dumps for no_inc_pix_cnt signal.

Change 125786 on 2003/10/09 by mearl@mearl_xenos_linux_orl

Fixed the unused port PA_SC_phase[0] when using ONEPPC

Change 125370 on 2003/10/07 by mearl@mearl_xenos_linux_orl

Fixed the SQ bug when bad pipe exists before a good pipe. Also, updated
       the RT trackers in the SC testbench.

Change 125314 on 2003/10/07 by chammer@chammer_xenos_linux_orl

Added ifdef to sc_quadmask.mc to remove quadcovered logic which is not used by
 the BC in Xenos.

Change 124776 on 2003/10/03 by donaldl@fl_donaldl_p4

Added new sc_itercmdfifo mems for one-prim-per-clock.

Change 124775 on 2003/10/03 by donaldl@fl_donaldl_p4

Changed bit-width of PA_SC_cntl1 from 30 bits to 29 bits.  The msb was not being used.

Change 124706 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Changed data width of PA_SC_cntl1 from 30 bits to 29 bits to match
the PA (ie. msb wasn't used).

Change 124705 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Updated MC clock period, input/output delays for new 90nm libraries.
```

```
Change 124608 on 2003/10/02 by mearl@mearl_xenos_linux_orl

Updated to handle up to 4 SIMD engines

Change 124434 on 2003/10/01 by mmang@mmang_xenos_linux_orl

1.  Turned on 3 simds in emulator (sc_interp.cpp,
    sq_block_model.cpp, and user_block_model.cpp).
2.  Turned on 3 simds in rtl (sc_packer.v,
    tb_sqsp.v, and vgt.v).
3.  Fixed bug in chip_vc.tree to get SQ_VC_simd_id
    and TC_VC_simd hooked up correctly.
4.  Fixed bug in sc_packer.v related to having a 2
    bit simd_id_sel.

Change 124373 on 2003/10/01 by mearl@mearl_xenos_linux_orl

Fixed timing paths through primdata selection logic

Change 123960 on 2003/09/30 by rramsey@rramsey_xenos_linux_orl

remove internal tracker enable

Change 123923 on 2003/09/29 by mearl@mearl_xenos_linux_orl

Fix to the emulator and corresponding hardware.

Change 123918 on 2003/09/29 by rramsey@rramsey_xenos_linux_orl

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

Change 123848 on 2003/09/29 by mearl@mearl_xenos_linux_orl

Add new memories for iter command FIFO.
```

```
Change 123755 on 2003/09/29 by mearl@mearl_xenos_linux_orl

Fix for timing problems, submitting new memories, using real memories for regressions.

Change 123537 on 2003/09/26 by chammer@chammer_xenos_linux_orl

Fixed random backpressure/input for all interfaces. Removed extra cycle of
 delay in SC_RC_rtr/RC_SC_hier_send path for non-rts version of testbench.

Change 122897 on 2003/09/23 by ctaylor@ctaylor_xenos_linux_orl

Removed 3,6,8 sample MSAA for Xenos.  Cleaned up remnants of render state leftover from
JSS.

Change 122683 on 2003/09/23 by mearl@mearl_crayola_linux_orl

One primitieve per clock changes in the back of the SC and front of the SQ. Right now,
the ONE_PRIM_PER_CLOCK define in
       header.v and SC_SQ_interface.v are needed for this change. Will update this to
ONEPPC, since this already exists in
       header.v. Also, the sim.cfg file does not have an ifdef, so is hardcoded to one
prim per clock.

Change 122402 on 2003/09/20 by mmang@mmang_crayola_linux_orl

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7.  In sq_export_alloc.v, handle position/main export id
    and parameter cache thread base for simd2/3.  Be able
    to handle one type down simd0/1 and a different type
    down simd2/3 on the same clock.
8.  In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
    gpr_alloc blocks return different acks, gpr bases,
    and gpr maxes.
9.  In sq_exp_alloc_ctrl.v, handle position/main export
    buffer management.  Be able handle one type down
    simd0/1 and a different type down simd2/3 on the same
    clock.
```

10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
    added muxing and memories to handle status bits, cfs
    state, and alu state. Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

Change 122323 on 2003/09/19 by chammer@chammer_xenos_linux_orl

Fixed sc_sx tracker for non-rts case, was not checking properly

Change 122289 on 2003/09/19 by donaldl@donaldl_crayola_linux_orl

Qualified the perf outputs (scis_discard, bb_discard, & supert_discard)
with pipe_rts_elat1 so they become known during reset.

Change 122072 on 2003/09/18 by donaldl@fl_donaldl_p4

Forced iST_LAST_PIXEL going to sc_pipe to zero to get vectors to work.

Change 121157 on 2003/09/13 by smoss@smoss_crayola_linux_orl_regress

   xenos updates

Change 120766 on 2003/09/11 by chammer@chammer_crayola_linux_orl

BC_SC_rtr is now tied at the chip level and can be driven in the SC testbench.

Change 120645 on 2003/09/11 by rramsey@rramsey_crayola_linux_orl

Remove some unused defines
Add reset condition for primdata pipe stages in qdpr_proc
Fix a bug with tp_count in fetch_arb when running with the VC
Increase loop_cnt for vc inject in tb_sqsp

Change 120631 on 2003/09/11 by chammer@chammer_crayola_linux_orl

```
Added SC_BC ports to chip_sc.tree as UNCONNECTED, tied BC_SC_RTR to 1

Change 120137 on 2003/09/09 by chammer@chammer_crayola_linux_orl

Added control to force invalid quads' data to zero, this is necessary because
 there are no "valids" on the SC to BC interface.

Change 119992 on 2003/09/08 by rramsey@rramsey_crayola_linux_orl

Add last_pixel logic to SC
Duplicate a bit in the qpp to help fanout

Change 119519 on 2003/09/04 by smoss@smoss_crayola_linux_orl_regress

   increased watchdog timeout by x10

Change 119475 on 2003/09/04 by chammer@chammer_crayola_linux_orl

Added four quad per clock interface between SC and BC.

Change 119369 on 2003/09/04 by rramsey@RRAMSEY_P4_r400_win

fix sensitivity list probs

Change 119023 on 2003/09/02 by ctaylor@ctaylor_crayola_linux_orl

Removal of JSS basics

Change 118398 on 2003/08/27 by donaldl@donaldl_crayola_linux_orl

Updated number of skid words for primfifo to 2 to prevent overflow of mem writes.
Placed common bit assignments for PA_SC signals outside ONEPPC ifdef to get around
synthesis errors.

Change 118171 on 2003/08/26 by rramsey@rramsey_crayola_linux_orl

update quad_select compare for q1 so it works with the 4qd/clk changes

Change 117706 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with
modifications to their test benches and added
    ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with
SIMD1_PRESENT macro in the SC files>

Change 117504 on 2003/08/21 by mmang@mmang_crayola_linux_orl
```

```
1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

Change 117456 on 2003/08/21 by donaldl@donaldl_crayola_linux_orl

Enabled for one primitive per clock performance.

Change 117311 on 2003/08/20 by rramsey@rramsey_crayola_linux_orl

Changes to sc for 4 qd/clk picker in KILL_ALL_PIXELS mode
Check in sc memory updates for Vivian
Add some missing connections in sqsp to fix compile warnings
Go to a global define for all trackers to control x vs 0 mismatch/warning
(MISMATCH_X_VS_0)

Change 117140 on 2003/08/19 by donaldl@donaldl_crayola_linux_orl

Updated for one primitive per clock but ifdef'd currently to work
as one primitive every 2 clocks.

Change 117103 on 2003/08/19 by donaldl@fl_donaldl_p4

Changed PA_SC_phase bit width back to 2.  The msb will be used to determine a clip
primitive.

Change 116908 on 2003/08/18 by mearl@mearl_crayola_linux_orl

This version of sc_packer has the newest bad pipe logic, all of the
       known bug fixes, and is the last version before the one primitive per
       clock changes.

Change 116762 on 2003/08/15 by donaldl@donaldl_crayola_unix_orl

Defines to enable one primitiver per clock and extra edge fractional bits

Change 116761 on 2003/08/15 by donaldl@fl_donaldl_p4

Used ifdef's to run at one primitive per clock.

Change 116038 on 2003/08/12 by mearl@mearl_crayola_linux_orl

       added changes for simd id pipe disable logic

Change 116036 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic
```

```
Change 116034 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 116033 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 116032 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 116031 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 115724 on 2003/08/10 by smoss@smoss_crayola_linux_orl_regress

   added coverage.f option

Change 114229 on 2003/07/31 by donaldl@fl_donaldl_p4

Updated for latest versions of sc_pipe, sc_coarse_walker, and sc_quadmask.

Change 113413 on 2003/07/27 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 113007 on 2003/07/24 by rramsey@RRAMSEY_P4_r400_win

add +define+MEM_CHECK_OFF unless compiling for gate sims

Change 111715 on 2003/07/17 by rramsey@RRAMSEY_P4_r400_win

some old fixes for an SC modelsim script

Change 111100 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

Change sc build scripts for TB_SC to tb_sc change
Add cmd line option for fsdb dumping (+SC_DEBUSSY=level)
Add verdi compile to build scripts
Change default build to use real mems

Change 111093 on 2003/07/15 by smoss@smoss_crayola_linux_orl

   decapitating tb_sc
```

```
Change 111089 on 2003/07/15 by grayc@grayc_crayola2_linux_orl

   causes a problem with Windows regressions ... removing

Change 111085 on 2003/07/15 by smoss@smoss_crayola_linux_orl_regress

   attempt to remove again

Change 111084 on 2003/07/15 by smoss@smoss_crayola_linux_orl_regress

   attempt to remove the capital of tb_sc

Change 111070 on 2003/07/14 by grayc@grayc_crayola2_linux_orl

   add a link  tb_sc->TB_SC

Change 110640 on 2003/07/12 by mmantor@mmantor_crayola_linux_orl

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

Change 110503 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed versions of the compiler for the rf memories.

Change 110494 on 2003/07/11 by smoss@smoss_crayola_linux_orl

   turned internal trackers off

Change 108140 on 2003/06/26 by rramsey@rramsey_crayola_linux_orl

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
```

```
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

Change 106938 on 2003/06/19 by viviana@viviana_crayola2_syn

Removed unused Virage files from the src directory.

Change 106274 on 2003/06/16 by rramsey@FL_RAMSEY_r400_win

add new rf block to vsim makefile

Change 105688 on 2003/06/11 by danh@danh_crayola1_linux_orl

Added sq_ef_pb_avail_la, changed nxt_sent_sq_cntl_cnt and itercmdfifo_re generation to
       resolve a sq.u_sq_ptr_buff.sq_event_fifo overflow error.

Change 104832 on 2003/06/08 by smoss@smoss_crayola_linux_orl_regress

   add rom disable bits

Change 103932 on 2003/06/03 by mmantor@mmantor_crayola_linux_orl

   update for new pipe disable routing

Change 101774 on 2003/05/20 by smoss@smoss_crayola_linux_orl

   test

Change 99221 on 2003/05/05 by grayc@grayc_crayola2_linux_orl

   changes for ncsim compile

Change 99134 on 2003/05/05 by viviana@viviana_crayola2_syn

Rebuilt the memories with 444 Mhz and Virage/3300 compiler.  Also, added
   sc_rf_awt_gate.v to sc.v for test purposes.

Change 98990 on 2003/05/04 by rramsey@rramsey_crayola_unix_orl
```

```
Fix for stipple when a real-time prim breaks in as one prim
is finishing, and a stippled line is sitting in the front
stage of the walker

Change 98461 on 2003/05/01 by rramsey@RRAMSEY_P4_r400_win

fixes for some of the non-context based sc perfcounters

Change 98046 on 2003/04/29 by danh@danh_crayola_linux_orl

Initial release.
```

```
Change 130601 on 2003/11/06 by smoss@smoss_crayola_linux_orl_regress

   housekeeping

Change 129739 on 2003/11/02 by smoss@smoss_xenos_linux_orl

   added vgt gate memory file to vgt dir

Change 128670 on 2003/10/27 by smoss@smoss_xenos_linux_orl

   combined ncverilog and vcs into one build, removed a few warnings

Change 128652 on 2003/10/27 by smoss@smoss_crayola_linux_orl_regress

   some housekeeping

Change 128372 on 2003/10/24 by smoss@smoss_parts_lib_release

   Checking in these files for Mr. Hartog after they passed release_parts_lib

Change 124987 on 2003/10/05 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 124757 on 2003/10/03 by rramsey@rramsey_xenos_linux_orl

move reg declarations out of always blocks for synthesis

Change 124738 on 2003/10/03 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 124503 on 2003/10/02 by bbuchner@bbuchner_xenos_linux_orl

added more performance counters to VGT to cover starved_busy, starved_idle and static
cases

Change 124434 on 2003/10/01 by mmang@mmang_xenos_linux_orl

1.  Turned on 3 simds in emulator (sc_interp.cpp,
    sq_block_model.cpp, and user_block_model.cpp).
2.  Turned on 3 simds in rtl (sc_packer.v,
    tb_sqsp.v, and vgt.v).
3.  Fixed bug in chip_vc.tree to get SQ_VC_simd_id
    and TC_VC_simd hooked up correctly.
4.  Fixed bug in sc_packer.v related to having a 2
    bit simd_id_sel.
```

```
Change 123918 on 2003/09/29 by rramsey@rramsey_xenos_linux_orl

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

Change 123458 on 2003/09/26 by jmarsano@jmarsano_r400_UNIX_new

Adding generated verilog for vgt_rf memories.

Change 122720 on 2003/09/23 by smoss@smoss_crayola_linux_orl_regress

   changed SIMD2_PRESENT to VGT_SIMD2_PRESENT until sq hardware catches up

Change 121175 on 2003/09/13 by smoss@smoss_parts_lib_release

   added some missing sensitivity list signals

Change 121157 on 2003/09/13 by smoss@smoss_crayola_linux_orl_regress

   xenos updates

Change 120331 on 2003/09/09 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 120187 on 2003/09/09 by rramsey@rramsey_crayola_linux_orl

checking in more of scott's vgt fixes:
       vgt_out_indx.v -- No logical change. Added an "Assert" to check assumption.
vgt_output.v -- Fix to SIMD select logic.

Change 120144 on 2003/09/09 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 119852 on 2003/09/06 by rramsey@rramsey_crayola_linux_orl
```

Check in Scott's changes for the vgt:

The current design of the VGT results in the restriction that all
the simd sets must have the same number of active pipes (with the exception
of simd pipes that are completely disabled). The emulator does not have
this restriction (each simd set can have a different number of active
pipes). If the hardware attempts to run a vector set and the non-zero
simd pipe sets are different, then the hardware will print an error message
and assert.

Connected the SIMD output from VGT.
Moved the logic for the ROM_BAD_PIPE_DISABLE signals from the vgt_vtx_reuse block to the vgt_output block.

Change 119393 on 2003/09/04 by smoss@smoss_crayola_linux_orl_regress

disable grouper tracker always

Change 118677 on 2003/08/29 by smoss@smoss_crayola_linux_orl_regress

included cp_r, corrected build error check

Change 117706 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with modifications to their test benches and added
ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with SIMD1_PRESENT macro in the SC files>

Change 117091 on 2003/08/19 by smoss@smoss_crayola_linux_orl_regress

more commonality

Change 115386 on 2003/08/07 by grayc@grayc_crayola2_linux_orl

partial change for pav and test
update for mh block file change

Change 114561 on 2003/08/01 by smoss@smoss_crayola_linux_orl_regress

added coverage for vcs
added coverage for cp
stop simulation during compile of vgt
modified fsdb generation for cp

Change 114404 on 2003/08/01 by amys@amys_r400_regress_linux

```
changes made to fix running ncsim using Orlando trackers

Change 111520 on 2003/07/16 by grayc@grayc_crayola2_linux_orl

   fix for new tile

Change 111422 on 2003/07/16 by grayc@grayc_crayola2_linux_orl

   delete KS tile ... add PAV and CP_R tile

Change 110527 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed the Virage compiler version.

Change 108121 on 2003/06/26 by smoss@smoss_crayola_linux_orl_regress

   $value$plusargs doesn't currently work properly for cadence changed logic to turn
off grouper by default

Change 107255 on 2003/06/20 by moev@moev2_r400_linux_marlboro

Makefile that uses ncverilog (it also uses modeltech),

Change 107249 on 2003/06/20 by moev@moev2_r400_linux_marlboro

deleted un-needed ports

Change 103932 on 2003/06/03 by mmantor@mmantor_crayola_linux_orl

   update for new pipe disable routing

Change 101651 on 2003/05/19 by moev@moev2_r400_linux_marlboro

added '0' constant to TST_awt_enable.

Change 100501 on 2003/05/12 by smoss@smoss_crayola_linux_orl_regress

   ncverilog for vgt pa

Change 100141 on 2003/05/09 by viviana@viviana_crayola2_syn

Corrected a wire name for new vgt_rf_awt_gate module addition.

Change 99058 on 2003/05/05 by viviana@viviana_crayola2_syn

New module added to vgt.v for test purposes.

Change 99057 on 2003/05/05 by viviana@viviana_crayola2_syn
```

```
New version of the virage compiler was received and memories were rebuilt.
   Also, a new module was added at the top level called vgt_rf_awt_gate.v for
   test purposes.
```

```
Change 132864 on 2003/11/19 by bhankins@bhankins_xenos_linux_orl

delete obsolete files

Change 130601 on 2003/11/06 by smoss@smoss_crayola_linux_orl_regress

   housekeeping

Change 130419 on 2003/11/06 by dclifton@dclifton_xenos_linux_orl

Update to account for module compiler library changes.

Change 130345 on 2003/11/05 by dclifton@dclifton_xenos_linux_orl

Update clock delay so sythesis will finish

Change 128670 on 2003/10/27 by smoss@smoss_xenos_linux_orl

   combined ncverilog and vcs into one build, removed a few warnings

Change 128652 on 2003/10/27 by smoss@smoss_crayola_linux_orl_regress

   some housekeeping

Change 126888 on 2003/10/16 by bhankins@bhankins_xenos_linux_orl

Fix perf monitoring signal

Change 126487 on 2003/10/14 by bhankins@bhankins_xenos_linux_orl

Change to try and improve on timing.  No functional change.

Change 125786 on 2003/10/09 by mearl@mearl_xenos_linux_orl

Fixed the unused port PA_SC_phase[0] when using ONEPPC

Change 125597 on 2003/10/08 by bhankins@bhankins_xenos_linux_orl

move adders outside of comb. process for timing.  no functional change.

Change 125257 on 2003/10/07 by dclifton@dclifton_xenos_linux_orl

Fixed latency in pa.  Added mc mux for fanout control on const muxes
for alu constant data in sp.

Change 124330 on 2003/10/01 by dclifton@dclifton_xenos_linux_orl

Updated timing parameters for 0.09um technology.
```

```
Change 124038 on 2003/09/30 by dclifton@dclifton_r400

Fixed busy and starved performance counters.

Change 121157 on 2003/09/13 by smoss@smoss_crayola_linux_orl_regress

   xenos updates

Change 120968 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

Updates to simd_id for the sx inteface to use the id sent from the vgt.
   Also, add support for up to four simds.

Change 119496 on 2003/09/04 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 119357 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Fixed w0 bug with clipped lines

Change 119356 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Fixed w0 bug with clipped lines

Change 119162 on 2003/09/03 by viviana@viviana_crayola2_syn

Memories for ONEPPC.

Change 118677 on 2003/08/29 by smoss@smoss_crayola_linux_orl_regress

   included cp_r, corrected build error check

Change 117974 on 2003/08/25 by smoss@smoss_crayola_linux_orl_regress

   incorrect define

Change 117937 on 2003/08/24 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 117737 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<added simd_id between vgtmod injector and the pa for test bench>

Change 117706 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl
```

<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with modifications to their test benches and added
    ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with SIMD1_PRESENT macro in the SC files>

Change 117091 on 2003/08/19 by smoss@smoss_crayola_linux_orl_regress

   more commonality

Change 117064 on 2003/08/19 by smoss@smoss_crayola_linux_orl

   common format for builds

Change 116692 on 2003/08/15 by smoss@smoss_crayola_linux_orl_regress

   add pa buildtb

Change 116660 on 2003/08/14 by dclifton@dclifton_r400

Added fix for clipped polymode lines.

Change 116318 on 2003/08/13 by dclifton@dclifton_r400

Update for changes in test I/O on pa

Change 115386 on 2003/08/07 by grayc@grayc_crayola2_linux_orl

   partial change for pav and test
   update for mh block file change

Change 114404 on 2003/08/01 by amys@amys_r400_regress_linux

changes made to fix running ncsim using Orlando trackers

Change 111722 on 2003/07/17 by amys@amys_crayola2_linux_orl

fixed a type in PA_PATH for the chip

Change 111515 on 2003/07/16 by grayc@grayc_crayola2_linux_orl

   fix for new tile path

Change 111422 on 2003/07/16 by grayc@grayc_crayola2_linux_orl

   delete KS tile ... add PAV and CP_R tile

Change 111062 on 2003/07/14 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 110877 on 2003/07/14 by dclifton@dclifton_r400

changed rom disable address

Change 110520 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed the virage compiler for rf memories.

Change 107802 on 2003/06/25 by moev@moev2_r400_linux_marlboro

Updates to the make file to verify virage RFs.

Change 106341 on 2003/06/16 by bhankins@bhankins_crayola_linux_orl

fix the generation of nan_kill_flag bits from being reset buy subsequent non-NaN numbers.

Change 104215 on 2003/06/05 by smoss@smoss_crayola_linux_orl

   pa.v back to new broken state

Change 104210 on 2003/06/05 by smoss@smoss_crayola_linux_orl

   removed sp disable and simd references to get back to stability

Change 104193 on 2003/06/05 by bhankins@FL_BHANKINS_P4

fix wiring error in bad pipe

Change 104124 on 2003/06/04 by smoss@smoss_crayola_linux_orl

   changed back to #161

Change 104116 on 2003/06/04 by smoss@smoss_crayola_linux_orl

   old version with pa_sc_phase fix

Change 103991 on 2003/06/04 by moev@moev2_r400_linux_marlboro

Makefile for the PA tile which uses soft variables such a ROOT & BRANCH. It also uses NCVerilog

Change 103989 on 2003/06/04 by viviana@viviana_crayola2_syn

Changed the processor to exclude the two memories for the ONEPPC define.

Change 103971 on 2003/06/04 by bhankins@fl_bhankins_r400_win

fixes to support bad pipe for 2 simds

Change 103958 on 2003/06/04 by bhankins@fl_bhankins_r400_win

minor fix

Change 103932 on 2003/06/03 by mmantor@mmantor_crayola_linux_orl

   update for new pipe disable routing

Change 103828 on 2003/06/03 by dclifton@dclifton_r400

Fixed PA_SC_phase so it works with stub file generator.

Change 103761 on 2003/06/03 by bhankins@fl_bhankins_r400_win

updates to support bad pipe for two simds

Change 103647 on 2003/06/02 by moev@moev2_r400_linux_marlboro

Made changes to the Virage patchbox to mimic the Virage order (as described in the Data Sheet).

Change 103611 on 2003/06/02 by bhankins@fl_bhankins_r400_win

fix syntax error

Change 103610 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate bad pipes for 2 simd engines.

New I/O is commented out for now for compatibility.

Change 103605 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate bad pipe signals for 2 simds

Change 103604 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate bad pipes for 2 simds

Change 103603 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate 2 simd bad pipe signals

Change 103602 on 2003/06/02 by bhankins@fl_bhankins_r400_win

```
changes to accomodate 2 simd bad pipe signals

Change 103563 on 2003/06/02 by dclifton@dclifton_r400

typo in STAR signals

Change 103385 on 2003/05/30 by moev@moev2_r400_linux_marlboro

added termination to TST_awt_enable

Change 103373 on 2003/05/30 by viviana@viviana_crayola2_syn

Added another 12x104 memory for xyz for the ONEPPC ifdef to the pa and reconnected
   the patchin/patchout signals.

Change 102947 on 2003/05/28 by viviana@viviana_crayola2_syn

Corrected the STAR_rf_testbus[7] wired to 64x128cm2 memory instead of
STAR_rf_testbus[6].

Change 102945 on 2003/05/28 by viviana@viviana_crayola2_syn

Corrected STAR_rf_testbus[7] wired to the 64x8cm2 memory instead of STAR_rf_testbus[8].

Change 101771 on 2003/05/20 by dclifton@dclifton_r400

Fixed some typos in STAR signal connections.
Added readback for cl_status.

Change 101696 on 2003/05/19 by viviana@viviana_crayola2_syn

Added an additional 10x96 memory to be used if ONEPPC is defined.

Change 101367 on 2003/05/16 by dclifton@dclifton_r400

Added one-prim-per-clock mode for setup engine.  Define ONEPPC to get compiler to build
for this mode.

Change 101360 on 2003/05/16 by dclifton@dclifton_r400

Added ONEPPC define for one-prim-per-clock build mode of setup engine.

Change 100501 on 2003/05/12 by smoss@smoss_crayola_linux_orl_regress

   ncverilog for vgt pa

Change 100243 on 2003/05/09 by dclifton@dclifton_r400
```

```
added pa_rf_awt_gate dependency for pa

Change 99799 on 2003/05/07 by viviana@viviana_crayola2_syn

Updated the virage memories built to include the atpg_gate and sync_reset.

Change 99736 on 2003/05/07 by viviana@viviana_crayola2_syn

Rebuilt the memories with virage/3300 at 444 Mhz from scratch.

Change 99129 on 2003/05/05 by viviana@viviana_crayola2_syn

Rebuilt the memories using Virage/3300 compiler and 444 Mhz.  Added pa_rf_awt_gate.v
   instantiated at the pa.v level and used for test purposes.

Change 98543 on 2003/05/01 by bhankins@fl_bhankins_r400_win

increase depth of vgt_to_ccgen fifo to 24
```

```
Change 131955 on 2003/11/14 by kmeekins@kmeekins_xenos_linux_orl

- Increased the L2 FIFOs from a max depth of 64 to 256.
  - Rewired the patchin and patchout signals to the memories.
  - Modified the register spec to have a larger programmable
    depth range for the L2 FIFO.
  - Changed the gc and chip builds to use the real memory models.

Change 131082 on 2003/11/10 by kmeekins@kmeekins_xenos_linux_orl

tb_vc.v
  ----------
  Fixed instantiation of vc now that delay is removed.

  sq_fetch_arb.v
  --------------
  Changed the bus width of vc_mini_count_q to accomidate the +2 modification.

  vcmi_requestor.v
  -----------------
  Increased the uvcmi_input_fifo FIFO depth to 8.
  Added the FIFO full to the performance monitor.

  tp.blk,
  vc.v,
  vc_perf_config.txt,
  vc_perfmon.v,
  vcmi.v
  ------------------------
  Added the FIFO full for the vcmi_input_fifo to the performance monitor.

Change 130693 on 2003/11/07 by kmeekins@kmeekins_xenos_linux_orl

chip_vc.tree,
  vc.v
  ----------------
  Removed the delay logic.

  tbmod_sqvc.v
  -------------
  Changed the L1 counter to use the pipelined elements of the FIFO.

Change 128624 on 2003/10/27 by mzini@mzini_crayola_linux_orl

 Added timeout count

Change 128464 on 2003/10/24 by kmeekins@kmeekins_xenos_linux_orl
```

```
  vc_cc.v,
  vc_cc_tag_compare.v,
  vc_cc_tag_process.v
  ---------------------------
  Added sector miss to the performance counters.

  vcdc.v
  ---------------------------
  Combined two combinational logic always blocks to elliminate a synthesis
  warning about having the same signal set in two different blocks.

  vcmi_receiver.v
  ---------------------------
  Corrected the timestamp delta calculation for the TWO_CHANNEL_VC.

  vcrg.v
  ---------------------------
  Added VC_PERF_send_event and VC_PERF_starved_idle_event to the performance counters.

tp.blk,
  vc.v,
  vc_perf_config.txt,
  vc_perfmon.v
  ---------------------------
  Added more performance counters.

  vcrg.cpp
  ---------------------------
  HACK to get system tests to match with the TP/TC (submitted for Marcos Zini).

  randomvc
  ---------------------------
  Made the usage message look pretty.

Change 126574 on 2003/10/14 by mzini@mzini_crayola_linux_orl

 Added ability for random tool to change rsp in mid-test plus TB can now handle this

Change 126550 on 2003/10/14 by kmeekins@kmeekins_xenos_linux_orl

Preventing an active VC_RSP_valid signal while redundant shader pipe operation is
disabled.

Change 126516 on 2003/10/14 by mzini@mzini_crayola_linux_orl

 VC TB redundancy change

Change 126491 on 2003/10/14 by kmeekins@kmeekins_xenos_linux_orl
```

```
Corrected syntax by defining vc_busy_in.

Change 126382 on 2003/10/13 by kmeekins@kmeekins_xenos_linux_orl

tp.blk,
  vc_perf_config.txt,
  vc_perfmon.v
  ------------------------
  Added a new performance monitor field for counting number of valids passed to the SP.

  vc.v,
  vcdc.v
  ------------------
  - Reformatted vc.v using more AUTO commands.
  - Added the new performance monitor field for counting valids passed to SP.
  - Corrected the valid logic to swizzle the data valids similar to the data for
    the redundant shader pipe logic.

  vcmi_receiver.v
  ----------------
  Corrected the timestamp delta equation.

Change 125352 on 2003/10/07 by kmeekins@kmeekins_xenos_linux_orl

Added the 128 bit memory hub interface RAM memory controller.

Change 125350 on 2003/10/07 by kmeekins@kmeekins_xenos_linux_orl

buildkdb,
  buildtb
  ----------
  Modified the scripts to NOT use the behavioral RAM models and to use the two channel
  (128 bit) memory interface.

  runvc
  -------
  Modified the script to have the option to run only the verilog simulation which
permits
  the user to generate the dump files from the full chip emulator.

  vc.v
  -----
  Corrected the instantiation of the modules associated with the two channel mode.

  vc_rf_128_awt_gate.v,
  vc_rf_128_fusebox.ctmc,
  vc_rf_128_fusebox.v,
```

```
  vc_rf_128_stp.v,
  vc_rf_128_testreg.v
  ------------------------
  Added the 128 bit memory hub interface version of the RAM memory controller.

  vcmi.v,
  vcmi_receiver.v,
  vcrg.v
  -------------------
  Included header.v to files that used the TWO_CHANNEL_VC directive.

Change 124844 on 2003/10/03 by mzini@mzini_crayola_linux_orl

 Ability for testbench to handle the L1 fifo depth being programmed

Change 124324 on 2003/10/01 by kmeekins@kmeekins_xenos_linux_orl

vc.v
  -----
  - Removed VC_SP_valid. Now the SP is usind all 16 valids.
  - Registered the ROM inputs.
  - Changed the ROM signals to the lower modules to reflect their registered status.

  vcdc.v,
  vcrg.v
  -------
  Changed the ROM signal names to reflect their registered status.

Change 123893 on 2003/09/29 by kmeekins@kmeekins_xenos_linux_orl

randomvc,
  regressvc,
  runvc
  ----------------
  Modified scripts to use Brian's changes for the Redundant Shader Pipe testing

  chip_vc.tree
  ------------
  Removed partially driven bits for SQ_VC_simd_id and TC_VC_simd as these are now
  connected in the SQ and TC.

  tb_vc.v,
  tbtrk_vc_out.v
  ---------------
  Modified the testbench and tracker to use Brian's changes for the Redundant
  Shader Pipe logic.

  vc.v,
```

```
  vcdc.v,
  vcrg.v
  -------
  Modified the RTL to use Brian's changes for the Redundant Shader Pipe logic.

Change 123562 on 2003/09/26 by kmeekins@kmeekins_xenos_linux_orl

tp.blk, tp.desc
  ---------------
  - Changed L1 request FIFO depth to reflect max 32 words
  - Corrected debug register fields

  randomvc
  --------
  - Modified to perform infinite number of sequential ramdom tests.
  - Updates pass/fail status after each run.

  vc_cc.v,
  vc_cc_loaded_busy.v,
  vc_cc_pack_align.v,
  vc_cc_tag_process.v
  --------------------
  Created an earlier version of the fetch_pending_en signal for the
  loaded_busy module to correct the cache_lin_in_use logic.

  vc.v,
  vc_rbiu.v,
  vcrp.v
  ------------
  - Changed the width of the RBIU_RP_L1_req_fifo_depth bus to accomidate
    a max of 32 words.
  - Corrected VC_SP_data_valid logic.

Change 123547 on 2003/09/26 by smoss@smoss_crayola_linux_orl_regress

   added vc_mem

Change 122753 on 2003/09/23 by mzini@mzini_crayola_linux_orl

 Added memory swap in VC testbench

Change 122631 on 2003/09/22 by smoss@smoss_parts_lib_release

   tb_vc changes

   1. changed opened to processed for script
   2. made makefiles more generic
```

```
Change 122180 on 2003/09/19 by smoss@smoss_crayola_linux_orl_regress

   changed final result message

Change 121958 on 2003/09/18 by kmeekins@kmeekins_xenos_linux_orl

Reverse integrated the changes from vc_cc_delay branch spec into the r400 depot.

Change 121157 on 2003/09/13 by smoss@smoss_crayola_linux_orl_regress

   xenos updates

Change 118590 on 2003/08/28 by bbuchner@bbuchner_crayola_linux_orl

fixed two channel mode to allow fully indpendent behavior on the two channels.

Change 118397 on 2003/08/27 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 118022 on 2003/08/25 by mzini@mzini_crayola_linux_orl

Bumped instruction fifo depth to 32

Change 118021 on 2003/08/25 by mzini@mzini_crayola_linux_orl

 Added support for 2 or 4 memory return paths.

Change 117993 on 2003/08/25 by bbuchner@bbuchner_crayola_linux_orl

rebuild of memories

Change 117814 on 2003/08/22 by bbuchner@bbuchner_crayola_linux_orl

added ifdef code that will build a two channel version of the VC

Change 117645 on 2003/08/21 by bbuchner@bbuchner_crayola_linux_orl

use behavioral mems

Change 116474 on 2003/08/14 by bbuchner@fl_bbuchner_r400_win

remove old memories

Change 116337 on 2003/08/13 by bbuchner@bbuchner_crayola_linux_orl

new memory build.  Delelted 16x70 memory.  changed 11h28x47 to 32x112
```

```
Change 116333 on 2003/08/13 by bbuchner@bbuchner_crayola_linux_orl

changed coher interfact to CP.  Provide  independent data valids to SP.
   REmove  instruction FIFO from RP.

Change 115723 on 2003/08/10 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 115488 on 2003/08/07 by bbuchner@bbuchner_crayola_linux_orl

build script for coverage results

Change 115112 on 2003/08/06 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 115005 on 2003/08/05 by kmeekins@kmeekins_crayola_linux_orl

Added the ability to build and simulate using either NC Verilog or VCS.
  Scripts will detect which environment you have loaded and use the
  appropriate tools.

Change 114915 on 2003/08/05 by mzini@mzini_crayola_linux_orl

 Old fix for VC_RP testbench

Change 114719 on 2003/08/04 by bbuchner@bbuchner_crayola_linux_orl

changed two memory sizes

Change 114530 on 2003/08/01 by bbuchner@bbuchner_crayola_linux_orl

provide for from 1-4 simd engines.

Change 114319 on 2003/07/31 by kmeekins@kmeekins_crayola_linux_orl

Makefiles used to build new libpli.so for VC PLI memory tasks.

Change 114156 on 2003/07/31 by kmeekins@kmeekins_crayola_linux_orl

Removed the bit field from the scalar VC_SP_data_valid to stop ncverilog errors.

Change 113553 on 2003/07/28 by bbuchner@bbuchner_crayola_linux_orl

added new performance capabilities

Change 113527 on 2003/07/28 by kmeekins@kmeekins_crayola_linux_orl
```

```
Modified code and added comments to remove/supress LEDA warnings/errors
  on code sections known to be error free.

Change 113236 on 2003/07/25 by kmeekins@kmeekins_crayola_linux_orl

Changed increment/decrement logic to relieve timing. Treating cc_freeze_b
  signal as late arriving.

Change 113217 on 2003/07/25 by kmeekins@kmeekins_crayola_linux_orl

Removed signals/ports that are no longer needed.
  Changed muxing logic in vc_cc_way_mem.v to help timing.

Change 113209 on 2003/07/25 by mzini@mzini_crayola_linux_orl

Made info field 25 bits to make room for the latency counters

Change 112962 on 2003/07/24 by mzini@mzini_crayola_linux_orl

Added delete option

Change 112903 on 2003/07/24 by jcarroll@jcarroll_crayola_linux_orl

              Added default values for the 'load_coher' signals.

Change 112626 on 2003/07/23 by kmeekins@kmeekins_crayola_linux_orl

Added more performance monitiors for checking the stall conditions.

Change 112438 on 2003/07/22 by bbuchner@bbuchner_crayola_linux_orl

make start signal to CC be a pulse

Change 112428 on 2003/07/22 by bbuchner@bbuchner_crayola_linux_orl

<fixed to match tc invalidate behavior

Change 112216 on 2003/07/21 by kmeekins@kmeekins_crayola_linux_orl

Added logic to invalidate the cache on an address range.
  Added the new CC module vc_cc_cache_invalidate.

Change 112189 on 2003/07/21 by bbuchner@bbuchner_crayola_linux_orl

new invalidation scheme, added more debug

Change 112149 on 2003/07/21 by jbrady@jbrady_crayola_linux_orl
```

```
Gate build.

Change 112147 on 2003/07/21 by jbrady@jbrady_crayola_linux_orl

Change VC_gpr_phase_q sense to match what is expected in gc.

Change 112143 on 2003/07/21 by mzini@mzini_crayola_linux_orl

 Delayed gpr_phase by 2 cycles to match the hardware

Change 111959 on 2003/07/18 by mzini@mzini_crayola_linux_orl

 Delete testcase if it passes

Change 111945 on 2003/07/18 by jcarroll@jcarroll_crayola_linux_orl

            Recoded the L2 Request Control Logic.
            No functional changes.  Restructured for future timing fixes between CC and
RP.

Change 111918 on 2003/07/18 by kmeekins@kmeekins_crayola_linux_orl

Added the request size to the cache tag.

Change 111737 on 2003/07/17 by kmeekins@kmeekins_crayola_linux_orl

Registered RP->CC bank read address and read enables to fix a timing path.
  Propagated the newly registered signals to the vc_cc_loaded_busy module.

Change 111621 on 2003/07/17 by jbrady@jbrady_crayola_linux_orl

In next_RG_RP_L2a_clamp, qualify clamp_min and clamp_max with the fact that
  the vert is valid. Otherwise our mux will output vert 0 index and clamp
  with vert 1 banks and tags.

Change 111541 on 2003/07/16 by kmeekins@kmeekins_crayola_linux_orl

Backed out the removal of the cache miss condition in the cache_line_in_use signal.
  The cache miss is needed to prevent stalls on a cache hit sector miss condition.

Change 111425 on 2003/07/16 by mzini@mzini_crayola_linux_orl

 Increased timeout counters

Change 111370 on 2003/07/16 by mzini@mzini_crayola_linux_orl

 Added option to generate incremental data
```

```
Change 111283 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

Corrected a problem that was permitting new allocations to proceed when
  there was still data in-flight. Now looking for fetch contitions as
  opposed to cache miss conditions.

Change 111267 on 2003/07/15 by jcarroll@jcarroll_crayola_linux_orl

Added a data ready for the L2 coast reg.

Change 111221 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

Fixed typo that resulted in wrong sector mask value.

Change 111186 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

  vc_cc.v
vc_cc_loaded_busy.v
  vc_cc_tag_process.v
  --------------------
  Added more signals to the debug bus.
  Created a third debug bus.

  vc.v
  vc_debug.v
  ----------
  Created CC_DEBUG_DATA_2 bus.

Change 111133 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

vc_cc.v
  vc_cc_tag_process.v
  -------------------
  Created signals for performance monitor and debug bus.

  vc_cc_pack_align.v
  vc_cc_loaded_busy.v
  -------------------
  Corrected timing loop.
  Removed unused signals.

Change 110827 on 2003/07/14 by mzini@mzini_crayola_linux_orl

 Added option to run the TB with the memory model generating incremental data for tests
other than random

Change 110640 on 2003/07/12 by mmantor@mmantor_crayola_linux_orl
```

```
<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

Change 110492 on 2003/07/11 by kmeekins@kmeekins_crayola_linux_orl

- Removed the CF_CC_stall signal
  - Added the debug and performance monitor signals to the vc_cc.v I/O.
    Temporarily driving these values to zero.

Change 110473 on 2003/07/11 by kmeekins@kmeekins_crayola_linux_orl

- Cleaned up signal names.
  - Corrected sector_loaded control logic for multi-cycle fetch operations.
  - Cleaned up sector mask logic for non-256 bit fetch requests.

Change 110443 on 2003/07/11 by bbuchner@bbuchner_crayola_linux_orl

    added CC debug path in to debug module

Change 110250 on 2003/07/10 by jbrady@jbrady_crayola_linux_orl

Select request bus based on bit 6 again, not bit 7. This is the proper interleave.

Change 110248 on 2003/07/10 by mzini@mzini_crayola_linux_orl

 Bit 6 of the address selects controller pair and bit 7 selects the controller

Change 110110 on 2003/07/09 by mzini@mzini_crayola_linux_orl

 Show usage

Change 109960 on 2003/07/09 by bbuchner@bbuchner_crayola_linux_orl

     added register readback, modified cache invalidate, removied dc busy
```

```
Change 109932 on 2003/07/09 by mzini@mzini_crayola_linux_orl

 Changed the serialization of the constant and remapped the gpr_phase to match the SQ
hardware

Change 109930 on 2003/07/09 by jbrady@jbrady_crayola_linux_orl

Reverse constant serialization.
 Receive sq send on cycles 2301, not 0123.

Change 109897 on 2003/07/09 by mzini@mzini_crayola_linux_orl

 Fixed typo

Change 109760 on 2003/07/08 by mzini@mzini_crayola_linux_orl

 Added more error checking

Change 109759 on 2003/07/08 by mzini@mzini_crayola_linux_orl

 Added comment

Change 109758 on 2003/07/08 by mzini@mzini_crayola_linux_orl

 Enabled random fifo depths

Change 109719 on 2003/07/08 by kmeekins@kmeekins_crayola_linux_orl

Moved the error checking to its own process. Now testing only the cache address
  that is getting written.

Change 109701 on 2003/07/08 by kmeekins@kmeekins_crayola_linux_orl

Initial release.

Change 109661 on 2003/07/08 by viviana@viviana_crayola2_syn

Changed to the latest version of the Virage compilers.

Change 109658 on 2003/07/08 by kmeekins@kmeekins_crayola_linux_orl

vc_cc.v
  -------
  - Created new register name request_size_d1_q.
  - Created new signal to indicate a request size greater than 256 bit mode
    and attached it to required module I/O.

  vc_cc_pack_align.v
```

```
  vc_cc_tag_process.v
  -------------------
  New signal I/O

  vc_cc_loaded_busy.v
  -------------------
  - Created a new storage bit for request size in each cache line.
  - Added new logic to prevent allocation if all requested sectors are not loaded.

Change 109631 on 2003/07/07 by mzini@mzini_crayola_linux_orl

 Delete the results directory if the random tests passes

Change 109555 on 2003/07/07 by kmeekins@kmeekins_crayola_linux_orl

vc_cc.v
  -------
  Added request size to the pack_align interface.

  vc_cc_pack_align.v
  ------------------
  Using the request size to modify the sector mask for requests. The 512 bit
  mode will force a fetch of both sectors but only if at least one of the sectors
  has been requested. This improves the efficiency between 256 and 512 bit modes.

  vc_cc_tag_compare.v
  -------------------
  Created a way write enable for tag 0 and tag 1 to better control how a way is
  written when the same way is effected by two different tags.

Change 109167 on 2003/07/03 by mzini@mzini_crayola_linux_orl

 Script to submit multiple random tests

Change 109128 on 2003/07/03 by mzini@mzini_crayola_linux_orl

 Added error checking in RP

Change 109020 on 2003/07/03 by mzini@mzini_crayola_linux_orl

 Bumped timeout counters

Change 108937 on 2003/07/02 by kmeekins@kmeekins_crayola_linux_orl

Seperated the set valids for each tag to permit cache hit status to each
  way that is dependent on the tags. This prevents a tag 0 hit from altering
  the way replacement policy for tag 1 and vice versa.
```

```
Change 108887 on 2003/07/02 by jcarroll@jcarroll_crayola_linux_orl

VCRP: added debug, performance and prog depth FIFOs

Change 108858 on 2003/07/02 by mzini@mzini_crayola_linux_orl

 Bumped timout counters

Change 108857 on 2003/07/02 by jcarroll@jcarroll_crayola_linux_orl

Updated signal name: VC_SP_xyzw_cycle

Change 108840 on 2003/07/02 by mzini@mzini_crayola_linux_orl

 Added usage message

Change 108818 on 2003/07/02 by bbuchner@bbuchner_crayola_linux_orl

updated I/O

Change 108808 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Testbench enhancements

Change 108781 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Bumped timeout counters

Change 108778 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Added a slow sq mode where simd grants are issued less often

Change 108764 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Fixed fail checking

Change 108728 on 2003/07/01 by kmeekins@kmeekins_crayola_linux_orl

Changed the sector valid logic to correctly use the tag set id in determining
  the write enable.

Change 108723 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Cleanup

Change 108718 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Added ability to run VC testbench without dumping signals
```

```
Change 108701 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Testbench was timing out early in random tests

Change 108691 on 2003/07/01 by jcarroll@jcarroll_crayola_linux_orl

Added more support for 3 float data format.

Change 108685 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Rewrote the RP testbench to handle random tests

Change 108681 on 2003/07/01 by kmeekins@kmeekins_crayola_linux_orl

Corrected logic for multicycle control.

Change 108616 on 2003/06/30 by jcarroll@jcarroll_crayola_linux_orl

Added support for 3 float data format.

Change 108572 on 2003/06/30 by jcarroll@jcarroll_crayola_linux_orl

VCRP: Added logic to handle an L2 request with 4 invalid banks.

Change 108556 on 2003/06/30 by jbrady@jbrady_crayola_linux_orl

Add new 3 float format to count override mux.

Change 108523 on 2003/06/30 by jbrady@jbrady_crayola_linux_orl

Send written signals to MH on 256 bit boundaries, not 128 bit.
 Fix hook-up of written in testbench - were driven to 1. Not sure how we were passing..

Change 108519 on 2003/06/30 by mzini@mzini_crayola_linux_orl

Fixed data in return data path

Change 108512 on 2003/06/30 by mzini@mzini_crayola_linux_orl

The MI now send a written on every 256 bits of data instead of 128

Change 108403 on 2003/06/27 by mzini@mzini_crayola_linux_orl

 Don't always send data when receiver is ready

Change 108358 on 2003/06/27 by mzini@mzini_crayola_linux_orl
```

```
 Randomize the rdy to the MI

Change 108353 on 2003/06/27 by jbrady@jbrady_crayola_linux_orl

Fix internal_pipe_freeze. Only freeze if stage 1 rts, otherwise I'm looking
  at old data.

Change 108336 on 2003/06/27 by kmeekins@kmeekins_crayola_linux_orl

Corrected more sector, bank bit field mismatches.
  Conditioned the sector loading bits with the fetch size so that a fetch
  size greater that 256 will always fetch both sectors.

Change 108249 on 2003/06/27 by jcarroll@jcarroll_crayola_linux_orl

Increased timeout count.

Change 108147 on 2003/06/26 by mzini@mzini_crayola_linux_orl

Added trackinh of the data that gets piped along the VC to the SP

Change 108132 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Add wait for license to simv command line.

Change 108112 on 2003/06/26 by jcarroll@jcarroll_crayola_linux_orl

When clamping, vert0_offset is used for both even and odd requests.

Change 108097 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Remove nusiance error check code.

Change 108096 on 2003/06/26 by kmeekins@kmeekins_crayola_linux_orl

Added a register on the input FIFO read data to help with critical path timing.
  Changed the fifo valid register delay being used by the pack and align logic.

Change 108058 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Fix nstate for state 0a. Fix for both requests valid and not conflicting, where
  request 1 has sector mask of 0x3 and request size is 256.

Change 108023 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Use bit 7 off address to determine which interface to place request on, not bit 6.
  Bit 7 makes the interleave 1024 bits between interfaces, 512 on each mc.
 Fix bug in 256 bit request mode state machine. nstate was wrong for only
```

```
  request 1 valid in state 0a.

Change 108015 on 2003/06/26 by moev@moev2_r400_linux_marlboro

Fixed STAR connections in particualr the cmdscin signals.
cm1 gets STAR_testbus_rf[6], cm2 gets STAR_testbus_rf[7] and cm4 gets
STAR_testbus_rf[8]

Change 107914 on 2003/06/25 by jcarroll@jcarroll_crayola_linux_orl

Removed the coast regs for the L2 read address.
       Added coast regs for the L2 read data.

Change 107913 on 2003/06/25 by mzini@mzini_crayola_linux_orl

 Fixed bug in data return path. Plus added other 2 return paths

Change 107907 on 2003/06/25 by kmeekins@kmeekins_crayola_linux_orl

Corrected sector valid write enable logic.

Change 107845 on 2003/06/25 by jbrady@jbrady_crayola_linux_orl

Monitor on negedge, not posedge. Don't set done if !rtr.

Change 107792 on 2003/06/25 by viviana@viviana_crayola2_syn

Connected the STAR test patch signals to L1 cache, L2 cache, L2a, L2b fifos.
   Rebuilt the memories deleting the pipeline register inside.

Change 107789 on 2003/06/25 by mzini@mzini_crayola_linux_orl

Fixed interface comparison in MI testbench

Change 107708 on 2003/06/24 by mzini@mzini_crayola_linux_orl

Module to kill the sim if rtr's go low for too long

Change 107649 on 2003/06/24 by mzini@mzini_crayola_linux_orl

Fixed buildtb script to only include rtr_checker if running the full VCTB

Change 107639 on 2003/06/24 by mzini@mzini_crayola_linux_orl

Added a module to track how long rtr's stay low and kill the sim

Change 107595 on 2003/06/24 by kmeekins@kmeekins_crayola_linux_orl
```

```
Separated cache flush from reset logic. Cache flush now only effects
  the sector valids registers.
  Changed I/O names for the clock, reset, and cache flush signals to match
  top level.

Change 107561 on 2003/06/23 by mzini@mzini_crayola_linux_orl

Changed script to take tests.run as default

Change 107529 on 2003/06/23 by viviana@viviana_crayola2_syn

Changed the 64x21 to a 64x19 memory in the rg.

Change 107527 on 2003/06/23 by viviana@viviana_crayola2_syn

Rebuilt the memories to delete 64x21 and add 64x19 in the rp.

Change 107525 on 2003/06/23 by jcarroll@jcarroll_crayola_linux_orl

Added test pin connections to RAMs.

Change 107487 on 2003/06/23 by jbrady@jbrady_crayola_linux_orl

Change request_size to a 2 bit field from 1 bit.

Change 107447 on 2003/06/23 by kmeekins@kmeekins_crayola_linux_orl

Qualified the II request valids with the fetch sector to ensure only those
  addresses in need of fetching are valid.

Change 107209 on 2003/06/20 by mzini@mzini_crayola_linux_orl

Created VC regression script

Change 107178 on 2003/06/20 by jbrady@jbrady_crayola_linux_orl

Fix tests for full/partial tests - the boundary conditions were not right.
 Change clamp_count for partial max - must consider 8 dwords, not just valid dwords.

Change 107094 on 2003/06/19 by jbrady@jbrady_crayola_linux_orl

Set clamped count to 7 for fully clamped verts. It was necessary for min clamping.
 Set vert_offset to dw_addr[3:0] always -- it doesn't matter in fully clamped cases
now.

Change 107072 on 2003/06/19 by jbrady@jbrady_crayola_linux_orl

Rename clamped_count to unclamped_count. It's a better name.
```

```
 Change unclamped_count to be count_lo - clamp_count - 1. It now reflects
  the number of clamped words in the vert, not per 8 dwords.
 For partial min, set vert_offset to dw_addr, not base_addr. This is necessary
  for the vcrp to know how many dw's to clamp at the beginning of the vert. Otherwise
  it's ambiguous which dw's are clamped, and which are unclamped.

Change 107070 on 2003/06/19 by jcarroll@jcarroll_crayola_linux_orl

Added logic to VCRP to handle clamp_x = 1

Change 107000 on 2003/06/19 by jbrady@jbrady_crayola_linux_orl

Move tag merge to after conflict detection. only merge if there are no conflicts.
 fixes merge_conflict test and is necessary for clamping.

Change 106891 on 2003/06/18 by bbuchner@bbuchner_crayola_linux_orl

add additional debug busses

Change 106842 on 2003/06/18 by jcarroll@jcarroll_crayola_linux_orl

Added all of the clamping logic.

Change 106795 on 2003/06/18 by jbrady@jbrady_crayola_linux_orl

Wire rbiu decoded fifo depth to vcmi_receiver fifos instead of hardcoding to 16.

Change 106783 on 2003/06/18 by bbuchner@bbuchner_crayola_linux_orl

added control and fifo size regs

Change 106727 on 2003/06/18 by mzini@mzini_crayola_linux_orl

Only capture data when both rdy and rtr are high

Change 106621 on 2003/06/17 by mzini@mzini_crayola_linux_orl

 Only compare valid verts when data gets moved from L2->l1

Change 106618 on 2003/06/17 by jbrady@jbrady_crayola_linux_orl

>    //  Even banks only conflict if even tags aren't equal. Therefore, we
 >    //   can compare vcrg4_gen_even_tag0_bank_mask instead of vcrg4_even_tag1_valid
 >    //   because there will not have been a merge. Same goes for valids.
 >    //   This helps timing. Same goes for odd bank conflict.

Change 106591 on 2003/06/17 by mzini@mzini_crayola_linux_orl
```

```
Randomize TC_VC_simd_id

Change 106581 on 2003/06/17 by jbrady@jbrady_crayola_linux_orl

Keep L1_rdy, L2a_rdy, and CC_rdy high even if rtr=0.
 Remove programmability from instruction fifo depth.

Change 106570 on 2003/06/17 by mzini@mzini_crayola_linux_orl

Made memory return data out of order by default

Change 106565 on 2003/06/17 by mzini@mzini_crayola_linux_orl

 Added option to return data from memory out of order

Change 106562 on 2003/06/17 by jbrady@jbrady_crayola_linux_orl

only write to input_fifo when rtr is high. cc leaves rdy high even when
  rtr is low.

Change 106553 on 2003/06/17 by mzini@mzini_crayola_linux_orl

 Make sure the RTR's are high before sampling data

Change 106539 on 2003/06/17 by mzini@mzini_crayola_linux_orl

Added VC->SQ interface tracking

Change 106512 on 2003/06/17 by jcarroll@jcarroll_crayola_linux_orl

Changed end_of_group logic to only strobe on last transfer.

Change 106483 on 2003/06/17 by mzini@mzini_crayola_linux_orl

Added more time at the end of the sim once the input files have been read

Change 106414 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Fixed the data return path from the MI for RP testbench

Change 106408 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Fixed vc_rg_rp2.tr file so that null_request field shows properly

Change 106390 on 2003/06/16 by jbrady@jbrady_crayola_linux_orl

Fix width of constant - it changed when we removed border color.
```

```
Change 106387 on 2003/06/16 by jcarroll@jcarroll_crayola_linux_orl

L2a interface change for clamping.

Change 106386 on 2003/06/16 by jbrady@jbrady_crayola_linux_orl

Remove border_color from vc.
 Move L2 null request into the L2 data field for non-clamped entries.

Change 106384 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Removed null_request and border_color from RG->RP1 interface

Change 106373 on 2003/06/16 by jcarroll@jcarroll_crayola_linux_orl

Removed internal register for gpr_phase so that output data
       will sync to external gpr_phase.

Change 106368 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Made tbmod_sqvc drive gpr_phase instead of tb_vc for the rp testbench

Change 106344 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Drive simd_id ready's in VC environment

Change 106320 on 2003/06/16 by jcarroll@jcarroll_crayola_linux_orl

Fixed a bug.  One piece of L2 read data was being lost when both
       L1 buffers were full and the entire L2 pipe was frozen.  Fixed by
       adding a coast reg that stores the L2 read address when the entire
       L2 pipeline is held.

Change 106311 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Set gpr_phase even when there's no valid data to the VC

Change 106181 on 2003/06/14 by mzini@mzini_crayola_linux_orl

 Removed print statements

Change 106179 on 2003/06/14 by mzini@mzini_crayola_linux_orl

 Make sure number of transfers on each tracked interface exactly matches betwee the HW
and emu

Change 106176 on 2003/06/14 by mzini@mzini_crayola_linux_orl
```

```
Renamed element to set

Change 106112 on 2003/06/13 by jbrady@jbrady_crayola_linux_orl

add 128x128 memory.

Change 106069 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

vc_cc.v
  -------
  Added a registered version of the input fifo read enable to detect a non-valid
  fifo entry for the CC->RP interface.

  vc_cc_pack_align.v
  ------------------
  - Fixed the CC_RP_L2b_rdy to permit a non-valid entry into the L2b FIFO.
  - Swizzled the bank mask bits to agree with the RG on the bank representation.

Change 106050 on 2003/06/13 by mzini@mzini_crayola_linux_orl

 Added gpr_phase in vc_rp_sp.dmp

Change 106031 on 2003/06/13 by mzini@mzini_crayola_linux_orl

Fixed vc output tracker

Change 106023 on 2003/06/13 by bbuchner@bbuchner_crayola_linux_orl

removed skew from DC signals; added thread type, cycle

Change 106012 on 2003/06/13 by jbrady@jbrady_crayola_linux_orl

Instantiate ati_dff_out's for all outputs instead of inferring regular flops.

Change 106009 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

Corrected multicycle determination logic.

Change 106008 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

Corrected syntax for user supplied compile options file.

Change 106007 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

Changed element_id to way_id to match spec and CC->MI port names.

Change 105940 on 2003/06/12 by jcarroll@jcarroll_crayola_linux_orl
```

```
Added RP_DC_thread_type to I/O
       First revision of VCRP with all functionality (except clamping).

Change 105927 on 2003/06/12 by mzini@mzini_crayola_linux_orl

 Added thread type

Change 105916 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Fix replication syntax error.

Change 105908 on 2003/06/12 by bbuchner@bbuchner_crayola_linux_orl

use behavioral memories

Change 105903 on 2003/06/12 by bbuchner@bbuchner_crayola_linux_orl

remove dup. tracker

Change 105900 on 2003/06/12 by kmeekins@kmeekins_crayola_linux_orl

Added tbmods for CC standalone testbench.
  Assigned values to MH_TC_start0, 1, and 2 to get stall and flush signals known.

Change 105888 on 2003/06/12 by mzini@mzini_crayola_linux_orl

 Fixed typo

Change 105869 on 2003/06/12 by mzini@mzini_crayola_linux_orl

 Fixed vc_out tracker

Change 105852 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Added gpr phase to Rp testbench

Change 105843 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Only compare valid dwords

Change 105829 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Add vcmi debug monitor ports.
 Propagate x's through some muxes.

Change 105823 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Do not trigger a compare if it's a null request
```

```
Change 105816 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Last and clamp were swaped

Change 105767 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Add vcrg debug monitor.

Change 105766 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Add debug monitor signals.
 Propagate x's in vcrg0_data_format_min_count case statement.

Change 105765 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Remove possible index out of range error for 12 & 8 dword verts on next_done.
 Remove leda error on size mismatch for done reset value.

Change 105756 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Reordered vc_L2_L1.tr

Change 105740 on 2003/06/12 by kmeekins@kmeekins_crayola_linux_orl

Added the macro for VC_PATH definition.

Change 105687 on 2003/06/11 by jcarroll@jcarroll_crayola_linux_orl

Updates to the VCRP ports
       Added yet more functionality!!!!!

Change 105679 on 2003/06/11 by jcarroll@jcarroll_crayola_linux_orl

Fixed model

Change 105675 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Once bank valids are set keep them set

Change 105671 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Setting only the valid bank readys on the CC->RP snoop bus

Change 105668 on 2003/06/11 by mzini@mzini_crayola_linux_orl

 Fixed copy-paste error
```

```
Change 105666 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Added RP->SP file

Change 105626 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Changed some assignments to non-blocking

Change 105610 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Fixed L2->L1 dump

Change 105607 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Added USE_BEHAVE_MEM define to the RP testbench

Change 105573 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Correctly read mi_rp file

Change 105566 on 2003/06/11 by mzini@mzini_crayola_linux_orl

CC->RP signals changed names

Change 105556 on 2003/06/11 by kmeekins@kmeekins_crayola_linux_orl

Changed the cache_flush logic to use cache_stall_q.

Change 105547 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Fixed build script

Change 105545 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Fixed build script

Change 105542 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Added RP tesbench modules

Change 105520 on 2003/06/11 by jbrady@jbrady_crayola_linux_orl

Use partial products to save area in addr_calc.

Change 105389 on 2003/06/10 by kmeekins@kmeekins_crayola_linux_orl

Added tbmod_rg_cc.v.
```

```
Change 105386 on 2003/06/10 by mzini@mzini_crayola_linux_orl

Additions for the CC testbench

Change 105384 on 2003/06/10 by kmeekins@kmeekins_crayola_linux_orl

Changed the LRU logic to use the set cache hit result. This correctected the
   problem of incrementing all but the hit way.

Change 105383 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add the following performance monitors:
 >               RG_PERF_megafetch_event,
 >               RG_PERF_end_of_group_event,
 >               RG_PERF_conflict_event,
 >               MI_PERF_requests_event

Change 105382 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add the following performance monitors:
 >               RG_PERF_megafetch_event,
 >               RG_PERF_end_of_group_event,
 >               RG_PERF_conflict_event,

Change 105371 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add performance monitor signal MI_PERF_requests_event.

Change 105370 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add performance monitor signal MI_PERF_requests_event.
 Enumerate state machine states with "parameter" to make leda happy.
 Declare next_vcmi1_request_0_mem_addr_msbs and next_vcmi1_request_1_mem_addr_msbs
  as intermediate steps in constructing next_vcmi1_request_0_mem_addr and
  next_vcmi1_request_1_mem_addr to make leda happy.

Change 105366 on 2003/06/10 by mzini@mzini_crayola_linux_orl

Resubmitting stupid fix

Change 105362 on 2003/06/10 by mzini@mzini_crayola_linux_orl

Drive mc_send2 and mc_send3 to 0 for now

Change 105353 on 2003/06/10 by bbuchner@bbuchner_crayola_linux_orl

added additional performance monitoring to RG
```

```
Change 105320 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

added performance monitor outputs RG_PERF_vertices_event, RG_PERF_clamped_event,
  RG_PERF_L2_request_event, RG_PERF_L1_request_event.
 moved dw_end_address calculation from vcrg_tag_gen to vcrg_addr_calc for timing.
 added count feature for backward compatibility. if count_lo is too small for
  data_format, we bump it up to the proper # of dwords for the data_format.

Change 105319 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

added the dw_end_addr calculation here. it's better for timing - mc can still make it.

Change 105317 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

dw_end_addr is calculated a cycle earlier for timing. it's now an input to the block,
  not calculated here.

Change 105316 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add 4 RG performance monitor outputs.

Change 105285 on 2003/06/10 by bbuchner@bbuchner_crayola_linux_orl

typo

Change 105047 on 2003/06/09 by bbuchner@bbuchner_crayola_linux_orl

       fixed merge problem

Change 105045 on 2003/06/09 by bbuchner@bbuchner_crayola_linux_orl

add debug module

Change 105041 on 2003/06/09 by jbrady@jbrady_crayola_linux_orl

Remove leda error by declaring intermediate end signal. Leda wants a carry bit.
  The carry bit is not flopped. Doesn't affect function or synthesis.

Change 104967 on 2003/06/09 by bbuchner@bbuchner_crayola_linux_orl

    added performance monitoring block

Change 104958 on 2003/06/09 by jbrady@jbrady_crayola_linux_orl

Implement rotating priority for selecting which mc to send to a particular bank.

Change 104566 on 2003/06/06 by kmeekins@kmeekins_crayola_linux_orl
```

```
Inserted AUTO_CONSTANT construct to remove constants from sensitivity lists.

Change 104543 on 2003/06/06 by kmeekins@kmeekins_crayola_linux_orl

Corrected templates to fix snooped write enable name changes.

Change 104439 on 2003/06/05 by viviana@viviana_crayola2_syn

vc_rf_awt_gate.v had two instantiations of the module.  This occurs whenever
   the directory where the virage files get generated is not removed before
   remaking any changes to any of the memories.

Change 104367 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

update cc bank write snoop interface.

Change 104361 on 2003/06/05 by jcarroll@jcarroll_crayola_linux_orl

Changed names of CC snooping signals.

Change 104349 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to relect they are no longer driven by registers.
  Changed bank write names to match change in snooped MI signals.

Change 104346 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to reflect that they are no longer driven by registers.
  Created delayed versions of the cache miss signals for tag 0 and 1 and
  connected them to vc_cc_loaded_busy for use with the cache line in use logic.

Change 104344 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to relect that they are no loger driven by registers.
  Added cache miss for tag 0 and tag 1 to input ports to use with the
  cache line in use logic.

Change 104341 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to reflect no longer driven by registers.

Change 104335 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

some regs had to be wires.

Change 104333 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

add RG_RP_L2a_vert_0_offset to vcrp instantiation.
```

```
Change 104321 on 2003/06/05 by mzini@mzini_crayola_linux_orl

Some signals in RP had name changes

Change 104318 on 2003/06/05 by jcarroll@jcarroll_crayola_linux_orl

I/O changes to L2a input data.

Change 104291 on 2003/06/05 by jcarroll@jcarroll_crayola_linux_orl

Change RAM sizes of L1 fifo and L2a fifo.
       Continued adding required functionality.
       Tons of internal name changes.

Change 104280 on 2003/06/05 by bbuchner@bbuchner_crayola_linux_orl

fixed leda errors.  Reduced SP return data width from 68 to 32 bits per index

Change 104218 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

Add thread_type to testbench.
 Fix dst_gpr in tbmod_sqvc.

Change 104201 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

change 16x69 memory to 16x70 to add thread_type.

Change 104200 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

Remove SQ_VC_send from RG_busy for synthesis reasons, and because we
  are covered by SQ_VC_wake_up for that cycle.
 Make vcrg4_request_size 2 bit vector to match the rest of the pipe.

Change 104199 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

Changed some memory files: 16x69 to 16x70
                           64x17 to 64x21
                           128x45 to 128x47

Change 104162 on 2003/06/04 by viviana@viviana_crayola2_syn

Changed 16x69 memory to 16x70, 64x17 to 64x21, 128x45 to 128x47 and
   added 2 more instances of 128x16.

Change 104158 on 2003/06/04 by kmeekins@kmeekins_crayola_linux_orl

Connected CF_CC_stall and CF_CC_cache_flush.
```

```
Change 104148 on 2003/06/04 by kmeekins@kmeekins_crayola_linux_orl

Simplified the sector fetch logic.
  Optimized the cache hit and cache miss logic.
  Corrected the fetch way generation for cache misses.

Change 104142 on 2003/06/04 by bbuchner@bbuchner_crayola_linux_orl

        connecte up cf unit

Change 104121 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

use non-block assignments in clock process.

Change 104120 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

connect memory return bus up to vc.
 extend reset a little longer.

Change 104117 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Add some new test signals for vcmi fifos 2 and 3.

Change 104114 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Added memory macro test I/O.

Change 104113 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

 Added arbiter and data path from input fifos to RP.
  Arbiter always gives priority to mc0 return data. This will change to
  a revolving priority in a later check-in.
 Added test I/O for memory macros.

Change 104112 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Add test I/O.

Change 104106 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Fixed typo

Change 104103 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Use non-blocking assignments where necessary

Change 104102 on 2003/06/04 by mzini@mzini_crayola_linux_orl
```

```
Added dump files coming out of memory and the MI

Change 104101 on 2003/06/04 by bbuchner@bbuchner_crayola_linux_orl

      fixing I/O, added cache flush moduel(not yet hooked up) and data converter unit

Change 104069 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Look for X's in the data readys

Change 104064 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

change to non-blocking assignments in clock process.

Change 104054 on 2003/06/04 by mzini@mzini_crayola_linux_orl

 Use Or'ed reset

Change 104040 on 2003/06/04 by mzini@mzini_crayola_linux_orl

 Look at thedelay reset

Change 104032 on 2003/06/04 by mzini@mzini_crayola_linux_orl

 Check for X's on the data ready

Change 104029 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Check for X's on the data ready's

Change 103984 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Added VC->SP tracker

Change 103970 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Renamed usc_ati_master_clock_gater_sclk_vc to uvc_ati_master_clock_gater_sclk_vc.

Change 103912 on 2003/06/03 by mzini@mzini_crayola_linux_orl

Added L2->L1 interface tracking

Change 103888 on 2003/06/03 by mzini@mzini_crayola_linux_orl

Added thread_type to VC
 Added TB_RP modules
```

```
Change 103789 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Remove 8x256 RAM macro from compile. It's not used anymore and was generating
  a warning.

Change 103777 on 2003/06/03 by viviana@viviana_crayola2_syn

Deleted two 8x256 memories.

Change 103776 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Change sclk to sclk_vc.
 Change reset to RS_MI_reset.
 Add I/O to RP (not driven yet).

Change 103775 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_MI_reset.

Change 103774 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_MI_reset.
 Add RP I/O to vcmi_receiver instantiation.

Change 103773 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_RG_reset.

Change 103772 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_RG_reset.
 Change some combinational assignments from non-blocking to blocking for leda.

Change 103771 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename usc_ati_master_clock_gater_vc_clk to usc_ati_master_clock_gater_sclk_vc.
 Rename resets on vcmi and vcrg to match vc names.
 Rename sclk on vcmi and vcrg to sclk_vc.

Change 103689 on 2003/06/02 by kmeekins@kmeekins_crayola_linux_orl

Included header.v.

Change 103681 on 2003/06/02 by mzini@mzini_crayola_linux_orl
```

```
SQ model now reads simd_id from the test file

Change 103655 on 2003/06/02 by jbrady@jbrady_crayola_linux_orl

Fix set bits in info field. Should include even/odd bit (mem_addr[6]).

Change 103649 on 2003/06/02 by jbrady@jbrady_crayola_linux_orl

Fixed a typo that caused one index to be repeated and one dropped.
 Fixed conflict_serialization. It wasn't holding it's value for external_freeze. Fix
  was to only let it change values with a vcrg5_load.

Change 103648 on 2003/06/02 by jbrady@jbrady_crayola_linux_orl

Change VC_TCx_info field to 8 bits wide, and drive it from vcmi_requestor.
 Enable VC_TCx_info tracker.

Change 103561 on 2003/06/02 by mzini@mzini_crayola_linux_orl

Force pre_rdy low once file has ended

Change 103527 on 2003/06/02 by mzini@mzini_crayola_linux_orl

Exclude vc_mem.v from rg testbencvh

Change 103525 on 2003/06/02 by mzini@mzini_crayola_linux_orl

Let the memory model drive MH->VC RTR's

Change 103500 on 2003/06/01 by mzini@mzini_crayola_linux_orl

Submodule testbench infrastructure in place

Change 103446 on 2003/05/30 by mzini@mzini_crayola_linux_orl

 Modified scripts and vc.v to handle module testbenches

Change 103382 on 2003/05/30 by bbuchner@bbuchner_crayola_linux_orl

       vc now builds with rest of chip

Change 103378 on 2003/05/30 by jbrady@jbrady_crayola_linux_orl

Remove ram macro index fifo and replace with flop based fifo. saves about
  0.078mm2 right now. may reduce it further...

Change 103308 on 2003/05/30 by mzini@mzini_crayola_linux_orl
```

```
 Fixed build script

Change 103286 on 2003/05/30 by jbrady@jbrady_crayola_linux_orl

changed clamping conflict logic:
    // ---------------------------------------------------------------
    //  Detect conflicts due to clamping
    //   Conflict when both verts are valid and vert 0 is clamped.
    //   Conflict when vert 1 is valid and clamped.
    //   Don't conflict when vert 0 is valid and clamped but vert 1 is not valid.
    //   If only vert 1 is valid, and it is clamped, we'll conflict and send
    //    an invalid vert 0, but this should be OK. It shouldn't happen in
    //    the real world anyway, because verts should be packed toward the
    //    lower relative offsets.
    // ---------------------------------------------------------------

Change 103270 on 2003/05/30 by mzini@mzini_crayola_linux_orl

Define _VCAPI

Change 103261 on 2003/05/30 by jbrady@jbrady_crayola_linux_orl

flop TC_VC0_rtr and TC_VC1_rtr before using them.

Change 103166 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

fix for l2a_vert_0_offset. was being set to vert_1_offset on 2nd cycle when only
  vert 0 was clamped. vert 1 was not clamped, so l2a_vert_0_offset should have
  vert 0's offset.

Change 103154 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

clamp count was not biased by 1, so change constant in subtract from 7 to 6.

Change 103092 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

change default parameter to match size of memory macro. this prevents synthesis
  from complaining during an analyze.

Change 103089 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

change default parameters to match actual size of fifo. this way synthesis
  doesn't complain about mismatching ports and always re-analyze this module.

Change 103085 on 2003/05/29 by kmeekins@kmeekins_crayola_linux_orl

Added the definitions for cc_rp_stall and cc_mi_stall.
```

```
Change 103084 on 2003/05/29 by kmeekins@kmeekins_crayola_linux_orl

Included transfer_cycle_q in the definition of CC_RP_L2b_rdy to prevent multiple
  L2b FIFO writes of the same request.

Change 103077 on 2003/05/29 by mzini@mzini_crayola_linux_orl

Fixed build script to include behavioranl memories for the RP block for simulation

Change 103071 on 2003/05/29 by viviana@viviana_crayola2_syn

Corrected the patchin and patchout signals.

Change 103056 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

Wired STAR_scforce_16 into vcrg. This goes along with the change from an 8 deep
  to 16 deep instruction fifo.

Change 103055 on 2003/05/29 by jcarroll@jcarroll_crayola_linux_orl

I/O changes (CC_RP readys)
       Adding more functionality

Change 103050 on 2003/05/29 by bbuchner@bbuchner_crayola_linux_orl

 fixed mismatching signal names

Change 103015 on 2003/05/29 by bbuchner@bbuchner_crayola_linux_orl

   fix signal name from L2B to L2b

Change 102979 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

Implement clamping feature
 change vert_0_offset to 4 bits from 5
 change to 16 deep instruction fifo
 add stage to pipe - new stage 4. output is now stage 5.

Change 102978 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

add RG_RP_L2a_clamp to RG instantiation
 change RG_RP_L2a_vert_1_offset to  RG_RP_L2a_data
 change RG_RP_L2a_vert_0_offset to 4 bits from 5 bits

Change 102977 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Added `include "vc_cc_define.v"
```

```
Change 102975 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

add clamping feature before tag generation
 change vert_offset to 4 bit field from 5 bits.

Change 102974 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

instantiate 16 deep memory macro from 8 deep. this goes with the change
  from a 4 dword to 8 dword machine.
 make default width 69 to match memory

Change 102973 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

add a missing 'end' statement

Change 102972 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

Increase counter limits to 16 for instruction fifo depth.

Change 102971 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

change 8 deep instruction fifo to 16 deep

Change 102970 on 2003/05/28 by bbuchner@bbuchner_crayola_linux_orl

  instantiate RP, modifiy signal names to match SP/SQ

Change 102968 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Changed input_fifo_rdata to use "wire" type.

Change 102961 on 2003/05/28 by mzini@mzini_crayola_linux_orl

Interface chnages for clamping

Change 102936 on 2003/05/28 by jcarroll@jcarroll_crayola_linux_orl

            Fixed syntax error on outreg_en.

Change 102930 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Initial release.

Change 102929 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Added input FIFO data fields.
```

```
Change 102928 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Removed include directive.

Change 102906 on 2003/05/28 by jcarroll@jcarroll_crayola_linux_orl

Added more of the functionality.

Change 102903 on 2003/05/28 by jcarroll@jcarroll_crayola_linux_orl

Added an output register enable (outreg_en)

Change 102901 on 2003/05/28 by viviana@viviana_crayola2_syn

Changed the 69x8 to 69x16, deleted 32x32 and replaced with 32x64.

Change 102892 on 2003/05/28 by mzini@mzini_crayola_linux_orl

runvc script now handles random tests

Change 102853 on 2003/05/28 by bbuchner@bbuchner_crayola_linux_orl

added vc_reset.v

Change 102840 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

fix i/o list finishing with ,
 instantiate fifos 3 and 4 for synthesis

Change 102837 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

Start of clamping logic.
 Fix for tag generation. Was adding 1 to tag_b bit 5 instead of bit 4.

Change 102812 on 2003/05/28 by mzini@mzini_crayola_linux_orl

 Added VC testbench HOWTO

Change 102728 on 2003/05/27 by bbuchner@fl_bbuchner_r400_win

vc reset logic

Change 102536 on 2003/05/25 by mzini@mzini_crayola_linux_orl

Properly initialize memory model

Change 102486 on 2003/05/24 by mzini@mzini_crayola_linux_orl
```

```
Script for running VC testbench tests

Change 102456 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

put lines of code inside begin/end for case. it was a cut/paste to the wrong
 lines.

Change 102455 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

don't send request on state 1 in 256 bit mode if both sector bits aren't set.

Change 102404 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

Fix lsb of address in states 00 and 10.

Change 102384 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Not ready for integration.

Change 102383 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Removed cache miss and sector miss signals from the I/O.
  Only used internally now.

Change 102381 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Maded major changes to use fetch and hit addresses to increment "busy" counter.

Change 102380 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Added definitions for RG_CC input FIFO parameters.

Change 102375 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

Issue two requests when in 256 bit mode and sector mask is '11'

Change 102367 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Changed reset to use cache_flush.

Change 102202 on 2003/05/22 by mzini@mzini_crayola_linux_orl

 Made rg->cc file wasier to read

Change 102132 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Added freeze logic.
```

```
Change 102125 on 2003/05/22 by jcarroll@jcarroll_crayola_linux_orl

Initial revision

Change 102116 on 2003/05/22 by jbrady@jbrady_crayola_linux_orl

fix typo. had /, should have been '

Change 102114 on 2003/05/22 by jbrady@jbrady_crayola_linux_orl

remove extra -v

Change 102112 on 2003/05/22 by jcarroll@jcarroll_crayola_linux_orl

Initial Revisision

Change 102105 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Included logic for determining fetch and cache hit addresses for
  tag 0 and tag 1.

Change 102091 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Added freeze logic.

Change 102089 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Added freeze logic.

Change 102075 on 2003/05/22 by jbrady@jbrady_crayola_linux_orl

Make change to tag gen logic to handle 8 dword verts now, not just four.
 Cache width stayed 512 bits, though, so I couldn't just change FOUR_DWORD_VERT
  in vc_common, because that assumed the cache doubled to 1024 bits with 256 bit
  banks. Now a vert can span 3 128 bit banks.

Change 101991 on 2003/05/21 by jcarroll@jcarroll_crayola_linux_orl

Initial checkin

Change 101946 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Remove another timing loop in external_pipe_freeze.

Change 101942 on 2003/05/21 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
```

```
  Not ready for integration.

Change 101922 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Add memory macros.

Change 101921 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Fix prog_depth width warnings.

Change 101920 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Module compiler source code for vcrg_addr_calc

Change 101919 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Use ati_dff_out for VC_SQ outputs.
 Fix timing loop in pipe_freeze/RG_RP_L1_rdy.

Change 101918 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

add vcmi memories to vcs invocation

Change 101885 on 2003/05/21 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Not ready for integration.

Change 101824 on 2003/05/20 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Not ready for integration.

Change 101796 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

fix typo on memory interface

Change 101732 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add test I/O.

Change 101730 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add in MH ports that were clobbered.

Change 101729 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Instantiate RAM and test I/O.
```

Change 101728 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Instantiate RAMs and test I/O.

Change 101727 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add test I/O.

Change 101726 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Instantiate test and scan logic and I/O.

Change 101725 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add test interface to vc instantiation - tie to zero and drive test clock.

Change 101724 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Put memory -v's in front of library -y's so we get the _rtl versions without
 timing.

Change 101682 on 2003/05/19 by viviana@viviana_crayola2_syn

Added the virage modules and memories.

Change 101640 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

fix prog_depth port width.

Change 101637 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

First check in. Just instantiates input fifos.

Change 101636 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

Add data and info ports to vcmi.

Change 101635 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

Instantiate vcmi_receiver.

Change 101633 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

Fix sensitivity list.

Change 101626 on 2003/05/19 by mzini@mzini_crayola_linux_orl

```
Fixed data return

Change 101590 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

Move stride and index_round from instruction fifo to constant fifo - they are
 only used for megafetches, and this saves area.

Change 101499 on 2003/05/18 by mzini@mzini_crayola_linux_orl

 Added MH->VC files

Change 101497 on 2003/05/18 by mzini@mzini_crayola_linux_orl

 Fixed random delays

Change 101423 on 2003/05/16 by mzini@mzini_crayola_linux_orl

Coded data return path in the memory model

Change 101388 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

add RG_busy output.
 set instruction fifo depth to 8.
 store index valids in index fifo now, not instruction fifo. they go in the sign
 position of the float index. the exponent msb's get cleared for negative numbers
 now, so negative numbers still clamp to zero because their exponent is < 64. this
 allows us to save 64 bits in instruction fifo, selected_valids muxing, and valid
 reconstruction flops.

Change 101387 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

valids don't come out of instruction fifo anymore. we get 16 valids with their
 indices out of the index fifo (valids in msb of index). the selected_valids
 mux goes away.

Change 101385 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

hardwire sign bit to 0 (positive). negative indices have their exponent
 clamped to <=63 now, so they are clamped to zero by the exponent compare.

Change 101384 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

add RG_busy port to vcrg

Change 101382 on 2003/05/16 by mzini@mzini_crayola_linux_orl

Instr FIFO depth changed from 16 to 8
```

```
Change 101364 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

qualify next_vc_tcx_send with vcmi1_rts, else we propogate x's

Change 101067 on 2003/05/14 by mzini@mzini_crayola_linux_orl

 Fixed rdy behacior

Change 101059 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

fix serialization of constant 1 base address.

Change 101049 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

fix type 2'b1 to 2'b01

Change 101035 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

add another condition to MI_CC_rtr (|| input_fifo_re) to prevent unnecessary
 lowering of rtr.

Change 101019 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

Don't send last_index_of_vv during both cycles of a conflict serialization. Only
 send it on the last cycle of the serialization.

Change 100934 on 2003/05/14 by mzini@mzini_crayola_linux_orl

 Added CC->MI interface tracker

Change 100872 on 2003/05/14 by mzini@mzini_crayola_linux_orl

Added MI->MH interface tracker

Change 100871 on 2003/05/14 by mzini@mzini_crayola_linux_orl

Stop sending ddata once the file is empty

Change 100833 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Fix stage 2 control.
 Fix typo where vc0_tc_request_type was assigned twice, and vc1 wasn't there at all.

Change 100809 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Force unused rtrs to 1

Change 100806 on 2003/05/13 by mzini@mzini_crayola_linux_orl
```

```
Fix cut/paste errors in output mux. Only change stage 2 control when vcmi2_load
 is true. Fix cut/paste error in vc0_tc_send flop.

Change 100793 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Added CC trackers and drivers

Change 100790 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

De-muxed piping of request_type.

Change 100780 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Only check one request for local memory aperature. Since both requests are to
 the same surface, they will both be local or agp. This saves some big comparitors.

Change 100770 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Initial check-in of memory interface module. Only has requestor, not data return
 path at this time.

Change 100768 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Add memory request ports to vc instantiation.

Change 100766 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Instantiate memory interface module (vcmi).

Change 100765 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Instead of sending fb_size, compute fb_start+fb_size and send it out as
 fb_end.

Change 100699 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Only enable SQ->VC interface after reset

Change 100671 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Only save megafetch_offset on megafetches. It was getting updated for minis also.

Change 100574 on 2003/05/12 by mzini@mzini_crayola_linux_orl

Fixed odd set conflict check

Change 100480 on 2003/05/12 by mzini@mzini_crayola_linux_orl
```

```
Fixed FIFO counts

Change 100254 on 2003/05/09 by mzini@mzini_crayola_linux_orl

Changed VCCC output monitors

Change 100190 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

change sector_mask to bank_mask

Change 100187 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

generate 4 bit bank mask rather than 2 bit sector mask. made it parametizable for
 4 or 8 dword indices.

Change 100185 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

Remove unused loop1 integer

Change 100182 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

change sector_mask to bank_mask. also change conflict detection logic to detect
 conflict between even0 and odd1, or between odd0 and even1

Change 100181 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

Add DWORD_SIZE and FOUR_DWORD_INDICES

Change 100180 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

Change RG_CC_sector_mask to RG_CC_bank_mask

Change 99998 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl

tb_vc - hook up rbbm interface
 vc_rbui - use registered version of rbbm inputs, not the inputs themselves

Change 99965 on 2003/05/08 by mzini@mzini_crayola_linux_orl

Fixed RBBM interface

Change 99956 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl

First check-in of RBBM interface and render state decode module for vc.

Change 99955 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl
```

```
Added rbbm interface and vc_rbiu.v

Change 99947 on 2003/05/08 by mzini@mzini_crayola_linux_orl

RBBM interface

Change 99946 on 2003/05/08 by mzini@mzini_crayola_linux_orl

Added RBBM interface

Change 99902 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl

Fix typo for syntax

Change 99868 on 2003/05/08 by mzini@mzini_crayola_linux_orl

Added VC behavioral memory

Change 99546 on 2003/05/07 by mzini@mzini_crayola_linux_orl

 Added vccc signals to testbench

Change 99528 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Parameterize # of SP's on instantiation of vc.v.

Change 99527 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Parameterize # of SP's (# of valids and indices)

Change 99524 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Leda clean up.
 Parameterize # of SP's.

Change 99522 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Add defines for parameterization of # of SP's.

Change 99521 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Add ifdef's around SP2 and SP3 input ports for 8 and 12 pipe versions.

Change 99183 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl

First check-in of common file with vc defines and parameters.

Change 99182 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl
```

```
Add set conflict detection and serialization.
 Fix RG_RP_L2a_null_request pipeline typo.

Change 99180 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl

Set next_vertex_pair_mask to 0 in the case where no indices in the group of 16
 were valid. This indicates a null request gets sent down the L2 fifo.

Change 99179 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl

Prevent x's from propagating through dw_addr or spans_banks into the tag valids by
 or'ing with vertex valid at the output of the module.

Change 98936 on 2003/05/02 by mzini@mzini_crayola_linux_orl

Fixed tag gen

Change 98935 on 2003/05/02 by mzini@mzini_crayola_linux_orl

Only check valid transfers on trackers

Change 98898 on 2003/05/02 by mzini@mzini_crayola_linux_orl

Added trackers for all the VC_RG outputs

Change 98893 on 2003/05/02 by jbrady@jbrady_crayola_linux_orl

qualify conflict_serialization assignment with vcrg3_ready

Change 98892 on 2003/05/02 by jbrady@jbrady_crayola_linux_orl

First check in of vcrg.

Change 98891 on 2003/05/02 by jbrady@jbrady_crayola_linux_orl

First check in of address generator.

Change 98757 on 2003/05/02 by mzini@mzini_crayola_linux_orl

 Added vc and tb_vc structures to parts_lib
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ais/sq_alu_instr_seq.v
... #17 change 51526 edit on 2002/09/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- gpr dealloc connected
- static gpr allocation added (but not enabled)
- ppb btwn pism and ptb added

... #16 change 50806 edit on 2002/09/11 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixes for bug326 and 329 - tests still fail, but for different reasons

... #15 change 48974 edit on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- needed to drive acfs_reading one cycle earlier for ACFS IS read
- updated/added new SQ_SP instruction interface

... #14 change 46251 edit on 2002/08/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates for pop/winner_ack status reg conflict

... #13 change 44201 edit on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- free_done fix: don't send on param_cache (vtx shdr) done
- sq: added SQ_SP_vsr_vu_valid
- updates to VISM to handle end_of_vector with invalid data

... #12 change 42150 edit on 2002/07/24 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed ais_acs_rd_addr for synthesis

... #11 change 41823 edit on 2002/07/22 by dougd@dougd_r400_linux_marlboro (ktext)

changed order of output declarations to come before their reg declarations so that
synopsys would not declare the outputs as wires

... #10 change 41217 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for sq-sx export

... #9 change 35005 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro (ktext)
```

```
more busy bits

... #8 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro (ktext)

many updates... some v2k removal

... #7 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

misc updates... alu_req logic updated in sq_status_reg

... #6 change 33492 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

various updates - instr start asserted to SP

... #5 change 32898 edit on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

... #4 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #3 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro (ktext)

       updates

... #2 change 26726 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...

... #1 change 23514 add on 2002/04/16 by vromaker@vromaker_r400_sun_marlboro (ktext)

updating with latest versions
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/sq.v
... #93 change 54212 edit on 2002/09/28 by dougd@dougd_r400_linux_marlboro (ktext)

corrected bit widths on some signals that caused errors in synthesis

... #92 change 54166 edit on 2002/09/27 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- SC_SQ interface updates
- also connected VGT_SQ_event to sq_vism

... #91 change 53800 edit on 2002/09/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for events flowing thru SQ
- cleared up issues with making individial vtx and pix thread buffers (and shared
thread_buff_cntl)
- fixed PV,PS bugs

... #90 change 53375 edit on 2002/09/24 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for moving event thru the SQ
- fixes for dealloc, and state_diff in thread buffers

... #89 change 53039 edit on 2002/09/23 by dougd@dougd_r400_linux_marlboro (ktext)

new modules to increase size of pixel thread buffer

... #88 change 51559 edit on 2002/09/13 by dougd@dougd_r400_linux_marlboro (ktext)

connect acs_rd_req to sq_aluconst_top (that input was floating)

... #87 change 51526 edit on 2002/09/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- gpr dealloc connected
- static gpr allocation added (but not enabled)
- ppb btwn pism and ptb added

... #86 change 51368 edit on 2002/09/13 by dougd@dougd_r400_linux_marlboro (ktext)

added some of the port connections necessary to support RBBM reading of the constant
store memories

... #85 change 50967 edit on 2002/09/12 by dougd@dougd_r400_linux_marlboro (ktext)

changed port name "i_context_switch" to "i_map_copy_start" for aluconst and texconst;
```

changed "i_state_change_flag" to "i_read_base_ld" and added ports based on state change
based on gfx_copy_state to sq_cfc

... #84 change 50916 edit on 2002/09/11 by dougd@dougd_r400_linux_marlboro (ktext)

connect context_switch based on gfx_copy_state in rbi; connect loading mechanism for
eo_rt start addresses for aluconst and texconst

... #83 change 50806 edit on 2002/09/11 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixes for bug326 and 329 - tests still fail, but for different reasons

... #82 change 50723 edit on 2002/09/11 by dougd@dougd_r400_linux_marlboro (ktext)

added support for real time mode

... #81 change 50193 edit on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updated kill_mask out to SX

... #80 change 50165 edit on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for pc write one cycle early

... #79 change 49848 edit on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

... #78 change 49291 edit on 2002/09/03 by dougd@dougd_r400_linux_marlboro (ktext)

removed context_misc_screen_xy_in_gpr0_set from sq.v and sq_rbbm_interface.v. added
address decoding for real time constants in sq_rbbm_interface.v

... #77 change 49220 edit on 2002/09/02 by dougd@dougd_r400_linux_marlboro (ktext)

brought in 3 more bits of rbi_addr and divide it by 6 to get the correct texture
constant address because the 6 Dwords in each constant are no longer packed on
boundaries of 8 Dwords but on boundaries of 6 Dwords.

... #76 change 49065 edit on 2002/08/30 by dougd@dougd_r400_linux_marlboro (ktext)

add "vs_num_reg + 1" logic and increase port size by 1 bit

```
... #75 change 48974 edit on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- needed to drive acfs_reading one cycle earlier for ACFS IS read
- updated/added new SQ_SP instruction interface

... #74 change 48558 edit on 2002/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for out-of-order thread processing: the 2 alu ctl flow sequencers
  now share one instr store read slot instead of alternating between two
  different slots (which allowed one to get ahead opf the other)
- thread counts from VISM and PISM to ais_output added at SQ level

... #73 change 48384 edit on 2002/08/27 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updates for ptr_buff/pism to align quad mask correctly
- additions for thread_count

... #72 change 48164 edit on 2002/08/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for individual macc write enables
- added the prev_pos_alloc inputs to the status regs (and logic to
  generate them in the tread buffer)

... #71 change 47160 edit on 2002/08/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

connected param_gen_pos to pism

... #70 change 47110 edit on 2002/08/20 by dougd@dougd_r400_linux_marlboro (ktext)

added the two rbbm registers that were missed in the last version

... #69 change 47072 edit on 2002/08/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updated param_wrap wires

... #68 change 46976 edit on 2002/08/20 by dougd@dougd_r400_linux_marlboro (ktext)

adding the remaining rbbm register outputs to sq_rbbm_interface and wired them up in
sq.v

... #67 change 46800 edit on 2002/08/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)
```

```
updated pism connections to local registers

... #66 change 46714 edit on 2002/08/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updated local register inputs to PISM

... #65 change 46642 edit on 2002/08/16 by dougd@dougd_r400_linux_marlboro (ktext)

added register outputs from rbbm_interface and vgt_event from sq_vism

... #64 change 46629 edit on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

more fixes for alloc size

... #63 change 46251 edit on 2002/08/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates for pop/winner_ack status reg conflict

... #62 change 44294 edit on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- 3 cycle delay added for free_done
- port width fixes

... #61 change 44201 edit on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- free_done fix: don't send on param_cache (vtx shdr) done
- sq: added SQ_SP_vsr_vu_valid
- updates to VISM to handle end_of_vector with invalid data

... #60 change 44010 edit on 2002/08/02 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- multi pixel vector fixes
- VISM fixed for 32 vertex test

... #59 change 43237 edit on 2002/07/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- temp fix to ptr buff to delay free_buff to SC
- comments in thread arb
- re-enabled alu interleaving
```

```
... #58 change 42997 edit on 2002/07/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- input arb now grants pix while pix is busy
       - pism skips idle if request is present
- interleaving disabled in sq.v

... #57 change 42084 edit on 2002/07/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed SQ_SC interface connections

... #56 change 41839 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- new, wider SC interface

... #55 change 41796 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- make the thread_id width consistent at 6 bits (except at the state mem address port)
- updated the SQ_TP and TP_SQ interface (got rid of SQ_TP_clause_num)

... #54 change 41748 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed state width for sythesis

... #53 change 41592 edit on 2002/07/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- interleaving is enabled
- fix for interleaving: cfs_type strap on ALU CFS 1 corrected to 2

... #52 change 41453 edit on 2002/07/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- ppb logic fix
       - fixed updated field position of thread_id w/in status (was causing
         a state_mem read address error since SMRA = winner[status[thread_id]]

... #51 change 41326 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- corrected exp_type for pix w/o z
- fixed cfs_export_id_q to load global_export_id_q only when allocating
- or'd more signals together in TIF to get a solid busy output
```

```
... #50 change 41217 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for sq-sx export

... #49 change 40937 edit on 2002/07/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added alu_instr_pending status bit
- added new SQ_SX_exp and SQ_SX_free interfaces (free is not functional)

... #48 change 40659 edit on 2002/07/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added 2nd alu cfs update interface to thread buff
- state read addr now status_thread_id[winner] as it should have been
- reg'd cfs_phase in thread buff to match reg'd update data

... #47 change 36278 edit on 2002/06/25 by dougd@dougd_r400_linux_marlboro (ktext)

added input VGT_SQ_event; changed VGT_SQ_vsisr_double to VGT_SQ_vsisr_continued

... #46 change 36192 edit on 2002/06/25 by dougd@dougd_r400_linux_marlboro (ktext)

added connections and function to support SQ_RBBM_cntx17_busy & SQ_RBBM_cntx0_busy,
however, at this time both of these signals are the same

... #45 change 35005 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

more busy bits

... #44 change 34969 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for CFI fetch (alloc had to update CFI ptr); added a few busy signals

... #43 change 34778 edit on 2002/06/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for pix shader alu instruction

... #42 change 34632 edit on 2002/06/17 by dougd@dougd_r400_linux_marlboro (ktext)

added a full subtract of the instruction store base address from the rbi_addr before
doing the divide by 3 to get the memory addr

... #41 change 34347 edit on 2002/06/15 by vromaker@vromaker_r400_linux_marlboro
```

(ktext)

fixes for sending interp ctl to SX/SP

... #40 change 34083 edit on 2002/06/14 by vromaker@vromaker_r400_linux_marlboro
(ktext)

sending correct export address in SP instruction

... #39 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

many updates... some v2k removal

... #38 change 33723 edit on 2002/06/13 by dougd@dougd_r400_linux_marlboro (ktext)

added context_valid from aluconst_top to sq_vism to enable/stall loading of control
packet from vgt until the alu constant store has been loaded for this state.

... #37 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

misc updates... alu_req logic updated in sq_status_reg

... #36 change 33492 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

various updates - instr start asserted to SP

... #35 change 33233 edit on 2002/06/11 by vromaker@vromaker_r400_linux_marlboro
(ktext)

SX exp added; tgt instr cnt from CFS to TIF fixed; alloc stuff added

... #34 change 32898 edit on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

... #33 change 32795 edit on 2002/06/07 by vromaker@vromaker_r400_linux_marlboro
(ktext)

       more updates

... #32 change 32472 edit on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro
(ktext)

       thread buff - arb interface updates

... #31 change 32295 edit on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro
(ktext)

commented out fsdbdumpmem

... #30 change 32104 edit on 2002/06/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

connected SQ_TP_send to internal SQ_TP_vld

... #29 change 31875 edit on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates

... #28 change 31693 edit on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates

... #27 change 31621 edit on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates

... #26 change 31586 edit on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates

... #25 change 31449 edit on 2002/06/03 by dougd@dougd_r400_linux_marlboro (ktext)

made temporary fix (marked with FIXME comment) to continue using TP_SQ_clause_num in
the port list instead of the newer (replacement) TP_SQ_thread_id which was declared a
wire set to "0" to keep gc_test.v working.

... #24 change 31389 edit on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updated

... #23 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates

... #22 change 31279 edit on 2002/05/31 by vromaker@vromaker_r400_linux_marlboro

(ktext)

updates

... #21 change 30987 edit on 2002/05/30 by dougd@dougd_r400_linux_marlboro (ktext)

added vs_instr_ptr, vs_resource and vs_first_thread as outputs from sq_vism

... #20 change 30559 edit on 2002/05/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

connected the gpr input mux sel

... #19 change 30516 edit on 2002/05/29 by dougd@dougd_r400_linux_marlboro (ktext)

added connection to gen_index_set output from sq_rbbm_interface

... #18 change 30289 edit on 2002/05/28 by dougd@dougd_r400_linux_marlboro (ktext)

added output "o_context_switch" to sq_rbbm_interface and connected it to
sq_aluconst_top and sq_texconst_top in sq.v
<enter description here>

... #17 change 30053 edit on 2002/05/24 by dougd@dougd_r400_linux_marlboro (ktext)

rbi_acs_rts was wired to both o_aluconst_rts and o_texconst_rts from sq_rbbm_interface:
fixed

... #16 change 29948 edit on 2002/05/24 by dougd@dougd_r400_linux_marlboro (ktext)

sq_rbbm_interface supports both old and new register `defines and has all the new state
registers. sq.v instantiates this sq_rbbm_interface.

... #15 change 29750 edit on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates.. now has clk and reset inputs...

... #14 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro
(ktext)

       updates

... #13 change 26717 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

sadf

... #12 change 25779 edit on 2002/05/01 by vromaker@vromaker_r400_sun_marlboro (ktext)

```
latest updates

... #11 change 21716 edit on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro (ktext)

update

... #10 change 21714 edit on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro (ktext)

update

... #9 change 21642 edit on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro (ktext)

SP_TP_const to 48 bits

... #8 change 21626 edit on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro (ktext)

latest fixes

... #7 change 21468 edit on 2002/04/02 by vromaker@vromaker_r400_sun_marlboro (ktext)

more fixes

... #6 change 21425 edit on 2002/04/02 by vromaker@vromaker_r400_sun_marlboro (ktext)

latest fixes

... #5 change 20660 edit on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro (ktext)

module name updated to sq

... #4 change 20657 edit on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro (ktext)

position_space -> pos_avail, buffer_space -> buf_avail

... #3 change 20655 edit on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro (ktext)

added SQ_TP_type, SQ_TP_send, un_TP_SQ_type, TP_SQ_rdy

... #2 change 20654 edit on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro (ktext)

un_SQ_TP_pmask -> un_SQ_TP_pix_mask (for n = 0..3)

... #1 change 20652 add on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro (ktext)

latest version - renamed from sequencer_top.v

//depot/r400/devel/parts_lib/src/gfx/sq/sequencer_top.v
```

```
... #4 change 19789 edit on 2002/03/20 by vromaker@vromaker_r400_sun_marlboro (text)

re-added SQ_SP_ijline, fixed SP_TP instr and const widths

... #3 change 19752 edit on 2002/03/20 by vromaker@vromaker_r400_sun_marlboro (text)

put SQ_SP_stall back in

... #2 change 19653 edit on 2002/03/19 by vromaker@vromaker_r400_sun_marlboro (text)

updated sq top

... #1 change 11107 branch on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)

mv block dirs to gfx

... ... branch from //depot/r400/devel/parts_lib/src/sq/sequencer_top.v#1,#3
//depot/r400/devel/parts_lib/src/sq/sequencer_top.v
... #3 change 10805 edit on 2001/11/27 by vromaker@vic_r400_src (text)

added some signals and changed a few signal names in an attempt to be more consistent
across all sq interfaces

... #2 change 10432 edit on 2001/11/20 by askende@andi_r400 (text)

more interface related updates

... #1 change 9921 add on 2001/11/14 by askende@andi_r400 (text)

first time check-in
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ais/sq_alu_instr_queue.v
... #19 change 53800 edit on 2002/09/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for events flowing thru SQ
- cleared up issues with making individial vtx and pix thread buffers (and shared
thread_buff_cntl)
- fixed PV,PS bugs

... #18 change 51526 edit on 2002/09/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- gpr dealloc connected
- static gpr allocation added (but not enabled)
- ppb btwn pism and ptb added

... #17 change 49848 edit on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

... #16 change 49059 edit on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed a few typos for the new SP instruction decode

... #15 change 48974 edit on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- needed to drive acfs_reading one cycle earlier for ACFS IS read
- updated/added new SQ_SP instruction interface

... #14 change 41796 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- make the thread_id width consistent at 6 bits (except at the state mem address port)
- updated the SQ_TP and TP_SQ interface (got rid of SQ_TP_clause_num)

... #13 change 41217 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for sq-sx export

... #12 change 35120 edit on 2002/06/20 by vromaker@vromaker_r400_linux_marlboro
(ktext)

changes for latest emulator
```

```
... #11 change 34111 edit on 2002/06/14 by vromaker@vromaker_r400_linux_marlboro
(ktext)

got rid of temp hack

... #10 change 34083 edit on 2002/06/14 by vromaker@vromaker_r400_linux_marlboro
(ktext)

sending correct export address in SP instruction

... #9 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro (ktext)

many updates... some v2k removal

... #8 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

misc updates... alu_req logic updated in sq_status_reg

... #7 change 33536 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

sending srcA gpr read addr one cycle earlier

... #6 change 33509 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed exporting bit by putting pred_sel bit in correctly

... #5 change 32898 edit on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

... #4 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #3 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro (ktext)

       updates

... #2 change 26726 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...

... #1 change 23514 add on 2002/04/16 by vromaker@vromaker_r400_sun_marlboro (ktext)

updating with latest versions
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/tis/sq_tex_instr_seq.v
... #19 change 51740 edit on 2002/09/16 by tien@tien_r400_devel_marlboro (ktext)

Interface change for post-June 15th inst/const

... #18 change 51526 edit on 2002/09/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- gpr dealloc connected
- static gpr allocation added (but not enabled)
- ppb btwn pism and ptb added

... #17 change 42684 edit on 2002/07/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- reverted valid_bits to go from lsb to msb

... #16 change 42096 edit on 2002/07/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- forced sq-tp pix_mask to 0xF

... #15 change 42069 edit on 2002/07/23 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- reversed order of valid_bits (aka pix_mask)

... #14 change 41796 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- make the thread_id width consistent at 6 bits (except at the state mem address port)
- updated the SQ_TP and TP_SQ interface (got rid of SQ_TP_clause_num)

... #13 change 38997 edit on 2002/07/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

not sure - checked in due to clean up

... #12 change 35005 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

more busy bits

... #11 change 34969 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for CFI fetch (alloc had to update CFI ptr); added a few busy signals
```

```
... #10 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

misc updates... alu_req logic updated in sq_status_reg

... #9 change 32898 edit on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

... #8 change 32275 edit on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro (ktext)

updated tex instr const_index field to the new format

... #7 change 31953 edit on 2002/06/05 by vromaker@vromaker_r400_linux_marlboro (ktext)

updated texture pipe output format

... #6 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #5 change 30971 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #4 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro (ktext)

       updates

... #3 change 26726 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...

... #2 change 23514 edit on 2002/04/16 by vromaker@vromaker_r400_sun_marlboro (ktext)

updating with latest versions

... #1 change 21073 add on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro (ktext)

initial version
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ss/sq_vtx_thread_buff.v
... #3 change 53800 edit on 2002/09/26 by vromaker@vromaker_r400_linux_marlboro (ktext)

- fixes for events flowing thru SQ
- cleared up issues with making individial vtx and pix thread buffers (and shared
thread_buff_cntl)
- fixed PV,PS bugs

... #2 change 53376 edit on 2002/09/24 by dougd@dougd_r400_linux_marlboro (ktext)

removed redundant declaration that caused synopsys compile error

... #1 change 53039 add on 2002/09/23 by dougd@dougd_r400_linux_marlboro (ktext)

new modules to increase size of pixel thread buffer
```

```
//depot/r400/devel/parts_lib/src/gfx/tp/tp.tree
... #31 change 52644 edit on 2002/09/19 by tien@tien_r400_devel_marlboro (text)

Fixed port mismatch for synth

... #30 change 50107 edit on 2002/09/08 by tien@tien_r400_devel_marlboro (text)

Added path to regdefs

... #29 change 49343 edit on 2002/09/03 by tien@tien_r400_devel_marlboro (text)

Added tpc reg and clk blocks
Finished hooking up tpc busies
More stuff with reducing aniso steps to tp_addresser
Removed aniso dz

... #28 change 49122 edit on 2002/08/30 by tien@tien_r400_devel_marlboro (text)

More changes for opcodes
Some reduction of precision in lod logic

... #27 change 48443 edit on 2002/08/27 by tien@tien_r400_devel_marlboro (text)

Change MCOPTS to do same opts as synthesis
Added getset block
Reduced aniso pipe to 4
Reduced LOD, COORD, and ALIGN fifos to 24 entries

... #26 change 47368 edit on 2002/08/21 by tien@tien_r400_devel_marlboro (text)

Does not work quite yet, I need to get this in for Andi to work on his half of the
change.

... #25 change 45943 edit on 2002/08/14 by tien@tien_r400_devel_marlboro (text)

Split up tp_lod_aniso for Set/Get Gradient stuff

... #24 change 45516 edit on 2002/08/12 by tien@tien_r400_devel_marlboro (text)

Updated rtest.pl to handle new fsdb location (link to atitmp)
Move all Module Compiler RTSs to central non-optreg'd MC file
Added more busy signal logic

... #23 change 45443 edit on 2002/08/12 by tien@tien_r400_devel_marlboro (text)

Added RBBM interface and tp_id fields

... #22 change 43409 edit on 2002/07/31 by tien@tien_r400_devel_marlboro (text)
```

```
Added some busy signals to tp_cg

... #21 change 43082 edit on 2002/07/30 by tien@tien_r400_devel_marlboro (text)

Fixed clock scripts
Added dbg msgs to virage_io script
Updated clock names

... #20 change 41989 edit on 2002/07/23 by tien@tien_r400_devel_marlboro (text)

Updated LOD logic and pipeline
Adjusted FIFOs accordingly

... #19 change 41580 edit on 2002/07/19 by tien@tien_r400_devel_marlboro (text)

Connected invalidate signal.
Fixed RTR from TC to TP.

... #18 change 40587 edit on 2002/07/15 by tien@tien_r400_devel_tx_marlboro (text)

Fixed many things:
  FIFO watermarks
  Added sp_tp_formatter - this will move to SP at some point
  Updated tc.tree for synth
  Fixed timing on TP_TC, TC_TP and SP_TP interfaces
  Write enables on FIFO output flops (OUTREG_EN)

... #17 change 34926 edit on 2002/06/19 by tien@tien_r400_devel_tx_marlboro (text)

Fixed some GC connection errors.
Cleaned up LOD logic a bit

... #16 change 34732 edit on 2002/06/18 by tien@tien_r400_devel_tx_marlboro (text)

Added clock gating blocks.
Fixed some issues with GC connection errors
Updated Makefiles

... #15 change 29623 edit on 2002/05/23 by tien@tien_r400_sun_marlboro (text)

Again, mainy changes.
I'm starting bugfixes based on simulation results

... #14 change 29059 edit on 2002/05/20 by tien@tien_r400_sun_marlboro (text)

Updated RAMS.
Updated FIFOs.
```

```
Re-did TT reg.
Autopiped parts of tpc_walker

... #13 change 27590 edit on 2002/05/13 by tien@tien_r400_sun_marlboro (text)

Some Aligner changes.

... #12 change 26950 edit on 2002/05/08 by tien@tien_r400_sun_marlboro (text)

Many changes:
Updated Synthesis FIFO instances
Fleshed out tp_addresser clamping logic

... #11 change 26396 edit on 2002/05/03 by tien@tien_r400_sun_marlboro (text)

MC verilog now uses .bvrl extension

... #10 change 26374 edit on 2002/05/03 by tien@tien_r400_sun_marlboro (text)

Many more changes for May 15th

... #9 change 25485 edit on 2002/04/30 by tien@tien_r400_sun_marlboro (text)

Many more changes
Cleaning up TPC<->TP signals
Getting block IO to actaul widths..

... #8 change 25284 edit on 2002/04/29 by tien@tien_r400_sun_marlboro (text)

Minor cleanup

... #7 change 23141 edit on 2002/04/12 by tien@tien_r400_sun_marlboro (text)

Many changes to get things working

... #6 change 22668 edit on 2002/04/10 by tien@tien_r400_sun_marlboro (text)

Some synthesis stuff, updated for Suba's port changes

... #5 change 22603 edit on 2002/04/10 by tien@tien_r400_sun_marlboro (text)

Some top level changes and many tp changes for synth

... #4 change 22244 edit on 2002/04/08 by tien@tien_r400_sun_marlboro (text)

Big changes:
Changed SCLK to iSCLK for synthesis
Changed SRST to srst for r400 naming convention
```

```
Fixed some top level issues with MH signal,
Stitched it Virage RAMs.

... #3 change 21378 edit on 2002/04/02 by tien@tien_r400_sun_marlboro (text)

More GC fixes

... #2 change 20903 edit on 2002/03/28 by tien@tien_r400_sun_marlboro (text)

A whole bunch of changes.  I finally figured out where I want tp and tpc stuff!
And NO, I didn't change the clock names yet.

... #1 change 19540 add on 2002/03/18 by tien@tien_r400_sun_marlboro (text)

ll* port changes to get things to compile
       tp code is initial check-ing of tp
       tc/Makefile is Makefile to build tc
       tp/Makefile is to build tp and tc together
       tp_tc_top.tree is a wrapper for tp*, tc, and tpc
       tp_top.tree is a wrapper for tp* and tpc
       tc.tree is for tc top level
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/cfs/sq_ctl_flow_seq.v
... #37 change 53434 edit on 2002/09/24 by vromaker@vromaker_r400_linux_marlboro
(ktext)

a few port mismatch fixes

... #36 change 53375 edit on 2002/09/24 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for moving event thru the SQ
- fixes for dealloc, and state_diff in thread buffers

... #35 change 52350 edit on 2002/09/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

ptr buff fix to work correctly with split 2-cycle transfers

... #34 change 50806 edit on 2002/09/11 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixes for bug326 and 329 - tests still fail, but for different reasons

... #33 change 50564 edit on 2002/09/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

update

... #32 change 49848 edit on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

... #31 change 48974 edit on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- needed to drive acfs_reading one cycle earlier for ACFS IS read
- updated/added new SQ_SP instruction interface

... #30 change 48558 edit on 2002/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for out-of-order thread processing: the 2 alu ctl flow sequencers
  now share one instr store read slot instead of alternating between two
  different slots (which allowed one to get ahead opf the other)
- thread counts from VISM and PISM to ais_output added at SQ level

... #29 change 46637 edit on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro
```

(ktext)

fix for alloc size

... #28 change 46629 edit on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

more fixes for alloc size

... #27 change 46251 edit on 2002/08/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates for pop/winner_ack status reg conflict

... #26 change 44355 edit on 2002/08/06 by dougd@dougd_r400_linux_marlboro (ktext)

changed default parameter values (was 8): STATE_WIDTH = 64; STATUS_WIDTH = 32; so that
select index would not be out of bounds and cause synthesis to error

... #25 change 44010 edit on 2002/08/02 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- multi pixel vector fixes
- VISM fixed for 32 vertex test

... #24 change 42246 edit on 2002/07/24 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed thread_id width (caused 2nd pix vector to be same as 1st)

... #23 change 42144 edit on 2002/07/24 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- thread_id width fixes

... #22 change 41748 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed state width for sythesis

... #21 change 41459 edit on 2002/07/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- more thread_id updates due to new location of thread_id in status register

... #20 change 41326 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

```
- corrected exp_type for pix w/o z
- fixed cfs_export_id_q to load global_export_id_q only when allocating
- or'd more signals together in TIF to get a solid busy output

... #19 change 41217 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for sq-sx export

... #18 change 40937 edit on 2002/07/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added alu_instr_pending status bit
- added new SQ_SX_exp and SQ_SX_free interfaces (free is not functional)

... #17 change 40659 edit on 2002/07/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added 2nd alu cfs update interface to thread buff
- state read addr now status_thread_id[winner] as it should have been
- reg'd cfs_phase in thread buff to match reg'd update data

... #16 change 34969 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for CFI fetch (alloc had to update CFI ptr); added a few busy signals

... #15 change 34778 edit on 2002/06/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for pix shader alu instruction

... #14 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

many updates... some v2k removal

... #13 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

misc updates... alu_req logic updated in sq_status_reg

... #12 change 33492 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

various updates - instr start asserted to SP

... #11 change 33348 edit on 2002/06/11 by vromaker@vromaker_r400_linux_marlboro
```

(ktext)

fixed tex instruction read pointer

... #10 change 33233 edit on 2002/06/11 by vromaker@vromaker_r400_linux_marlboro
(ktext)

SX exp added; tgt instr cnt from CFS to TIF fixed; alloc stuff added

... #9 change 32795 edit on 2002/06/07 by vromaker@vromaker_r400_linux_marlboro (ktext)

more updates

... #8 change 31953 edit on 2002/06/05 by vromaker@vromaker_r400_linux_marlboro (ktext)

updated texture pipe output format

... #7 change 31875 edit on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #6 change 31693 edit on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #5 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #4 change 31279 edit on 2002/05/31 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #3 change 30971 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #2 change 30458 edit on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #1 change 30284 add on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro (ktext)

moved file from tis to cfs

//depot/r400/devel/parts_lib/src/gfx/sq/tis/sq_ctl_flow_seq.v
... #5 change 30286 delete on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

```
removing from tis

... #4 change 30282 edit on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates...

... #3 change 30159 edit on 2002/05/27 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #2 change 30048 edit on 2002/05/24 by vromaker@vromaker_r400_linux_marlboro (ktext)

checkpoint update

... #1 change 29768 add on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro (ktext)

initial version
```

```
//depot/r400/devel/parts_lib/src/gfx/tp/tp.v
... #9 change 46241 delete on 2002/08/15 by tien@tien_r400_devel_marlboro (ktext)

Removed for Perforce

... #8 change 44953 edit on 2002/08/08 by tien@tien_r400_devel_marlboro (ktext)

Cleaned up LOD logic

... #7 change 44326 edit on 2002/08/05 by tien@txsyn_r400_rel_marlboro (ktext)

Fixed timing loop in tpc_fifos
Fixed tp.v port issue

... #6 change 43082 edit on 2002/07/30 by tien@tien_r400_devel_marlboro (ktext)

Fixed clock scripts
Added dbg msgs to virage_io script
Updated clock names

... #5 change 42573 edit on 2002/07/26 by tien@tien_r400_devel_marlboro (ktext)

Updated LOD logic
Modified output FIFO to handling hicolor reordering (control still needed)
Added tp_out_fifo_ram
Fixed ram wrappers

... #4 change 42158 add on 2002/07/24 by tien@tien_r400_devel_marlboro (ktext)

Checking these in for synthesis

... #3 change 19543 delete on 2002/03/18 by tien@tien_r400_sun_marlboro (text)

No longer a true source file, generated by tp.tree

... #2 change 19540 edit on 2002/03/18 by tien@tien_r400_sun_marlboro (text)

l1* port changes to get things to compile
       tp code is initial check-ing of tp
       tc/Makefile is Makefile to build tc
       tp/Makefile is to build tp and tc together
       tp_tc_top.tree is a wrapper for tp*, tc, and tpc
       tp_top.tree is a wrapper for tp* and tpc
       tc.tree is for tc top level

... #1 change 11102 branch on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)

mv to tp to gfx
```

```
... ... branch from //depot/r400/devel/parts_lib/src/tp/tp.v#1
//depot/r400/devel/parts_lib/src/tp/tp.v
... #1 change 10378 add on 2001/11/20 by tien@devel_tien_r400_sun_marlboro (text)

Texture pipe top level
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ia/sq_input_arb.v
... #8 change 50503 edit on 2002/09/10 by vromaker@vromaker_r400_linux_marlboro (ktext)

another PV/PS phase swap bug fix

... #7 change 49848 edit on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro (ktext)

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

... #6 change 42997 edit on 2002/07/29 by vromaker@vromaker_r400_linux_marlboro (ktext)

- input arb now grants pix while pix is busy
       - pism skips idle if request is present
- interleaving disabled in sq.v

... #5 change 30971 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #4 change 30559 edit on 2002/05/29 by vromaker@vromaker_r400_linux_marlboro (ktext)

connected the gpr input mux sel

... #3 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro (ktext)

       updates

... #2 change 26726 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...

... #1 change 25183 add on 2002/04/26 by vromaker@vromaker_r400_sun_marlboro (ktext)

file updates
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_export_buffers.v
... #2 change 53483 edit on 2002/09/24 by askende@askende_r400_linux_marlboro (ktext)

 renamed the .ctmc files by adding the sx prefix

... #1 change 53452 add on 2002/09/24 by askende@askende_r400_linux_marlboro (ktext)

adding new files after having renamed existing ones
       with sx_*
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/tis/sq_tex_instr_queue.v
... #11 change 41796 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- make the thread_id width consistent at 6 bits (except at the state mem address port)
- updated the SQ_TP and TP_SQ interface (got rid of SQ_TP_clause_num)

... #10 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

many updates... some v2k removal

... #9 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

misc updates... alu_req logic updated in sq_status_reg

... #8 change 33509 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed exporting bit by putting pred_sel bit in correctly

... #7 change 32898 edit on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

... #6 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #5 change 30971 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #4 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro (ktext)

       updates

... #3 change 26726 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...

... #2 change 23514 edit on 2002/04/16 by vromaker@vromaker_r400_sun_marlboro (ktext)

updating with latest versions

... #1 change 21075 add on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro (ktext)

initial version
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/misc/sq_defs.v
... #12 change 49848 edit on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

... #11 change 48844 edit on 2002/08/29 by dougd@dougd_r400_linux_marlboro (ktext)

added support for gen_index (auto-count), vgt events and fixed some bugs

... #10 change 42107 edit on 2002/07/23 by markf@markf_r400_linux_marlboro (ktext)

Updated SC->SQ interface

... #9 change 41839 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro (ktext)

- new, wider SC interface

... #8 change 41796 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro (ktext)

- make the thread_id width consistent at 6 bits (except at the state mem address port)
- updated the SQ_TP and TP_SQ interface (got rid of SQ_TP_clause_num)

... #7 change 40937 edit on 2002/07/16 by vromaker@vromaker_r400_linux_marlboro (ktext)

- added alu_instr_pending status bit
- added new SQ_SX_exp and SQ_SX_free interfaces (free is not functional)

... #6 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #5 change 30971 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #4 change 29767 edit on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #3 change 29311 edit on 2002/05/21 by vromaker@vromaker_r400_linux_marlboro (ktext)

added SQ_CTL_PKT_WIDTH back in

... #2 change 29136 edit on 2002/05/20 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates...
```

```
... #1 change 26726 add on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/is/sq_instruction_store.v
... #15 change 51368 edit on 2002/09/13 by dougd@dougd_r400_linux_marlboro (ktext)

added some of the port connections necessary to support RBBM reading of the constant
store memories

... #14 change 50723 edit on 2002/09/11 by dougd@dougd_r400_linux_marlboro (ktext)

added support for real time mode

... #13 change 48932 edit on 2002/08/29 by dougd@dougd_r400_linux_marlboro (ktext)

replaced address constant with value defined in sq_reg.v

... #12 change 45291 edit on 2002/08/09 by dougd@dougd_r400_linux_marlboro (ktext)

removed "[0:0]" from "input [0:0] clk;" in sq_status_reg.v to prevent synopsys tcl
script error during synthesis. Removed divide-by-3 code in sq_instruction_store.v to
prevent synthesis error.

... #11 change 41218 edit on 2002/07/18 by dougd@dougd_r400_linux_marlboro (ktext)

more changes to support synthesis

... #10 change 40943 edit on 2002/07/16 by dougd@dougd_r400_linux_marlboro (ktext)

original submission of virage memory *.ctmc files. The *.v files were modified to
support synthesis.

... #9 change 34632 edit on 2002/06/17 by dougd@dougd_r400_linux_marlboro (ktext)

added a full subtract of the instruction store base address from the rbi_addr before
doing the divide by 3 to get the memory addr

... #8 change 31880 edit on 2002/06/04 by dougd@dougd_r400_linux_marlboro (ktext)

changed the timing of the CP write to use the same non-registered input address mux as
the reads

... #7 change 31821 edit on 2002/06/04 by dougd@dougd_r400_linux_marlboro (ktext)

fix bug in previous version

... #6 change 31818 edit on 2002/06/04 by dougd@dougd_r400_linux_marlboro (ktext)

removed register stage for address into RAM

... #5 change 31805 edit on 2002/06/04 by dougd@dougd_r400_linux_marlboro (ktext)
```

```
connected o_is_data to read_data

... #4 change 31427 edit on 2002/06/03 by dougd@dougd_r400_linux_marlboro (ktext)

replaced i_cf_addr with i_alu0_cf_addr, i_alu1_cf_addr, i_tex_cf_addr and replaced
i_alu_phase with i_is_sub_phase.

... #3 change 27332 edit on 2002/05/10 by dougd@dougd_r400_sun_marlboro (ktext)

added a divide by 3 to the incoming RBI address to generate the correct instruction
memory address

... #2 change 27093 edit on 2002/05/08 by dougd@dougd_r400_sun_marlboro (ktext)

changed the values assigned to i_is_phase

... #1 change 26852 add on 2002/05/07 by dougd@dougd_r400_sun_marlboro (ktext)

renamed module from is.v to sq_instruction_store.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/sp.v
... #32 change 54226 edit on 2002/09/29 by askende@askende_r400_linux_marlboro (text)

fixing width mismatches warnings out of bcons on some of the top level IOs

... #31 change 52052 edit on 2002/09/17 by askende@askende_r400_sun_marlboro (text)

changes to :

1. interpolators to handle sub-norm ij values.
2. scalar engine result back to GPRs.
3. gc.tree regarding the tp_sp_valid signals.

... #30 change 48978 edit on 2002/08/30 by askende@askende_r400_sun_marlboro (text)

checking in changes related to the new instruction interface

... #29 change 47863 edit on 2002/08/23 by askende@askende_r400_sun_marlboro (text)

added sq_sp_gpr_wr_ena signal for all the phases of a vector unit.

... #28 change 47646 edit on 2002/08/22 by askende@askende_r400_sun_marlboro (text)

final version related to TP-SP interface change as well as going to new SC_SX rb id
modification

... #27 change 46419 edit on 2002/08/15 by askende@askende_r400_sun_marlboro (text)

renaming

... #26 change 46373 edit on 2002/08/15 by askende@askende_r400_sun_marlboro (text)

renamed some of the modules

... #25 change 45473 edit on 2002/08/12 by askende@askende_r400_sun_marlboro (text)

1. top level changes related vsr_vu_valid
2. modified some of the shader opcodes (SET, MASK, CND)

... #24 change 43147 edit on 2002/07/30 by askende@askende_r400_sun_marlboro (text)

explictly declared the instance for q_cg_sp_pm_enb

... #23 change 42930 edit on 2002/07/29 by askende@askende_r400_sun_marlboro (text)

changed the input sclk signal to sclk_global to support synthesis...
still uses "sclk" internaly after sclk has been assigned sclk_global
```

... #22 change 42729 edit on 2002/07/26 by askende@askende_r400_sun_marlboro (text)

changed the name from isq_stall to q_sq_stall

... #21 change 41109 edit on 2002/07/17 by askende@askende_r400_sun_marlboro (text)

top level changes driven by the changes in related to SQ-SX export
allocation/deallocation interface.

... #20 change 36078 edit on 2002/06/25 by askende@askende_r400_sun_marlboro (text)

Added power managment controls signals at the top level : CG_<block>_pm_enb.

... #19 change 35940 edit on 2002/06/24 by askende@askende_r400_sun_marlboro (text)

a few changes related to shader pipe

... #18 change 34344 edit on 2002/06/15 by markf@markf_r400_linux_marlboro (text)

Added srst to interpolator module

... #17 change 34222 edit on 2002/06/14 by askende@askende_r400_sun_marlboro (text)

at this point the PA block gets the valid position data

... #16 change 33340 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (text)

adding the top level signal called TP_SP_data_valid

... #15 change 33157 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (text)

added the masking logic for the GPR write path

... #14 change 31724 integrate on 2002/06/04 by askende@askende_r400_sun_marlboro
(text)

changes at the top level

1. adding sp_sx_exp_dest port to sp.v
2. connecting the sp_tp_fetch_addr ports at the top level
3. changing the sp_sx_exp_dest port from 7 bits to 6 bits in sx.v

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/sp.v#4
... #13 change 31584 integrate on 2002/06/03 by askende@askende_r400_sun_marlboro
(text)

intergrating

```
... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/sp.v#3
... #12 change 31296 integrate on 2002/05/31 by askende@askende_r400_sun_marlboro
(text)

changes to signal naming

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/sp.v#2
... #11 change 28947 edit on 2002/05/17 by askende@askende_r400_sun_marlboro (text)

1. modified the top level sp.v file.
2. exposed the texture fetch path all the way from macc_gpr to sp.v.
3. modified and tested the interp_ctl.v ...the ij buffer control logic.
4. replaced the dum_mem_p2 with virage rtl behavioral model.

... #10 change 28403 edit on 2002/05/16 by askende@askende_r400_sun_marlboro (text)

new top level reflection the changes in SC-SP interpolation interface ...going from one
high precision + 3 low precision interpolators to 4 high precision ones.

... #9 change 27070 edit on 2002/05/08 by askende@askende_r400_sun_marlboro (text)

Paul checking in as Andi

... #8 change 27028 integrate on 2002/05/08 by sallen@sallen_r400_lin_marlboro (text)

first round of ferret changes for gc.v testbench
   add parts_lib/s**/test/gc

... ... ignored //depot/r400/branches/branch_ferret/parts_lib/src/gfx/sp/sp.v#5
... #7 change 26985 edit on 2002/05/08 by askende@askende_r400_sun_marlboro (text)

latest top level as well as some changes regarding clock/reset signal naming

... #6 change 24984 integrate on 2002/04/25 by sallen@sallen_r400_lin_marlboro (text)

ferret updates
     - add mem fill/dump
     - add rbbm register read/writes
     - add ferret_memload test

... ... copy from //depot/r400/branches/branch_ferret/parts_lib/src/gfx/sp/sp.v#4
... #5 change 21971 edit on 2002/04/04 by askende@askende_r400_sun_marlboro (text)

new top level revision
```

```
... #4 change 21447 edit on 2002/04/02 by askende@askende_r400_sun_marlboro (text)

new top level revision to enable the GC integration.

... #3 change 20621 edit on 2002/03/26 by askende@askende_r400_sun_marlboro (text)

another naming update

... #2 change 20586 edit on 2002/03/26 by askende@askende_r400_sun_marlboro (text)

updated the top level interfaces for the GC integration effort.

... #1 change 20547 branch on 2002/03/26 by pmitchel@pmitchel_entire_depot_win (text)

rename

... ... branch from //depot/r400/devel/parts_lib/src/gfx/sp/shader.v#1,#8
//depot/r400/devel/parts_lib/src/gfx/sp/shader.v
... #8 change 20544 edit on 2002/03/26 by askende@askende_r400_sun_marlboro (text)

no changes ...is being checked in so the file can be renamed

... #7 change 20543 edit on 2002/03/26 by askende@askende_r400_sun_marlboro (text)

new rev ....changed the name of the top level from module "shader" to "sp"

... #6 change 17964 edit on 2002/03/07 by askende@askende_r400_sun_marlboro (text)

backing up changes

... #5 change 17855 edit on 2002/03/07 by pmitchel@pmitchel_r400_sun_marlboro (ktext)

changed type

... #4 change 17850 edit on 2002/03/07 by pmitchel@pmitchel_r400_sun_marlboro (text)

testing $Id$

... #3 change 16541 edit on 2002/02/25 by askende@askende_r400_sun_marlboro (text)

new revision of the shader pipe logic.
renamed some of the signals throughout the hierarchy.

... #2 change 14831 edit on 2002/02/07 by askende@askende_r400_sun_marlboro (text)

updated the external interfaces to the latest spec.

... #1 change 11107 branch on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)
```

```
mv block dirs to gfx

... ... branch from //depot/r400/devel/parts_lib/src/sp/shader.v#1,#2
//depot/r400/devel/parts_lib/src/sp/shader.v
... #2 change 10478 edit on 2001/11/21 by askende@andi_r400 (text)

further update of the I/O definition

... #1 change 9918 add on 2001/11/14 by askende@andi_r400 (text)

first time check-in
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/tis/sq_target_instr_fetch.v
... #17 change 53800 edit on 2002/09/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for events flowing thru SQ
- cleared up issues with making individial vtx and pix thread buffers (and shared
thread_buff_cntl)
- fixed PV,PS bugs

... #16 change 49848 edit on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

... #15 change 41796 edit on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- make the thread_id width consistent at 6 bits (except at the state mem address port)
- updated the SQ_TP and TP_SQ interface (got rid of SQ_TP_clause_num)

... #14 change 41326 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- corrected exp_type for pix w/o z
- fixed cfs_export_id_q to load global_export_id_q only when allocating
- or'd more signals together in TIF to get a solid busy output

... #13 change 41217 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for sq-sx export

... #12 change 34969 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for CFI fetch (alloc had to update CFI ptr); added a few busy signals

... #11 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

many updates... some v2k removal

... #10 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

misc updates... alu_req logic updated in sq_status_reg
```

```
... #9 change 31875 edit on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #8 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #7 change 31279 edit on 2002/05/31 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #6 change 30971 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #5 change 29767 edit on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #4 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro (ktext)

       updates

... #3 change 26726 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...

... #2 change 23514 edit on 2002/04/16 by vromaker@vromaker_r400_sun_marlboro (ktext)

updating with latest versions

... #1 change 21074 add on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro (ktext)

update
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_macc32.mc
... #9 change 53006 edit on 2002/09/23 by askende@askende_r400_sun_marlboro (text)

new code added to the scalar engine

... #8 change 52906 edit on 2002/09/21 by askende@askende_r400_sun_marlboro (text)

adding clamp to the vector unit alu

... #7 change 52508 edit on 2002/09/19 by askende@askende_r400_sun_marlboro (text)

changes:

1. corrected an overflow condition in the multiply logic of the interpolators
2. rewrote the gpr write-back path logic for the scalar results

... #6 change 52052 edit on 2002/09/17 by askende@askende_r400_sun_marlboro (text)

changes to :

1. interpolators to handle sub-norm ij values.
2. scalar engine result back to GPRs.
3. gc.tree regarding the tp_sp_valid signals.

... #5 change 51731 edit on 2002/09/16 by askende@askende_r400_sun_marlboro (text)

backing up changes

... #4 change 51440 edit on 2002/09/13 by askende@askende_r400_sun_marlboro (text)

changes:

1.fixed overflow detection logic in macc32
2. fixed RECIP and RECIP_SQRT logic in scalar_lut
3. replaced gpr_cmask = 0xf with the value driven by SQ

... #3 change 50812 edit on 2002/09/11 by askende@askende_r400_sun_marlboro (text)

1.fixed a bug related to sp_macc32 add logic
2.renaming the scalar_lut.mc to sp_scalar_lut.mc

... #2 change 49872 edit on 2002/09/05 by askende@askende_r400_sun_marlboro (text)

changes related to syntax and new instruction interface

... #1 change 46348 add on 2002/08/15 by askende@askende_r400_sun_marlboro (text)

this check in is related to renaming some of the files to sp_*
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/macc32.mc
... #7 change 46373 delete on 2002/08/15 by askende@askende_r400_sun_marlboro (text)

renamed some of the modules

... #6 change 46340 edit on 2002/08/15 by askende@askende_r400_sun_marlboro (text)

submitting a bunch of changes related to reducing area for the macc32 unit

... #5 change 45966 edit on 2002/08/14 by askende@askende_r400_sun_marlboro (text)

1. argument selection logic bug fix related to argument modifier "negate"
2. grouped all the `defines and #defines in sp_defines.v and sp_defines_mc.mc

... #4 change 17964 edit on 2002/03/07 by askende@askende_r400_sun_marlboro (text)

backing up changes

... #3 change 16541 edit on 2002/02/25 by askende@askende_r400_sun_marlboro (text)

new revision of the shader pipe logic.
renamed some of the signals throughout the hierarchy.

... #2 change 14099 edit on 2002/01/28 by askende@andi_r400 (text)

new rev

... #1 change 13945 add on 2002/01/25 by askende@andi_r400 (text)

first time check in
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_macc_gpr.v
... #6 change 52508 edit on 2002/09/19 by askende@askende_r400_sun_marlboro (ktext)

changes:

1. corrected an overflow condition in the multiply logic of the interpolators
2. rewrote the gpr write-back path logic for the scalar results

... #5 change 51440 edit on 2002/09/13 by askende@askende_r400_sun_marlboro (ktext)

changes:

1.fixed overflow detection logic in macc32
2. fixed RECIP and RECIP_SQRT logic in scalar_lut
3. replaced gpr_cmask = 0xf with the value driven by SQ

... #4 change 49872 edit on 2002/09/05 by askende@askende_r400_sun_marlboro (ktext)

changes related to syntax and new instruction interface

... #3 change 48978 edit on 2002/08/30 by askende@askende_r400_sun_marlboro (ktext)

checking in changes related to the new instruction interface

... #2 change 46373 edit on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

renamed some of the modules

... #1 change 46348 add on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

this check in is related to renaming some of the files to sp_*

//depot/r400/devel/parts_lib/src/gfx/sp/vector/macc_gpr.v
... #17 change 46373 delete on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

renamed some of the modules

... #16 change 41492 edit on 2002/07/19 by askende@askende_r400_sun_marlboro (ktext)

bit-blasted the virage memory instances for synthesis purposes.

... #15 change 35940 edit on 2002/06/24 by askende@askende_r400_sun_marlboro (ktext)

a few changes related to shader pipe

... #14 change 34222 edit on 2002/06/14 by askende@askende_r400_sun_marlboro (ktext)

at this point the PA block gets the valid position data
```

... #13 change 33393 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (ktext)

fixed a bug related to gpr_wr_ena control signal generation.

... #12 change 33222 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (ktext)

changed the enable for the GPR read cycles to be high all the time. This is a hack for the time being

... #11 change 33157 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (ktext)

added the masking logic for the GPR write path

... #10 change 32079 integrate on 2002/06/05 by askende@askende_r400_sun_marlboro (ktext)

set the correct number of words (parameter) for the macc_gpr register file

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/macc_gpr.v#4
... #9 change 31995 integrate on 2002/06/05 by askende@askende_r400_sun_marlboro (ktext)

registered the output of the register file (GPRs) to line up with the phase_mux control signal

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/macc_gpr.v#3
... #8 change 31584 integrate on 2002/06/03 by askende@askende_r400_sun_marlboro (ktext)

intergrating

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/macc_gpr.v#2
... #7 change 28947 edit on 2002/05/17 by askende@askende_r400_sun_marlboro (ktext)

1. modified the top level sp.v file.
2. exposed the texture fetch path all the way from macc_gpr to sp.v.
3. modified and tested the interp_ctl.v ...the ij buffer control logic.
4. replaced the dum_mem_p2 with virage rtl behavioral model.

... #6 change 26985 edit on 2002/05/08 by askende@askende_r400_sun_marlboro (ktext)

latest top level as well as some changes regarding clock/reset signal naming

... #5 change 17964 edit on 2002/03/07 by askende@askende_r400_sun_marlboro (ktext)

```
backing up changes

... #4 change 17602 edit on 2002/03/05 by askende@askende_r400_sun_marlboro (ktext)

intergrated the scalar unit with the vector unit module

... #3 change 16541 edit on 2002/02/25 by askende@askende_r400_sun_marlboro (ktext)

new revision of the shader pipe logic.
renamed some of the signals throughout the hierarchy.

... #2 change 14458 edit on 2002/02/01 by askende@askende_r400_sun_marlboro (ktext)

backing up code changes

... #1 change 14434 add on 2002/02/01 by askende@askende_r400_sun_marlboro (ktext)

first time checked in.

//depot/r400/devel/parts_lib/src/gfx/sp/vector/macc_reg.v
... #4 change 14433 delete on 2002/02/01 by askende@askende_r400_sun_marlboro (text)

this file is being deleted. It is no longer needed. It is being replace by a new file
named macc_gpr.v

... #3 change 14432 edit on 2002/02/01 by askende@askende_r400_sun_marlboro (text)

checking it in so it can be removed from Perforce.
This file is no longer needed. A new file macc_gpr.v has been introduced to replace
this one.

... #2 change 14314 edit on 2002/01/31 by askende@andi_r400 (text)

saving the changes so I can reconfigure my devel_askende area

... #1 change 11107 branch on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)

mv block dirs to gfx

... ... branch from //depot/r400/devel/parts_lib/src/sp/vector/macc_reg.v#1
//depot/r400/devel/parts_lib/src/sp/vector/macc_reg.v
... #2 change 11107 delete on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)

mv block dirs to gfx

... #1 change 6810 add on 2001/09/21 by askende@andi_r400_devel (text)
```

```
newly added files
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa_ccg_sxifsm.v
... #13 change 53101 edit on 2002/09/23 by bhankins@fl_bhankins_r400_win (ktext)

initialized full and empty signals of sx_pending_fifo

... #12 change 50981 edit on 2002/09/12 by bhankins@fl_bhankins_r400_win (ktext)

fix sensitivity list

... #11 change 50958 edit on 2002/09/12 by bhankins@fl_bhankins_r400_win (ktext)

fix an overzealous fix

... #10 change 50953 edit on 2002/09/12 by bhankins@fl_bhankins_r400_win (ktext)

changed erroneous blocking signals to non blocking

... #9 change 49612 edit on 2002/09/05 by bhankins@fl_bhankins_r400_win (ktext)

added two more inputs into the generation of the clipper_busy signal:

current_state_empty from the clipper state machine, and

sx_pending_fifo_empty, from the shader export interface module.

... #8 change 44956 edit on 2002/08/08 by bhankins@fl_bhankins_r400_win (ktext)

implement latest changes - nan discard, bad pipe support, and state

based point size during ucp clipping.

... #7 change 43324 edit on 2002/07/31 by bhankins@fl_bhankins_r400_win (ktext)

sensitivity list fix

... #6 change 42201 edit on 2002/07/24 by bhankins@fl_bhankins_r400_win (ktext)

fix synthesis warning

... #5 change 34526 edit on 2002/06/17 by bhankins@fl_bhankins_r400_win (ktext)

add 1 to param_cache_indx state

... #4 change 33525 edit on 2002/06/12 by bhankins@fl_bhankins_r400_win (ktext)

update shader export interface, clip code generator and

clipper to match csim ccgen.cpp and clip.cpp
```

```
changelist #33001

... #3 change 29516 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

updates on sxif state

... #2 change 29459 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

updates to fix state i/o and use proper state_storage modules

... #1 change 29233 add on 2002/05/21 by bhankins@fl_bhankins_r400_win (ktext)

initial checkin (changed names)
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx.v
... #39 change 54226 edit on 2002/09/29 by askende@askende_r400_linux_marlboro (text)

fixing width mismatches warnings out of bcons on some of the top level IOs

... #38 change 53452 edit on 2002/09/24 by askende@askende_r400_linux_marlboro (text)

adding new files after having renamed existing ones
       with sx_*

... #37 change 50534 edit on 2002/09/10 by askende@askende_r400_sun_marlboro (text)

adding new changes related to alloc-dealloc logic

... #36 change 49505 edit on 2002/09/04 by askende@askende_r400_sun_marlboro (text)

changes related to :

1. predicate in SP vector unit
2. export avail space reporting to SQ in SX

... #35 change 48841 edit on 2002/08/29 by sallen@sallen_r400_lin_marlboro (text)

-finish up _pm_enb and _pm_en set to 1, clocks run now
   -also set busy signals low in blocks that don't drive them
   -fix mh DEPS file

... #34 change 48695 edit on 2002/08/28 by askende@askende_r400_sun_marlboro (text)

fixed :

1. sx_sc quad interface bug
2. ij buffer data loading sequence bug
3. mislalignment between PC parameter data and ij data at the input of the
interpolators

... #33 change 47500 edit on 2002/08/22 by askende@askende_r400_sun_marlboro (text)

modified top level sp and sx.

1. Removed sc_sx_tilex, tiley buses from the sx.v
2. Brought sp_tp_formatter logic over to sp.v from tp.v

... #32 change 45473 edit on 2002/08/12 by askende@askende_r400_sun_marlboro (text)

1. top level changes related vsr_vu_valid
2. modified some of the shader opcodes (SET, MASK, CND)
```

... #31 change 43743 edit on 2002/08/01 by askende@askende_r400_sun_marlboro (text)

synthesis related changes

... #30 change 41593 edit on 2002/07/19 by askende@askende_r400_sun_marlboro (text)

fixed the rbbm read back path.

... #29 change 41394 edit on 2002/07/18 by askende@askende_r400_sun_marlboro (text)

tied a few top level signals...first triangle passes..again.

... #28 change 41307 edit on 2002/07/18 by askende@askende_r400_sun_marlboro (text)

backing up changes

... #27 change 41109 edit on 2002/07/17 by askende@askende_r400_sun_marlboro (text)

top level changes driven by the changes in related to SQ-SX export
allocation/deallocation interface.

... #26 change 40969 edit on 2002/07/17 by askende@askende_r400_sun_marlboro (text)

1. New SQ_SX export interface
2. Added the top level registers for the (i/o registers) using ati_dff_in and
ati_dff_out

... #25 change 40688 edit on 2002/07/15 by askende@askende_r400_sun_marlboro (text)

backing up changes. Changed a few signal names

... #24 change 36078 edit on 2002/06/25 by askende@askende_r400_sun_marlboro (text)

Added power managment controls signals at the top level : CG_<block>_pm_enb.

... #23 change 35059 edit on 2002/06/19 by askende@askende_r400_sun_marlboro (text)

SX to RB interface working at this point

... #22 change 34667 edit on 2002/06/18 by askende@askende_r400_sun_marlboro (text)

a few fixes related to the first triangle

... #21 change 34222 edit on 2002/06/14 by askende@askende_r400_sun_marlboro (text)

at this point the PA block gets the valid position data

... #20 change 33361 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (text)

```
tied SX_SQ_pos_avail to 1'b1

... #19 change 31724 integrate on 2002/06/04 by askende@askende_r400_sun_marlboro
(text)

changes at the top level

1. adding sp_sx_exp_dest port to sp.v
2. connecting the sp_tp_fetch_addr ports at the top level
3. changing the sp_sx_exp_dest port from 7 bits to 6 bits in sx.v

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sx/sx.v#2
... #18 change 30064 edit on 2002/05/24 by askende@askende_r400_sun_marlboro (text)

submitting the latest changes regarding :

1. export write interface,
2. position data interface..now supporting both buffers (position and auxiliary).

... #17 change 26643 edit on 2002/05/06 by askende@askende_r400_sun_marlboro (text)

1.tied the top level sx.v to export_control.v
2.added partial logic on the position inteface in export_control.v

... #16 change 26241 edit on 2002/05/03 by askende@askende_r400_sun_marlboro (text)

more updates to the top level.

1.added RB#_SX_index_op
3.added SX_RBBM_busy

... #15 change 25664 edit on 2002/04/30 by askende@askende_r400_sun_marlboro (text)

new top level ..
Includes the new RB to SX interface definition where color interface has been separated
from
index request interface.

... #14 change 25347 edit on 2002/04/29 by askende@askende_r400_sun_marlboro (text)

backing up new code

... #13 change 22104 edit on 2002/04/05 by askende@askende_r400_sun_marlboro (text)

new rev of the top level. corrected the width of some of the RBBM interface
signals/buses
```

```
... #12 change 22100 edit on 2002/04/05 by askende@askende_r400_sun_marlboro (text)

new top level file revision.
added the RBBM interface definition.

... #11 change 21971 edit on 2002/04/04 by askende@askende_r400_sun_marlboro (text)

new top level revision

... #10 change 21443 edit on 2002/04/02 by askende@askende_r400_sun_marlboro (text)

renamed some of the IO names to enable the GC integration.

... #9 change 21310 edit on 2002/04/01 by askende@askende_r400_sun_marlboro (text)

completed the parameter cache read/write logic including the parameter selection (flat
vs. gouraud) as well as the paremeter difference engine logic for the interpolators.

... #8 change 21078 edit on 2002/03/29 by askende@askende_r400_sun_marlboro (text)

completed the vertex parameter read/write in/out of parameter cache logic.
completed the vertex parameter routing and selection.
a vorking version of the above.
a working version of the testbench.

... #7 change 20984 edit on 2002/03/28 by askende@askende_r400_sun_marlboro (text)

work in progress ..more additions

... #6 change 20704 edit on 2002/03/27 by askende@askende_r400_sun_marlboro (text)

new top level rev. of the sx.v

... #5 change 20677 edit on 2002/03/27 by askende@askende_r400_sun_marlboro (text)

new rev.

... #4 change 20665 edit on 2002/03/27 by askende@askende_r400_sun_marlboro (text)

a new rev of the top level sx interface definition

... #3 change 20624 edit on 2002/03/26 by askende@askende_r400_sun_marlboro (text)

another rev of the sx.v interface definitions

... #2 change 20010 edit on 2002/03/21 by askende@askende_r400_sun_marlboro (text)
```

```
first revision of the top level for the Shader Export.

... #1 change 11107 branch on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)

mv block dirs to gfx

... ... branch from //depot/r400/devel/parts_lib/src/sx/sx.v#1
//depot/r400/devel/parts_lib/src/sx/sx.v
... #1 change 11069 add on 2001/12/03 by wlawless@wlawless (text)

Initial port list for sx.v
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_macc.v
... #14 change 53874 edit on 2002/09/26 by askende@askende_r400_linux_marlboro (ktext)

fixed a "logic timing" problem related to Scalar Result write-back path into GPRs

... #13 change 52906 edit on 2002/09/21 by askende@askende_r400_sun_marlboro (ktext)

adding clamp to the vector unit alu

... #12 change 52508 edit on 2002/09/19 by askende@askende_r400_sun_marlboro (ktext)

changes:

1. corrected an overflow condition in the multiply logic of the interpolators
2. rewrote the gpr write-back path logic for the scalar results

... #11 change 52052 edit on 2002/09/17 by askende@askende_r400_sun_marlboro (ktext)

changes to :

1. interpolators to handle sub-norm ij values.
2. scalar engine result back to GPRs.
3. gc.tree regarding the tp_sp_valid signals.

... #10 change 51592 edit on 2002/09/13 by askende@askende_r400_sun_marlboro (ktext)

modified the swizzle select logic

... #9 change 51440 edit on 2002/09/13 by askende@askende_r400_sun_marlboro (ktext)

changes:

1.fixed overflow detection logic in macc32
2. fixed RECIP and RECIP_SQRT logic in scalar_lut
3. replaced gpr_cmask = 0xf with the value driven by SQ

... #8 change 50534 edit on 2002/09/10 by askende@askende_r400_sun_marlboro (ktext)

adding new changes related to alloc-dealloc logic

... #7 change 50404 edit on 2002/09/10 by askende@askende_r400_sun_marlboro (ktext)

more changes related to area savings and logic optimizations.

... #6 change 49872 edit on 2002/09/05 by askende@askende_r400_sun_marlboro (ktext)

changes related to syntax and new instruction interface
```

```
... #5 change 48978 edit on 2002/08/30 by askende@askende_r400_sun_marlboro (ktext)

checking in changes related to the new instruction interface

... #4 change 47441 edit on 2002/08/21 by askende@askende_r400_sun_marlboro (ktext)

reworked the staging registers

... #3 change 47181 edit on 2002/08/20 by askende@askende_r400_sun_marlboro (ktext)

changed the staging registers to be vertical feeding into macc

... #2 change 46373 edit on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

renamed some of the modules

... #1 change 46348 add on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

this check in is related to renaming some of the files to sp_*

//depot/r400/devel/parts_lib/src/gfx/sp/vector/macc.v
... #15 change 46373 delete on 2002/08/15 by askende@askende_r400_sun_marlboro (text)

renamed some of the modules

... #14 change 46340 edit on 2002/08/15 by askende@askende_r400_sun_marlboro (text)

submitting a bunch of changes related to reducing area for the macc32 unit

... #13 change 45966 edit on 2002/08/14 by askende@askende_r400_sun_marlboro (text)

1. argument selection logic bug fix related to argument modifier "negate"
2. grouped all the `defines and #defines in sp_defines.v and sp_defines_mc.mc

... #12 change 45473 edit on 2002/08/12 by askende@askende_r400_sun_marlboro (text)

1. top level changes related vsr_vu_valid
2. modified some of the shader opcodes (SET, MASK, CND)

... #11 change 43690 edit on 2002/08/01 by askende@askende_r400_sun_marlboro (text)

modifications related to synthesis

... #10 change 42463 edit on 2002/07/25 by askende@askende_r400_sun_marlboro (text)

maybe a syntax problem with [0:0] input declaration

... #9 change 34222 edit on 2002/06/14 by askende@askende_r400_sun_marlboro (text)
```

```
at this point the PA block gets the valid position data

... #8 change 31584 integrate on 2002/06/03 by askende@askende_r400_sun_marlboro (text)

intergrating

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/macc.v#2
... #7 change 26985 edit on 2002/05/08 by askende@askende_r400_sun_marlboro (text)

latest top level as well as some changes regarding clock/reset signal naming

... #6 change 17964 edit on 2002/03/07 by askende@askende_r400_sun_marlboro (text)

backing up changes

... #5 change 17602 edit on 2002/03/05 by askende@askende_r400_sun_marlboro (text)

intergrated the scalar unit with the vector unit module

... #4 change 16541 edit on 2002/02/25 by askende@askende_r400_sun_marlboro (text)

new revision of the shader pipe logic.
renamed some of the signals throughout the hierarchy.

... #3 change 14458 edit on 2002/02/01 by askende@askende_r400_sun_marlboro (text)

backing up code changes

... #2 change 14314 edit on 2002/01/31 by askende@andi_r400 (text)

saving the changes so I can reconfigure my devel_askende area

... #1 change 11107 branch on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)

mv block dirs to gfx

... ... branch from //depot/r400/devel/parts_lib/src/sp/vector/macc.v#1,#2
//depot/r400/devel/parts_lib/src/sp/vector/macc.v
... #3 change 11107 delete on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro (text)

mv block dirs to gfx

... #2 change 6887 edit on 2001/09/25 by askende@andi_r400_devel (text)

more changes
```

```
... #1 change 5440 add on 2001/08/16 by askende@andi_r400_devel (text)

adding source code into source control
```

```
//depot/r400/devel/parts_lib/src/gfx/sc/sc.v
... #79 change 54251 edit on 2002/09/29 by mmantor@mmantor_r400_win (ktext)

added sc_rbiu read back bus hook up with it forced to zero at reset

... #78 change 53774 edit on 2002/09/26 by donaldl@fl_donaldl_p4 (ktext)

Update with latest changes to real-time stream registers:  separated z_min & z_max,
expanded prim_type to 3 bits, and added zy_max.

... #77 change 53580 edit on 2002/09/25 by rramsey@RRAMSEY_P4_r400_win (ktext)

Add SuperTile state to sc_rbiu, sc_state, and top level
Add SuperTileDiscardPrim logic to sc_pipe
Add SuperTileDiscardTile logic to sc_quadmask
Increase event_id to 5 bits through quadmask
Increase event_id to 5 bits for all top level signals

... #76 change 53506 edit on 2002/09/25 by mmantor@mmantor_r400_win (ktext)

made event id 5 bits from qpp_proc to the back of SC and changed csim dumps for the
whole sc

... #75 change 53400 edit on 2002/09/24 by mmantor@mmantor_r400_win (ktext)

restructured the sc_iter.v to skew outputs of sp and sq/sx and put fifo in for sq/sx
delay, updated the busy logic along with the delay for sp buffer decrement and new sp
buffer management currently limited to two buffer usage and new signal to the sq for
vism arbiter to wait until sp ij buffers have data.

... #74 change 53121 edit on 2002/09/23 by donaldl@fl_donaldl_p4 (ktext)

Removed top level muxing of real-time stream data.

... #73 change 53080 edit on 2002/09/23 by donaldl@fl_donaldl_p4 (ktext)

Added support for real-time streams.

... #72 change 52127 edit on 2002/09/17 by ctaylor@fl_ctaylor_r400_dtwin_marlboro
(ktext)

Fix Viz Query State to be hooked up to qdpr_proc

... #71 change 51961 edit on 2002/09/17 by rramsey@RRAMSEY_P4_r400_win (ktext)

Hook up detail mask context_id input to qpp output (instead of qpp state lookup signal)
Add some signal declarations to clean up compiler warnings
```

```
... #70 change 51712 edit on 2002/09/16 by donaldl@fl_donaldl_p4 (ktext)

Added write_confirm logic.

... #69 change 51360 edit on 2002/09/13 by kmeekins@kmeekins_r400_win (ktext)

sc_detail_mask_accum:
- added logic for determining context 0 and context 1 to 7 busy
- added three new I/O signals for teh busy logic

sc:
- connected new sc_detail_mask_accum I/O to sc_iter and sc_qdpr_proc

sc_iter:
- or'ed in the sc_detail_mask_accum busy signals to the
  pkr_iter_cntx0_busy and the pkr_iter_cntx1to7_busy signals
- added the sc_detail_mask_accum busy signals to the I/O

... #68 change 51175 edit on 2002/09/12 by mmantor@mmantor_r400_win (ktext)

added state data for the implementation of xyface, centers, multipass pixel shaders.
added delay for free buff signal and early sp_pv_cnt for sc to sq interface timing
changes.

... #67 change 50797 edit on 2002/09/11 by rramsey@RRAMSEY_P4_r400_win (ktext)

Add viz_query stuff to sc rtl
vq state data is driven with temps for now (regs don't seem to get loaded)

... #66 change 50714 edit on 2002/09/11 by mmantor@mmantor_r400_win (ktext)

added sc_sample_cntl from state block to iter and fixed a sensitivity list problem

... #65 change 50450 edit on 2002/09/10 by rramsey@RRAMSEY_P4_r400_win (ktext)

Fix signed/unsigned compare problem in coarse_walker by making x/y_curr values signed
Clean up stipple state
Fix stipple_cnt and stipple_ptr logic in coarse_walker
Add second BB input to quadmask

... #64 change 50205 edit on 2002/09/09 by donaldl@fl_donaldl_p4 (ktext)

Added new scissor bounding box (ie. 2nd scissor x/y min/max values) and expanded bit
widths for them and x/y current signals.

... #63 change 49023 edit on 2002/08/30 by rramsey@RRAMSEY_P4_r400_win (ktext)

Changes to sc RTL to get line stipple working
```

```
  Should pass stipple tests as long as the line is not scissored

This coarse_walker mc code uses the collapsible pipeline which fixes a bug,
but probably does not meet timing

... #62 change 48736 edit on 2002/08/29 by rramsey@RRAMSEY_P4_r400_win (ktext)

Turn rcc trackers back on so we can debug z problems
Connect z state select to cw_state_id
Connect tilex/tiley inputs to z block to coarsewalker outputs
Fix latency for tilex/tiley outputs
Make quadmask mc match bvrl (latency = 3)

... #61 change 48708 edit on 2002/08/29 by kmeekins@kmeekins_r400_win (ktext)

Changed the state id for the z_interp states to use the id from the quadmask and not
the Z FIFO.

... #60 change 48608 edit on 2002/08/28 by rramsey@RRAMSEY_P4_r400_win (ktext)

Updates to sc RTL to get state/event/event_id routed through qpp/pkr/iterator
Adding line stipple to coarse_walker.mc and quadmask.mc
Change sc_quadmask latency to 3

Z is still mismatching
cliprect tests are broken again

... #59 change 48528 edit on 2002/08/28 by kmeekins@kmeekins_r400_win (ktext)

Removed max_sample_dist from getting passed into the tile fifo.

... #58 change 48524 edit on 2002/08/28 by kmeekins@kmeekins_r400_win (ktext)

Expanded dz/dx and dz/dy into the z_interp.
Added the quadcovered mask.

... #57 change 48502 edit on 2002/08/28 by donaldl@fl_donaldl_p4 (ktext)

1. Remove state_id[2:0] and event_id[3:0] from prim fifo.

2. Remove state_id[2:0] from z fifo.

3. Pipe down state_id[2:0], event, st_max_sample_dist[3:0], x_major from sc_pipe to
tile fifo.

4. Increase bit widths (ie. lsbs) of edge distances going from sc_pipe to
sc_coarse_walker to tile fifo.
```

```
... #56 change 47599 edit on 2002/08/22 by viviana@viviana_crayola_linux_orl (ktext)

The iSV_JSS_SAMPLE_SEL bus in sc.v was getting the st_jss_sample15 through
st_jss_sample0
   3-bit busses from sample0 to sample 15. They were switched so that the 48 bit bus
got
   the individual 3 bit busses from 15 down to 0.  This was done to match the compare
values
   from the C sim.

... #55 change 47126 edit on 2002/08/20 by kmeekins@kmeekins_r400_win (ktext)

Increased z_min and z_max bit widths from 14 to 18 bits each. The
new format leading into the sc_z_interp is now s3.14 2's comp.

Added macros to define the bit positions of the PA to SC interface.

Connected z_min, z_max, and clipped_prim in the test bench.

... #54 change 46867 edit on 2002/08/19 by donaldl@fl_donaldl_p4 (ktext)

Updated sc_pipe (to match csim) --

1.  derived x_min, x_max, y_min, y_max

2.  Removed st_max_minus_1.  Not needed anymore.

... #53 change 46591 edit on 2002/08/16 by kmeekins@kmeekins_r400_win (ktext)

Added the changes to zmin and zmax for polyoffset.
Decoding the state variable MSAA_ENABLE and pipeing it to the RC.
Adjusted the compare points on the z data bus.
Expanded the covered signal to a 16 bit bus to handle the quad covered mask.

... #52 change 45387 edit on 2002/08/12 by rramsey@FL_RAMSEY_r400_win (ktext)

1. Change sc_sp dump to leave out 1clk transfers to the sq
2. Remove temp drivers for cliprects in sc.v
3. Temp fix to coarse_walker to only pop zfifo when a valid end_of_prim is leaving

... #51 change 45264 edit on 2002/08/09 by rramsey@RRAMSEY_P4_r400_win (ktext)

Clean up some code for multi-state tests

... #50 change 43702 edit on 2002/08/01 by rramsey@RRAMSEY_P4_r400_win (ktext)

Remove unused inputs from sc_pipe instance
```

```
... #49 change 42515 edit on 2002/07/25 by mmantor@mmantor_r400_win (ktext)

finished sample mask change for aa and 1 clk increase latency

... #48 change 42506 edit on 2002/07/25 by mmantor@mmantor_r400_win (ktext)

added the latest baryc code and routed new state data

... #47 change 42469 edit on 2002/07/25 by rramsey@RRAMSEY_P4_r400_win (ktext)

Hook up tilex/y mod3 signals to quadmask outputs

... #46 change 42142 edit on 2002/07/24 by donaldl@fl_donaldl_p4 (ktext)

Created mem_stub for Z fifo.

... #45 change 41950 edit on 2002/07/23 by rramsey@rramsey_crayola_unix_orl (ktext)

Add xmajor to sc_quadmask and connect it to qpp inputs

... #44 change 41821 edit on 2002/07/22 by mmantor@mmantor_r400_win (ktext)

* added pipe stages in sc_qdpr_proc and sc_iter for increased latency of module
compiler code.
* switch interconnect between samplemask and barc logic to be sample_id's instead of
offsets
* connected lod_correct values completely
* connected new state data
* rewired sc_sq interface and widened to handle larger lod_correct terms
*misc test bench and signal connections through the sc

... #43 change 41610 edit on 2002/07/19 by donaldl@fl_donaldl_p4 (ktext)

Added fanned out pipe_freeze_b_dly to go directly to prim fifo write enable.

... #42 change 40920 edit on 2002/07/16 by donaldl@fl_donaldl_p4 (ktext)

Added support for Z functions.

... #41 change 40548 edit on 2002/07/15 by mmantor@mmantor_r400_win (ktext)

added rb_id and split though the sc and fixed some bugs associated with it.  Renamed
all RC_SC_heir_xx signals to RC_SC_hier_xxx

... #40 change 39965 edit on 2002/07/12 by rramsey@RRAMSEY_P4_r400_win (ktext)

Update sc rtl to work with new block file defs
Clean up sc Makefile
```

```
... #39 change 39493 edit on 2002/07/10 by grayc@grayc_r400_win (ktext)

missed one signal in interface_regs block :-(

... #38 change 38969 edit on 2002/07/09 by grayc@grayc_r400_win (ktext)

fixed port connections

... #37 change 38922 edit on 2002/07/08 by grayc@grayc_r400_win (ktext)

moved most top level registers into a block sc_interface_regs

... #36 change 36233 edit on 2002/06/25 by mmantor@mmantor_r400_win (ktext)

first full pass at the sc_busy is done.

... #35 change 36227 edit on 2002/06/25 by donaldl@fl_donaldl_p4 (ktext)

Cleaned up anti-alias state variable names.

... #34 change 36193 edit on 2002/06/25 by donaldl@fl_donaldl_p4 (ktext)

Changed signal names on input busy signals from pkr_iter to sc_stage_reg.

... #33 change 36148 edit on 2002/06/25 by mmantor@mmantor_r400_win (ktext)

adding the sc busy determination logic, there will be an update

... #32 change 35920 edit on 2002/06/24 by rramsey@RRAMSEY_P4_r400_win (ktext)

Reformat sc_sx dump for rb_id/split/tilex/tiley change
Change sc_primfifo to use memory based fifo and modify qpp to
  remove a reg stage and pop the fifo one clk later
Add cntx0_dec and cntx17_dec signals to qpp for front-pipe
  busy count decrementing
Add RC_SC_rb_id and RC_SC_split signals to sc top and pipe
  those sigs all the way to the qpp outputs
Update sc_sx tracker to handle new emu dump file format
  rb_id and split are not being compared yet since RC drivers
  are not in RTL yet

... #31 change 35836 edit on 2002/06/24 by mmantor@mmantor_r400_win (ktext)

added pkr busy signals

... #30 change 35649 edit on 2002/06/21 by donaldl@fl_donaldl_p4 (ktext)
```

```
Added initial logic support for context0 and context1to7 busy signals.

... #29 change 34331 edit on 2002/06/15 by donaldl@fl_donaldl_p4 (ktext)

Clear the valid signal from sc_coarse_dly during SRST.

... #28 change 33628 edit on 2002/06/12 by mmantor@mmantor_r400_win (ktext)

got sc to sp interface working in the sc

... #27 change 33369 edit on 2002/06/11 by donaldl@fl_donaldl_p4 (ktext)

Added iterator block (ie. sc_iter).

... #26 change 33104 edit on 2002/06/10 by donaldl@fl_donaldl_p4 (ktext)

Registered RC_SC_HEIR_MASK, RC_SC_HEIR_SEND, and SC_RC_HEIR_RTR using ati_dff flops.

... #25 change 32993 edit on 2002/06/10 by rramsey@RRAMSEY_P4_r400_win (ktext)

This time really remove unused state inputs

... #24 change 32985 edit on 2002/06/10 by rramsey@RRAMSEY_P4_r400_win (ktext)

Add aa_mask to sc_rbiu decode and sc_state block
Add state index selects for qdpr_proc and iterator blocks
Fix problem with testbench rc_sc driver
Remove temp state inputs from sc.v

... #23 change 32891 edit on 2002/06/10 by donaldl@fl_donaldl_p4 (ktext)

Changed for state variables .o work with rbiu

... #22 change 32699 edit on 2002/06/07 by rramsey@RRAMSEY_P4_r400_win (ktext)

Add rc_sc inputs and sc_rc trackers to tb_sc
Add out_compare.v and ../tb_sc_qdpr_proc/out_compare.v to tb_sc and sc Makefile
Correct clk and rst inputs to usc_qdpr_proc in sc.v

... #21 change 32511 edit on 2002/06/06 by donaldl@fl_donaldl_p4 (ktext)

Merge with latest version

... #20 change 32497 edit on 2002/06/06 by mmantor@mmantor_r400_win (ktext)

updated for packer changes and gc level compile

... #19 change 32460 edit on 2002/06/06 by mmantor@mmantor_r400_win (ktext)
```

```
updated top level for gc integration issues and to work with latest packer

... #18 change 32082 edit on 2002/06/05 by rramsey@RRAMSEY_P4_r400_win (ktext)

Updates to sc rtl
Remove oQPP_Q0_VALID and oQPP_Q1_VALID from sc_qdpr_proc.v
Add event flag to primitive fifo
Update sc_qdpr_proc testbench

... #17 change 31964 edit on 2002/06/05 by mmantor@mmantor_r400_win (ktext)

added initial sc_packer code to the sc.v  and a test bench for it

... #16 change 31924 edit on 2002/06/05 by donaldl@fl_donaldl_p4 (ktext)

Corrected some bit width signals while instantiating.

... #15 change 31807 edit on 2002/06/04 by donaldl@fl_donaldl_p4 (ktext)

Added sc_coarse_dly

... #14 change 31702 edit on 2002/06/04 by rramsey@rrhome_r400_win (ktext)

Change sc_quad_select instance to sc_qdpr_proc and add associated signals
Add sc_qdpr_proc to Makefile

... #13 change 31317 edit on 2002/06/01 by donaldl@fl_donaldl_p4 (ktext)

Removed sc_busy

... #12 change 30808 edit on 2002/05/30 by rramsey@RRAMSEY_P4_r400_win (ktext)

adding sc_quad_select rtl, and updating sc.v to include it

... #11 change 28521 edit on 2002/05/16 by donaldl@fl_donaldl_p4 (ktext)

Fixed errors when loading in vsim

... #10 change 28391 edit on 2002/05/16 by donaldl@fl_donaldl_p4 (ktext)

Added first cut of rbbm interface and state variables.

... #9 change 27740 edit on 2002/05/13 by donaldl@fl_donaldl_p4 (ktext)

Instantiated sc_stage_reg unit, primitive fifo, Z fifo, and tile fifo.

... #8 change 27075 edit on 2002/05/08 by donaldl@fl_donaldl_p4 (ktext)
```

```
Added changes to clk gating logic.  Added null prim input to sc_pipe.

... #7 change 25866 edit on 2002/05/01 by donaldl@fl_donaldl_p4 (ktext)

Instantiated sc_pipe, sc_coarse_walker, & sc_quadmask blocks.

... #6 change 25324 edit on 2002/04/29 by mmantor@mmantor_r400_win (ktext)

updated spec for PA_SC_su interface changes
updated sc.v and created tb directories

... #5 change 23321 edit on 2002/04/15 by mmantor@mmantor_r400_win (ktext)

seperated some sc_interp stuff for hardware modeling of output controllers

... #4 change 21452 edit on 2002/04/02 by mmantor@mmantor_r400_win (ktext)

removed sc_rbbm_nrtrtr

... #3 change 20769 edit on 2002/03/27 by mmantor@mmantor_r400_win (ktext)

updated for interface integration changes

... #2 change 20474 edit on 2002/03/26 by mmantor@mmantor_r400_win (ktext)

updated for spec changes

... #1 change 19542 add on 2002/03/18 by mmantor@mmantor_r400_win (ktext)

initial top level for the pa and sc verilog files
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ais/sq_ais_output.v
... #26 change 53800 edit on 2002/09/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for events flowing thru SQ
- cleared up issues with making individial vtx and pix thread buffers (and shared
thread_buff_cntl)
- fixed PV,PS bugs

... #25 change 50294 edit on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

update to write enables due to PV, PS cycle swap

... #24 change 50193 edit on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updated kill_mask out to SX

... #23 change 50165 edit on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for pc write one cycle early

... #22 change 49848 edit on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

... #21 change 48974 edit on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- needed to drive acfs_reading one cycle earlier for ACFS IS read
- updated/added new SQ_SP instruction interface

... #20 change 48558 edit on 2002/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for out-of-order thread processing: the 2 alu ctl flow sequencers
  now share one instr store read slot instead of alternating between two
  different slots (which allowed one to get ahead opf the other)
- thread counts from VISM and PISM to ais_output added at SQ level

... #19 change 48384 edit on 2002/08/27 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updates for ptr_buff/pism to align quad mask correctly
```

```
- additions for thread_count

... #18 change 48164 edit on 2002/08/26 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for individual macc write enables
- added the prev_pos_alloc inputs to the status regs (and logic to
  generate them in the tread buffer)

... #17 change 46251 edit on 2002/08/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates for pop/winner_ack status reg conflict

... #16 change 41217 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for sq-sx export

... #15 change 40937 edit on 2002/07/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- added alu_instr_pending status bit
- added new SQ_SX_exp and SQ_SX_free interfaces (free is not functional)

... #14 change 40686 edit on 2002/07/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- updated decode for exports to be the same as in the AIQ: this
  fixes extraneous GPR writes

... #13 change 34539 edit on 2002/06/17 by vromaker@vromaker_r400_linux_marlboro
(ktext)

temp hack to param cache write addr and enable to move them out 1 cycle

... #12 change 34083 edit on 2002/06/14 by vromaker@vromaker_r400_linux_marlboro
(ktext)

sending correct export address in SP instruction

... #11 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro
(ktext)

many updates... some v2k removal

... #10 change 33554 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)
```

```
moved gpr_rd_en one cycle earlier for srcA

... #9 change 33536 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

sending srcA gpr read addr one cycle earlier

... #8 change 32898 edit on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

... #7 change 32275 edit on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro (ktext)

updated tex instr const_index field to the new format

... #6 change 30816 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed blocking assignment on SQ_SP_gpr_wr_en

... #5 change 30562 edit on 2002/05/29 by vromaker@vromaker_r400_linux_marlboro (ktext)

fixed input_sel output

... #4 change 30559 edit on 2002/05/29 by vromaker@vromaker_r400_linux_marlboro (ktext)

connected the gpr input mux sel

... #3 change 27050 edit on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro (ktext)

       updates

... #2 change 26726 edit on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro (ktext)

submitting all...

... #1 change 23514 add on 2002/04/16 by vromaker@vromaker_r400_sun_marlboro (ktext)

updating with latest versions
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ca/sq_thread_arb.v
... #24 change 53375 edit on 2002/09/24 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixes for moving event thru the SQ
- fixes for dealloc, and state_diff in thread buffers

... #23 change 48558 edit on 2002/08/28 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fix for out-of-order thread processing: the 2 alu ctl flow sequencers
  now share one instr store read slot instead of alternating between two
  different slots (which allowed one to get ahead opf the other)
- thread counts from VISM and PISM to ais_output added at SQ level

... #22 change 46517 edit on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed thread read state machine typo

... #21 change 46251 edit on 2002/08/15 by vromaker@vromaker_r400_linux_marlboro
(ktext)

updates for pop/winner_ack status reg conflict

... #20 change 44548 edit on 2002/08/06 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- status register shift connection bug fixed

... #19 change 43237 edit on 2002/07/30 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- temp fix to ptr buff to delay free_buff to SC
- comments in thread arb
- re-enabled alu interleaving

... #18 change 42996 edit on 2002/07/29 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- fixed priority encoders (was reversed)

... #17 change 41831 edit on 2002/07/22 by dougd@dougd_r400_linux_marlboro (ktext)

added `include "../misc/sq_defs.v"

... #16 change 40937 edit on 2002/07/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)
```

```
- added alu_instr_pending status bit
- added new SQ_SX_exp and SQ_SX_free interfaces (free is not functional)

... #15 change 39972 edit on 2002/07/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixes for 2 pixel vectors

... #14 change 39731 edit on 2002/07/11 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixes for 2 pix vectors

... #13 change 34969 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for CFI fetch (alloc had to update CFI ptr); added a few busy signals

... #12 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

misc updates... alu_req logic updated in sq_status_reg

... #11 change 33492 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro
(ktext)

various updates - instr start asserted to SP

... #10 change 32898 edit on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

... #9 change 32472 edit on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro (ktext)

       thread buff - arb interface updates

... #8 change 31693 edit on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #7 change 31621 edit on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #6 change 31586 edit on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro (ktext)
```

```
updates

... #5 change 31361 edit on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #4 change 31279 edit on 2002/05/31 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #3 change 30971 edit on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #2 change 29767 edit on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro (ktext)

updates

... #1 change 28916 add on 2002/05/17 by vromaker@vromaker_r400_linux_marlboro (ktext)

new sq files for clause-less state management : initial, not complete, versions
```

```
//depot/r400/devel/parts_lib/src/gfx/sp/vector/sp_vector.v
... #11 change 54226 edit on 2002/09/29 by askende@askende_r400_linux_marlboro (ktext)

fixing width mismatches warnings out of bcons on some of the top level IOs

... #10 change 53986 edit on 2002/09/26 by askende@askende_r400_linux_marlboro (ktext)

1.add the scalar SUB opcode
       2. replaced one of the skid_buff_top fifos with an ati_fifo_top instance

... #9 change 53874 edit on 2002/09/26 by askende@askende_r400_linux_marlboro (ktext)

fixed a "logic timing" problem related to Scalar Result write-back path into GPRs

... #8 change 52508 edit on 2002/09/19 by askende@askende_r400_sun_marlboro (ktext)

changes:

1. corrected an overflow condition in the multiply logic of the interpolators
2. rewrote the gpr write-back path logic for the scalar results

... #7 change 52052 edit on 2002/09/17 by askende@askende_r400_sun_marlboro (ktext)

changes to :

1. interpolators to handle sub-norm ij values.
2. scalar engine result back to GPRs.
3. gc.tree regarding the tp_sp_valid signals.

... #6 change 51440 edit on 2002/09/13 by askende@askende_r400_sun_marlboro (ktext)

changes:

1.fixed overflow detection logic in macc32
2. fixed RECIP and RECIP_SQRT logic in scalar_lut
3. replaced gpr_cmask = 0xf with the value driven by SQ

... #5 change 49872 edit on 2002/09/05 by askende@askende_r400_sun_marlboro (ktext)

changes related to syntax and new instruction interface

... #4 change 48978 edit on 2002/08/30 by askende@askende_r400_sun_marlboro (ktext)

checking in changes related to the new instruction interface

... #3 change 47863 edit on 2002/08/23 by askende@askende_r400_sun_marlboro (ktext)

added sq_sp_gpr_wr_ena signal for all the phases of a vector unit.
```

```
... #2 change 46373 edit on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

renamed some of the modules

... #1 change 46348 add on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

this check in is related to renaming some of the files to sp_*

//depot/r400/devel/parts_lib/src/gfx/sp/vector/vector.v
... #19 change 46373 delete on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

renamed some of the modules

... #18 change 42463 edit on 2002/07/25 by askende@askende_r400_sun_marlboro (ktext)

maybe a syntax problem with [0:0] input declaration

... #17 change 41109 edit on 2002/07/17 by askende@askende_r400_sun_marlboro (ktext)

top level changes driven by the changes in related to SQ-SX export
allocation/deallocation interface.

... #16 change 36075 edit on 2002/06/25 by askende@askende_r400_sun_marlboro (ktext)

three bug fixes:

1. vector.v
    gpr_cmask is daizy_chained from one macc_gpr to the other
2.export_buffers.v
    mem_we is used instead of the registered version of it.

... #15 change 34222 edit on 2002/06/14 by askende@askende_r400_sun_marlboro (ktext)

at this point the PA block gets the valid position data

... #14 change 33393 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (ktext)

fixed a bug related to gpr_wr_ena control signal generation.

... #13 change 33346 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (ktext)

added a top level signal called TP_SP_data_valid which propagate all the way down to
vector.v

... #12 change 33157 edit on 2002/06/11 by askende@askende_r400_sun_marlboro (ktext)

added the masking logic for the GPR write path
```

```
... #11 change 31724 integrate on 2002/06/04 by askende@askende_r400_sun_marlboro
(ktext)

changes at the top level

1. adding sp_sx_exp_dest port to sp.v
2. connecting the sp_tp_fetch_addr ports at the top level
3. changing the sp_sx_exp_dest port from 7 bits to 6 bits in sx.v

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/vector.v#4
... #10 change 31584 integrate on 2002/06/03 by askende@askende_r400_sun_marlboro
(ktext)

intergrating

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/vector.v#3
... #9 change 31296 integrate on 2002/05/31 by askende@askende_r400_sun_marlboro
(ktext)

changes to signal naming

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/vector.v#2
... #8 change 28947 edit on 2002/05/17 by askende@askende_r400_sun_marlboro (ktext)

1. modified the top level sp.v file.
2. exposed the texture fetch path all the way from macc_gpr to sp.v.
3. modified and tested the interp_ctl.v ...the ij buffer control logic.
4. replaced the dum_mem_p2 with virage rtl behavioral model.

... #7 change 26985 edit on 2002/05/08 by askende@askende_r400_sun_marlboro (ktext)

latest top level as well as some changes regarding clock/reset signal naming

... #6 change 17964 edit on 2002/03/07 by askende@askende_r400_sun_marlboro (ktext)

backing up changes

... #5 change 17602 edit on 2002/03/05 by askende@askende_r400_sun_marlboro (ktext)

intergrated the scalar unit with the vector unit module

... #4 change 16541 edit on 2002/02/25 by askende@askende_r400_sun_marlboro (ktext)

new revision of the shader pipe logic.
```

```
renamed some of the signals throughout the hierarchy.

... #3 change 14458 edit on 2002/02/01 by askende@askende_r400_sun_marlboro (ktext)

backing up code changes

... #2 change 14314 edit on 2002/01/31 by askende@andi_r400 (ktext)

saving the changes so I can reconfigure my devel_askende area

... #1 change 14288 add on 2002/01/30 by askende@andi_r400 (ktext)

first time checked in

//depot/r400/devel/parts_lib/src/gfx/sp/vector/vector.v
... #19 change 46373 delete on 2002/08/15 by askende@askende_r400_sun_marlboro (ktext)

renamed some of the modules

... #18 change 42463 edit on 2002/07/25 by askende@askende_r400_sun_marlboro (ktext)

maybe a syntax problem with [0:0] input declaration

... #17 change 41109 edit on 2002/07/17 by askende@askende_r400_sun_marlboro (ktext)

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... #16 change 36075 edit on 2002/06/25 by askende@askende_r400_sun_marlboro (ktext)

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1. vector.v
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2.export_buffers.v
    mem_we is used instead of the registered version of it.

... #15 change 34222 edit on 2002/06/14 by askende@askende_r400_sun_marlboro (ktext)

at this point the PA block gets the valid position data

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vector.v

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//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/vector.v#4
... #10 change 31584 integrate on 2002/06/03 by askende@askende_r400_sun_marlboro
(ktext)

intergrating

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/vector.v#3
... #9 change 31296 integrate on 2002/05/31 by askende@askende_r400_sun_marlboro
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changes to signal naming

... ... copy from
//depot/r400/branches/devel_askende_branch/parts_lib/src/gfx/sp/vector/vector.v#2
... #8 change 28947 edit on 2002/05/17 by askende@askende_r400_sun_marlboro (ktext)

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4. replaced the dum_mem_p2 with virage rtl behavioral model.

... #7 change 26985 edit on 2002/05/08 by askende@askende_r400_sun_marlboro (ktext)

latest top level as well as some changes regarding clock/reset signal naming

... #6 change 17964 edit on 2002/03/07 by askende@askende_r400_sun_marlboro (ktext)

backing up changes

... #5 change 17602 edit on 2002/03/05 by askende@askende_r400_sun_marlboro (ktext)

```
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... #4 change 16541 edit on 2002/02/25 by askende@askende_r400_sun_marlboro (ktext)

new revision of the shader pipe logic.
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... #3 change 14458 edit on 2002/02/01 by askende@askende_r400_sun_marlboro (ktext)

backing up code changes

... #2 change 14314 edit on 2002/01/31 by askende@andi_r400 (ktext)

saving the changes so I can reconfigure my devel_askende area

... #1 change 14288 add on 2002/01/30 by askende@andi_r400 (ktext)

first time checked in
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/ss/sq_pix_thread_buff.v
... #4 change 54201 edit on 2002/09/28 by dougd@dougd_r400_linux_marlboro (ktext)

corrected the `defines in the parameter list of the instantiation of
sq_thread_buff_cntl from those for "vtx" to those for "pix"

... #3 change 53800 edit on 2002/09/26 by vromaker@vromaker_r400_linux_marlboro (ktext)

- fixes for events flowing thru SQ
- cleared up issues with making individial vtx and pix thread buffers (and shared
thread_buff_cntl)
- fixed PV,PS bugs

... #2 change 53376 edit on 2002/09/24 by dougd@dougd_r400_linux_marlboro (ktext)

removed redundant declaration that caused synopsys compile error

... #1 change 53039 add on 2002/09/23 by dougd@dougd_r400_linux_marlboro (ktext)

new modules to increase size of pixel thread buffer
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_parameter_caches.v
... #1 change 53452 add on 2002/09/24 by askende@askende_r400_linux_marlboro (ktext)

adding new files after having renamed existing ones
       with sx_*
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_export_control.v
... #4 change 54226 edit on 2002/09/29 by askende@askende_r400_linux_marlboro (ktext)

fixing width mismatches warnings out of bcons on some of the top level IOs

... #3 change 53986 edit on 2002/09/26 by askende@askende_r400_linux_marlboro (ktext)

1.add the scalar SUB opcode
       2. replaced one of the skid_buff_top fifos with an ati_fifo_top instance

... #2 change 53486 edit on 2002/09/24 by askende@askende_r400_linux_marlboro (ktext)

   renaming files to sx_<file_name>

... #1 change 53452 add on 2002/09/24 by askende@askende_r400_linux_marlboro (ktext)

adding new files after having renamed existing ones
       with sx_*
```

```
//depot/r400/devel/parts_lib/src/gfx/sq/misc/sq_export_alloc.v
... #16 change 50806 edit on 2002/09/11 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fixes for bug326 and 329 - tests still fail, but for different reasons

... #15 change 46629 edit on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

more fixes for alloc size

... #14 change 46574 edit on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro
(ktext)

fix for SQ_SX_export_id (was connected to wrong signal)

... #13 change 44314 edit on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

more delay for free_done

... #12 change 44294 edit on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- 3 cycle delay added for free_done
- port width fixes

... #11 change 44010 edit on 2002/08/02 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- multi pixel vector fixes
- VISM fixed for 32 vertex test

... #10 change 41326 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro
(ktext)

- corrected exp_type for pix w/o z
- fixed cfs_export_id_q to load global_export_id_q only when allocating
- or'd more signals together in TIF to get a solid busy output

... #9 change 41217 edit on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro (ktext)

- fixes for sq-sx export

... #8 change 40937 edit on 2002/07/16 by vromaker@vromaker_r400_linux_marlboro (ktext)

- added alu_instr_pending status bit
- added new SQ_SX_exp and SQ_SX_free interfaces (free is not functional)
```

```
... #7 change 34969 edit on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro (ktext)

fix for CFI fetch (alloc had to update CFI ptr); added a few busy signals

... #6 change 34083 edit on 2002/06/14 by vromaker@vromaker_r400_linux_marlboro (ktext)

sending correct export address in SP instruction

... #5 change 33977 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro (ktext)

changed polarity of exp_pix

... #4 change 33940 edit on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro (ktext)

many updates... some v2k removal

... #3 change 33615 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

misc updates... alu_req logic updated in sq_status_reg

... #2 change 33492 edit on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro (ktext)

various updates - instr start asserted to SP

... #1 change 33233 add on 2002/06/11 by vromaker@vromaker_r400_linux_marlboro (ktext)

SX exp added; tgt instr cnt from CFS to TIF fixed; alloc stuff added
```

```
//depot/r400/devel/parts_lib/src/gfx/sx/sx_param_cache_ctl.v
... #2 change 53483 edit on 2002/09/24 by askende@askende_r400_linux_marlboro (ktext)

 renamed the .ctmc files by adding the sx prefix

... #1 change 53452 add on 2002/09/24 by askende@askende_r400_linux_marlboro (ktext)

adding new files after having renamed existing ones
       with sx_*
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa.v
... #77 change 54077 edit on 2002/09/27 by dclifton@dclifton_r400 (ktext)

Added read-back capability to pa_ag and updated tbmod_rbbm_pa to check any reads.

... #76 change 54008 edit on 2002/09/27 by bhankins@fl_bhankins_r400_win (ktext)

Eliminate separate primic_event fifo.

Rename primic_state fifo to vgt_to_clips.

Add null_prim to vgt p bus.

Fix state select bug in pa_cl_vert_store_nopos.

Fix fifo depths to match csim.

Remade tbmod_vgttoclip from scratch.

... #75 change 51484 edit on 2002/09/13 by dclifton@dclifton_r400 (ktext)

Increased width of event_id to 5 bits

... #74 change 51432 edit on 2002/09/13 by bhankins@fl_bhankins_r400_win (ktext)

increased event id through clipper from 4 to 5 bits

... #73 change 51103 edit on 2002/09/12 by bhankins@fl_bhankins_r400_win (ktext)

fixed two drivers on one signal

... #72 change 51089 edit on 2002/09/12 by dclifton@dclifton_r400 (ktext)

Fixed a bunch of leda errors

... #71 change 50770 edit on 2002/09/11 by dclifton@dclifton_r400 (ktext)

Fixed lint warnings, added vte_busy to pa_rbbm_busy output

... #70 change 49945 edit on 2002/09/06 by bhankins@fl_bhankins_r400_win (ktext)

removed unused bit from clip_to_arb bus

... #69 change 49612 edit on 2002/09/05 by bhankins@fl_bhankins_r400_win (ktext)

added two more inputs into the generation of the clipper_busy signal:

current_state_empty from the clipper state machine, and
```

sx_pending_fifo_empty, from the shader export interface module.

... #68 change 49269 edit on 2002/09/03 by bhankins@fl_bhankins_r400_win (ktext)

replace vgt_to_clips fifo with primic_element_fifo and primic_state_fifo.

... #67 change 48492 edit on 2002/08/28 by bhankins@fl_bhankins_r400_win (ktext)

changed state variable index used by vert_store from that coming from ccg to that
coming from primic interface, and removed state_var_indx from ccg to clip interface.

... #66 change 48390 edit on 2002/08/27 by dclifton@dclifton_r400 (ktext)

Fixed test bench and I/O for active high CG_PA_pm_en

... #65 change 48356 edit on 2002/08/27 by bhankins@fl_bhankins_r400_win (ktext)

rename vgt p bus null_prim signal to event_flag

... #64 change 48348 edit on 2002/08/27 by sallen@sallen_r400_lin_marlboro (ktext)

update _pm_enb to use positive sense of clock

... #63 change 48209 edit on 2002/08/27 by bhankins@fl_bhankins_r400_win (ktext)

removed commented line.

... #62 change 44956 edit on 2002/08/08 by bhankins@fl_bhankins_r400_win (ktext)

implement latest changes - nan discard, bad pipe support, and state

based point size during ucp clipping.

... #61 change 44885 edit on 2002/08/08 by dclifton@dclifton_r400 (ktext)

Widened zmin/zmax to allow clamp -8 to +8, forced backfacing to zero for normal lines
and points.

... #60 change 44078 edit on 2002/08/02 by dclifton@dclifton_r400 (ktext)

Deleting unused i/o between blocks.

... #59 change 43725 edit on 2002/08/01 by bhankins@fl_bhankins_r400_win (ktext)

fixed some synopsys warnings

... #58 change 43657 edit on 2002/08/01 by bhankins@fl_bhankins_r400_win (ktext)

separate position and point size write addresses

... #57 change 43338 edit on 2002/07/31 by bhankins@fl_bhankins_r400_win (ktext)

removed provoking_vertex output from pa_clipper.v

... #56 change 43304 edit on 2002/07/31 by bhankins@fl_bhankins_r400_win (ktext)

increased pa s-bus input prim_type from 3 to 4 bits

... #55 change 42412 edit on 2002/07/25 by dclifton@dclifton_r400 (ktext)

Removed reset from pa_rbiu

... #54 change 42317 edit on 2002/07/25 by bhankins@fl_bhankins_r400_win (ktext)

use point (not position) address, for writing to point and position memories, since it is updated last.

... #53 change 42205 edit on 2002/07/24 by bhankins@fl_bhankins_r400_win (ktext)

1. move event input from p to s bus

2. add in event and event_id

3. start to add in point size logic. still has bugs.

... #52 change 42161 edit on 2002/07/24 by bhankins@fl_bhankins_r400_win (ktext)

added logic for clipper read access to point size memory

... #51 change 40996 edit on 2002/07/17 by dclifton@dclifton_r400 (ktext)

Replace updated version of pa_cl_ve.bvrl, reverted pa to use lower case I/O names in pa_cl_ve

... #50 change 40974 edit on 2002/07/17 by bhankins@fl_bhankins_r400_win (ktext)

change to match pa_cl_ve i/o signal names

... #49 change 40037 edit on 2002/07/12 by dclifton@dclifton_r400 (ktext)

Delete several unused signals

... #48 change 39973 edit on 2002/07/12 by dclifton@dclifton_r400 (ktext)

First check-in of new state variable design.

```
... #47 change 39499 edit on 2002/07/10 by dclifton@dclifton_r400 (ktext)

Updates for Z precision and provoking vtx changes

... #46 change 39026 edit on 2002/07/09 by bhankins@fl_bhankins_r400_win (ktext)

cleanup baryc-su i/f, and add ability to get point size from ag.

... #45 change 38665 edit on 2002/07/08 by bhankins@fl_bhankins_r400_win (ktext)

add separate cl/su baryc i/f

... #44 change 38651 edit on 2002/07/08 by bhankins@fl_bhankins_r400_win (ktext)

add separate baryc i/f to su

... #43 change 36790 edit on 2002/06/27 by bhankins@fl_bhankins_r400_win (ktext)

fix rtrs to vgt

... #42 change 36710 edit on 2002/06/27 by bhankins@fl_bhankins_r400_win (ktext)

wire in pa_cl_rei

... #41 change 35740 edit on 2002/06/24 by bhankins@fl_bhankins_r400_win (ktext)

used the right flop for busy signal

... #40 change 35556 edit on 2002/06/21 by bhankins@fl_bhankins_r400_win (ktext)

put some more logic behind PA_RBBM_busy to include clipper and

input and output dff's.

... #39 change 35095 edit on 2002/06/20 by bhankins@fl_bhankins_r400_win (ktext)

started to add event signal into pa.  for now it pretty much passes through from vgt
through 1-clk clipper to su.

... #38 change 33578 edit on 2002/06/12 by dclifton@dclifton_r400 (ktext)

Added new clipper/su baryc interface to SU, added VGT draw initiator state variable for
SU

... #37 change 33525 edit on 2002/06/12 by bhankins@fl_bhankins_r400_win (ktext)

update shader export interface, clip code generator and
```

clipper to match csim ccgen.cpp and clip.cpp

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... #36 change 32552 edit on 2002/06/07 by bhankins@fl_bhankins_r400_win (ktext)

changed prim_type to 3 bits

... #35 change 32397 edit on 2002/06/06 by dclifton@dclifton_r400 (ktext)

Changed all internal signals in pa.v to lower case, carried change down into SU, VTE, and VE

... #34 change 32279 edit on 2002/06/06 by dclifton@dclifton_r400 (ktext)

Connected up some rcpeng signals

... #33 change 32148 edit on 2002/06/05 by dclifton@dclifton_r400 (ktext)

Connecting outputs of PA_SX

... #32 change 32129 edit on 2002/06/05 by dclifton@dclifton_r400 (ktext)

Fixed pa_sx output register connections

... #31 change 31962 edit on 2002/06/05 by dclifton@dclifton_r400 (ktext)

Connected up su_busy to PA_RBBM_busy and deleted PA_RBBM_ntrrtr from pa (tie hi at rbbm)

... #30 change 31922 edit on 2002/06/05 by bhankins@fl_bhankins_r400_win (ktext)

increased deallocate_slot to three bits

... #29 change 31871 edit on 2002/06/04 by dclifton@dclifton_r400 (ktext)

connected up pa_rbbm_busy with su_busy

... #28 change 31744 edit on 2002/06/04 by dclifton@dclifton_r400 (ktext)

Updates to get rid of unknowns

... #27 change 31615 edit on 2002/06/03 by dclifton@dclifton_r400 (ktext)

Debugging--intermediate check in

... #26 change 31578 edit on 2002/06/03 by dclifton@dclifton_r400 (ktext)

Widened pa_su_cntl bus, temp fixed clip_su_dealloc_slot and ove_waddr mismatch.

... #25 change 31459 edit on 2002/06/03 by grayc@grayc_r400_win (ktext)

updates for integration

... #24 change 29913 edit on 2002/05/24 by bhankins@fl_bhankins_r400_win (ktext)

updates

... #23 change 29831 edit on 2002/05/24 by bhankins@fl_bhankins_r400_win (ktext)

misc wiring fixes

... #22 change 29705 edit on 2002/05/23 by fhsien@fhsien_r400_unix_marlboro (ktext)

Update pa.v for GC core

... #21 change 29699 edit on 2002/05/23 by dclifton@dclifton_r400 (ktext)

Updated vte interface with lowercase names

... #20 change 29652 edit on 2002/05/23 by bhankins@fl_bhankins_r400_win (ktext)

minor mod to state interfaces of pa_clipper and pa_sxifccg

... #19 change 29521 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

updates

... #18 change 29486 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

minor fixes

... #17 change 29469 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

make fixes to pa_clipper/rbiu state interface.

added pa_cl_rei

... #16 change 29468 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

removed debug-only signals from i/o

... #15 change 29319 edit on 2002/05/21 by dclifton@dclifton_r400 (ktext)

A few updates

```
... #14 change 29261 edit on 2002/05/21 by bhankins@fl_bhankins_r400_win (ktext)

started to add pa_clipper, pa_sxifccg

... #13 change 29064 edit on 2002/05/20 by bhankins@fl_bhankins_r400_win (ktext)

comment out references to pa_clip_pkg.v

... #12 change 29051 edit on 2002/05/20 by bhankins@fl_bhankins_r400_win (ktext)

added pa_sxifccg.v and pa_clipper.v

... #11 change 28343 edit on 2002/05/16 by grayc@grayc_r400_win (ktext)

another wiring error

... #10 change 28339 edit on 2002/05/16 by grayc@grayc_r400_win (ktext)

fix wiring errors

... #9 change 28328 edit on 2002/05/16 by grayc@grayc_crayola_unix_orl (ktext)

added `include "header.v" on files

... #8 change 27954 edit on 2002/05/14 by grayc@grayc_r400_win (ktext)

additional mods for interfacing registers, adding common blocks, etc

... #7 change 27800 edit on 2002/05/14 by grayc@grayc_r400_win (ktext)

updates for clocks and reset ...

... #6 change 27390 edit on 2002/05/10 by dclifton@dclifton_r400 (ktext)

Update for SU I/O changes (event, provokingvtx)
A few changes to state register implementation
Added rbiu and su to pa top block

... #5 change 27227 edit on 2002/05/09 by grayc@grayc_r400_win (ktext)

mods for integration

... #4 change 21044 edit on 2002/03/29 by mmantor@mmantor_r400_win (ktext)

added new signals from vgt and renamed two in the pa-> sx interface as a result of
reviews
```

```
... #3 change 20769 edit on 2002/03/27 by mmantor@mmantor_r400_win (ktext)

updated for interface integration changes

... #2 change 20474 edit on 2002/03/26 by mmantor@mmantor_r400_win (ktext)

updated for spec changes

... #1 change 19542 add on 2002/03/18 by mmantor@mmantor_r400_win (ktext)

initial top level for the pa and sc verilog files
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa_ag.v
... #27 change 54130 edit on 2002/09/27 by dclifton@dclifton_r400 (ktext)

Instantiated the real rams into the fifos.

... #26 change 54077 edit on 2002/09/27 by dclifton@dclifton_r400 (ktext)

Added read-back capability to pa_ag and updated tbmod_rbbm_pa to check any reads.

... #25 change 51338 edit on 2002/09/13 by dclifton@dclifton_r400 (ktext)

Fixed LEDA errors

... #24 change 49945 edit on 2002/09/06 by bhankins@fl_bhankins_r400_win (ktext)

removed unused bit from clip_to_arb bus

... #23 change 47996 edit on 2002/08/26 by bhankins@fl_bhankins_r400_win (ktext)

connect clip_state_var_indx_r0

... #22 change 47808 edit on 2002/08/23 by bhankins@fl_bhankins_r400_win (ktext)

enable clipper vert_store to access point size memory when the ccg isn't.

... #21 change 45373 edit on 2002/08/12 by grayc@grayc_r400_win (ktext)

temp fix for read data bus

... #20 change 45185 edit on 2002/08/09 by mmang@fl_mmang_r400_win (ktext)

Added logic to support state based point size ucp clipping in clipper.

... #19 change 43657 edit on 2002/08/01 by bhankins@fl_bhankins_r400_win (ktext)

separate position and point size write addresses

... #18 change 43319 edit on 2002/07/31 by bhankins@fl_bhankins_r400_win (ktext)

bug fix in selection of point size memory read address

... #17 change 42406 edit on 2002/07/25 by bhankins@fl_bhankins_r400_win (ktext)

undo previous change.  hangs some tests.  will investigate.

... #16 change 42339 edit on 2002/07/25 by bhankins@fl_bhankins_r400_win (ktext)

altered the priority of read access to pointsize memory
```

```
... #15 change 42161 edit on 2002/07/24 by bhankins@fl_bhankins_r400_win (ktext)

added logic for clipper read access to point size memory

... #14 change 41199 edit on 2002/07/18 by grayc@grayc_crayola_unix_orl (ktext)

changed component name for Stub'd memory

... #13 change 40982 edit on 2002/07/17 by grayc@grayc_crayola_unix_orl (ktext)

removed defparam (not supported by synthesis)

... #12 change 40652 edit on 2002/07/15 by mmang@fl_mmang_r400_win (ktext)

Added AG logic for point sprite clipping states.

... #11 change 36737 edit on 2002/06/27 by bhankins@fl_bhankins_r400_win (ktext)

fix sensitivity lists

... #10 change 34697 edit on 2002/06/18 by dclifton@dclifton_r400 (ktext)

Align latency with vector engine

... #9 change 33524 edit on 2002/06/12 by mmang@fl_mmang_r400_win (ktext)

Added clipper decode support for SMC_T_BLEND_(PREV/CURR)_(0/1), SMC_CLIP_DIST_(VV/UCP),
SMC_EDGE_DISTANCE_(0/1), and SMC_T_FACTOR_(PREV/CURR)_(0/1).

... #8 change 32321 edit on 2002/06/06 by mmang@fl_mmang_r400_win (ktext)

1.  Fix things lost in merge.
2.  Added register to be compatable with ati_1rp_state_storage.

... #7 change 32308 edit on 2002/06/06 by mmang@fl_mmang_r400_win (ktext)

1.  Increased src_vertex_indx from clip sm to 7 bits.
2.  Decreased ve_out_addr to 6 bits.
3.  Added decode for clip states SMC_OUTPUT_FIRST_BARYC_?,
    SMC_OUTPUT_FIRST_CLIP_POS_?, SMC_T_BLEND_PREV_ABC_?, and
    SMC_T_BLEND_CURR_ABC_?.

... #6 change 32245 edit on 2002/06/06 by bhankins@fl_bhankins_r400_win (ktext)

qualified decode on xfc

... #5 change 31557 edit on 2002/06/03 by dclifton@dclifton_r400 (ktext)
```

```
Changed commas in sensitivity lists to "or"

... #4 change 31459 edit on 2002/06/03 by grayc@grayc_r400_win (ktext)

updates for integration

... #3 change 30066 edit on 2002/05/24 by mmang@fl_mmang_r400_win (ktext)

1. Added VteIn.dmp and AgVeOut.dmp compares.
2. Added #0.5 delay to input drives and output compares.
3. Added agve_dly_valid to help sync AgVeOut compare.
4. Increased clip to AG state_var_indx to 3 bits.
5. Increased Ag to Vte opcode to 3 bits.
6. Fixed y swizzle select bug.
7. Renamed AgState.dmp to RbiuAg.dmp.

... #2 change 28328 edit on 2002/05/16 by grayc@grayc_crayola_unix_orl (ktext)

added `include "header.v" on files

... #1 change 24394 add on 2002/04/22 by mmantor@mmantor_r400_win (ktext)

added initial pa_ag code and testbench
```

```
//depot/r400/devel/parts_lib/src/gfx/pa/pa_sxifccg.v
... #14 change 54107 edit on 2002/09/27 by dclifton@dclifton_r400 (ktext)

Swapped out pa_ccg_vgt_to_ccgen_fifo, pa_cl_ccgen_to_clipcc_fifo, and
pa_cl_primic_to_clprim_fifo with ati_fifo.

... #13 change 50424 edit on 2002/09/10 by bhankins@fl_bhankins_r400_win (ktext)

change fifo instance names to align with convention

... #12 change 49612 edit on 2002/09/05 by bhankins@fl_bhankins_r400_win (ktext)

added two more inputs into the generation of the clipper_busy signal:

current_state_empty from the clipper state machine, and

sx_pending_fifo_empty, from the shader export interface module.

... #11 change 49504 edit on 2002/09/04 by bhankins@fl_bhankins_r400_win (ktext)

replace instances of ati_fifo_top with unique modules.

modified Makefile to reflect changes.

... #10 change 44956 edit on 2002/08/08 by bhankins@fl_bhankins_r400_win (ktext)

implement latest changes - nan discard, bad pipe support, and state

based point size during ucp clipping.

... #9 change 42317 edit on 2002/07/25 by bhankins@fl_bhankins_r400_win (ktext)

use point (not position) address, for writing to point and position memories, since it
is updated last.

... #8 change 33525 edit on 2002/06/12 by bhankins@fl_bhankins_r400_win (ktext)

update shader export interface, clip code generator and

clipper to match csim ccgen.cpp and clip.cpp

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... #7 change 29839 edit on 2002/05/24 by bhankins@fl_bhankins_r400_win (ktext)

backed state io down to just the bits for pa_sxifccg.v

... #6 change 29825 edit on 2002/05/24 by bhankins@fl_bhankins_r400_win (ktext)
```

```
mod to state i/o

... #5 change 29516 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

updates on sxif state

... #4 change 29459 edit on 2002/05/22 by bhankins@fl_bhankins_r400_win (ktext)

updates to fix state i/o and use proper state_storage modules

... #3 change 29235 edit on 2002/05/21 by bhankins@fl_bhankins_r400_win (ktext)

update (changed names of instantiated modules)

... #2 change 29032 edit on 2002/05/20 by bhankins@fl_bhankins_r400_win (ktext)

updates to support integration into pa.v

... #1 change 29029 add on 2002/05/20 by bhankins@fl_bhankins_r400_win (ktext)

Initial checkin
```

```
Change 54194 on 2002/09/28 by johnchen@johnchen_r400_linux_marlboro

reserve three cachelines for all memory formats, even 16bits expanded

Change 54131 on 2002/09/27 by jayw@jayw_r400_linux_marlboro

fixed back tile_done for zero mask tiles.
       expand_fifo fix to kill when doing flushes.

Change 54112 on 2002/09/27 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed color_expand logic to include cmask_enable (from color0_info register).

Change 54075 on 2002/09/27 by paulv@paulv_r400_linux_marlboro_rbrc

Use d_state_index instead of state_index for getting signals (cmask_enable,
zmask_enable, etc.) to determine surface_enabled.

Change 53904 on 2002/09/26 by johnchen@johnchen_r400_linux_marlboro

updating quaddata path to include surface_enable

Change 53882 on 2002/09/26 by paulv@paulv_r400_linux_marlboro_rbrc

Made a few optimizations and a bug fix or two.

Change 53881 on 2002/09/26 by paulv@paulv_r400_linux_marlboro_rbrc

Connected the RBM_RBT_rtr_r and RBM_RBT_rtr_w signals throughout the code where needed.

Change 53837 on 2002/09/26 by wlawless@wlawless_r400_linux_marlboro

all kind of stuff,

Change 53715 on 2002/09/25 by johnchen@johnchen_r400_linux_marlboro

timing fixes

Change 53711 on 2002/09/25 by johnchen@johnchen_r400_linux_marlboro

timing fixes

Change 53703 on 2002/09/25 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed surface_enabled bit and some logic using the signal.

Change 53649 on 2002/09/25 by paulv@paulv_r400_linux_marlboro_rbrc
```

```
Fixed some code discrepancies between the write fifo sizes and logic that depends on
the sizes (counters, full bits, etc.).

Change 53633 on 2002/09/25 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed tile cache to a).  only flush when the RBC tells to (through RBC_RBT_flush) and
b). to only flush if not having a probe miss (which needs to do a mc read).

Change 53604 on 2002/09/25 by wlawless@wlawless_r400_linux_marlboro

added a pipe delay to blend enable for timing

Change 53576 on 2002/09/25 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed all logic with writing to quad cache with rbd data, modifying inflight counts,
writing out a tile from the quad cache to the tile cache and writing that tile to the
correct location in the tile cache.

Change 53465 on 2002/09/24 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed addend1 of the mac2D equation (was taking the wrong bits from the surface_pitch).

Change 53455 on 2002/09/24 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed all pertinent leda errors/warnings.

Change 53323 on 2002/09/24 by wlawless@wlawless_r400_linux_marlboro

redid color_event_flush.... added back in the some_free which is now call
       reload_pipe2....

Change 53180 on 2002/09/23 by johnchen@johnchen_r400_linux_marlboro

quaddata_update fix

Change 53112 on 2002/09/23 by johnchen@johnchen_r400_linux_marlboro

more quaddata fixes

Change 53105 on 2002/09/23 by paulv@paulv_r400_linux_marlboro_rbrc

Now send probes to RBD even if z and stencil are disabled.

Change 53098 on 2002/09/23 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed a typo.

Change 53090 on 2002/09/23 by paulv@paulv_r400_linux_marlboro_rbrc
```

Added z_enable bit between depth and tile (so the quad cache knows when to update the zrange and smask, and not just the inflight counts).

Change 53075 on 2002/09/23 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed address size of the write fifos (now use defines).

Change 52971 on 2002/09/22 by johnchen@johnchen_r400_linux_marlboro

search timing fixes

Change 52931 on 2002/09/21 by paulv@paulv_r400_linux_marlboro_rbrc

Made fix for reading of uninitialized quad cache data.

Change 52930 on 2002/09/21 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed bug with uninitialized bit generation.

Change 52925 on 2002/09/21 by johnchen@johnchen_r400_linux_marlboro

quaddata update checkin

Change 52888 on 2002/09/20 by paulv@paulv_r400_linux_marlboro_rbrc

Fixes and some minor code-rewriting to correctly implement reading and writing to/from the quad cache for ALL tiles, with the exception of ones where the surface_enabled (disabled??) bit is inactive (active). This bit has not been added to the rb registers, so its hardcoded for now.

Change 52737 on 2002/09/20 by wlawless@wlawless_r400_linux_marlboro

fixed latches

Change 52595 on 2002/09/19 by johnchen@johnchen_r400_linux_marlboro

checkin quaddata IOs

Change 52578 on 2002/09/19 by jayw@jayw_r400_linux_marlboro

fix for flush tile section not written to.

Change 52471 on 2002/09/19 by jayw@jayw_r400_linux_marlboro

extra depth to fifos for performance.

Change 52470 on 2002/09/19 by jayw@jayw_r400_linux_marlboro

```
color_flush_event stays till nothing to flush

Change 52414 on 2002/09/18 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed typo and a timing issue with the new rbd_probe fifo.

Change 52404 on 2002/09/18 by johnchen@johnchen_r400_linux_marlboro

add frag address to RBD_RBC

Change 52376 on 2002/09/18 by wlawless@wlawless_r400_linux_marlboro

added to extra fragment probe logic
changed bus name to probe_rts_cam for rts_cam.... etc.

Change 52368 on 2002/09/18 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed all register decode logic to use defines (as found in rb_reg.v).

Change 52316 on 2002/09/18 by paulv@paulv_r400_linux_marlboro_rbrc

Added fifo (with skid) for output data to RBD probe.  Also made interface a true rts-
rtr interface.

Change 52247 on 2002/09/18 by wlawless@wlawless_r400_linux_marlboro

added a do_multi_sample for flush event

Change 52218 on 2002/09/18 by jayw@jayw_r400_linux_marlboro

Some defaults for the ram by request of Rob.  -- jayw

Change 52191 on 2002/09/17 by johnchen@johnchen_r400_linux_marlboro

fix the condition when MC return data is out of order because of multiple queues

Change 52173 on 2002/09/17 by jayw@jayw_r400_linux_marlboro

3 fixes.
       a. color_flush_event did not set set_auto_flush due to timing.
       b. popping off blend fifo for event even when empty.
       c. cam_page_hit_00 (et. al.) were 26 bits not one bit.

Change 52144 on 2002/09/17 by jayw@jayw_r400_linux_marlboro

a fix try3
```

```
Change 52128 on 2002/09/17 by jayw@jayw_r400_linux_marlboro

missing required pa_reg.v include

Change 52064 on 2002/09/17 by jayw@jayw_r400_linux_marlboro

potential fix for basic dither test.
       checked in early for Frank Hsien.

Change 51988 on 2002/09/17 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed ROP3 pixelsize logic and moved it after the actual pixel_format instantiations
since it was kind of confusing putting it before them.

Change 51892 on 2002/09/16 by paulv@paulv_r400_linux_marlboro_rbrc

Some lines went way beyond the max column width spec'd out in the verilog coding
guidelines.  Brought these lines back down to earth.

Change 51880 on 2002/09/16 by johnchen@johnchen_r400_linux_marlboro

fix some resolve problem

Change 51875 on 2002/09/16 by johnchen@johnchen_r400_linux_marlboro

RBT_RBD_probe

Change 51848 on 2002/09/16 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed some typos/incomplete logic.

Change 51847 on 2002/09/16 by paulv@paulv_r400_linux_marlboro_rbrc

Added color swap prior to alpha blender.

Change 51811 on 2002/09/16 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed rbd_rbt probe signals (some were out of sync/a cycle off and the valid needed to
depend on event).

Change 51804 on 2002/09/16 by jayw@jayw_r400_linux_marlboro

Fixed bruntest -s -t gl_src_alpha rbrc r400rb_alpha_source
       OR bruntest -s -t comb_dst_plus_src r400rb_basic_color_combination

Change 51798 on 2002/09/16 by jayw@jayw_r400_linux_marlboro

ROP3 for pixel 1 was getting wrong SRC pixel information for SEL.
```

```
Change 51796 on 2002/09/16 by jayw@jayw_r400_linux_marlboro

added the ability to handle unknowns where it needs to.

Change 51794 on 2002/09/16 by jayw@jayw_r400_linux_marlboro

Fixed some but not all of the back pressure typos.
       Fixed skid of fifos to correct size, i.e. 3.

Change 51793 on 2002/09/16 by jayw@jayw_r400_linux_marlboro

read strobe disconnected until RB and prove reg reads work

Change 51724 on 2002/09/16 by paulv@paulv_r400_linux_marlboro_rbrc

Introduced a bug where d_head_tag_valid was not getting active (because the signal was
based on whether the cmask_fifo_empty bit was 0 and not 1 like it should have been).

Change 51718 on 2002/09/16 by wlawless@wlawless_r400_linux_marlboro

fixed leda stuff

Change 51693 on 2002/09/16 by jayw@jayw_r400_linux_marlboro

Official rb leda file.

Change 51685 on 2002/09/16 by wlawless@wlawless_r400_linux_marlboro

fixed latches

Change 51500 on 2002/09/13 by paulv@paulv_r400_linux_marlboro_rbrc

Made RBT_RBD_probe_snd dependent on z_enable and stencil_enable.

Change 51477 on 2002/09/13 by jayw@jayw_r400_linux_marlboro

more changes to fix ram port and naming problems.

Change 51476 on 2002/09/13 by paulv@paulv_r400_linux_marlboro_rbrc

Added flush and invalidate logic for tile cache (signal from RBC).  NOTE:  since the
flush and invalidate define has yet to be defined in vgt_reg.v, this is temporarily
replaced with 16'hffff.

Change 51470 on 2002/09/13 by jayw@jayw_r400_linux_marlboro

renamed from 128x32 to 32x128 (32 high, 128 wide)
```

Change 51212 on 2002/09/12 by jayw@jayw_r400_linux_marlboro

fragment cache rams

Change 51184 on 2002/09/12 by jayw@jayw_r400_linux_marlboro

Leda fixes and attempted bug fixes.

Change 51163 on 2002/09/12 by wlawless@wlawless_r400_linux_marlboro

added the fragment stuff

Change 51161 on 2002/09/12 by wlawless@wlawless_r400_linux_marlboro

added fragment stuff

Change 51160 on 2002/09/12 by wlawless@wlawless_r400_linux_marlboro

adding all the multi-sample stuff

Change 50988 on 2002/09/12 by jayw@jayw_r400_linux_marlboro

fixed pin typo

Change 50980 on 2002/09/12 by jayw@jayw_r400_linux_marlboro

run_leda -f rb_leda.f

Change 50975 on 2002/09/12 by jayw@jayw_r400_linux_marlboro

event flush is now supported.
       several leda netlist connection fixes.
       an attempt to fix a bug found by Vic.

Change 50824 on 2002/09/11 by paulv@paulv_r400_linux_marlboro_rbrc

Added rtr from RBD probe interface for hiz probe. Changed almost all the rts signals to snd signals (since most don't really correspond to the ready to receive signal functionality--they are more like valids). Added surface synchronization signals for tile cache (don't do anything right now).

Change 50822 on 2002/09/11 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed a race condition with the generation of the queue_full bits and add the surface synchronization logic for tile. Also renamed rts signals to snd signals (since they really don't represent the meaning of ready to send).

Change 50769 on 2002/09/11 by johnchen@johnchen_r400_linux_marlboro

add includes to rb_rbd_cache_write and add IOs for RBT_RBD_probe and RBD_RBT_quaddata

Change 50606 on 2002/09/10 by johnchen@johnchen_r400_linux_marlboro

added three bits for valid and two bits for dirty to the depth cache

Change 50571 on 2002/09/10 by paulv@paulv_r400_linux_marlboro_rbrc

Last update introduced a bug/typo (rb_rc_hier_mask and rb_rc_hier_split weren't being output correctly). Fixed.

Change 50535 on 2002/09/10 by paulv@paulv_r400_linux_marlboro_rbrc

Removed ati input flop for RC_RB_hier_rtr (done in rb_rbt_hiz.v) and removed the ati output flops for RB_RC_hier* signals (also done in rb_rbt_hiz.v).

Change 50510 on 2002/09/10 by jayw@jayw_r400_linux_marlboro

Runs basic dither test, many fixes for color_combination too.

Change 50496 on 2002/09/10 by paulv@paulv_r400_linux_marlboro

Testbenches and vector files that are no longer needed.

Change 50460 on 2002/09/10 by paulv@paulv_r400_linux_marlboro

Test bench no longer needed.

Change 50305 on 2002/09/09 by paulv@paulv_r400_linux_marlboro_rbrc

Removed fmask_base register (gone) and corrected fragment local address calculation.

Change 50116 on 2002/09/09 by johnchen@johnchen_r400_linux_marlboro

fix some tag problems for 16bits depth

Change 50062 on 2002/09/06 by paulv@paulv_r400_linux_marlboro_rbrc

Added support for infinities and NaNs.

Change 50061 on 2002/09/06 by jayw@jayw_r400_linux_marlboro

Events flow down pipe. All milestone_event tests should run.

Change 50060 on 2002/09/06 by jayw@jayw_r400_linux_marlboro

Changes for event handling.

Change 50044 on 2002/09/06 by paulv@paulv_r400_linux_marlboro_rbrc

Removed sync signal to RBM and added RBT_RBD_probe_tile_<x,y> signals out of tile.

Change 50043 on 2002/09/06 by paulv@paulv_r400_linux_marlboro_rbrc

Removed sync input signal.

Change 50042 on 2002/09/06 by paulv@paulv_r400_linux_marlboro_rbrc

Fixes for address calculation logic.

Change 50023 on 2002/09/06 by johnchen@johnchen_r400_linux_marlboro

fix a small stencil hang

Change 50008 on 2002/09/06 by jayw@jayw_r400_linux_marlboro

Changes for event processing.

Change 49924 on 2002/09/06 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed address calculation for 2d surfaces (3d slice surface address calculation still broken).

Change 49904 on 2002/09/06 by johnchen@johnchen_r400_linux_marlboro

initial stencil hookup

Change 49815 on 2002/09/05 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed bug with color probe fifo being written when event occurs (should not have happened).

Change 49742 on 2002/09/05 by paulv@paulv_r400_linux_marlboro_rbrc

Removed event from color probe interface and made a fix for the event logic.

Change 49741 on 2002/09/05 by paulv@paulv_r400_linux_marlboro_rbrc

Removed sync_done bit from rbm.

Change 49740 on 2002/09/05 by paulv@paulv_r400_linux_marlboro_rbrc

Minor interface changes between tile, color, depth and the rbm.

Change 49738 on 2002/09/05 by paulv@paulv_r400_linux_marlboro_rbrc

Added surface synchronization logic.

Change 49720 on 2002/09/05 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed rts when event was high (at output).

Change 49611 on 2002/09/05 by jayw@jayw_r400_linux_marlboro

added ALL inflight wires for debug ONLY.

Change 49603 on 2002/09/04 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed event logic (the mask identifier in the tile cache, a misalignment of the event and mask out of rb_rbt_hiz_quad_checker and an incorrect mask out of rb_tile_fifo.v).

Change 49602 on 2002/09/04 by paulv@paulv_r400_linux_marlboro_rbrc

John found a bug with the intermingling of read and write requests. Sometimes a write request would be incorrectly made to the MC even though the RBM would not count it.

Change 49560 on 2002/09/04 by paulv@paulv_r400_linux_marlboro_rbrc

Added rb_reg.v to list of included files at top of code.

Change 49557 on 2002/09/04 by paulv@paulv_r400_linux_marlboro_rbrc

Added macro instantiation.

Change 49535 on 2002/09/04 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 49534 on 2002/09/04 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 49513 on 2002/09/04 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed size of ram data (from 219 bits to 223 bits).

Change 49512 on 2002/09/04 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed typo with generation of fragment address type (2d or 3d slice) flag.

Change 49443 on 2002/09/04 by jayw@jayw_r400_linux_marlboro

```
Fixed register copy.
       All milestone_tri tests pass.

Change 49420 on 2002/09/03 by paulv@paulv_r400_linux_marlboro_rbrc

Initial version.

Change 49419 on 2002/09/03 by paulv@paulv_r400_linux_marlboro_rbrc

Updates to get fragment interface implemented.  Also includes state read address fix
for state decode and the fixing of all important leda warnings and errors.

Change 49413 on 2002/09/03 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed read address for state decode.

Change 49411 on 2002/09/03 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed fog counter to max out at 5 instead of 6 (the number of cycles to get through the
alpha blender).

Change 49410 on 2002/09/03 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed module name to match file name.

Change 49246 on 2002/09/03 by jayw@jayw_r400_linux_marlboro

All milestone_tri tests pass with this fix.
       Counter must be 5 bits not 4 bits.
       Simulation time must be high than default for tri60x60, tri64x64.

Change 49134 on 2002/08/30 by jayw@jayw_r400_linux_marlboro

removed clock gater because of skew
       fixed state copy in RC for
       comb_src_minus_dst  of r400rb_color_combination

Change 49058 on 2002/08/30 by paulv@paulv_r400_linux_marlboro_rbrc

More fixes to get more tests passing, including reworking the tile cache to NOT use the
next data in the fifo (next_head_fifo_data) and instead use the current head of the
fifo (with the addition of a necessary state machine).

Change 48904 on 2002/08/29 by johnchen@johnchen_r400_linux_marlboro

addressing fix

Change 48841 on 2002/08/29 by sallen@sallen_r400_lin_marlboro
```

```
-finish up _pm_enb and _pm_en set to 1, clocks run now
   -also set busy signals low in blocks that don't drive them
   -fix mh DEPS file

Change 48829 on 2002/08/29 by wlawless@wlawless_r400_linux_marlboro

ran some debug on fragment probe stuff and made some fixes

Change 48751 on 2002/08/29 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed a stupid bug I implemented yesterday (used quad_cache_valids in cacheline
allocation logic).

Change 48728 on 2002/08/29 by jayw@jayw_r400_linux_marlboro

This is rb_clock.v#5 before the change to cg_rb_pm_enable
       as this has not yet been released.

Change 48701 on 2002/08/29 by johnchen@johnchen_r400_linux_marlboro_rbrc

24 bit fixed point depth

Change 48648 on 2002/08/28 by paulv@paulv_r400_linux_marlboro_rbrc

Real fix this time for reading quad cache uninitialized tiledata (previous attempt was
found to break certain test cases).

Change 48542 on 2002/08/28 by paulv@paulv_r400_linux_marlboro_rbrc

Fixed problem with uninitialized quad cache cachelines in the quad_checker of the HiZ
block.

Change 48447 on 2002/08/27 by paulv@paulv_r400_linux_marlboro

More fixes to get the entire milestone_tri test suite working.  Also reworked the quad
cache allocation scheme to be more robust (now takes in info from HiZ--tile_failed and
done_w_tile, if HiZ isn't enabled).

Change 48348 on 2002/08/27 by sallen@sallen_r400_lin_marlboro

update _pm_enb to use positive sense of clock

Change 48298 on 2002/08/27 by wlawless@wlawless_r400_linux_marlboro

fragment probe mask

Change 48296 on 2002/08/27 by wlawless@wlawless_r400_linux_marlboro
```

Initial add of the fragment probe stuff

Change 48222 on 2002/08/27 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 48193 on 2002/08/26 by paulv@paulv_r400_linux_marlboro

Fixed all bugs found with small suite of tests (milestone_tri), using the rbrc testbench.

Change 48192 on 2002/08/26 by paulv@paulv_r400_linux_marlboro

Updated tile subblock interface (and did some signal renaming to match the coding guidelines).

Change 48191 on 2002/08/26 by paulv@paulv_r400_linux_marlboro

More fixes, this time to the logic that determines if a read or write (or both) can be made. Added to the logic the signals denoting when a MC queue (for each client) is full.

Change 48121 on 2002/08/26 by jayw@jayw_r400_linux_marlboro_rbrc

Duh! bug fix, my own fault. -- jay
Address of fifo one bit too small!

Change 48004 on 2002/08/26 by paulv@paulv_r400_linux_marlboro

Got word that the agp queue was only 2-deep. Made necessary fixes.

Change 48000 on 2002/08/26 by paulv@paulv_r400_linux_marlboro

Write queues were supposed to be 16 (I changed them to 8 like the read versions). Fixed.

Change 47991 on 2002/08/26 by paulv@paulv_r400_linux_marlboro

Forgot to fix the adjustment of the tile and agp queue counters. Fixed.

Change 47987 on 2002/08/26 by paulv@paulv_r400_linux_marlboro

Changed tile and agp queue counters to 8 deep also.

Change 47922 on 2002/08/23 by paulv@paulv_r400_linux_marlboro

Fixed queue sizes for ab/cd queues (from 16 to 8).

Change 47747 on 2002/08/23 by jayw@jayw_r400_linux_marlboro

A fix for tri32_pix4 of milestone_tri that appears to have been missed.

Change 47682 on 2002/08/22 by jayw@jayw_r400_linux_marlboro_rbrc

fix for overfilling fifo (try 2)

Change 47670 on 2002/08/22 by jayw@jayw_r400_linux_marlboro_rbrc

PaulV fixed the next fifo head pointer. For milestone_tri.

Change 47669 on 2002/08/22 by jayw@jayw_r400_linux_marlboro_rbrc

all quads of a tile are removed by detailed walk fix.

Change 47667 on 2002/08/22 by jayw@jayw_r400_linux_marlboro_rbrc

fixes many milestone_tri bugs

Change 47555 on 2002/08/22 by paulv@paulv_r400_linux_marlboro

Fixed all leda warnings and errors.

Change 47554 on 2002/08/22 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 47527 on 2002/08/22 by paulv@paulv_r400_linux_marlboro

Fixed errors and warnings found with leda and fixed the tile cache fifo counter to
correctly take into account the delay from the RB to RC.

Change 47439 on 2002/08/21 by johnchen@johnchen_r400_linux_marlboro_rbrc

fix timing path for the decrement part of the inflight_count

Change 47357 on 2002/08/21 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 47260 on 2002/08/21 by johnchen@johnchen_r400_linux_marlboro

fix for handling flush stall

Change 47256 on 2002/08/21 by paulv@paulv_r400_linux_marlboro

Fixed the read enable strobe to be based on state like the
write enable is.

Change 47255 on 2002/08/21 by paulv@paulv_r400_linux_marlboro

Renamed a signal to match the signal name in the qc.

Change 47253 on 2002/08/21 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 47250 on 2002/08/21 by wlawless@wlawless_r400_linux_marlboro

fixed state_gfx_re

Change 47194 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Latest compile, with some fixes and modifications.

Change 47188 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Forgot to add in the round in factor with the max term.

Change 47186 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 47182 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Fixed a typo with the generation of the new center, slope_x and slope_y values.

Change 47180 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Replaced with verilog.

Change 47153 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Fixed a few minor bugs.

Change 47079 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Added another pipeline stage since z check takes an extra cycle (from 2 to 3), added
tile_failed flag, and corrected some misconceptions I had of the logic.

Change 47077 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 47076 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Replaced by verilog.

Change 47057 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Fixed coarse_fifo size mismatch (should have been 190, but was 180).

Change 47043 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Multiple fixes, all or most related to hiz.

Change 47042 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Renamed c_probe_cmask signal to color block to c_probe_coarse_mask.

Change 47030 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Fixed depthrange decompression and compression.

Change 47028 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Initial version (replaced module compiler versions).

Change 47018 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Some additional inputs, signal size corrections (covered now 16 bits), quad cache connected, and some signal renaming.

Change 46984 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Fixed module name to match file name.

Change 46977 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Overwriting Jay's temporary fix. The real fix belongs in rb_rbt_tc_fifo, which wasn't repositioning the next_head pointer properly upon fifo empty. Also some other fixes/changes (quad cache I/O, hiz I/O, etc.).

Change 46975 on 2002/08/20 by paulv@paulv_r400_linux_marlboro

Fixed next_head pointer when fifo gets empty.

Change 46952 on 2002/08/20 by wlawless@wlawless_r400_linux_marlboro

renamed this with rb_

Change 46951 on 2002/08/20 by wlawless@wlawless_r400_linux_marlboro

renames ati_fifo_cam with rb in front

Change 46896 on 2002/08/19 by paulv@paulv_r400_linux_marlboro

These files have been converted into verilog (due to the increased amount of muxing needed).

Change 46773 on 2002/08/19 by johnchen@johnchen_r400_linux_marlboro

fix latch

Change 46752 on 2002/08/19 by jayw@jayw_r400_linux_marlboro_rbrc

fixed several bugs for the milestone_tri tests under the rbrc testbench

Change 46738 on 2002/08/19 by paulv@paulv_r400_linux_marlboro

Fixed testbench to match newest hw code.

Change 46699 on 2002/08/19 by johnchen@johnchen_r400_linux_marlboro

gate off some cache signals to get better timing

Change 46679 on 2002/08/17 by jayw@jayw_r400_linux_marlboro_rbrc

Fixed a bug for milestone tests under rbrc test bench.
       This bug can cause RB hangs. and whole missing tiles.

Change 46292 on 2002/08/15 by paulv@paulv_r400_linux_marlboro

Due to timing problems in the format block of the alpha blender, needed to add another pipe stage.

Change 46291 on 2002/08/15 by wlawless@wlawless_r400_linux_marlboro

changed toggle for c_blend for paul's timing fix

Change 46080 on 2002/08/14 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 46079 on 2002/08/14 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 45871 on 2002/08/13 by johnchen@johnchen_r400_linux_marlboro

```
fix 16bit depth memory loading issue

Change 45598 on 2002/08/13 by johnchen@johnchen_r400_linux_marlboro

fixed some addressing problems for 16 bits depth

Change 45502 on 2002/08/12 by paulv@paulv_r400_linux_marlboro

Reverted subset bit selection back to what it was (which was correct).

Change 45385 on 2002/08/12 by paulv@paulv_r400_linux_marlboro

Fixed queue subset bit determination from the address (was bit 6, now bit 1, which is
bit 6 of a 32-bit address).

Change 45221 on 2002/08/09 by wlawless@wlawless_r400_linux_marlboro

tied off depth

Change 45154 on 2002/08/09 by paulv@paulv_r400_linux_marlboro

Some name changing, signal adding, and leda warning/error removing.

Change 45069 on 2002/08/08 by paulv@paulv_r400_linux_marlboro

Added delay directive.

Change 44686 on 2002/08/07 by paulv@paulv_r400_linux_marlboro

Added reset flip flops for pixel valid signal.

Change 44683 on 2002/08/07 by wlawless@wlawless_r400_linux_marlboro

reset the tile done sig

Change 44625 on 2002/08/07 by wlawless@wlawless_r400_linux_marlboro

flopped thetile done

Change 44599 on 2002/08/07 by johnchen@johnchen_r400_linux_marlboro

fix some depth hangs

Change 44231 on 2002/08/05 by wlawless@wlawless_r400_linux_marlboro

added a default for synthesis

Change 44227 on 2002/08/05 by johnchen@johnchen_r400_linux_marlboro
```

fix some latch issues and correct the RBM_RBD_tag decode

Change 43787 on 2002/08/01 by johnchen@johnchen_r400_linux_marlboro

remove inferred latches

Change 43740 on 2002/08/01 by wlawless@wlawless_r400_linux_marlboro

added defaults to case statement to cover no latches....

Change 43671 on 2002/08/01 by paulv@paulv_r400_linux_marlboro

Fixed event and color_expand signal path to RBC.

Change 43670 on 2002/08/01 by paulv@paulv_r400_linux_marlboro

Fixed address generation (to MC) for both reads and writes.

Change 43441 on 2002/07/31 by paulv@paulv_r400_linux_marlboro

Connected the color_expand and flush_event signal from rbt to rbc.

Change 43437 on 2002/07/31 by johnchen@johnchen_r400_linux_marlboro

correct cache controller for last_quad and tile_id

Change 43305 on 2002/07/31 by jayw@jayw_r400_linux_marlboro

implied latch fix for vic's 5 vector triangle.

Change 43256 on 2002/07/30 by johnchen@johnchen_r400_linux_marlboro

add last_quad and tile_id signals to depth

Change 43196 on 2002/07/30 by wlawless@wlawless_r400_linux_marlboro

Added fulsh event

Change 43193 on 2002/07/30 by wlawless@wlawless_r400_linux_marlboro

color flush event

Change 43180 on 2002/07/30 by paulv@paulv_r400_linux_marlboro

Connected tile_cache_cline (tile_id) to depth block.

Change 42975 on 2002/07/29 by jayw@jayw_r400_linux_marlboro

fixed the byte enables

Change 42944 on 2002/07/29 by jayw@jayw_r400_linux_marlboro

fixed virage rams with correct pin order and added soft reset

Change 42935 on 2002/07/29 by jayw@jayw_r400_linux_marlboro

fixed undriven soft reset and hier split

Change 42932 on 2002/07/29 by johnchen@johnchen_r400_linux_marlboro

fix the connections to the rams

Change 42927 on 2002/07/29 by jayw@jayw_r400_linux_marlboro

removed extra definition of rbc_rbt_tile_id

Change 42922 on 2002/07/29 by johnchen@johnchen_r400_linux_marlboro

fixes for bus width mismatches

Change 42920 on 2002/07/29 by jayw@jayw_r400_linux_marlboro

Fixed bad virage invokation.

Change 42815 on 2002/07/27 by paulv@paulv_r400_linux_marlboro

Fixed the tag size going from the RBD to the RBM (was 7, but only needed 6 bits).

Change 42814 on 2002/07/27 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 42813 on 2002/07/27 by paulv@paulv_r400_linux_marlboro

Added 2 more tile module compiler files.

Change 42812 on 2002/07/27 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 42811 on 2002/07/27 by paulv@paulv_r400_linux_marlboro

Fixed a few errors/warnings found by leda.

Change 42756 on 2002/07/26 by paulv@paulv_r400_linux_marlboro

```
Fixed a few signals/signal sizes.

Change 42700 on 2002/07/26 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 42699 on 2002/07/26 by paulv@paulv_r400_linux_marlboro

Added memory macro for cache.

Change 42698 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

moved to subdirectory virage

Change 42696 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

insert 'rb standard' 96x96 ram for branching to virage...

Change 42685 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

move them all to subdir virage

Change 42682 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

depth cache ram

Change 42673 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

depth cache rams

Change 42671 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

byte enable rams for color cache

Change 42670 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

attempting to put real virage rams as sub-sub module.

Change 42669 on 2002/07/26 by jayw@jayw_r400_linux_marlboro

adding 'real' rams as sub-sub-module

Change 42622 on 2002/07/26 by paulv@paulv_r400_linux_marlboro

Fixed unattached signal (tile_cache_state) and renamed all rb_tile_fifo input signals
to tile_cache_* (from RC_RB_*).
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Change 42606 on 2002/07/26 by paulv@paulv_r400_linux_marlboro

Fixed a bug when generating the invalid_fifo_data signal (used to denote when an invalid event (non-flush) comes into the tile cache from the RC).

Change 42587 on 2002/07/26 by wlawless@wlawless_r400_linux_marlboro

bus width miss match

Change 42560 on 2002/07/25 by paulv@paulv_r400_linux_marlboro

Intial version.

Change 42559 on 2002/07/25 by paulv@paulv_r400_linux_marlboro

Changed heir to hier (the proper spelling).

Change 42558 on 2002/07/25 by paulv@paulv_r400_linux_marlboro

Added event and state to output of tile cache. Made tile cache RAM 65x128 since virage will not produce a 64x128 RAM with subwords and fixed the tile_cache_cline output signal to be 8 bits instead of 4. Memory macro not instantiated yet (code commented out).

Change 42557 on 2002/07/25 by paulv@paulv_r400_linux_marlboro

Added tile cache to tile logic.

Change 42548 on 2002/07/25 by jayw@jayw_r400_linux_marlboro

replace with sw=1

Change 42544 on 2002/07/25 by jayw@jayw_r400_linux_marlboro

with Andi's help

Change 42543 on 2002/07/25 by jayw@jayw_r400_linux_marlboro

added busy and clean

Change 42542 on 2002/07/25 by jayw@jayw_r400_linux_marlboro

hier rename and busy

Change 42541 on 2002/07/25 by jayw@jayw_r400_linux_marlboro

heir rename and busy

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Change 42475 on 2002/07/25 by wlawless@wlawless_r400_linux_marlboro

added the tile done through everything

Change 42466 on 2002/07/25 by paulv@paulv_r400_linux_marlboro

Added tile_id_<i,o> pass-through signal.

Change 42427 on 2002/07/25 by paulv@paulv_r400_linux_marlboro

Added last_quad_<i,o> pass-through signal.  Fixed cam lookup logic for when
color_expand is on (renamed fast_clear to color_expand, its proper name).

Change 42378 on 2002/07/25 by wlawless@wlawless_r400_linux_marlboro

another change for synthesis

Change 42358 on 2002/07/25 by wlawless@wlawless_r400_linux_marlboro

just broke up some code for synthesis

Change 42325 on 2002/07/25 by paulv@paulv_r400_linux_marlboro

Fixed state_gfx_we/state_we signals.

Change 42319 on 2002/07/25 by wlawless@wlawless_r400_linux_marlboro

bus width typo

Change 42284 on 2002/07/24 by paulv@paulv_r400_linux_marlboro

Updated state_decode logic for register reads.

Change 42282 on 2002/07/24 by jayw@jayw_r400_linux_marlboro

missing file stolen from wlawless's directory.
       for rbbm reg reads.

Change 42218 on 2002/07/24 by wlawless@wlawless_r400_linux_marlboro

All rbbm read stuff,

Change 42199 on 2002/07/24 by paulv@paulv_r400_linux_marlboro

Optimized clrcmp_control register decode and added strobe bits to all state_storage
instantiations.

Change 42175 on 2002/07/24 by wlawless@wlawless_r400_linux_marlboro
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added the read path

Change 42157 on 2002/07/24 by jayw@jayw_r400_linux_marlboro

Typo on reset initialization for Rob

Change 42151 on 2002/07/24 by wlawless@wlawless_r400_linux_marlboro

fixed the blend cam outputs, there were not connected

Change 42148 on 2002/07/24 by wlawless@wlawless_r400_linux_marlboro

fixed typo for non-blocking

Change 42126 on 2002/07/24 by jayw@jayw_r400_linux_marlboro

for real register files.

Change 42020 on 2002/07/23 by paulv@paulv_r400_linux_marlboro

Added register read logic.

Change 42008 on 2002/07/23 by wlawless@wlawless_r400_linux_marlboro

put in the rbbm_int... tied off for now

Change 41996 on 2002/07/23 by wlawless@wlawless_r400_linux_marlboro

a bunch of fixes got lost..... don't know

Change 41916 on 2002/07/23 by wlawless@wlawless_r400_linux_marlboro

added 'include 's

Change 41904 on 2002/07/23 by wlawless@wlawless_r400_linux_marlboro

remove tire sm_zero

Change 41878 on 2002/07/22 by paulv@paulv_r400_linux_marlboro

Added quad_cache_stall signal, removed rtr to quad_cache (for tiledata) and now if other_tiledata_fifo (depthrange, smask and zmask) fills up, stall tile cache (don't read tile cache for data from tc fifo).

Change 41855 on 2002/07/22 by paulv@paulv_r400_linux_marlboro

Added cacheline (with offset) and valid signal (for quad cache).

```
Change 41834 on 2002/07/22 by paulv@paulv_r400_linux_marlboro

Fixed some signals and corresponding logic.  Mostly, signals labeled with "RBD_RBT" and
vice versa were changed to quad_cache.

Change 41806 on 2002/07/22 by jayw@jayw_r400_linux_marlboro

reset q_rbt_rbd_dec_mask

Change 41768 on 2002/07/22 by wlawless@wlawless_r400_linux_marlboro

set to no background

Change 41746 on 2002/07/22 by wlawless@wlawless_r400_linux_marlboro

jayw releasing attempted fix for 2nd triangle
       appears to run 1st okay, not tested yet on 2nd.

Change 41645 on 2002/07/19 by paulv@paulv_r400_linux_marlboro

Fixed bugs found with *simple* test bench, added rbc cmask reads to tile cache and
added some fast_color_clear functionality.

Change 41644 on 2002/07/19 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 41513 on 2002/07/19 by wlawless@wlawless_r400_linux_marlboro

more color expand fix,

Change 41454 on 2002/07/19 by paulv@paulv_r400_linux_marlboro

Pre-fast_color_clear functionality checkin.  All bugs found with *simple* testbench
fixed.

Change 41421 on 2002/07/18 by johnchen@johnchen_r400_linux_marlboro

code for 16 bits expended depth

Change 41334 on 2002/07/18 by wlawless@wlawless_r400_linux_marlboro

adding files.f for leda

Change 41271 on 2002/07/18 by paulv@paulv_r400_linux_marlboro

Updated code to reflect the RBT spec written by Jay.  NOTE:  the bvrl file has the
```

```
delay removed from the flop (for easier debugging).

Change 41211 on 2002/07/18 by wlawless@wlawless_r400_linux_marlboro

Connected the rb_color busy to the output busy0,
unconnected the color expand bit

Change 41204 on 2002/07/18 by wlawless@wlawless_r400_linux_marlboro

got the color expand working, the background reg need to be written

Change 40831 on 2002/07/16 by wlawless@wlawless_r400_linux_marlboro

Yet another state block, custom for the sx block

Change 40830 on 2002/07/16 by wlawless@wlawless_r400_linux_marlboro

Added the logic to hold the pipe if the same quad is in the
blend pipe or the fifo to the blend pipe.... CAM lookup..

Change 40664 on 2002/07/15 by paulv@paulv_r400_linux_marlboro

Connected word signal (denotes upper or lower 128 bits of 256-bit data transfer) from
MC->RBM->RBT.

Change 40645 on 2002/07/15 by paulv@paulv_r400_linux_marlboro

Added rb_rbt_tc_addr_calc.mc and .bvrl link.

Change 40642 on 2002/07/15 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 40627 on 2002/07/15 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 40626 on 2002/07/15 by paulv@paulv_r400_linux_marlboro

Added blend cam lookup logic and fast_color_clear pass-thru signal.

Change 40170 on 2002/07/12 by paulv@paulv_r400_linux_marlboro

Fixed some bugs found with early test bench and leda.

Change 40167 on 2002/07/12 by paulv@paulv_r400_linux_marlboro

Added cacheline valid bit to determine a cacheline hit.
```

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Change 39920 on 2002/07/12 by johnchen@johnchen_r400_sun_marlboro

initial submit for rb depth logic

Change 39744 on 2002/07/11 by wlawless@wlawless_r400_linux_marlboro

added the state for Blend Enable into the rb_probe block....!!!

Change 39465 on 2002/07/10 by paulv@paulv_r400_linux_marlboro

Fixed subnorm calculation.

Change 39455 on 2002/07/10 by paulv@paulv_r400_linux_marlboro

Fixed clamping of negative unsigned number formats (e.g., -300 for a urf number is
illegal).  All negative numbers representing unsigned number formats are clamped to 0.

Change 39445 on 2002/07/10 by wlawless@wlawless_r400_linux_marlboro

fixed the byte enables to work with/out doing a memory read

Change 39384 on 2002/07/10 by paulv@paulv_r400_linux_marlboro

Added pixel_valid bit (pipelined through blender).

Change 39161 on 2002/07/09 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 38343 on 2002/07/05 by subad@subad_r400_linux_marlboro

added //make_syn comments to use deps.pl script to generate tcd.syn file.
       Changed some instance names to match standards.
       Regenerated tcd.syn using deps.pl script

Change 37884 on 2002/07/03 by paulv@paulv_r400_linux_marlboro

Removed RBT_RBM_bytevalid signal.  Also shrunk RBT_RBM_tag to 5 bits (from 7 bits).

Change 37876 on 2002/07/03 by wlawless@wlawless_r400_linux_marlboro

in RC fixed a warning, wire declaired twice
moved the RBBM out of probe and put it into color.v
in probe instanciated the state module, no logical changes

Change 37817 on 2002/07/03 by wlawless@wlawless_r400_linux_marlboro
```

```
fixed the toggle for blend read
   also added a gate of 0's if blend is off, blender needs 0's

Change 37626 on 2002/07/02 by wlawless@wlawless_r400_linux_marlboro

better fix for previous bug, read and write be in back-to-back cycles
changed the early_cache_line back to 12 from 11...

Change 37579 on 2002/07/02 by jayw@jayw_r400_linux_marlboro

1st triangle

Change 37578 on 2002/07/02 by jayw@jayw_r400_linux_marlboro

1st triangle.

Change 37492 on 2002/07/01 by wlawless@wlawless_r400_linux_marlboro

fixed toggle for writing BE's, also fixed SX typo..., Runs 1st triangle

Change 37404 on 2002/07/01 by paulv@paulv_r400_linux_marlboro

Added testing for samples 2,3 and 4 (6 and 8 should behave like 3 and 4, respectively).

Change 37402 on 2002/07/01 by paulv@paulv_r400_linux_marlboro

Fixed problem with >=2 samples.

Change 37208 on 2002/06/28 by paulv@paulv_r400_linux_marlboro

Added Jay's fixes to the 2d byte address.

Change 37192 on 2002/06/28 by paulv@paulv_r400_linux_marlboro

Initial version.  Just for 1 sample/pixel.

Change 37190 on 2002/06/28 by paulv@paulv_r400_linux_marlboro

Fixed some bugs found with test bench.

Change 37052 on 2002/06/28 by wlawless@wlawless_r400_linux_marlboro

fixed typo in previous fix

Change 37034 on 2002/06/28 by wlawless@wlawless_r400_linux_marlboro

Changed the probe increment to match each rb ID..
```

Change 36869 on 2002/06/27 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 36848 on 2002/06/27 by paulv@paulv_r400_linux_marlboro

Mistake in spec. rb_mc_access_requestqueue needs to be specified for both reads AND writes.

Change 36813 on 2002/06/27 by paulv@paulv_r400_linux_marlboro

Fixed validrequest to mc for a write request.

Change 36775 on 2002/06/27 by wlawless@wlawless_r400_linux_marlboro

toggle alignment

Change 36470 on 2002/06/26 by wlawless@wlawless_r400_linux_marlboro

added pixel y0

Change 36456 on 2002/06/26 by paulv@paulv_r400_linux_marlboro

Added output valid bit (pixel_y0) for color cache.

Change 36405 on 2002/06/26 by paulv@paulv_r400_linux_marlboro

Fixed subnorm logic.

Change 36363 on 2002/06/26 by wlawless@wlawless_r400_linux_marlboro

fixed typo

Change 36361 on 2002/06/26 by wlawless@wlawless_r400_linux_marlboro

ram data backwards, pixel mask bits needed a side register

Change 36279 on 2002/06/25 by paulv@paulv_r400_linux_marlboro

Fixed a bug where the mantissa's binary point of the src & dst channels did not line up with the mantissa's binary point of the multiplication results.

Change 36146 on 2002/06/25 by paulv@paulv_r400_linux_marlboro

Added detail mask logic, cleaned up state decode module instantiations and fixed some leda warnings/errors.

Change 36136 on 2002/06/25 by paulv@paulv_r400_linux_marlboro

Added color_sel_o, renamed all state info (e.g., we, addr, etc) signals to be similar to other blocks (for instance, state_we was rbbm_rb_we in my blender code) and fixed decoding of rop3 registers (correct register was colorcontrol, not 2d_format_rop3, which is a shadow register--but need to also handle writing to it).

Change 36105 on 2002/06/25 by wlawless@wlawless_r400_linux_marlboro

some timing alignment between state and reading the cache data

Change 35840 on 2002/06/24 by wlawless@wlawless_r400_linux_marlboro

fixed address coversion to 31:5

Change 35748 on 2002/06/24 by paulv@paulv_r400_linux_marlboro

Fixed rts to quad_ram interface when sx fifo pointer was wrong (e.g., ptr points to sx1 fifo, but data in sx0 fifo). Also fixed state decode index signals (was using input from RBT; should have been flopped version).

Change 35666 on 2002/06/21 by paulv@paulv_r400_linux_marlboro

Fixed all bugs found with personal test bench and june 15th 1st triangle test bench.

Change 35538 on 2002/06/21 by wlawless@wlawless_r400_linux_marlboro

fixed xoe in the rc

Change 35531 on 2002/06/21 by paulv@paulv_r400_linux_marlboro

Last fix was bogus. This is the real fixed version.

Change 35530 on 2002/06/21 by paulv@paulv_r400_linux_marlboro

no longer needed

Change 35519 on 2002/06/21 by paulv@paulv_r400_linux_marlboro

Fixed 3d macro offset calculation and 2d subset offset calculation.

Change 35481 on 2002/06/21 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 35479 on 2002/06/21 by wlawless@wlawless_r400_linux_marlboro

autoflush delay write

```
Change 35468 on 2002/06/21 by wlawless@wlawless_r400_linux_marlboro

rbbm decode had a bug

Change 35373 on 2002/06/20 by paulv@paulv_r400_linux_marlboro

Alpha blender submodule is now only 4 cycles long.

Change 35309 on 2002/06/20 by paulv@paulv_r400_linux_marlboro

Added rop3 logic.  Also shrunk pipeline to 14 cycles (was 15).

Change 35307 on 2002/06/20 by fhsien@fhsien_r400_linux_marlboro

Updating names

Change 35298 on 2002/06/20 by paulv@paulv_r400_linux_marlboro

Was 5 cycles long.  Now is 4.

Change 35210 on 2002/06/20 by jayw@MA_JAYW

fixed misspelled context done busy to RC

Change 35138 on 2002/06/20 by wlawless@wlawless_r400_linux_marlboro

don't remember

Change 35024 on 2002/06/19 by wlawless@wlawless_r400_linux_marlboro

state decode for GFX state 0 was wrong,

Change 34919 on 2002/06/19 by paulv@paulv_r400_linux_marlboro

Removed RB_MC_access_subset signal (for rbm).

Change 34916 on 2002/06/19 by jayw@MA_JAYW

really removed subset to MC

Change 34762 on 2002/06/18 by wlawless@wlawless_r400_linux_marlboro

fixed rb_color states_bits to state_index
some clock name problems

Change 34755 on 2002/06/18 by wlawless@wlawless_r400_linux_marlboro

fixed clock
```

Change 34744 on 2002/06/18 by paulv@paulv_r400_linux_marlboro

Changed state decode logic to use many less registers (but some additional muxing).

Change 34649 on 2002/06/18 by paulv@paulv_r400_linux_marlboro

Fixed the output of a few color formats (color_8_8, color_16_16, etc.).

Change 34538 on 2002/06/17 by paulv@paulv_r400_linux_marlboro

Fixed all plausible errors and warnings produced by leda.

Change 34525 on 2002/06/17 by paulv@paulv_r400_linux_marlboro

Fixed pixels used for chromakeying (was using incorrect bits in the AND phase).

Change 34507 on 2002/06/17 by paulv@paulv_r400_linux_marlboro

Added chroma keying logic.

Change 34187 on 2002/06/14 by wlawless@wlawless_r400_linux_marlboro

added a separate state block, looks much nicer...
also, a steve allen edit of the tree file

Change 33891 on 2002/06/13 by paulv@paulv_r400_linux_marlboro

Test bench files for rb_rbd_quad_address_calc.v.

Change 33890 on 2002/06/13 by paulv@paulv_r400_linux_marlboro

Fixed all bugs related to June 15th operationality, including any x's, z's and some
control signals/logic.

Change 33887 on 2002/06/13 by paulv@paulv_r400_linux_marlboro

For some reason, the source code still had 3 registers instead of the promised 2.

Change 33874 on 2002/06/13 by wlawless@wlawless_r400_linux_marlboro

clk stuff

Change 33801 on 2002/06/13 by rbell@rbell_crayola_sun_cvd

Fixes/hacks to get the first chip integration compile to work.

Change 33731 on 2002/06/13 by wlawless@wlawless_r400_linux_marlboro

```
fixed up state stuff

Change 33728 on 2002/06/13 by paulv@paulv_r400_linux_marlboro

Fixed graphics copy macro (from GFX_COPY_STATE to GFX_GFX_COPY_STATE).

Change 33656 on 2002/06/12 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 33655 on 2002/06/12 by paulv@paulv_r400_linux_marlboro

June 15th functionality (color cache only) working.  Some other minor issues resolved
(page changing, for one).

Change 33573 on 2002/06/12 by paulv@paulv_r400_linux_marlboro

Fixed all valid errors/warnings found with leda.

Change 33500 on 2002/06/12 by wlawless@wlawless_r400_linux_marlboro

added fifo busy to rb_color_busy

Change 33499 on 2002/06/12 by wlawless@wlawless_r400_linux_marlboro

Added rb_color_busy

Change 33444 on 2002/06/12 by wlawless@wlawless_r400_linux_marlboro

       added to disable autofluch when delay = 0

Change 33432 on 2002/06/12 by wlawless@wlawless_r400_linux_marlboro

changed addr to 27 bit

Change 33426 on 2002/06/12 by paulv@paulv_r400_linux_marlboro

Made RBC_RBM_color_address two separate (read and write) addresses.

Change 33412 on 2002/06/12 by wlawless@wlawless_r400_linux_marlboro

added color cache write request bus

Change 33308 on 2002/06/11 by wlawless@wlawless_r400_sun_marlboro

rb update prior to simulation
```

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Change 33249 on 2002/06/11 by paulv@paulv_r400_linux_marlboro

Fixed some bugs found with test bench.

Change 33247 on 2002/06/11 by wlawless@wlawless_r400_linux_marlboro

clean up from leda

Change 33149 on 2002/06/11 by wlawless@wlawless_r400_linux_marlboro

cleaned up signal names for compile

Change 33141 on 2002/06/11 by wlawless@wlawless_r400_linux_marlboro

added clk gating stuff

Change 33038 on 2002/06/10 by wlawless@wlawless_r400_linux_marlboro

new rb_clock file

Change 33020 on 2002/06/10 by paulv@paulv_r400_linux_marlboro

Fixed all errors, signal mismatches, etc. and added RBBM state decode logic.

Change 33014 on 2002/06/10 by paulv@paulv_r400_linux_marlboro

Added header.

Change 33013 on 2002/06/10 by johnchen@johnchen_r400_sun_marlboro

initial rb_depth for compiling

Change 32919 on 2002/06/10 by wlawless@wlawless_r400_linux_marlboro

added wire statement for signals

Change 32893 on 2002/06/10 by wlawless@wlawless_r400_linux_marlboro

renamed

Change 32892 on 2002/06/10 by wlawless@wlawless

made rb_

Change 32888 on 2002/06/10 by wlawless@wlawless_r400_linux_marlboro

don't know
```

Change 32828 on 2002/06/07 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 32720 on 2002/06/07 by paulv@paulv_r400_linux_marlboro

Removed valid signals from fifos (not needed--empty and full bits generated by fifo
will denote if there are any valid requests) and fixed some bit selections.

Change 32694 on 2002/06/07 by paulv@paulv_r400_linux_marlboro

Added rbm interface.

Change 32664 on 2002/06/07 by wlawless@wlawless_r400_linux_marlboro

don't remember

Change 32645 on 2002/06/07 by wlawless@wlawless_r400_linux_marlboro

fixed signal name typo

Change 32634 on 2002/06/07 by wlawless@wlawless_r400_linux_marlboro

renamed depth

Change 32632 on 2002/06/07 by wlawless@wlawless_r400_linux_marlboro

removed toggle from blend

Change 32631 on 2002/06/07 by paulv@paulv_r400_linux_marlboro

Fixed pixel bits needed for dither (x bits come in as 3-bit vector and a 0 or 1 is
concatenated at the end depending on the pixel). Y pixel bits ok.

Change 32624 on 2002/06/07 by wlawless@wlawless_r400_linux_marlboro

fixed up signal to get rid of all warning, fixed quad XY size for dither

Change 32549 on 2002/06/07 by paulv@paulv_r400_linux_marlboro

Fixed color_array and color_slice definitions for color1-3.

Change 32544 on 2002/06/07 by wlawless@wlawless_r400_linux_marlboro

initial add

Change 32516 on 2002/06/06 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 32508 on 2002/06/06 by paulv@paulv_r400_linux_marlboro

Forgot to declare the rtr (stall) signal.

Change 32506 on 2002/06/06 by paulv@paulv_r400_linux_marlboro

Previous checkin went bust somehow. This is the proper version of the code.

Change 32502 on 2002/06/06 by paulv@paulv_r400_linux_marlboro

Optimized the code to complete in 2 cycles (and shrink the area by 1/4 or so), added a delay signal and fixed a few bugs.

Change 32323 on 2002/06/06 by wlawless@wlawless_r400_linux_marlboro

added 4 bits of x & y for dither

Change 32291 on 2002/06/06 by paulv@paulv_r400_linux_marlboro

Fixed some of the vector sizes.

Change 32182 on 2002/06/05 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 32181 on 2002/06/05 by paulv@paulv_r400_linux_marlboro

Fixed rb_mc_address_calc instantiation.

Change 32178 on 2002/06/05 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 32043 on 2002/06/05 by wlawless@wlawless_r400_linux_marlboro

changed name to rb_tile.v

Change 32042 on 2002/06/05 by wlawless@wlawless

changed name to rb_tile.v

Change 31851 on 2002/06/04 by paulv@paulv_r400_linux_marlboro

Fixed a few things, including removing subset signals from clients, added MC_RB_addrmapcols (for page size determination) and a few other minor problems.

Change 31800 on 2002/06/04 by wlawless@wlawless_r400_linux_marlboro

Cleaned up some stuff for simulation

Change 31749 on 2002/06/04 by paulv@paulv_r400_linux_marlboro

All code necessary for June 15th is in but needs to be tested.

Change 31571 on 2002/06/03 by paulv@paulv_r400_linux_marlboro

Fixed swap. It has been moved before the pixels are formatted and allowed bypassed pixels (the 32-bits/component variety) to be swappable.

Change 31498 on 2002/06/03 by paulv@paulv_r400_linux_marlboro

Defined copy signal for state decoders.

Change 31497 on 2002/06/03 by paulv@paulv_r400_linux_marlboro

Removed component_mask signal.

Change 31496 on 2002/06/03 by paulv@paulv_r400_linux_marlboro

Changed FMT defines to COLOR and am now using NUMBER defines.

Change 31171 on 2002/05/31 by wlawless@wlawless_r400_linux_marlboro

Change a lot of state storage stuff

Change 31149 on 2002/05/31 by wlawless@wlawless

moved to common

Change 31147 on 2002/05/31 by wlawless@wlawless

moved to common

Change 31145 on 2002/05/31 by wlawless@wlawless

nothing

Change 31102 on 2002/05/31 by wlawless@wlawless_r400_linux_marlboro

commented out the RBM for now

Change 31101 on 2002/05/31 by wlawless@wlawless

get rid of this

Change 31036 on 2002/05/31 by wlawless@wlawless_r400_linux_marlboro

add a mux and nomux version

Change 31009 on 2002/05/31 by wlawless@wlawless_r400_linux_marlboro

put copy back in

Change 30913 on 2002/05/30 by wlawless@wlawless_r400_linux_marlboro

fixed the rnm name

Change 30911 on 2002/05/30 by paulv@paulv_r400_linux_marlboro

THe file has been moved to its correct folder (mc_interface). It can now be safely deleted (unlike before).

Change 30910 on 2002/05/30 by paulv@paulv_r400_linux_marlboro

Initial version (not complete).

Change 30902 on 2002/05/30 by pmitchel@pmitchel_entire_depot_win

recovering deleted file

Change 30900 on 2002/05/30 by paulv@paulv_r400_linux_marlboro

This file does not belong here.

Change 30899 on 2002/05/30 by fhsien@fhsien_r400_unix_marlboro

TkP4 - RENAME

Change 30897 on 2002/05/30 by wlawless@wlawless_r400_linux_marlboro

new, much simpler state storage.......
       also made with flops not latches

Change 30896 on 2002/05/30 by paulv@paulv_r400_linux_marlboro

Initial version.

Change 30594 on 2002/05/29 by paulv@paulv_r400_linux_marlboro

Removed data valid signals and added cacheline_early_o (the second to last pipeline stage of the cacheline signal).

Change 30582 on 2002/05/29 by wlawless@wlawless_r400_linux_marlboro

added the write to the cache path

Change 30528 on 2002/05/29 by paulv@paulv_r400_linux_marlboro

Added stall signal (only used for TC--set high for RB).

Change 30267 on 2002/05/28 by paulv@paulv_r400_linux_marlboro

Fixed color<x>_info state decode and used defines for register bit selections.

Change 29664 on 2002/05/23 by wlawless@wlawless_r400_linux_marlboro

Added the quad offset into everything

Change 29601 on 2002/05/22 by paulv@paulv_r400_sun_marlboro

Updated test bench to match latest changes to alpha blender.

Change 29528 on 2002/05/22 by wlawless@wlawless_r400_linux_marlboro

finished connecting up blend

Change 29327 on 2002/05/21 by paulv@paulv_r400_sun_marlboro

Fixed data bypass path for 128-bit pixels.

Change 29175 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Changed the ati_state_storage instantiations to state_storage_reg instantiations.

Change 29174 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Fixed a few color formatting bugs (e.g., blue in red channel, red in blue channel,
exponents incorrect).

Change 29173 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Some signals were not connected correctly. This has been resolved.

Change 29169 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Fixed negate logic (was incomplete, thus creating latches).

Change 29129 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Fixed pixel bits used for dithering. The second pixel in the 1/2 quad needed to have

'1' added to the x bits.

Change 29098 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Fixed a few things (src_color is a 256-bit vector, there are 4 bits of pixel coordinate to do dithering, etc.) and added a valid signal.

Change 29097 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Updated dither code and round in factor (now 8 bits).

Change 29096 on 2002/05/20 by paulv@paulv_r400_sun_marlboro

Updated dither code and made round factor 8 bits.

Change 29080 on 2002/05/20 by wlawless@wlawless_r400_linux_marlboro

fixed name

Change 28783 on 2002/05/17 by paulv@paulv_r400_sun_marlboro

Fixed some formatting bugs found with testbench.

Change 28781 on 2002/05/17 by paulv@paulv_r400_sun_marlboro

Updated test bench to mimic latest changes in source code.

Change 28658 on 2002/05/17 by paulv@paulv_r400_sun_marlboro

Renamed byte_offset to quad_offset and changed cacheline signal from 6 to 7 bits.

Change 28657 on 2002/05/17 by paulv@paulv_r400_sun_marlboro

Added blender shell.

Change 28653 on 2002/05/17 by paulv@paulv_r400_sun_marlboro

Initial version.

Change 28504 on 2002/05/16 by paulv@paulv_r400_sun_marlboro

Updated with latest register values, corrected some signals and added some other features.

Change 28420 on 2002/05/16 by wlawless@wlawless_r400_linux_marlboro

Checked in for Paul to edit rb_color.v

```
Change 28353 on 2002/05/16 by wlawless@wlawless_r400_linux_marlboro

Added a state machine for cache blend read...

Change 28285 on 2002/05/15 by paulv@paulv_r400_sun_marlboro

Updated with latest (correct) color formats and numbers.  Also implemented dithering
(truncate, round or dither).

Change 28105 on 2002/05/15 by jayw@MA_JAYW

Remove RB_MC_access_subset.
RB_MC_access_address is[31:5], a device address.

Change 28099 on 2002/05/15 by paulv@paulv_r400_sun_marlboro

Updated degamma table (now with more x's!!).

Change 27960 on 2002/05/14 by wlawless@wlawless_r400_linux_marlboro

cleaned up signal names... WFL

Change 27852 on 2002/05/14 by wlawless@wlawless_r400_linux_marlboro

Added the blend cache read signals

Change 27735 on 2002/05/13 by jayw@MA_JAYW

added cp_rb_pm_enb and fixed new rb->sx interface syntax.

Change 27705 on 2002/05/13 by jayw@MA_JAYW

updated color and index interface to SX

Change 27615 on 2002/05/13 by wlawless@wlawless_r400_linux_marlboro

fixed name

Change 27614 on 2002/05/13 by wlawless@wlawless_r400_sun_marlboro

Fixed naming to rb_ for everything

Change 27346 on 2002/05/10 by wlawless@wlawless_r400_sun_marlboro

renamed rb_

Change 27344 on 2002/05/10 by wlawless@wlawless_r400_sun_marlboro
```

```
rename rb_

Change 27340 on 2002/05/10 by wlawless@wlawless_r400_sun_marlboro

renamed rb_

Change 27338 on 2002/05/10 by wlawless@wlawless_r400_sun_marlboro

changed names to rb_

Change 27337 on 2002/05/10 by wlawless@wlawless_r400_sun_marlboro

changed name to rb_

Change 27225 on 2002/05/09 by paulv@paulv_r400_sun_marlboro

Mantissa table now 1 bit bigger (slope now 7 bits).  Other changes necessary to get
degamma accurate for 32-bit pixels (e.g., slightly bigger final mult, etc.).

Change 27212 on 2002/05/09 by wlawless@wlawless_r400_sun_marlboro

modified Increment in_flight count... fun fun
       new block to make it complie correctly rb_c_cache.v

Change 27191 on 2002/05/09 by paulv@paulv_r400_sun_marlboro

Code no longer needed.

Change 27190 on 2002/05/09 by paulv@paulv_r400_sun_marlboro

Test bench files now go into src folder.

Change 27102 on 2002/05/08 by paulv@paulv_r400_sun_marlboro

All necessary logic (deformat, degamma, etc.) fixed.

Change 26929 on 2002/05/08 by wlawless@wlawless_r400_sun_marlboro

added all io ports and ram read cam lookup

Change 26407 on 2002/05/03 by paulv@paulv_r400_sun_marlboro

Updated code to reflect architectural changes and new tables.

Change 26324 on 2002/05/03 by paulv@paulv_r400_sun_marlboro

Some minor fixes and area/timing optimizations.
```

```
Change 25993 on 2002/05/02 by wlawless@wlawless_r400_sun_marlboro

On going work, added rb_sx_int.v throught the level of heir
       and ran a sim on sx requests :)

Change 25938 on 2002/05/01 by paulv@paulv_r400_sun_marlboro

Initial version.

Change 25831 on 2002/05/01 by paulv@paulv_r400_sun_marlboro

Added capability to handle subnorms.

Change 25796 on 2002/05/01 by paulv@paulv_r400_sun_marlboro

Changed the constant exponent (from 8 to 7) and the 13-bit final multiplicand.

Change 25572 on 2002/04/30 by paulv@paulv_r400_sun_marlboro

Fixed fog factor.

Change 25414 on 2002/04/29 by paulv@paulv_r400_sun_marlboro

Fixed an exponent.

Change 25343 on 2002/04/29 by wlawless@wlawless

re named this to rb_sx_int.v

Change 25341 on 2002/04/29 by wlawless@wlawless_r400_sun_marlboro

rb color to SX Block interface

Change 25338 on 2002/04/29 by paulv@paulv_r400_sun_marlboro

Constant was wrong.  Corrected.

Change 25315 on 2002/04/29 by paulv@paulv_r400_sun_marlboro

One of the constants was incorrect.  Fixed now.

Change 25182 on 2002/04/26 by paulv@paulv_r400_sun_marlboro

Degamma now fully operational (Microsoft equation fully implemented and working).

Change 24691 on 2002/04/24 by paulv@paulv_r400_sun_marlboro

These files have been moved into the color subfolder.
```

Change 24690 on 2002/04/24 by paulv@paulv_r400_sun_marlboro

Moved from top level rb directory to here.

Change 24689 on 2002/04/24 by paulv@paulv_r400_sun_marlboro

Don't need anymore.

Change 24688 on 2002/04/24 by paulv@paulv_r400_sun_marlboro

Need to check in because all alpha blender files are going into the color folder.

Change 24687 on 2002/04/24 by paulv@paulv_r400_sun_marlboro

A few modifications to improve area (slightly) and timing (somewhat).

Change 24678 on 2002/04/24 by wlawless@wlawless_r400_sun_marlboro

This is a list of some RB color verification ideas....

Change 24655 on 2002/04/23 by paulv@paulv_r400_sun_marlboro

Replaced x's with 0's (as was done by Synopsys in obtaining the gates).

Change 24582 on 2002/04/23 by wlawless@wlawless_r400_sun_marlboro

Initial add

Change 24580 on 2002/04/23 by wlawless@wlawless_r400_sun_marlboro

initial place holder

Change 24578 on 2002/04/23 by wlawless@wlawless_r400_sun_marlboro

initial place holder

Change 24573 on 2002/04/23 by wlawless@wlawless_r400_sun_marlboro

This is the initial add of the RenderBackend Color .v files

Change 24571 on 2002/04/23 by paulv@paulv_r400_sun_marlboro

New degamma files (original rb_rbc_degamma.mc split into 4 separate modules, not including wrapper rb_rbc_degamma.v).

Change 24519 on 2002/04/23 by jayw@MA_JAYW

changed tag between MC and RB to 9 bits.

Change 24404 on 2002/04/22 by paulv@paulv_r400_sun_marlboro

Degamma logic is now 3 clock cycles wide. Instead of using one file for alpha bypass for gamma and degamma, now need 2.

Change 24403 on 2002/04/22 by paulv@paulv_r400_sun_marlboro

Fixed normalize logic.

Change 24256 on 2002/04/22 by paulv@paulv_r400_sun_marlboro

Removed normalize logic at beginning of gamma code--it is done by the alpha blender on output.

Change 23592 on 2002/04/17 by paulv@paulv_r400_sun_marlboro

This is the synthesized version of rb_rbc_degamma.mc. Since the mc file contains don't cares that can not be simulated properly, this version will be used throughout test/synthesis.

Change 23454 on 2002/04/16 by paulv@paulv_r400_sun_marlboro

Initial version.

Change 23347 on 2002/04/15 by paulv@paulv_r400_sun_marlboro

Forgot to remove autopipelining and put registers at bottom.

Change 23308 on 2002/04/15 by paulv@paulv_r400_sun_marlboro

Initial version.

Change 23303 on 2002/04/15 by paulv@paulv_r400_sun_marlboro

Split mantissa LUT into 3 tables. Some of the mantissa's LUT values have don't cares ('x') (before they were hard-coded), so the logic had to change slightly (1->3 tables and a final concatenate). Because of this, Synopsys optimizes the code and produces few gates (timing seemed to improve also).

Change 22999 on 2002/04/12 by paulv@paulv_r400_sun_marlboro

Initial version.

Change 22464 on 2002/04/09 by paulv@paulv_r400_sun_marlboro

Minor update.

```
Change 22415 on 2002/04/08 by paulv@paulv_r400_sun_marlboro

Initial versions.

Change 21622 on 2002/04/03 by jayw@MA_JAYW

RBBM_a is 15 bits

Change 21429 on 2002/04/02 by paulv@paulv_r400_sun_marlboro

Minor fix (removed a mux that wasn't necessary).

Change 21377 on 2002/04/02 by jayw@MA_JAYW

added RB_MH_queuecount
and removed tile_done from RBs.

Change 21365 on 2002/04/02 by jayw@MA_JAYW

MH_RB_queuecount_external is now MH_RB_queuecount

Change 21286 on 2002/04/01 by jayw@MA_JAYW

fixed to output RB_MC_access and
the rtr and send from RB to RC for coarse,
this is not 4 pins not one.

Change 21072 on 2002/03/29 by paulv@paulv_r400_sun_marlboro

Fixed dst from 32-bit IEEE fp to 22-bit internal fp.

Change 20993 on 2002/03/28 by paulv@paulv_r400_sun_marlboro

Updated code with recent additions/fixes.

Change 20767 on 2002/03/27 by jayw@MA_JAYW

changed RC_RB0_ names to u0_RC_RB, strange but true.

Change 20766 on 2002/03/27 by jayw@MA_JAYW

changed RB0_RC to u0_RB_RC naming convention! duh!

Change 20748 on 2002/03/27 by jayw@MA_JAYW

removed SX0_RB_color_valid and SX1_RB_color_valid.
unnecessary as _send works for this.
```

```
Change 20721 on 2002/03/27 by jayw@MA_JAYW

removed bogus offset x and offset y from detail bus.
added event bit to coarse bus.

Change 20691 on 2002/03/27 by jayw@MA_JAYW

Added missing individual send/rtr between
RC and RB for the detail bus.

Change 20684 on 2002/03/27 by jayw@MA_JAYW

fixed name of switched RB_SX0_quad_rtr
fixed input of soft reset.

Change 20573 on 2002/03/26 by jayw@MA_JAYW

Several bus name changes.
Added RB->RC system context bus.

Change 20533 on 2002/03/26 by jayw@MA_JAYW

several changes.
Added RBBM interface.
Redid MC interface.
Should match latest SX interfaces.

Change 19793 on 2002/03/20 by paulv@paulv_r400_sun_marlboro

Initial version.

Change 19396 on 2002/03/18 by paulv@paulv_r400_sun_marlboro

Bugs found with test bench have been fixed.

Change 18728 on 2002/03/13 by paulv@paulv_r400_sun_marlboro

Added timescale directive.

Change 18713 on 2002/03/13 by paulv@paulv_r400_sun_marlboro

Added timescale directive.

Change 18603 on 2002/03/12 by paulv@paulv_r400_sun_marlboro

Rewrote most of pixel format to work correctly and include number clamping and
rounding.
```

```
Change 18432 on 2002/03/11 by paulv@paulv_r400_sun_marlboro

Fixed two's complement bug in SRF format.

Change 17856 on 2002/03/07 by paulv@paulv_r400_sun_marlboro

Moved flops into subblock (rb_rbc_pixel_deformat).

Change 17724 on 2002/03/06 by paulv@paulv_r400_sun_marlboro

More optimizations.

Change 17572 on 2002/03/05 by paulv@paulv_r400_sun_marlboro

Optimized code.

Change 17189 on 2002/03/01 by paulv@paulv_r400_sun_marlboro

Initial version.

Change 11361 on 2001/12/07 by wlawless@wlawless

fixed comment

Change 11330 on 2001/12/06 by wlawless@wlawless

Initial port list only check in

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx
```

```
Change 54226 on 2002/09/29 by askende@askende_r400_linux_marlboro

fixing width mismatches warnings out of bcons on some of the top level IOs

Change 53986 on 2002/09/26 by askende@askende_r400_linux_marlboro

1.add the scalar SUB opcode
       2. replaced one of the skid_buff_top fifos with an ati_fifo_top instance

Change 53487 on 2002/09/24 by askende@askende_r400_linux_marlboro

renaming files to sx_<file_name>

Change 53486 on 2002/09/24 by askende@askende_r400_linux_marlboro

   renaming files to sx_<file_name>

Change 53483 on 2002/09/24 by askende@askende_r400_linux_marlboro

 renamed the .ctmc files by adding the sx prefix

Change 53453 on 2002/09/24 by askende@askende_r400_linux_marlboro

renaming the files to sx_<file_name>

Change 53452 on 2002/09/24 by askende@askende_r400_linux_marlboro

adding new files after having renamed existing ones
       with sx_*

Change 53413 on 2002/09/24 by askende@askende_r400_linux_marlboro

1. removed quads with mask = 0 from the stream.
       2. reworked the position export control logic.

Change 52170 on 2002/09/17 by askende@askende_r400_sun_marlboro

fix a export buffer write pointer problem and added more comments

Change 50534 on 2002/09/10 by askende@askende_r400_sun_marlboro

adding new changes related to alloc-dealloc logic

Change 49872 on 2002/09/05 by askende@askende_r400_sun_marlboro

changes related to syntax and new instruction interface

Change 49505 on 2002/09/04 by askende@askende_r400_sun_marlboro
```

```
changes related to :

1. predicate in SP vector unit
2. export avail space reporting to SQ in SX

Change 48841 on 2002/08/29 by sallen@sallen_r400_lin_marlboro

-finish up _pm_enb and _pm_en set to 1, clocks run now
   -also set busy signals low in blocks that don't drive them
   -fix mh DEPS file

Change 48695 on 2002/08/28 by askende@askende_r400_sun_marlboro

fixed :

1. sx_sc quad interface bug
2. ij buffer data loading sequence bug
3. mislalignment between PC parameter data and ij data at the input of the
interpolators

Change 48340 on 2002/08/27 by askende@askende_r400_sun_marlboro

reworked part of the export space allocation/deallocation logic.

Change 48205 on 2002/08/27 by askende@askende_r400_sun_marlboro

added for the first time

Change 48197 on 2002/08/27 by askende@askende_r400_sun_marlboro

no longer needed...the rb id gets sent down from SC to SX ...

Change 48196 on 2002/08/27 by askende@askende_r400_sun_marlboro

added a separate file for all `defines in SX...primarly in sx_export_control.v

Change 48195 on 2002/08/27 by askende@askende_r400_sun_marlboro

changes in allocatio/deallocation logic. The first 4 pixel vector tests out of
milestone_tri work as of this point.

Change 48094 on 2002/08/26 by askende@askende_r400_sun_marlboro

backing up changes

Change 47646 on 2002/08/22 by askende@askende_r400_sun_marlboro
```

```
final version related to TP-SP interface change as well as going to new SC_SX rb id
modification

Change 47500 on 2002/08/22 by askende@askende_r400_sun_marlboro

modified top level sp and sx.

1. Removed sc_sx_tilex, tiley buses from the sx.v
2. Brought sp_tp_formatter logic over to sp.v from tp.v

Change 46934 on 2002/08/19 by askende@askende_r400_sun_marlboro

submitting a change related in generating an rb0_read_valid signal going into export
buffer module eventually used to generate a sx_rb#_color_send signal.

Change 46673 on 2002/08/17 by askende@askende_r400_sun_marlboro

time out on RB3 index color request wasn't respected. SX can service the same RB only
once every four cycles.

Change 45473 on 2002/08/12 by askende@askende_r400_sun_marlboro

1. top level changes related vsr_vu_valid
2. modified some of the shader opcodes (SET, MASK, CND)

Change 43744 on 2002/08/01 by askende@askende_r400_sun_marlboro

more synthesis mods

Change 43743 on 2002/08/01 by askende@askende_r400_sun_marlboro

synthesis related changes

Change 43513 on 2002/07/31 by askende@askende_r400_sun_marlboro

syntax correction related to bit-blasted memories

Change 43190 on 2002/07/30 by askende@askende_r400_sun_marlboro

synthesis mod

Change 42974 on 2002/07/29 by askende@askende_r400_sun_marlboro

synthesis related mod...

Change 42779 on 2002/07/26 by askende@askende_r400_sun_marlboro

rearranged the PC read pointers to account for the SC change
```

Change 42095 on 2002/07/23 by askende@askende_r400_sun_marlboro

swapped around the parameter cache read pointers to compensate for the scan converter's vertex indexing change.

Change 41593 on 2002/07/19 by askende@askende_r400_sun_marlboro

fixed the rbbm read back path.

Change 41541 on 2002/07/19 by askende@askende_r400_sun_marlboro

a working first and seconde polygon test rev of this file.

Change 41492 on 2002/07/19 by askende@askende_r400_sun_marlboro

bit-blasted the virage memory instances for synthesis purposes.

Change 41394 on 2002/07/18 by askende@askende_r400_sun_marlboro

tied a few top level signals...first triangle passes..again.

Change 41310 on 2002/07/18 by askende@askende_r400_sun_marlboro

adding the ctmc configuration files into source control for synthesis support

Change 41307 on 2002/07/18 by askende@askende_r400_sun_marlboro

backing up changes

Change 41109 on 2002/07/17 by askende@askende_r400_sun_marlboro

top level changes driven by the changes in related to SQ-SX export allocation/deallocation interface.

Change 40969 on 2002/07/17 by askende@askende_r400_sun_marlboro

1. New SQ_SX export interface
2. Added the top level registers for the (i/o registers) using ati_dff_in and ati_dff_out

Change 40688 on 2002/07/15 by askende@askende_r400_sun_marlboro

backing up changes. Changed a few signal names

Change 40604 on 2002/07/15 by askende@askende_r400_sun_marlboro

added support for two pixel vectors when both vectors coming on the same alu_id thread.

```
Change 37492 on 2002/07/01 by wlawless@wlawless_r400_linux_marlboro

fixed toggle for writing BE's, also fixed SX typo..., Runs 1st triangle

Change 36832 on 2002/06/27 by jayw@jayw_r400_linux_marlboro

I now register each rb's bank at the start of each's multi-cycle
       read out of the four buffers.

Change 36078 on 2002/06/25 by askende@askende_r400_sun_marlboro

Added power managment controls signals at the top level : CG_<block>_pm_enb.

Change 36076 on 2002/06/25 by askende@askende_r400_sun_marlboro

rb3_read_index is used into assignment of export_read_index, instead of registered
version of it (q_rb3_read_index).

Change 36075 on 2002/06/25 by askende@askende_r400_sun_marlboro

three bug fixes:

1. vector.v
    gpr_cmask is daizy_chained from one macc_gpr to the other
2.export_buffers.v
    mem_we is used instead of the registered version of it.

Change 35940 on 2002/06/24 by askende@askende_r400_sun_marlboro

a few changes related to shader pipe

Change 35583 on 2002/06/21 by askende@askende_r400_sun_marlboro

fixed bugs related to SX_RB_color interface....valid signals were not driven correctly

Change 35367 on 2002/06/20 by askende@askende_r400_sun_marlboro

fixed a bug related to generating the right quad index for the second SP pipe data.

Change 35255 on 2002/06/20 by askende@askende_r400_sun_marlboro

fixed a bug related to quad_send SX_RB interface

Change 35059 on 2002/06/19 by askende@askende_r400_sun_marlboro

SX to RB interface working at this point
```

Change 34667 on 2002/06/18 by askende@askende_r400_sun_marlboro

a few fixes related to the first triangle

Change 34592 on 2002/06/17 by askende@askende_r400_sun_marlboro

removed from sx...they are now under sx/param_sub/

Change 34587 on 2002/06/17 by askende@askende_r400_sun_marlboro

reorganized the perforce tree stucture by creating a param_sub directory under sx
branch

Change 34325 on 2002/06/14 by askende@askende_r400_sun_marlboro

fixed a timing issue related to pa_pos_skid_buff...

Change 34222 on 2002/06/14 by askende@askende_r400_sun_marlboro

at this point the PA block gets the valid position data

Change 33361 on 2002/06/11 by askende@askende_r400_sun_marlboro

tied SX_SQ_pos_avail to 1'b1

Change 32457 on 2002/06/06 by askende@askende_r400_sun_marlboro

a working version of the sx-pa position interface

Change 31892 on 2002/06/04 by askende@askende_r400_sun_marlboro

fixed a few problems related to the position read request interface between PA and SX.
At this point everything work with exception of the sp_pa_pos_valid that needs to stay
high for 4 cycles
once a read has been granted to the clipper/pa.

Change 31724 on 2002/06/04 by askende@askende_r400_sun_marlboro

changes at the top level

1. adding sp_sx_exp_dest port to sp.v
2. connecting the sp_tp_fetch_addr ports at the top level
3. changing the sp_sx_exp_dest port from 7 bits to 6 bits in sx.v

Change 30941 on 2002/05/30 by askende@askende_r400_sun_marlboro

fixed a signal naming bug

```
Change 30702 on 2002/05/29 by askende@askende_r400_sun_marlboro

integrate

Change 30544 on 2002/05/29 by askende@askende_r400_sun_marlboro

backing up changes

Change 30064 on 2002/05/24 by askende@askende_r400_sun_marlboro

submitting the latest changes regarding :

1. export write interface,
2. position data interface..now supporting both buffers (position and auxiliary).

Change 26645 on 2002/05/06 by askende@askende_r400_sun_marlboro

backing up new code.

Change 26643 on 2002/05/06 by askende@askende_r400_sun_marlboro

1.tied the top level sx.v to export_control.v
2.added partial logic on the position inteface in export_control.v

Change 26241 on 2002/05/03 by askende@askende_r400_sun_marlboro

more updates to the top level.

1.added RB#_SX_index_op
3.added SX_RBBM_busy

Change 25664 on 2002/04/30 by askende@askende_r400_sun_marlboro

new top level ..
Includes the new RB to SX interface definition where color interface has been separated
from
index request interface.

Change 25347 on 2002/04/29 by askende@askende_r400_sun_marlboro

backing up new code

Change 25062 on 2002/04/25 by askende@askende_r400_sun_marlboro

1.added the test bench logic to the repository.
2.backing up latest changes to the export control logic

Change 23716 on 2002/04/17 by askende@askende_r400_sun_marlboro
```

```
first time check in.

Change 23162 on 2002/04/12 by askende@askende_r400_sun_marlboro

deleting this file. being replaced with export_control.

Change 23160 on 2002/04/12 by askende@askende_r400_sun_marlboro

being checked in so it can later be deleted.

Change 23159 on 2002/04/12 by askende@askende_r400_sun_marlboro

first time checked in. Replaced export_buffer.v with export_control.v

Change 22754 on 2002/04/10 by askende@askende_r400_sun_marlboro

1.adding the alpha_color_test module into source control
2.a new version of the export_buffer logic
  new feature :
   a. "quad buffer" and "detailed quad buffer" implemented
   b. alpha and color testing being implemented
   c. quad interface from SX to RB implemented

Change 22104 on 2002/04/05 by askende@askende_r400_sun_marlboro

new rev of the top level. corrected the width of some of the RBBM interface
signals/buses

Change 22100 on 2002/04/05 by askende@askende_r400_sun_marlboro

new top level file revision.
added the RBBM interface definition.

Change 21972 on 2002/04/04 by askende@askende_r400_sun_marlboro

first time checked in.

Change 21971 on 2002/04/04 by askende@askende_r400_sun_marlboro

new top level revision

Change 21443 on 2002/04/02 by askende@askende_r400_sun_marlboro

renamed some of the IO names to enable the GC integration.

Change 21310 on 2002/04/01 by askende@askende_r400_sun_marlboro
```

```
completed the parameter cache read/write logic including the parameter selection (flat
vs. gouraud) as well as the paremeter difference engine logic for the interpolators.

Change 21078 on 2002/03/29 by askende@askende_r400_sun_marlboro

completed the vertex parameter read/write in/out of parameter cache logic.
completed the vertex parameter routing and selection.
a vorking version of the above.
a working version of the testbench.

Change 20984 on 2002/03/28 by askende@askende_r400_sun_marlboro

work in progress ..more additions

Change 20761 on 2002/03/27 by askende@askende_r400_sun_marlboro

additional behavioral code

Change 20760 on 2002/03/27 by askende@askende_r400_sun_marlboro

first time checked in.

Change 20704 on 2002/03/27 by askende@askende_r400_sun_marlboro

new top level rev. of the sx.v

Change 20677 on 2002/03/27 by askende@askende_r400_sun_marlboro

new rev.

Change 20665 on 2002/03/27 by askende@askende_r400_sun_marlboro

a new rev of the top level sx interface definition

Change 20625 on 2002/03/26 by askende@askende_r400_sun_marlboro

initial check in.

Change 20624 on 2002/03/26 by askende@askende_r400_sun_marlboro

another rev of the sx.v interface definitions

Change 20010 on 2002/03/21 by askende@askende_r400_sun_marlboro

first revision of the top level for the Shader Export.

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro
```

```
mv block dirs to gfx

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 11069 on 2001/12/03 by wlawless@wlawless

Initial port list for sx.v

Change 11057 on 2001/12/03 by wlawless@wlawless

nothing

Change 9415 on 2001/11/07 by mmantor@mmantor_r400

create the director
```

```
Change 54226 on 2002/09/29 by askende@askende_r400_linux_marlboro

fixing width mismatches warnings out of bcons on some of the top level IOs

Change 54216 on 2002/09/28 by tien@tien_r400_devel_marlboro

Adjusted pipe stages
Bug fix

Change 54093 on 2002/09/27 by tien@tien_r400_devel_marlboro

Width of exp3:2 vector fixed

Change 53986 on 2002/09/26 by askende@askende_r400_linux_marlboro

1.add the scalar SUB opcode
       2. replaced one of the skid_buff_top fifos with an ati_fifo_top instance

Change 53874 on 2002/09/26 by askende@askende_r400_linux_marlboro

fixed a "logic timing" problem related to Scalar Result write-back path into GPRs

Change 53006 on 2002/09/23 by askende@askende_r400_sun_marlboro

new code added to the scalar engine

Change 52906 on 2002/09/21 by askende@askende_r400_sun_marlboro

adding clamp to the vector unit alu

Change 52838 on 2002/09/20 by askende@askende_r400_sun_marlboro

fixed a bug related to sete opcode

Change 52508 on 2002/09/19 by askende@askende_r400_sun_marlboro

changes:

1. corrected an overflow condition in the multiply logic of the interpolators
2. rewrote the gpr write-back path logic for the scalar results

Change 52134 on 2002/09/17 by askende@askende_r400_sun_marlboro

renamed some of the modules to sp_*

Change 52110 on 2002/09/17 by askende@askende_r400_sun_marlboro

removed after being renamed to two new ones starting with sp_*
```

```
Change 52109 on 2002/09/17 by askende@askende_r400_sun_marlboro

renaming the files to include sp_* in the front of the name

Change 52107 on 2002/09/17 by askende@askende_r400_sun_marlboro

deleted after checking in new ones renamed sp_*

Change 52105 on 2002/09/17 by askende@askende_r400_sun_marlboro

renamed the modules to sp_*

Change 52052 on 2002/09/17 by askende@askende_r400_sun_marlboro

changes to :

1. interpolators to handle sub-norm ij values.
2. scalar engine result back to GPRs.
3. gc.tree regarding the tp_sp_valid signals.

Change 51731 on 2002/09/16 by askende@askende_r400_sun_marlboro

backing up changes

Change 51592 on 2002/09/13 by askende@askende_r400_sun_marlboro

modified the swizzle select logic

Change 51560 on 2002/09/13 by askende@askende_r400_sun_marlboro

submitting changes related to scalar engine. The latency through the scalar pipe is 7
cycles at this point.

Change 51442 on 2002/09/13 by askende@askende_r400_sun_marlboro

removed from the depot after  they were renamed to sp_*

Change 51440 on 2002/09/13 by askende@askende_r400_sun_marlboro

changes:

1.fixed overflow detection logic in macc32
2. fixed RECIP and RECIP_SQRT logic in scalar_lut
3. replaced gpr_cmask = 0xf with the value driven by SQ

Change 50846 on 2002/09/11 by askende@askende_r400_sun_marlboro
```

```
modified the sp_defines_mc.mc

Change 50834 on 2002/09/11 by askende@askende_r400_sun_marlboro

renaming of the scalar_lut to sp_scalar_lut

Change 50830 on 2002/09/11 by askende@askende_r400_sun_marlboro

added for the first time

Change 50812 on 2002/09/11 by askende@askende_r400_sun_marlboro

1.fixed a bug related to sp_macc32 add logic
2.renaming the scalar_lut.mc to sp_scalar_lut.mc

Change 50534 on 2002/09/10 by askende@askende_r400_sun_marlboro

adding new changes related to alloc-dealloc logic

Change 50528 on 2002/09/10 by tien@tien_r400_devel_marlboro

Fixed instance names
Finished sp_tp code to handle all cases

Change 50404 on 2002/09/10 by askende@askende_r400_sun_marlboro

more changes related to area savings and logic optimizations.

Change 49872 on 2002/09/05 by askende@askende_r400_sun_marlboro

changes related to syntax and new instruction interface

Change 49505 on 2002/09/04 by askende@askende_r400_sun_marlboro

changes related to :

1. predicate in SP vector unit
2. export avail space reporting to SQ in SX

Change 48978 on 2002/08/30 by askende@askende_r400_sun_marlboro

checking in changes related to the new instruction interface

Change 48695 on 2002/08/28 by askende@askende_r400_sun_marlboro

fixed :

1. sx_sc quad interface bug
```

2. ij buffer data loading sequence bug
3. mislalignment between PC parameter data and ij data at the input of the interpolators

Change 48197 on 2002/08/27 by askende@askende_r400_sun_marlboro

no longer needed...the rb id gets sent down from SC to SX ...

Change 47863 on 2002/08/23 by askende@askende_r400_sun_marlboro

added sq_sp_gpr_wr_ena signal for all the phases of a vector unit.

Change 47656 on 2002/08/22 by askende@askende_r400_sun_marlboro

bringing the sp_tp_formatter to sp from tp

Change 47646 on 2002/08/22 by askende@askende_r400_sun_marlboro

final version related to TP-SP interface change as well as going to new SC_SX rb id modification

Change 47441 on 2002/08/21 by askende@askende_r400_sun_marlboro

reworked the staging registers

Change 47181 on 2002/08/20 by askende@askende_r400_sun_marlboro

changed the staging registers to be vertical feeding into macc

Change 46419 on 2002/08/15 by askende@askende_r400_sun_marlboro

renaming

Change 46417 on 2002/08/15 by askende@askende_r400_sun_marlboro

renaming

Change 46373 on 2002/08/15 by askende@askende_r400_sun_marlboro

renamed some of the modules

Change 46348 on 2002/08/15 by askende@askende_r400_sun_marlboro

this check in is related to renaming some of the files to sp_*

Change 46341 on 2002/08/15 by askende@askende_r400_sun_marlboro

old modules ...no longer needed

```
Change 46340 on 2002/08/15 by askende@askende_r400_sun_marlboro

submitting a bunch of changes related to reducing area for the macc32 unit

Change 45966 on 2002/08/14 by askende@askende_r400_sun_marlboro

1. argument selection logic bug fix related to argument modifier "negate"
2. grouped all the `defines and #defines in sp_defines.v and sp_defines_mc.mc

Change 45593 on 2002/08/13 by askende@askende_r400_sun_marlboro

files with #define(s) specific to mc module only

Change 45489 on 2002/08/12 by askende@askende_r400_sun_marlboro

this files includes all the `define(s) for the shader block

Change 45473 on 2002/08/12 by askende@askende_r400_sun_marlboro

1. top level changes related vsr_vu_valid
2. modified some of the shader opcodes (SET, MASK, CND)

Change 45315 on 2002/08/09 by askende@askende_r400_sun_marlboro

more opcodes implemented

Change 43690 on 2002/08/01 by askende@askende_r400_sun_marlboro

modifications related to synthesis

Change 43147 on 2002/07/30 by askende@askende_r400_sun_marlboro

explictly declared the instance for q_cg_sp_pm_enb

Change 42930 on 2002/07/29 by askende@askende_r400_sun_marlboro

changed the input sclk signal to sclk_global to support synthesis...
still uses "sclk" internaly after sclk has been assigned sclk_global

Change 42729 on 2002/07/26 by askende@askende_r400_sun_marlboro

changed the name from isq_stall to q_sq_stall

Change 42617 on 2002/07/26 by askende@askende_r400_sun_marlboro

renamed the clock from CLK to sclk
```

```
Change 42463 on 2002/07/25 by askende@askende_r400_sun_marlboro

maybe a syntax problem with [0:0] input declaration

Change 42461 on 2002/07/25 by askende@askende_r400_sun_marlboro

adding synthesis related fixes.

1. added a virage bit-blasted memory component to sp_vsr_ctl.v
2. fixed a syntax problem with interp_ctl.v
3. added the clock into the io list for hi_prec_int.mc module

Change 41492 on 2002/07/19 by askende@askende_r400_sun_marlboro

bit-blasted the virage memory instances for synthesis purposes.

Change 41337 on 2002/07/18 by desiree@desiree_r400_sun_marlboro

Testing check-in

Change 41336 on 2002/07/18 by desiree@desiree_r400_sun_marlboro

First add of syn file

Change 41310 on 2002/07/18 by askende@askende_r400_sun_marlboro

adding the ctmc configuration files into source control for synthesis support

Change 41109 on 2002/07/17 by askende@askende_r400_sun_marlboro

top level changes driven by the changes in related to SQ-SX export
allocation/deallocation interface.

Change 40968 on 2002/07/17 by askende@askende_r400_sun_marlboro

first time checked in.
this file represents the implementation of all the vector opcodes with exception of the
ones that have MUL or ADD at their base.

Change 37589 on 2002/07/02 by jayw@jayw_r400_linux_marlboro

1st triangle, mucho chango.
handles zero, subnorms, etc...

Change 36771 on 2002/06/27 by jayw@MA_JAYW

the exponent was not generated correctly, now fixed.
I also fixed normalization of zero values.
```

```
I also added subnorm compatibility.

NOTE:  This codes need time and someone to clean the syntax!!!

Change 36390 on 2002/06/26 by jayw@jayw_r400_linux_marlboro

Reflects change in normalize.mc.

Change 36383 on 2002/06/26 by jayw@MA_JAYW

mark fowler found this, the
normalize needs to subtract the number of leading zeros
when shifting the mantissa left.  -- jay

Change 36340 on 2002/06/26 by markf@markf_r400_linux_marlboro

Changed exponent bias for i,j from 10 to 6

Change 36339 on 2002/06/26 by markf@markf_r400_linux_marlboro

Changed exponent bias for i,j from 10 to 6

Change 36078 on 2002/06/25 by askende@askende_r400_sun_marlboro

Added power managment controls signals at the top level : CG_<block>_pm_enb.

Change 36075 on 2002/06/25 by askende@askende_r400_sun_marlboro

three bug fixes:

1. vector.v
    gpr_cmask is daizy_chained from one macc_gpr to the other
2.export_buffers.v
    mem_we is used instead of the registered version of it.

Change 35940 on 2002/06/24 by askende@askende_r400_sun_marlboro

a few changes related to shader pipe

Change 34667 on 2002/06/18 by askende@askende_r400_sun_marlboro

a few fixes related to the first triangle

Change 34502 on 2002/06/17 by sallen@sallen_r400_lin_marlboro

ferret: cons updates for dependencies
           local csrc files to speed up compiles
           fix time out counter to update during register writes
```

Change 34345 on 2002/06/15 by markf@markf_r400_linux_marlboro

Added sclk and srst to interp_ctl, fixed half_swap signal, other stuff.

Change 34344 on 2002/06/15 by markf@markf_r400_linux_marlboro

Added srst to interpolator module

Change 34222 on 2002/06/14 by askende@askende_r400_sun_marlboro

at this point the PA block gets the valid position data

Change 33393 on 2002/06/11 by askende@askende_r400_sun_marlboro

fixed a bug related to gpr_wr_ena control signal generation.

Change 33346 on 2002/06/11 by askende@askende_r400_sun_marlboro

added a top level signal called TP_SP_data_valid which propagate all the way down to vector.v

Change 33340 on 2002/06/11 by askende@askende_r400_sun_marlboro

adding the top level signal called TP_SP_data_valid

Change 33222 on 2002/06/11 by askende@askende_r400_sun_marlboro

changed the enable for the GPR read cycles to be high all the time. This is a hack for the time being

Change 33157 on 2002/06/11 by askende@askende_r400_sun_marlboro

added the masking logic for the GPR write path

Change 32779 on 2002/06/07 by askende@askende_r400_sun_marlboro

adding a behavioral model of a dual-ported 128x128 register file

Change 32777 on 2002/06/07 by askende@askende_r400_sun_marlboro

no longer needed

Change 32769 on 2002/06/07 by askende@askende_r400_sun_marlboro

adding into the database....the dummy memory module does not provide sub-word masking.

Change 32079 on 2002/06/05 by askende@askende_r400_sun_marlboro

```
set the correct number of words (parameter) for the macc_gpr register file

Change 31995 on 2002/06/05 by askende@askende_r400_sun_marlboro

registered the output of the register file (GPRs) to line up with the phase_mux control
signal

Change 31776 on 2002/06/04 by sallen@sallen_r400_lin_marlboro

   ferret allow user to set VCSBUILD in Construct file
   clean up unit/gc level Construct files a bit
   make macc32 testbench work with VCSBUILD

Change 31724 on 2002/06/04 by askende@askende_r400_sun_marlboro

changes at the top level

1. adding sp_sx_exp_dest port to sp.v
2. connecting the sp_tp_fetch_addr ports at the top level
3. changing the sp_sx_exp_dest port from 7 bits to 6 bits in sx.v

Change 31584 on 2002/06/03 by askende@askende_r400_sun_marlboro

intergrating

Change 31558 on 2002/06/03 by pmitchel@pmitchel_r400_linux_marlboro

test

Change 31296 on 2002/05/31 by askende@askende_r400_sun_marlboro

changes to signal naming

Change 30706 on 2002/05/29 by askende@askende_r400_sun_marlboro

new rev

Change 29993 on 2002/05/24 by askende@askende_r400_sun_marlboro

latest code.

Change 28948 on 2002/05/17 by askende@askende_r400_sun_marlboro

first time checked in ....virage behavioral rtl model for a 16x200sw4 register file.

Change 28947 on 2002/05/17 by askende@askende_r400_sun_marlboro
```

```
1. modified the top level sp.v file.
2. exposed the texture fetch path all the way from macc_gpr to sp.v.
3. modified and tested the interp_ctl.v ...the ij buffer control logic.
4. replaced the dum_mem_p2 with virage rtl behavioral model.

Change 28538 on 2002/05/16 by askende@askende_r400_sun_marlboro

new rev of the vsr control logic ...a working version

Change 28403 on 2002/05/16 by askende@askende_r400_sun_marlboro

new top level reflection the changes in SC-SP interpolation interface ...going from one
high precision + 3 low precision interpolators to 4 high precision ones.

Change 27787 on 2002/05/13 by askende@askende_r400_sun_marlboro

first time checked in

Change 27100 on 2002/05/08 by askende@askende_r400_sun_marlboro

first time checked in.
this block represents the control logic for reading and writting the vertex index stage
registers.

Change 27070 on 2002/05/08 by askende@askende_r400_sun_marlboro

Paul checking in as Andi

Change 27028 on 2002/05/08 by sallen@sallen_r400_lin_marlboro

first round of ferret changes for gc.v testbench
   add parts_lib/s**/test/gc

Change 26988 on 2002/05/08 by askende@askende_r400_sun_marlboro

first time checked in

Change 26985 on 2002/05/08 by askende@askende_r400_sun_marlboro

latest top level as well as some changes regarding clock/reset signal naming

Change 24984 on 2002/04/25 by sallen@sallen_r400_lin_marlboro

ferret updates
     - add mem fill/dump
     - add rbbm register read/writes
     - add ferret_memload test
```

```
Change 21971 on 2002/04/04 by askende@askende_r400_sun_marlboro

new top level revision

Change 21447 on 2002/04/02 by askende@askende_r400_sun_marlboro

new top level revision to enable the GC integration.

Change 20621 on 2002/03/26 by askende@askende_r400_sun_marlboro

another naming update

Change 20586 on 2002/03/26 by askende@askende_r400_sun_marlboro

updated the top level interfaces for the GC integration effort.

Change 20547 on 2002/03/26 by pmitchel@pmitchel_entire_depot_win

rename

Change 20544 on 2002/03/26 by askende@askende_r400_sun_marlboro

no changes ...is being checked in so the file can be renamed

Change 20543 on 2002/03/26 by askende@askende_r400_sun_marlboro

new rev ....changed the name of the top level from module "shader" to "sp"

Change 18789 on 2002/03/13 by askende@askende_r400_sun_marlboro

first time checked in.

Change 18349 on 2002/03/11 by askende@askende_r400_sun_marlboro

first time checked in

Change 18348 on 2002/03/11 by askende@askende_r400_sun_marlboro

first time checked in

Change 17964 on 2002/03/07 by askende@askende_r400_sun_marlboro

backing up changes

Change 17855 on 2002/03/07 by pmitchel@pmitchel_r400_sun_marlboro

changed type
```

```
Change 17850 on 2002/03/07 by pmitchel@pmitchel_r400_sun_marlboro

testing $Id$

Change 17602 on 2002/03/05 by askende@askende_r400_sun_marlboro

intergrated the scalar unit with the vector unit module

Change 17601 on 2002/03/05 by askende@askende_r400_sun_marlboro

first time check in.

Change 17600 on 2002/03/05 by askende@askende_r400_sun_marlboro

no longer needed

Change 17098 on 2002/02/28 by askende@askende_r400_sun_marlboro

modified some of the gpr write/read enable signal generation from the shader_test.v
level

Change 16766 on 2002/02/26 by askende@askende_r400_sun_marlboro

removed from database ...no longer needed

Change 16542 on 2002/02/25 by askende@askende_r400_sun_marlboro

no longer needed

Change 16541 on 2002/02/25 by askende@askende_r400_sun_marlboro

new revision of the shader pipe logic.
renamed some of the signals throughout the hierarchy.

Change 16540 on 2002/02/25 by askende@askende_r400_sun_marlboro

shader top level test bench ....first time checked in.

Change 15621 on 2002/02/15 by pmitchel@pmitchel_r400_sun_marlboro

testing diffs with rcs keywords; added header.txt to file

Change 14831 on 2002/02/07 by askende@askende_r400_sun_marlboro

updated the external interfaces to the latest spec.

Change 14458 on 2002/02/01 by askende@askende_r400_sun_marlboro
```

```
backing up code changes

Change 14434 on 2002/02/01 by askende@askende_r400_sun_marlboro

first time checked in.

Change 14433 on 2002/02/01 by askende@askende_r400_sun_marlboro

this file is being deleted. It is no longer needed. It is being replace by a new file
named macc_gpr.v

Change 14432 on 2002/02/01 by askende@askende_r400_sun_marlboro

checking it in so it can be removed from Perforce.
This file is no longer needed. A new file macc_gpr.v has been introduced to replace
this one.

Change 14369 on 2002/01/31 by askende@askende_r400_sun_marlboro

this file was used for testing a few perforce features.
it is no longer needed.

Change 14358 on 2002/01/31 by pmitchel@pmitchel_samba_test

samba test cont...

Change 14355 on 2002/01/31 by pmitchel@pmitchel_samba_test

testing out use of samba w/perforce

Change 14314 on 2002/01/31 by askende@andi_r400

saving the changes so I can reconfigure my devel_askende area

Change 14288 on 2002/01/30 by askende@andi_r400

first time checked in

Change 14099 on 2002/01/28 by askende@andi_r400

new rev

Change 13946 on 2002/01/25 by askende@andi_r400

first time checked in

Change 13945 on 2002/01/25 by askende@andi_r400
```

```
first time check in

Change 12120 on 2001/12/20 by askende@andi_r400

added FRACT support in the scalar engine

Change 12076 on 2001/12/19 by askende@andi_r400

new updates. The ADD and ADD_PREV have been added.

Change 12051 on 2001/12/19 by askende@andi_r400

new rev

Change 11956 on 2001/12/18 by askende@andi_r400

first time entered under source control

Change 11954 on 2001/12/18 by askende@andi_r400

another revision of the scalar unit code
at this point ...the latency is 8.

Change 11807 on 2001/12/14 by askende@andi_r400

removed the low precision path (log2(x) and lit) from the Scalar engine.

Change 11732 on 2001/12/13 by askende@andi_r400

took out the vector engine related code.
synthesis of the scalar unit was done for the first time.

Change 11623 on 2001/12/12 by askende@andi_r400

first revision

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 10478 on 2001/11/21 by askende@andi_r400

further update of the I/O definition
```

```
Change 9918 on 2001/11/14 by askende@andi_r400

first time check-in

Change 8480 on 2001/10/25 by askende@andi_r400

inserted into source control by Andi S.

Change 6887 on 2001/09/25 by askende@andi_r400_devel

more changes

Change 6810 on 2001/09/21 by askende@andi_r400_devel

newly added files
```

```
Change 54212 on 2002/09/28 by dougd@dougd_r400_linux_marlboro

corrected bit widths on some signals that caused errors in synthesis

Change 54202 on 2002/09/28 by dougd@dougd_r400_linux_marlboro

increased size of vtx_alloc_space because vs_num_reg is 1 less than the actual value we
want to req

Change 54201 on 2002/09/28 by dougd@dougd_r400_linux_marlboro

corrected the `defines in the parameter list of the instantiation of
sq_thread_buff_cntl from those for "vtx" to those for "pix"

Change 54166 on 2002/09/27 by vromaker@vromaker_r400_linux_marlboro

- SC_SQ interface updates
- also connected VGT_SQ_event to sq_vism

Change 53873 on 2002/09/26 by dougd@dougd_r400_linux_marlboro

defined wires for vss and vdd for virage memories

Change 53800 on 2002/09/26 by vromaker@vromaker_r400_linux_marlboro

- fixes for events flowing thru SQ
- cleared up issues with making individial vtx and pix thread buffers (and shared
thread_buff_cntl)
- fixed PV,PS bugs

Change 53737 on 2002/09/25 by dougd@dougd_r400_linux_marlboro

reduced size of cfc constant store

Change 53736 on 2002/09/25 by dougd@dougd_r400_linux_marlboro

added 2 bits to width of vism skid buffer

Change 53735 on 2002/09/25 by dougd@dougd_r400_linux_marlboro

changed sizes of virage rams for mapping tables

Change 53730 on 2002/09/25 by dougd@dougd_r400_linux_marlboro

set all generate flags to "true"

Change 53434 on 2002/09/24 by vromaker@vromaker_r400_linux_marlboro
```

```
a few port mismatch fixes

Change 53376 on 2002/09/24 by dougd@dougd_r400_linux_marlboro

removed redundant declaration that caused synopsys compile error

Change 53375 on 2002/09/24 by vromaker@vromaker_r400_linux_marlboro

- fixes for moving event thru the SQ
- fixes for dealloc, and state_diff in thread buffers

Change 53204 on 2002/09/23 by dougd@dougd_r400_linux_marlboro

corrected mix of assigments: next_old_context <= old_context_q;    // synopsys doesn't
like "<=" mixed with "="

Change 53136 on 2002/09/23 by dougd@dougd_r400_linux_marlboro

remove "wire [7:0] temp6 = i_addr_in/6;" which cause synthesis error

Change 53039 on 2002/09/23 by dougd@dougd_r400_linux_marlboro

new modules to increase size of pixel thread buffer

Change 52738 on 2002/09/20 by vromaker@vromaker_r400_linux_marlboro

event fifo to pism/ptb fixes

Change 52350 on 2002/09/18 by vromaker@vromaker_r400_linux_marlboro

ptr buff fix to work correctly with split 2-cycle transfers

Change 52270 on 2002/09/18 by dougd@dougd_r400_linux_marlboro

corrected width of constant assigned to alloc_size_q from 2 to 4

Change 52212 on 2002/09/18 by dougd@dougd_r400_linux_marlboro

modified fix to sq_valid_2_q that was entered in the previous version

Change 52164 on 2002/09/17 by dougd@dougd_r400_linux_marlboro

added more to fix for sq_qual_2_q of previous version

Change 52160 on 2002/09/17 by dougd@dougd_r400_linux_marlboro

make sc_valid_2_q stay asserted until there is a SC_SQ_valid
```

Change 51789 on 2002/09/16 by dougd@dougd_r400_linux_marlboro

fixed bug with SQ_RBB_rs outputting x's; fixed bug with code added to support rbbm diagnostic read of constant store memories

Change 51740 on 2002/09/16 by tien@tien_r400_devel_marlboro

Interface change for post-June 15th inst/const

Change 51675 on 2002/09/15 by dougd@dougd_r400_linux_marlboro

fixed bug in rbbm diagnostic read interface

Change 51559 on 2002/09/13 by dougd@dougd_r400_linux_marlboro

connect acs_rd_req to sq_aluconst_top (that input was floating)

Change 51526 on 2002/09/13 by vromaker@vromaker_r400_linux_marlboro

- gpr dealloc connected
- static gpr allocation added (but not enabled)
- ppb btwn pism and ptb added

Change 51368 on 2002/09/13 by dougd@dougd_r400_linux_marlboro

added some of the port connections necessary to support RBBM reading of the constant store memories

Change 50967 on 2002/09/12 by dougd@dougd_r400_linux_marlboro

changed port name "i_context_switch" to "i_map_copy_start" for aluconst and texconst; changed "i_state_change_flag" to "i_read_base_ld" and added ports based on state change based on gfx_copy_state to sq_cfc

Change 50916 on 2002/09/11 by dougd@dougd_r400_linux_marlboro

connect context_switch based on gfx_copy_state in rbi; connect loading mechanism for eo_rt start addresses for aluconst and texconst

Change 50806 on 2002/09/11 by vromaker@vromaker_r400_linux_marlboro

fixes for bug326 and 329 - tests still fail, but for different reasons

Change 50723 on 2002/09/11 by dougd@dougd_r400_linux_marlboro

added support for real time mode

Change 50564 on 2002/09/10 by vromaker@vromaker_r400_linux_marlboro

```
update

Change 50503 on 2002/09/10 by vromaker@vromaker_r400_linux_marlboro

another PV/PS phase swap bug fix

Change 50458 on 2002/09/10 by dougd@dougd_r400_linux_marlboro

these files moved to directory where they are used

Change 50294 on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro

update to write enables due to PV, PS cycle swap

Change 50193 on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro

updated kill_mask out to SX

Change 50165 on 2002/09/09 by vromaker@vromaker_r400_linux_marlboro

fix for pc write one cycle early

Change 50034 on 2002/09/06 by dougd@dougd_r400_linux_marlboro

initial submission of skid buf ram for sq_rbbm_interface

Change 49970 on 2002/09/06 by vromaker@vromaker_r400_linux_marlboro

minor udpates

Change 49848 on 2002/09/05 by vromaker@vromaker_r400_linux_marlboro

- added predicate, kill mask, pv/ps detection
- swapped PV and PS write gpr phase

Change 49671 on 2002/09/05 by dougd@dougd_r400_sun_marlboro

changed sizes of new_map_ram, map_ram and freelist to cover full size of texconst_mem

Change 49291 on 2002/09/03 by dougd@dougd_r400_linux_marlboro

removed context_misc_screen_xy_in_gpr0_set from sq.v and sq_rbbm_interface.v. added
address decoding for real time constants in sq_rbbm_interface.v

Change 49226 on 2002/09/02 by dougd@dougd_r400_sun_marlboro

initial checkin
```

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Change 49220 on 2002/09/02 by dougd@dougd_r400_linux_marlboro

brought in 3 more bits of rbi_addr and divide it by 6 to get the correct texture
constant address because the 6 Dwords in each constant are no longer packed on
boundaries of 8 Dwords but on boundaries of 6 Dwords.

Change 49065 on 2002/08/30 by dougd@dougd_r400_linux_marlboro

add "vs_num_reg + 1" logic and increase port size by 1 bit

Change 49059 on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro

fixed a few typos for the new SP instruction decode

Change 48976 on 2002/08/30 by dougd@dougd_r400_linux_marlboro

make o_v_ld_cntl_pkt deassert the next clk after receiving i_vtb_rtr

Change 48974 on 2002/08/30 by vromaker@vromaker_r400_linux_marlboro

- needed to drive acfs_reading one cycle earlier for ACFS IS read
- updated/added new SQ_SP instruction interface

Change 48932 on 2002/08/29 by dougd@dougd_r400_linux_marlboro

replaced address constant with value defined in sq_reg.v

Change 48844 on 2002/08/29 by dougd@dougd_r400_linux_marlboro

added support for gen_index (auto-count), vgt events and fixed some bugs

Change 48558 on 2002/08/28 by vromaker@vromaker_r400_linux_marlboro

- fix for out-of-order thread processing: the 2 alu ctl flow sequencers
  now share one instr store read slot instead of alternating between two
  different slots (which allowed one to get ahead opf the other)
- thread counts from VISM and PISM to ais_output added at SQ level

Change 48384 on 2002/08/27 by vromaker@vromaker_r400_linux_marlboro

- updates for ptr_buff/pism to align quad mask correctly
- additions for thread_count

Change 48164 on 2002/08/26 by vromaker@vromaker_r400_linux_marlboro

- fixes for individual macc write enables
- added the prev_pos_alloc inputs to the status regs (and logic to
```

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  generate them in the tread buffer)

Change 47553 on 2002/08/22 by vromaker@vromaker_r400_linux_marlboro

- ptr buff changed for out-of-order quads
- pism: now add 1 to ps_num_reg to get the number of GPRs to alloc

Change 47160 on 2002/08/20 by vromaker@vromaker_r400_linux_marlboro

connected param_gen_pos to pism

Change 47110 on 2002/08/20 by dougd@dougd_r400_linux_marlboro

added the two rbbm registers that were missed in the last version

Change 47072 on 2002/08/20 by vromaker@vromaker_r400_linux_marlboro

updated param_wrap wires

Change 46976 on 2002/08/20 by dougd@dougd_r400_linux_marlboro

adding the remaining rbbm register outputs to sq_rbbm_interface and wired them up in
sq.v

Change 46800 on 2002/08/19 by vromaker@vromaker_r400_linux_marlboro

updated pism connections to local registers

Change 46714 on 2002/08/19 by vromaker@vromaker_r400_linux_marlboro

updated local register inputs to PISM

Change 46643 on 2002/08/16 by dougd@dougd_r400_linux_marlboro

added vgt_event to port list

Change 46642 on 2002/08/16 by dougd@dougd_r400_linux_marlboro

added register outputs from rbbm_interface and vgt_event from sq_vism

Change 46637 on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro

fix for alloc size

Change 46629 on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro

more fixes for alloc size
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Change 46574 on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro

fix for SQ_SX_export_id (was connected to wrong signal)

Change 46517 on 2002/08/16 by vromaker@vromaker_r400_linux_marlboro

fixed thread read state machine typo

Change 46382 on 2002/08/15 by vromaker@vromaker_r400_linux_marlboro

fixed pop_thread to be only one cycle

Change 46251 on 2002/08/15 by vromaker@vromaker_r400_linux_marlboro

updates for pop/winner_ack status reg conflict

Change 45784 on 2002/08/13 by dougd@dougd_r400_linux_marlboro

fixed synchronization of writes to RAM by removing input flop on i_texconst_phase to be
compatible with same change made in sq_texconst_mem.v sometime ago. Also updated local
testbench for sq_texconst block.

Change 45466 on 2002/08/12 by askende@askende_r400_sun_marlboro

checking in with Vic's permission changes related to vsr_vu_valid

Change 45406 on 2002/08/12 by dougd@dougd_r400_linux_marlboro

add change to deassert q_ins_sel when  i_ins_rtr is returned.

Change 45291 on 2002/08/09 by dougd@dougd_r400_linux_marlboro

removed "[0:0]" from "input [0:0] clk;" in sq_status_reg.v to prevent synopsys tcl
script error during synthesis. Removed divide-by-3 code in sq_instruction_store.v to
prevent synthesis error.

Change 45271 on 2002/08/09 by dougd@dougd_r400_linux_marlboro

add i_texconst_rtr to deassert q_tex_sel

Change 45079 on 2002/08/08 by efong@efong_crayola_linux_cvd

removed all the hacked files

Change 44548 on 2002/08/06 by vromaker@vromaker_r400_linux_marlboro

- status register shift connection bug fixed
```

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Change 44376 on 2002/08/06 by dougd@dougd_r400_linux_marlboro

changed default parameter values STATE_WIDTH =64; CFS_STATE_WIDTH = 32; STATUS_WIDTH =
32; to prevent index select errors in synthesis

Change 44356 on 2002/08/06 by dougd@dougd_r400_linux_marlboro

changed default parameter value of 16 to STATUS_WIDTH = 32; to prevent error: slice
direction does not match array direction in synthesis

Change 44355 on 2002/08/06 by dougd@dougd_r400_linux_marlboro

changed default parameter values (was 8): STATE_WIDTH = 64; STATUS_WIDTH = 32; so that
select index would not be out of bounds and cause synthesis to error

Change 44314 on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro

more delay for free_done

Change 44294 on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro

- 3 cycle delay added for free_done
- port width fixes

Change 44234 on 2002/08/05 by sallen@sallen_r400_lin_marlboro

ferret: finish up backdoor ucode loading, pli changes, etc

Change 44201 on 2002/08/05 by vromaker@vromaker_r400_linux_marlboro

- free_done fix: don't send on param_cache (vtx shdr) done
- sq: added SQ_SP_vsr_vu_valid
- updates to VISM to handle end_of_vector with invalid data

Change 44010 on 2002/08/02 by vromaker@vromaker_r400_linux_marlboro

- multi pixel vector fixes
- VISM fixed for 32 vertex test

Change 43237 on 2002/07/30 by vromaker@vromaker_r400_linux_marlboro

- temp fix to ptr buff to delay free_buff to SC
- comments in thread arb
- re-enabled alu interleaving

Change 42997 on 2002/07/29 by vromaker@vromaker_r400_linux_marlboro

- input arb now grants pix while pix is busy
```

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       - pism skips idle if request is present
- interleaving disabled in sq.v

Change 42996 on 2002/07/29 by vromaker@vromaker_r400_linux_marlboro

- fixed priority encoders (was reversed)

Change 42684 on 2002/07/26 by vromaker@vromaker_r400_linux_marlboro

- reverted valid_bits to go from lsb to msb

Change 42415 on 2002/07/25 by dougd@dougd_r400_linux_marlboro

added ati_rbbm_intf to complete the RBB_rd path

Change 42246 on 2002/07/24 by vromaker@vromaker_r400_linux_marlboro

- fixed thread_id width (caused 2nd pix vector to be same as 1st)

Change 42150 on 2002/07/24 by vromaker@vromaker_r400_linux_marlboro

- fixed ais_acs_rd_addr for synthesis

Change 42144 on 2002/07/24 by vromaker@vromaker_r400_linux_marlboro

- thread_id width fixes

Change 42107 on 2002/07/23 by markf@markf_r400_linux_marlboro

Updated SC->SQ interface

Change 42096 on 2002/07/23 by vromaker@vromaker_r400_linux_marlboro

- forced sq-tp pix_mask to 0xF

Change 42084 on 2002/07/23 by vromaker@vromaker_r400_linux_marlboro

- fixed SQ_SC interface connections

Change 42069 on 2002/07/23 by vromaker@vromaker_r400_linux_marlboro

- reversed order of valid_bits (aka pix_mask)

Change 41959 on 2002/07/23 by vromaker@vromaker_r400_linux_marlboro

- right shift 1 into MSB of valid_bit string (instead of left shift into LSB)

Change 41839 on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro
```

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- new, wider SC interface

Change 41838 on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro

delete

Change 41831 on 2002/07/22 by dougd@dougd_r400_linux_marlboro

added `include "../misc/sq_defs.v"

Change 41826 on 2002/07/22 by dougd@dougd_r400_linux_marlboro

changed parameter STATUS_WIDTH value from 4 to 16 to prevent compilation problems in
synthesis

Change 41823 on 2002/07/22 by dougd@dougd_r400_linux_marlboro

changed order of output declarations to come before their reg declarations so that
synopsys would not declare the outputs as wires

Change 41804 on 2002/07/22 by dougd@dougd_r400_linux_marlboro

created sq_rbbm_skid_buf with virage mem to replace ati_skid_buff

Change 41796 on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro

- make the thread_id width consistent at 6 bits (except at the state mem address port)
- updated the SQ_TP and TP_SQ interface (got rid of SQ_TP_clause_num)

Change 41748 on 2002/07/22 by vromaker@vromaker_r400_linux_marlboro

fixed state width for sythesis

Change 41592 on 2002/07/19 by vromaker@vromaker_r400_linux_marlboro

- interleaving is enabled
- fix for interleaving: cfs_type strap on ALU CFS 1 corrected to 2

Change 41459 on 2002/07/19 by vromaker@vromaker_r400_linux_marlboro

- more thread_id updates due to new location of thread_id in status register

Change 41453 on 2002/07/19 by vromaker@vromaker_r400_linux_marlboro

- ppb logic fix
       - fixed updated field position of thread_id w/in status (was causing
         a state_mem read address error since SMRA = winner[status[thread_id]]
```

```
Change 41326 on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro

- corrected exp_type for pix w/o z
- fixed cfs_export_id_q to load global_export_id_q only when allocating
- or'd more signals together in TIF to get a solid busy output

Change 41297 on 2002/07/18 by dougd@dougd_r400_linux_marlboro

fix typo in previous checkin

Change 41259 on 2002/07/18 by dougd@dougd_r400_linux_marlboro

intitial checkin of skid buffer used in sq_vism.v

Change 41218 on 2002/07/18 by dougd@dougd_r400_linux_marlboro

more changes to support synthesis

Change 41217 on 2002/07/18 by vromaker@vromaker_r400_linux_marlboro

- fixes for sq-sx export

Change 41188 on 2002/07/17 by efong@efong_crayola_linux_cvd

put in `endif

Change 40943 on 2002/07/16 by dougd@dougd_r400_linux_marlboro

original submission of virage memory *.ctmc files. The *.v files were modified to
support synthesis.

Change 40937 on 2002/07/16 by vromaker@vromaker_r400_linux_marlboro

- added alu_instr_pending status bit
- added new SQ_SX_exp and SQ_SX_free interfaces (free is not functional)

Change 40686 on 2002/07/15 by vromaker@vromaker_r400_linux_marlboro

- updated decode for exports to be the same as in the AIQ: this
  fixes extraneous GPR writes

Change 40659 on 2002/07/15 by vromaker@vromaker_r400_linux_marlboro

- added 2nd alu cfs update interface to thread buff
- state read addr now status_thread_id[winner] as it should have been
- reg'd cfs_phase in thread buff to match reg'd update data
```

Change 39972 on 2002/07/12 by vromaker@vromaker_r400_linux_marlboro

fixes for 2 pixel vectors

Change 39731 on 2002/07/11 by vromaker@vromaker_r400_linux_marlboro

fixes for 2 pix vectors

Change 39002 on 2002/07/09 by vromaker@vromaker_r400_linux_marlboro

misc

Change 38998 on 2002/07/09 by vromaker@vromaker_r400_linux_marlboro

temp file

Change 38997 on 2002/07/09 by vromaker@vromaker_r400_linux_marlboro

not sure - checked in due to clean up

Change 36278 on 2002/06/25 by dougd@dougd_r400_linux_marlboro

added input VGT_SQ_event; changed VGT_SQ_vsisr_double to VGT_SQ_vsisr_continued

Change 36192 on 2002/06/25 by dougd@dougd_r400_linux_marlboro

added connections and function to support SQ_RBBM_cntx17_busy & SQ_RBBM_cntx0_busy,
however, at this time both of these signals are the same

Change 36176 on 2002/06/25 by markf@markf_r400_linux_marlboro

Tied SQ_RBBM_nrtrtr to SQ_RBBM_rtr

Change 35120 on 2002/06/20 by vromaker@vromaker_r400_linux_marlboro

changes for latest emulator

Change 35005 on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro

more busy bits

Change 34969 on 2002/06/19 by vromaker@vromaker_r400_linux_marlboro

fix for CFI fetch (alloc had to update CFI ptr); added a few busy signals

Change 34833 on 2002/06/18 by vromaker@vromaker_r400_linux_marlboro

fix for wrong thread type

Change 34806 on 2002/06/18 by vromaker@vromaker_r400_linux_marlboro

took away 4 cycles of delay on pix_gpr_wr{addr, en}

Change 34778 on 2002/06/18 by vromaker@vromaker_r400_linux_marlboro

fix for pix shader alu instruction

Change 34632 on 2002/06/17 by dougd@dougd_r400_linux_marlboro

added a full subtract of the instruction store base address from the rbi_addr before
doing the divide by 3 to get the memory addr

Change 34631 on 2002/06/17 by vromaker@vromaker_r400_linux_marlboro

hack to delay SC input 16 cycles

Change 34606 on 2002/06/17 by dougd@dougd_r400_linux_marlboro

commented out the change made in the last version because it needs to be released at
the same time as another change in the sq to work properly

Change 34588 on 2002/06/17 by vromaker@vromaker_r400_linux_marlboro

added delays for SQ_SP_interp ctl and SQ_SP_gpr_write for interp data

Change 34547 on 2002/06/17 by dougd@dougd_r400_linux_marlboro

fixed bug in o_vector_valid where it was setting one too many bits.

Change 34539 on 2002/06/17 by vromaker@vromaker_r400_linux_marlboro

temp hack to param cache write addr and enable to move them out 1 cycle

Change 34347 on 2002/06/15 by vromaker@vromaker_r400_linux_marlboro

fixes for sending interp ctl to SX/SP

Change 34111 on 2002/06/14 by vromaker@vromaker_r400_linux_marlboro

got rid of temp hack

Change 34086 on 2002/06/14 by rbell@crayola_misc_linux

Fixed runsim to return rc no larger than 255.
Fixes for the full chip build

Change 34083 on 2002/06/14 by vromaker@vromaker_r400_linux_marlboro

sending correct export address in SP instruction

Change 34062 on 2002/06/14 by dougd@dougd_r400_linux_marlboro

replaced the v2k indexed part select implementation with muxes

Change 33977 on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro

changed polarity of exp_pix

Change 33940 on 2002/06/13 by vromaker@vromaker_r400_linux_marlboro

many updates... some v2k removal

Change 33853 on 2002/06/13 by rbell@rbell_crayola_sun_cvd

Had to create more "hacked" files...port mismatches. Must be fixed later

Change 33801 on 2002/06/13 by rbell@rbell_crayola_sun_cvd

Fixes/hacks to get the first chip integration compile to work.

Change 33723 on 2002/06/13 by dougd@dougd_r400_linux_marlboro

added context_valid from aluconst_top to sq_vism to enable/stall loading of control
packet from vgt until the alu constant store has been loaded for this state.

Change 33615 on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro

misc updates... alu_req logic updated in sq_status_reg

Change 33554 on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro

moved gpr_rd_en one cycle earlier for srcA

Change 33536 on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro

sending srcA gpr read addr one cycle earlier

Change 33519 on 2002/06/12 by dougd@dougd_r400_linux_marlboro

fix bug in o_context_valid being set correctly

Change 33509 on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro

fixed exporting bit by putting pred_sel bit in correctly

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Change 33492 on 2002/06/12 by vromaker@vromaker_r400_linux_marlboro

various updates - instr start asserted to SP

Change 33348 on 2002/06/11 by vromaker@vromaker_r400_linux_marlboro

fixed tex instruction read pointer

Change 33233 on 2002/06/11 by vromaker@vromaker_r400_linux_marlboro

SX exp added; tgt instr cnt from CFS to TIF fixed; alloc stuff added

Change 32898 on 2002/06/10 by vromaker@vromaker_r400_linux_marlboro

fixed sq-sp gpr_rd_en; changed "state" to "context_id" in instr pipes

Change 32795 on 2002/06/07 by vromaker@vromaker_r400_linux_marlboro

       more updates

Change 32774 on 2002/06/07 by dougd@dougd_r400_linux_marlboro

fix typo bug in last version

Change 32767 on 2002/06/07 by dougd@dougd_r400_linux_marlboro

added input i_vtb_rtr to complement o_v_ld_cntl_pkt to form handshake

Change 32678 on 2002/06/07 by dougd@dougd_r400_linux_marlboro

fix bug in address decode logic

Change 32472 on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro

       thread buff - arb interface updates

Change 32366 on 2002/06/06 by dougd@dougd_r400_linux_marlboro

initial checkin

Change 32295 on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro

commented out fsdbdumpmem

Change 32275 on 2002/06/06 by vromaker@vromaker_r400_linux_marlboro

updated tex instr const_index field to the new format
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Change 32269 on 2002/06/06 by dougd@dougd_r400_linux_marlboro

remove input register on i_texconst_phase to sync data xfer to sq

Change 32225 on 2002/06/06 by dougd@dougd_r400_linux_marlboro

fix bug in o_context_switch in sq_rbbm_interface and set map_copy_cntr to 3'd7 at reset
in sq_const_map_cntl

Change 32159 on 2002/06/05 by dougd@dougd_r400_linux_marlboro

add decode of gfx_draw_initiator to rbbm_interface to generate context switch to force
a map_copy operation in const_map_cntl

Change 32104 on 2002/06/05 by vromaker@vromaker_r400_linux_marlboro

connected SQ_TP_send to internal SQ_TP_vld

Change 31996 on 2002/06/05 by dougd@dougd_r400_linux_marlboro

o_v_grp_addr was being incremented 1 cycle too early. Fixed.

Change 31953 on 2002/06/05 by vromaker@vromaker_r400_linux_marlboro

updated texture pipe output format

Change 31884 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

initial checkin

Change 31883 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

fixed bug

Change 31880 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

changed the timing of the CP write to use the same non-registered input address mux as
the reads

Change 31875 on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro

updates

Change 31866 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

added connections to o_inst_base_vtx and o_inst_base_pix
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Change 31821 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

fix bug in previous version

Change 31818 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

removed register stage for address into RAM

Change 31805 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

connected o_is_data to read_data

Change 31700 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

changed <= to = in combinatorial blocks to satisfy Leda

Change 31699 on 2002/06/04 by dougd@dougd_r400_linux_marlboro

initial checkin of useful files

Change 31693 on 2002/06/04 by vromaker@vromaker_r400_linux_marlboro

updates

Change 31621 on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro

updates

Change 31586 on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro

updates

Change 31449 on 2002/06/03 by dougd@dougd_r400_linux_marlboro

made temporary fix (marked with FIXME comment) to continue using TP_SQ_clause_num in
the port list instead of the newer (replacement) TP_SQ_thread_id which was declared a
wire set to "0" to keep gc_test.v working.

Change 31428 on 2002/06/03 by dougd@dougd_r400_linux_marlboro

added tempory wire o_vs_base_set = o_vs_program_base_set;

Change 31427 on 2002/06/03 by dougd@dougd_r400_linux_marlboro

replaced i_cf_addr with i_alu0_cf_addr, i_alu1_cf_addr, i_tex_cf_addr and replaced
i_alu_phase with i_is_sub_phase.

Change 31389 on 2002/06/03 by vromaker@vromaker_r400_linux_marlboro
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updated

Change 31361 on 2002/06/02 by vromaker@vromaker_r400_linux_marlboro

updates

Change 31279 on 2002/05/31 by vromaker@vromaker_r400_linux_marlboro

updates

Change 31031 on 2002/05/31 by dougd@dougd_r400_linux_marlboro

added functionality for o_vs_first_thread

Change 30987 on 2002/05/30 by dougd@dougd_r400_linux_marlboro

added vs_instr_ptr, vs_resource and vs_first_thread as outputs from sq_vism

Change 30971 on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro

updates

Change 30816 on 2002/05/30 by vromaker@vromaker_r400_linux_marlboro

fixed blocking assignment on SQ_SP_gpr_wr_en

Change 30762 on 2002/05/29 by dougd@dougd_r400_linux_marlboro

fixed various bugs

Change 30562 on 2002/05/29 by vromaker@vromaker_r400_linux_marlboro

fixed input_sel output

Change 30559 on 2002/05/29 by vromaker@vromaker_r400_linux_marlboro

connected the gpr input mux sel

Change 30516 on 2002/05/29 by dougd@dougd_r400_linux_marlboro

added connection to gen_index_set output from sq_rbbm_interface

Change 30462 on 2002/05/28 by dougd@dougd_r400_linux_marlboro

o_v_gpr_we was "X" so hardwired o_v_gpr_we = 1'b1; as a temporary fix.

Change 30458 on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro
```

updates

Change 30340 on 2002/05/28 by dougd@dougd_r400_linux_marlboro

wired up outputs from new registers to old versions of same outputs. This is tempory
until we switch over completely to the new register spec.

Change 30289 on 2002/05/28 by dougd@dougd_r400_linux_marlboro

added output "o_context_switch" to sq_rbbm_interface and connected it to
sq_aluconst_top and sq_texconst_top in sq.v
<enter description here>

Change 30286 on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro

removing from tis

Change 30284 on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro

moved file from tis to cfs

Change 30282 on 2002/05/28 by vromaker@vromaker_r400_linux_marlboro

updates...

Change 30159 on 2002/05/27 by vromaker@vromaker_r400_linux_marlboro

updates

Change 30053 on 2002/05/24 by dougd@dougd_r400_linux_marlboro

rbi_acs_rts was wired to both o_aluconst_rts and o_texconst_rts from sq_rbbm_interface:
fixed

Change 30048 on 2002/05/24 by vromaker@vromaker_r400_linux_marlboro

checkpoint update

Change 30021 on 2002/05/24 by dougd@dougd_r400_linux_marlboro

extended duration of i_map_copy_active to hold rtr inactive 1 more tick to allow pa to
be allocated.

Change 29966 on 2002/05/24 by dougd@dougd_r400_linux_marlboro

changed include file

Change 29948 on 2002/05/24 by dougd@dougd_r400_linux_marlboro

sq_rbbm_interface supports both old and new register `defines and has all the new state registers. sq.v instantiates this sq_rbbm_interface.

Change 29802 on 2002/05/23 by dougd@dougd_r400_linux_marlboro

fixed various bugs

Change 29768 on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro

initial version

Change 29767 on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro

updates

Change 29750 on 2002/05/23 by vromaker@vromaker_r400_linux_marlboro

updates.. now has clk and reset inputs...

Change 29311 on 2002/05/21 by vromaker@vromaker_r400_linux_marlboro

added SQ_CTL_PKT_WIDTH back in

Change 29136 on 2002/05/20 by vromaker@vromaker_r400_linux_marlboro

updates...

Change 28916 on 2002/05/17 by vromaker@vromaker_r400_linux_marlboro

new sq files for clause-less state management : initial, not complete, versions

Change 28866 on 2002/05/17 by dougd@dougd_r400_linux_marlboro

minor logic fixes

Change 28533 on 2002/05/16 by dougd@dougd_r400_linux_marlboro

tempory use to allow compile until new register spec is implemented.

Change 28531 on 2002/05/16 by dougd@dougd_r400_linux_marlboro

added temporary include of ../sq_reg_old.v to allow compile until the new register spec is implemented

Change 27919 on 2002/05/14 by dougd@dougd_r400_linux_marlboro

this is the old register spec which is needed while we are still using rtl based on this spec

Change 27917 on 2002/05/14 by dougd@dougd_r400_sun_marlboro

changed `include "register_addr.v to `include "../sq_register_addr.v to allow compilation of rtl based on old register spec

Change 27837 on 2002/05/14 by dougd@dougd_r400_linux_marlboro

added prefix sq_ to module and file name

Change 27828 on 2002/05/14 by vromaker@vromaker_r400_linux_marlboro

added fifo_regs_ctl to sq/misc

Change 27332 on 2002/05/10 by dougd@dougd_r400_sun_marlboro

added a divide by 3 to the incoming RBI address to generate the correct instruction memory address

Change 27179 on 2002/05/09 by dougd@dougd_r400_sun_marlboro

changed size of outputs o_inst_base_vtx and o_inst_base_pix from 8x because they are not state(context) registers

Change 27099 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

added outputs for the initial set of state registers in sq.v

Change 27093 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

changed the values assigned to i_is_phase

Change 27092 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

added sq_ as prefix to module and file names

Change 27088 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

added sq_ as prefix to module and file

Change 27087 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

added sq_ prefix to module and file names

Change 27050 on 2002/05/08 by vromaker@vromaker_r400_linux_marlboro

```
       updates

Change 26913 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

this module was renamed to sq_instruction_store.v

Change 26907 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

this file was renamed to sq_vism.v

Change 26905 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

changed some IO names

Change 26903 on 2002/05/08 by dougd@dougd_r400_sun_marlboro

changed module name from vism to sq_vism. changed some IO names.

Change 26852 on 2002/05/07 by dougd@dougd_r400_sun_marlboro

renamed module from is.v to sq_instruction_store.v

Change 26785 on 2002/05/07 by dougd@dougd_r400_sun_marlboro

initial version is incomplete and in development.

Change 26731 on 2002/05/07 by vromaker@vromaker_r400_linux_marlboro

delete

Change 26729 on 2002/05/07 by vromaker@vromaker_r400_linux_marlboro

delete

Change 26726 on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro

submitting all...

Change 26717 on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro

sadf

Change 26716 on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro

        asdf

Change 26713 on 2002/05/07 by vromaker@vromaker_r400_sun_marlboro
```

```
       asdf

Change 26584 on 2002/05/06 by dougd@dougd_r400_sun_marlboro

added outputs o_vism_busy (to arbiter) and o_sp_vsr_read to shader pipe to control
reading VSR during GPR loading. Removed input i_gpr_phase_mux as it was unused.

Change 26219 on 2002/05/03 by dougd@dougd_r400_sun_marlboro

initial submit for sq/vism rtl

Change 26218 on 2002/05/03 by dougd@dougd_r400_sun_marlboro

initial submit for sq/is rtl

Change 26217 on 2002/05/03 by dougd@dougd_r400_sun_marlboro

initial submit for sq/cfc rtl

Change 26216 on 2002/05/03 by dougd@dougd_r400_sun_marlboro

initial submit for sq/texconst rtl

Change 26214 on 2002/05/03 by dougd@dougd_r400_sun_marlboro

initial submit for sq/aluconst rtl

Change 26208 on 2002/05/03 by dougd@dougd_r400_sun_marlboro

intitial submit.

Change 25779 on 2002/05/01 by vromaker@vromaker_r400_sun_marlboro

latest updates

Change 25625 on 2002/04/30 by vromaker@vromaker_r400_sun_marlboro

       updates

Change 25183 on 2002/04/26 by vromaker@vromaker_r400_sun_marlboro

file updates

Change 24711 on 2002/04/24 by vromaker@vromaker_r400_sun_marlboro

ping-pong buffer (ctl and storage, width parameterized)

Change 24469 on 2002/04/23 by vromaker@vromaker_r400_sun_marlboro
```

```
mux to select gfx register data based on state (context)

Change 24081 on 2002/04/19 by vromaker@vromaker_r400_sun_marlboro

initial versions

Change 23514 on 2002/04/16 by vromaker@vromaker_r400_sun_marlboro

updating with latest versions

Change 21716 on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro

update

Change 21714 on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro

update

Change 21642 on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro

SP_TP_const to 48 bits

Change 21626 on 2002/04/03 by vromaker@vromaker_r400_sun_marlboro

latest fixes

Change 21468 on 2002/04/02 by vromaker@vromaker_r400_sun_marlboro

more fixes

Change 21425 on 2002/04/02 by vromaker@vromaker_r400_sun_marlboro

latest fixes

Change 21081 on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro


Change 21079 on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro

initial version

Change 21075 on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro

initial version

Change 21074 on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro
```

```
update

Change 21073 on 2002/03/29 by vromaker@vromaker_r400_sun_marlboro

initial version

Change 20660 on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro

module name updated to sq

Change 20657 on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro

position_space -> pos_avail, buffer_space -> buf_avail

Change 20655 on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro

added SQ_TP_type, SQ_TP_send, un_TP_SQ_type, TP_SQ_rdy

Change 20654 on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro

un_SQ_TP_pmask -> un_SQ_TP_pix_mask (for n = 0..3)

Change 20652 on 2002/03/27 by vromaker@vromaker_r400_sun_marlboro

latest version - renamed from sequencer_top.v

Change 19789 on 2002/03/20 by vromaker@vromaker_r400_sun_marlboro

re-added SQ_SP_ijline, fixed SP_TP instr and const widths

Change 19752 on 2002/03/20 by vromaker@vromaker_r400_sun_marlboro

put SQ_SP_stall back in

Change 19726 on 2002/03/20 by vromaker@vromaker_r400_sun_marlboro

updates

Change 19653 on 2002/03/19 by vromaker@vromaker_r400_sun_marlboro

updated sq top

Change 18260 on 2002/03/08 by vromaker@vromaker_r400_sun_marlboro

initial version

Change 18257 on 2002/03/08 by vromaker@vromaker_r400_sun_marlboro
```

```
initial version

Change 18256 on 2002/03/08 by vromaker@vromaker_r400_sun_marlboro

initial version

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 10805 on 2001/11/27 by vromaker@vic_r400_src

added some signals and changed a few signal names in an attempt to be more consistent
across all sq interfaces

Change 10432 on 2001/11/20 by askende@andi_r400

more interface related updates

Change 9921 on 2001/11/14 by askende@andi_r400

first time check-in

Change 9462 on 2001/11/07 by mmantor@mmantor_r400

new
```

Change 54251 on 2002/09/29 by mmantor@mmantor_r400_win

added sc_rbiu read back bus hook up with it forced to zero at reset

Change 54245 on 2002/09/29 by mmantor@mmantor_r400_win

one more leda error fix

Change 54244 on 2002/09/29 by mmantor@mmantor_r400_win

misc error

Change 54243 on 2002/09/29 by mmantor@mmantor_r400_win

typo error assign

Change 54242 on 2002/09/29 by mmantor@mmantor_r400_win

output assigned multiple times

Change 54241 on 2002/09/29 by mmantor@mmantor_r400_win

fixed bit widths

Change 54222 on 2002/09/28 by mmantor@mmantor_r400_win

corrected some sensitivity list

Change 54127 on 2002/09/27 by mmantor@mmantor_r400_win

fixed a sp_ij_buf_cnt bug and added multi pass pixel vector processing capability

Change 54057 on 2002/09/27 by mmantor@mmantor_r400_win

prevent a free_buf from happening until both the sq and sp had a pv buffer in use.

Change 54047 on 2002/09/27 by mmantor@mmantor_r400_win

fixed prim_data reset width assignment

Change 54036 on 2002/09/27 by rramsey@RRAMSEY_P4_r400_win

Update status

Change 53822 on 2002/09/26 by rramsey@RRAMSEY_P4_r400_win

Update status

```
Change 53794 on 2002/09/26 by rramsey@RRAMSEY_P4_r400_win

Update with status from sept 26

Change 53788 on 2002/09/26 by rramsey@RRAMSEY_P4_r400_win

Clean up pasc dump file (only used in standalone sc)
Fix bugs in supertile discard prim logic
Fix compile warning in itercmdfifo

Change 53777 on 2002/09/26 by donaldl@fl_donaldl_p4

Merged with previous revs.

Change 53776 on 2002/09/26 by donaldl@donaldl_crayola_unix_orl

Expanded event_id to 5 bits.

Change 53774 on 2002/09/26 by donaldl@fl_donaldl_p4

Update with latest changes to real-time stream registers:  separated z_min & z_max,
expanded prim_type to 3 bits, and added zy_max.

Change 53773 on 2002/09/26 by donaldl@fl_donaldl_p4

Expanded event_id to 5 bits.

Change 53772 on 2002/09/26 by donaldl@fl_donaldl_p4

Update with latest changes to real-time stream registers:  separated z_min & z_max,
expanded prim_type to 3 bits, and added zy_max.

Change 53665 on 2002/09/25 by mmantor@mmantor_r400_win

fixed prim type with the real time flag being sent to sq and some sensitivity list and
width mismatch issues

Change 53580 on 2002/09/25 by rramsey@RRAMSEY_P4_r400_win

Add SuperTile state to sc_rbiu, sc_state, and top level
Add SuperTileDiscardPrim logic to sc_pipe
Add SuperTileDiscardTile logic to sc_quadmask
Increase event_id to 5 bits through quadmask
Increase event_id to 5 bits for all top level signals

Change 53510 on 2002/09/25 by kmeekins@kmeekins_crayola_unix_orl

Expanded the event_id to 5 bits.
```

Change 53508 on 2002/09/25 by donaldl@donaldl_crayola_unix_orl

Added real-time stream inputs.

Change 53506 on 2002/09/25 by mmantor@mmantor_r400_win

made event id 5 bits from qpp_proc to the back of SC and changed csim dumps for the whole sc

Change 53501 on 2002/09/25 by rramsey@RRAMSEY_P4_r400_win

Add mux for rts/non-rts primdata

Change 53400 on 2002/09/24 by mmantor@mmantor_r400_win

restructured the sc_iter.v to skew outputs of sp and sq/sx and put fifo in for sq/sx delay, updated the busy logic along with the delay for sp buffer decrement and new sp buffer management currently limited to two buffer usage and new signal to the sq for vism arbiter to wait until sp ij buffers have data.

Change 53159 on 2002/09/23 by kmeekins@kmeekins_crayola_unix_orl

Corrected the e2 equations to use the new formats for the deltas that
now have 8 fractional bits instead of 4.

Change 53135 on 2002/09/23 by donaldl@fl_donaldl_p4

Storage register for real-time stream data.

Change 53121 on 2002/09/23 by donaldl@fl_donaldl_p4

Removed top level muxing of real-time stream data.

Change 53119 on 2002/09/23 by donaldl@fl_donaldl_p4

Added real-time stream inputs.

Change 53080 on 2002/09/23 by donaldl@fl_donaldl_p4

Added support for real-time streams.

Change 53079 on 2002/09/23 by donaldl@donaldl_crayola_unix_orl

Piped rt_valid through.

Change 53078 on 2002/09/23 by donaldl@donaldl_crayola_unix_orl

```
Cleaned up real-time streams to match emulator.

Change 53066 on 2002/09/23 by rramsey@RRAMSEY_P4_r400_win

Disable some more field compares on event transfers
Change pa_sc input method to allow tb to make decisions based on prim/event read from
suscan
Add EVENT_WITHOUT_CONTEXT_ENABLE parameter to tb_sc, default is 1
Add BACKPRESSURE_ENABLE parameter to tb_sc, default is 1

These changes allow tb_sc to pass events through the sc without loading state so we can
verify events are truly context independent (except vizq_start/end)

Change 53033 on 2002/09/23 by rramsey@RRAMSEY_P4_r400_win

Rework some logic to improve timing in stage_reg
Change logic on pre_prim_we from MUX to AND gates so first prim is defined (clip_prim
was undefined at rst, which caused an x to propogate out to prim_we)
Clean up compile warning in z_fifo

Change 53010 on 2002/09/23 by kmeekins@kmeekins_r400_win

Selected r400su_baryc_test_03

Change 52774 on 2002/09/20 by rramsey@RRAMSEY_P4_r400_win

Update some status

Change 52773 on 2002/09/20 by rramsey@RRAMSEY_P4_r400_win

Add some intermediate signals to fix a crash in modelsim

Change 52720 on 2002/09/20 by rramsey@RRAMSEY_P4_r400_win

Couple of fixes for bbfract and fill_rule covered determinations

Change 52708 on 2002/09/20 by rramsey@RRAMSEY_P4_r400_win

Update with status from the 19th

Change 52567 on 2002/09/19 by smoss@smoss_crayola_linux_orl_regress

   New dump files

Change 52551 on 2002/09/19 by rramsey@RRAMSEY_P4_r400_win

Clean up RTS data in the SC
Change sc_walker so that hw_scissor is passed down instead of recalculated in the
```

```
walker
Remove registry check for covered edge bias fix, it's always on now
Add covered edge bias fix to RTL (sc_pipe)
Clean up some compile warnings in the qpp
Add some documentation on line_stipple

Change 52408 on 2002/09/18 by kmeekins@kmeekins_r400_win

Selected r400sc_line_expand_width_msaa_8_01.

Change 52400 on 2002/09/18 by kmeekins@kmeekins_r400_win

Disabled compare of edge values (E0y, E0, E1x, E1, E2x, and E2) during "Event".

Change 52319 on 2002/09/18 by rramsey@RRAMSEY_P4_r400_win

clean up some compiler warnings

Change 52273 on 2002/09/18 by rramsey@RRAMSEY_P4_r400_win

Add rect_v1,2,3 to sc_sq primtype remapping

Change 52267 on 2002/09/18 by kmeekins@kmeekins_r400_win

Removed all clock-to-Q delays on register assignments because the synthesis
tools/scripts are too dumb to figure out clever techniques to make debugging easier.

Change 52137 on 2002/09/17 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Add Rect V1-V3 support to HW

Change 52127 on 2002/09/17 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Fix Viz Query State to be hooked up to qdpr_proc

Change 52080 on 2002/09/17 by kmeekins@kmeekins_crayola_linux_orl

Cleaned up the errors/warnings reported by running "leda".
Moved the clock-to-Q delay macro to a compiler directive to remove synthesis warnings.

Change 52075 on 2002/09/17 by rramsey@RRAMSEY_P4_r400_win

Add tracker for vizq

Change 52069 on 2002/09/17 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Update Real-Time Stream Misc register fields for correct width.
Fix Inf/NaN handling bugs in both Emu and H/W for SC Baryc.
```

```
Delete "old" sc_baryc.mc to prevent confusion.

Change 51961 on 2002/09/17 by rramsey@RRAMSEY_P4_r400_win

Hook up detail mask context_id input to qpp output (instead of qpp state lookup signal)
Add some signal declarations to clean up compiler warnings

Change 51821 on 2002/09/16 by rramsey@RRAMSEY_P4_r400_win

Add missing signals to sensitivity list

Change 51797 on 2002/09/16 by mmantor@mmantor_r400_win

fixed sc dump for dumping of sc_sp xyface data
enabled center/centroid/xyface output of sc hardware
changed scrcc interface to ignore msaa_en for event tiles

Change 51749 on 2002/09/16 by rramsey@RRAMSEY_P4_r400_win

Disable compares of tile-level bounding boxes for events (cw and qm outputs)
Add compare for covered at qm output
Add placeholder for RTS flag at qm output

Change 51712 on 2002/09/16 by donaldl@fl_donaldl_p4

Added write_confirm logic.

Change 51706 on 2002/09/16 by donaldl@fl_donaldl_p4

Added write_confirm logic

Change 51702 on 2002/09/16 by donaldl@fl_donaldl_p4

Added write_confirm logic

Change 51699 on 2002/09/16 by donaldl@donaldl_crayola_unix_orl

Add write_confirm logic.

Change 51492 on 2002/09/13 by mmantor@mmantor_r400_win

added backface to packer output dump and connected through the iterator as well as
packer tracker.

Change 51478 on 2002/09/13 by rramsey@RRAMSEY_P4_r400_win

Add pattern_order to stipple mask logic
```

```
Change 51427 on 2002/09/13 by rramsey@RRAMSEY_P4_r400_win

Update stipple test status, now working on r400sc_polygon_stipple_01

Change 51371 on 2002/09/13 by kmeekins@kmeekins_r400_win

Selected the r400sc_bres_cntl_04 test.

Change 51365 on 2002/09/13 by kmeekins@kmeekins_r400_win

Added the logic for generating the context 0 and context 1 to 7 busy
signals. Modified the dump files to facilitate testing of the busy
signals.

Change 51360 on 2002/09/13 by kmeekins@kmeekins_r400_win

sc_detail_mask_accum:
- added logic for determining context 0 and context 1 to 7 busy
- added three new I/O signals for teh busy logic

sc:
- connected new sc_detail_mask_accum I/O to sc_iter and sc_qdpr_proc

sc_iter:
- or'ed in the sc_detail_mask_accum busy signals to the
  pkr_iter_cntx0_busy and the pkr_iter_cntx1to7_busy signals
- added the sc_detail_mask_accum busy signals to the I/O

Change 51342 on 2002/09/13 by rramsey@RRAMSEY_P4_r400_win

Update status w/ pipe.bvrl fix

Change 51337 on 2002/09/13 by rramsey@RRAMSEY_P4_r400_win

Zero out max_sample_dist output if aa (jss or ms) is not enabled

This fixes r400sc_point_list_09, and probably others mismatching on sc_rcc_covered

Change 51318 on 2002/09/13 by rramsey@RRAMSEY_P4_r400_win

Update with regression results from 9/12/2002

Change 51185 on 2002/09/12 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Fix SC HW to not filter out events from RB or downstream blocks

Change 51175 on 2002/09/12 by mmantor@mmantor_r400_win
```

```
added state data for the implementation of xyface, centers, multipass pixel shaders.
added delay for free buff signal and early sp_pv_cnt for sc to sq interface timing
changes.

Change 51070 on 2002/09/12 by rramsey@RRAMSEY_P4_r400_win

Update status

Change 51039 on 2002/09/12 by rramsey@FL_RAMSEY_r400_win

sc_walker.cpp:
Fix tileMod3 calc to match hardware for tiles outside of window
Remove check that kept nullprims from flipping the tile BB
sc_coarse_walker.mc,bvrl:
Fix bit width on stipple curr x/y
Add check to flip tile BB if tile is outside of draw window

Change 50960 on 2002/09/12 by bbuchner@fl_bbuchner_r400_win

change dumpfile path

Change 50885 on 2002/09/11 by grayc@grayc_crayola_linux_orl

   file needed for leda

Change 50815 on 2002/09/11 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Moved 6-Sample MSAA Sample #2 location from ULC-rel 2,5 to 1,5 to alleviate degen tri
in texture lod computations. (HW and EMU and fixed 1 test).

Change 50797 on 2002/09/11 by rramsey@RRAMSEY_P4_r400_win

Add viz_query stuff to sc rtl
vq state data is driven with temps for now (regs don't seem to get loaded)

Change 50750 on 2002/09/11 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Added Centers/XY support to baryc block.
Reduced baryc quad_x,y from 13 bits to 12 bits which is correct.
Updated associated testbench.

Change 50748 on 2002/09/11 by rramsey@RRAMSEY_P4_r400_win

Fix an fpos conflict hang condition (inputs switch to new prim data with fpos, but no
valid quads)
Make end_of_prim logic match csim

This fixes r400vgt_hos_auto_index_quad_list_01 , and hopefully the other failing HOS
```

tests

Change 50714 on 2002/09/11 by mmantor@mmantor_r400_win

added sc_sample_cntl from state block to iter and fixed a sensitivity list problem

Change 50664 on 2002/09/10 by mmantor@mmantor_r400_win

added xyface data piped through the baryc pipe and added centers generation control to the bc pipe. xyface data still requires more changes before it works completely

Change 50452 on 2002/09/10 by rramsey@rramsey_crayola_unix_orl

Add second BB input and change usage for wind/prim BB's

Change 50450 on 2002/09/10 by rramsey@RRAMSEY_P4_r400_win

Fix signed/unsigned compare problem in coarse_walker by making x/y_curr values signed
Clean up stipple state
Fix stipple_cnt and stipple_ptr logic in coarse_walker
Add second BB input to quadmask

Change 50215 on 2002/09/09 by donaldl@fl_donaldl_p4

Merged version.

Change 50211 on 2002/09/09 by donaldl@donaldl_crayola_unix_orl

Increased by 1 the bit widths for x/y min/max and x/y current signals.

Change 50208 on 2002/09/09 by viviana@viviana_r400_win

Added Vivian to debugging r400su_triarea_test_03.

Change 50207 on 2002/09/09 by donaldl@donaldl_crayola_unix_orl

Increased by 1 the bit widths for x/y min/max and x/y current signals.

Change 50205 on 2002/09/09 by donaldl@fl_donaldl_p4

Added new scissor bounding box (ie. 2nd scissor x/y min/max values) and expanded bit widths for them and x/y current signals.

Change 49989 on 2002/09/06 by viviana@viviana_r400_win

Added vivian to the r400su_triarea_test_02 for debugging.

Change 49961 on 2002/09/06 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

```
Make MPASS_PIX_VEC_PER_PASS 20 bits since SQ auto-inc cannot be any bigger due to FltPt
restrictions.
Add PA_SC_CNTL_STATUS.MPASS_OVERFLOW status flag.
Changed name and added new event for controlling MPASS pixel shaders
and SQ vertex and pixel counters.
Added SC->CP VizQuery and MP PixShader dumps.
Made window_offset register fields 15 bits instead of 16.
Added SC MP PixShader logic.
Added new signal to SC->SQ interface to prevent incrementation of pixel count for
"discarded" MP Pix Shader Pixel Vectors.
Fixed MSAA bug where samples 4-7 were not being set to 0 when MSAA was disabled.  Fixed
both EMU and RTL.

Change 49953 on 2002/09/06 by rramsey@RRAMSEY_P4_r400_win

SC_STANDALONE
  Update standalone with msb addition for walker dumps

Change 49812 on 2002/09/05 by rramsey@RRAMSEY_P4_r400_win

Rework stipple logic to bring in timing

Change 49746 on 2002/09/05 by rramsey@RRAMSEY_P4_r400_win

Working on sc_sq miscompare

Change 49721 on 2002/09/05 by kmeekins@kmeekins_crayola_unix_orl

Forgot to submit the changes. See changelog 49701.

Change 49701 on 2002/09/05 by kmeekins@kmeekins_crayola_unix_orl

Changed dye2_ge_0 to an unsigned bit to get correct .bvrl.
Corrected logic for determining what quad row/columns to include in quad covered.

Change 49696 on 2002/09/05 by smoss@smoss_crayola_win

d is not c

Change 49676 on 2002/09/05 by viviana@viviana_crayola_linux_orl

       Changed the generation of max_grad so that the sign bit is zero.  Also,
       changed the sc_fp_mult for sc_zmult_se8m23_se8m23 which is Clay's
       multiplier used in the sc_baryc_ij.mc.

Change 49673 on 2002/09/05 by viviana@viviana_crayola_linux_orl
```

```
Changed the generation of max_grad so that the sign bit is zero.  Also,
   changed the sc_fp_mult for sc_zmult_se8m23_se8m23 which is Clay's multiplier
   used in sc_baryc_ij.mc.

Change 49640 on 2002/09/05 by donaldl@fl_donaldl_p4

Refix non-collapseable pipe.  The previous merge corrupted it.

Change 49639 on 2002/09/05 by donaldl@donaldl_crayola_unix_orl

Refix non-collapseable pipe.  The previous merge corrupted it.

Change 49620 on 2002/09/05 by rramsey@RRAMSEY_P4_r400_win

Change bit_cnt logic to use mc block to (hopefully) fix timing

Change 49617 on 2002/09/05 by rramsey@RRAMSEY_P4_r400_win

Remove clk directive, increase sum output to 5 bits

Change 49615 on 2002/09/05 by rramsey@rramsey_crayola_unix_orl

Try using MC to fix a timing problem through an adder

Change 49574 on 2002/09/04 by smoss@smoss_crayola_win

SU test

Change 49550 on 2002/09/04 by donaldl@fl_donaldl_p4

To get real-time changes working (1st pass).  Changed output delay for oRT_VALID.

Change 49514 on 2002/09/04 by kmeekins@kmeekins_r400_win

Well, what about this one...?

Change 49476 on 2002/09/04 by kmeekins@kmeekins_r400_win

r400sc_diamond_exit_05

Change 49472 on 2002/09/04 by donaldl@donaldl_crayola_unix_orl

Changed output delay for oRT_VALID

Change 49464 on 2002/09/04 by donaldl@donaldl_crayola_unix_orl

Fixed typo for flipped_elat1 equation.
```

Change 49463 on 2002/09/04 by donaldl@donaldl_crayola_unix_orl

To get real-time streams working and fix non-collapseable pipe.

Change 49461 on 2002/09/04 by donaldl@fl_donaldl_p4

To support changes in sc_quadmask and get real-time streams working.

Change 49460 on 2002/09/04 by donaldl@fl_donaldl_p4

Removed st_max_sample_dist_out[3:0].

Change 49459 on 2002/09/04 by donaldl@fl_donaldl_p4

Comment out real-time until all integrated.

Change 49458 on 2002/09/04 by kmeekins@kmeekins_r400_win

Fixing r400sc_line_aa_shader_01.

Change 49457 on 2002/09/04 by donaldl@fl_donaldl_p4

Added real-time stream compares.

Change 49456 on 2002/09/04 by kmeekins@kmeekins_crayola_unix_orl

Fixed quadcovered mask for Bottom quads with Max sample distance and
bounding box fractional bits set to full range.

Change 49454 on 2002/09/04 by kmeekins@kmeekins_r400_win

Enabled checking of covered quads mask.

Change 49450 on 2002/09/04 by viviana@viviana_crayola_unix_orl

Signed up for the poly offset first test failure.

Change 49432 on 2002/09/04 by rramsey@RRAMSEY_P4_r400_win

Update with Steve's latest status, 92% passing now!

Change 49370 on 2002/09/03 by rramsey@RRAMSEY_P4_r400_win

Only send 1clk transfer for fpos if it hasn't already been sent with a row

Change 49347 on 2002/09/03 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Fix bb_frac mask with JSS bug in HW.

```
Change 49320 on 2002/09/03 by ctaylor@fl_ctaylor_r400_win_marlboro

working jss point test with frac mask.

Change 49294 on 2002/09/03 by rramsey@RRAMSEY_P4_r400_win

Update status

Change 49283 on 2002/09/03 by rramsey@RRAMSEY_P4_r400_win

tracking spreadsheet to coordinate debugging efforts

Change 49261 on 2002/09/03 by rramsey@RRAMSEY_P4_r400_win

Fix state select for cliprect_enable
Add some debug prim counters to tb_sc
Reset rbbm signals during SRST

Change 49260 on 2002/09/03 by viviana@viviana_crayola_unix_orl

Ran the file through a dos2unix command to remove dos carriage return characters.

Change 49101 on 2002/08/30 by kmeekins@kmeekins_crayola_unix_orl

Corrected floating point multiply.
Adjusted latencies to match new input sources.

Change 49091 on 2002/08/30 by kmeekins@kmeekins_crayola_unix_orl

Changed index used to determine overflow condition for exponent addition.

Change 49085 on 2002/08/30 by mmantor@mmantor_r400_win

rest of the change for fpos

Change 49080 on 2002/08/30 by mmantor@mmantor_r400_win

fixed a bug with the fpos signal

Change 49070 on 2002/08/30 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Fixed register delay bug with prim_type (and xmajor) from yesterday fix.

Change 49052 on 2002/08/30 by rramsey@RRAMSEY_P4_r400_win

Fix context-related bug that was causing tb to hang
```

```
Change 49044 on 2002/08/30 by rramsey@RRAMSEY_P4_r400_win

Fix polarity on watchdog check for freeze signal

Change 49023 on 2002/08/30 by rramsey@RRAMSEY_P4_r400_win

Changes to sc RTL to get line stipple working
  Should pass stipple tests as long as the line is not scissored

This coarse_walker mc code uses the collapsible pipeline which fixes a bug,
but probably does not meet timing

Change 48779 on 2002/08/29 by ctaylor@ctaylor_crayola_unix_orl

Fixed missing output assignments of poly_offset scale/offset register selects.

Change 48777 on 2002/08/29 by ctaylor@ctaylor_crayola_unix_orl

Fixed typo bug where tile_x[9] was used to add 4096 to tile_y instead of tile_y[9].

Change 48736 on 2002/08/29 by rramsey@RRAMSEY_P4_r400_win

Turn rcc trackers back on so we can debug z problems
Connect z state select to cw_state_id
Connect tilex/tiley inputs to z block to coarsewalker outputs
Fix latency for tilex/tiley outputs
Make quadmask mc match bvrl (latency = 3)

Change 48708 on 2002/08/29 by kmeekins@kmeekins_r400_win

Changed the state id for the z_interp states to use the id from the quadmask and not
the Z FIFO.

Change 48687 on 2002/08/28 by rramsey@RRAMSEY_P4_r400_win

Back out the coarse_walker change to make the pipe non-collapsible, it was causing
tests to fail
Fix comment in zfifo so it's identified correctly on overflow
Disable sc_rcc compares until we can get things ironed out

Change 48654 on 2002/08/28 by kmeekins@kmeekins_crayola_unix_orl

Changed QM latency to 3.

Change 48625 on 2002/08/28 by kmeekins@kmeekins_crayola_unix_orl

Increased QM latency to 3.
```

```
Change 48615 on 2002/08/28 by ctaylor@ctaylor_crayola_unix_orl

       Add logic for vertex 3 determination for reference vert for lines/points/rects

Change 48608 on 2002/08/28 by rramsey@RRAMSEY_P4_r400_win

Updates to sc RTL to get state/event/event_id routed through qpp/pkr/iterator
Adding line stipple to coarse_walker.mc and quadmask.mc
Change sc_quadmask latency to 3

Z is still mismatching
cliprect tests are broken again

Change 48591 on 2002/08/28 by kmeekins@kmeekins_crayola_unix_orl

Fixed delta_xy to match emulator.
Reduced the dz/dx and dz/dy gradients to 32 bits before determining the max_grad.

Change 48571 on 2002/08/28 by grayc@grayc_crayola_linux_orl

   temp fix to zero the block read data

Change 48536 on 2002/08/28 by kmeekins@kmeekins_crayola_unix_orl

Added the quadcovered functionallity.

Change 48534 on 2002/08/28 by kmeekins@kmeekins_crayola_unix_orl

Increased the quadmask latency to account for the quadcovered operations.

Change 48533 on 2002/08/28 by kmeekins@kmeekins_crayola_unix_orl

Changed wires to signed to get correct sign extension.
Modified clamp to work with negative values.

Change 48528 on 2002/08/28 by kmeekins@kmeekins_r400_win

Removed max_sample_dist from getting passed into the tile fifo.

Change 48524 on 2002/08/28 by kmeekins@kmeekins_r400_win

Expanded dz/dx and dz/dy into the z_interp.
Added the quadcovered mask.

Change 48509 on 2002/08/28 by donaldl@fl_donaldl_p4

Updated to match latest compare dump files.
```

Change 48504 on 2002/08/28 by donaldl@fl_donaldl_p4

Updated to match latest compare dump files.

Change 48502 on 2002/08/28 by donaldl@fl_donaldl_p4

1. Remove state_id[2:0] and event_id[3:0] from prim fifo.

2. Remove state_id[2:0] from z fifo.

3. Pipe down state_id[2:0], event, st_max_sample_dist[3:0], x_major from sc_pipe to tile fifo.

4. Increase bit widths (ie. lsbs) of edge distances going from sc_pipe to sc_coarse_walker to tile fifo.

Change 48498 on 2002/08/28 by donaldl@fl_donaldl_p4

Changed data widths on prim fifo data, z fifo data, and tile fifo data to account for removing/adding event, event_id[3:0], and state_id[2:0].

Change 48494 on 2002/08/28 by donaldl@fl_donaldl_p4

Pipe down x_major, state_id[2:0], and st_max_sample_dist[3:0].

Also for sc_coarse_walker, first cut at real-time streams.

Change 48490 on 2002/08/28 by donaldl@donaldl_crayola_unix_orl

Pipe down x_major, state_id[2:0], and st_max_sample_dist[3:0].
Also for sc_coarse_walker, first cut at real-time streams.

Change 48488 on 2002/08/28 by donaldl@fl_donaldl_p4

Removed state_var_indx[2:0] going to Z fifo.

Change 48483 on 2002/08/28 by donaldl@donaldl_crayola_unix_orl

Remove state_var_indx[2:0] to Z fifo.

Change 48370 on 2002/08/27 by ctaylor@ctaylor_crayola_unix_orl

Update new AA sample locations.

Change 48353 on 2002/08/27 by rramsey@rramsey_crayola_unix_orl

Tighten timing on pixelmask outputs

Change 48337 on 2002/08/27 by rramsey@RRAMSEY_P4_r400_win

Register inputs to help break sc critical path

Change 48331 on 2002/08/27 by rramsey@rramsey_crayola_unix_orl

Tighten output constraints on pixelmask outputs to help with packer timing

Change 48321 on 2002/08/27 by rramsey@RRAMSEY_P4_r400_win

Update tb_sc random script and config file to use $WORK_ROOT env variable to determine path info
(default of c: is used if $WORK_ROOT is not set). This means paths in cfg files should start with "/" instead of "c:/" or "d:/" and the perl script will prepend the drive letter

Change 48277 on 2002/08/27 by rramsey@RRAMSEY_P4_r400_win

- Fix problem with sq buf/cntl counts that let the testbench counters get out of sync with the iterator counters if an sq transfer happened on the same clk as (wait_cnt==0)
- Fix a problem that was causing the tb to drop the last rbbm transfer (this was hanging the testbench when running with the new cache_flush events)

Change 48249 on 2002/08/27 by rramsey@rramsey_crayola_unix_orl

Change to only send context_done events to the RC

Change 48176 on 2002/08/26 by ctaylor@ctaylor_crayola_unix_orl

Update 2,3,6 and 8 Sample locations for FINAL positions

Change 48163 on 2002/08/26 by ctaylor@ctaylor_crayola_unix_orl

Add rounding to baryc_back multiplier to fix 1/w precision concern.

Change 48112 on 2002/08/26 by rramsey@RRAMSEY_P4_r400_win

Update tb_sc to support clipped primitives
Fix a couple of mux selects in sc_stage_reg so it handles clipped primitives correctly

Change 48090 on 2002/08/26 by kmeekins@kmeekins_crayola_unix_orl

Truncated the LS Bit of oZ_TC to make room for the MultiSample bit on
the z-plane bus.

Change 48077 on 2002/08/26 by smoss@smoss_crayola_win

delete this file

Change 47894 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

For the last time??

Change 47879 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

Again

Change 47866 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

Again

Change 47858 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

And again

Change 47857 on 2002/08/23 by rramsey@RRAMSEY_P4_r400_win

Remove E0y, E1x, E2x compares from PIPE/out_compare until the RTL is checked in
Change the rst signal that was being checked in PACKER/out_compare (modelsim was crashing on me)
Fix a small bug with lines in sc_pipe.bvrl

Change 47853 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

  Another try

Change 47847 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

And again

Change 47846 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

Trying again

Change 47831 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

Update for correctly? compiled mc code.

Change 47799 on 2002/08/23 by ctaylor@ctaylor_crayola_unix_orl

  Fix 3-input adder to do true 2's comp for source operands

Change 47758 on 2002/08/23 by rramsey@RRAMSEY_P4_r400_win

Add TB_PACKER/out_compare.v to tb_sc dependencies

```
Change 47599 on 2002/08/22 by viviana@viviana_crayola_linux_orl

The iSV_JSS_SAMPLE_SEL bus in sc.v was getting the st_jss_sample15 through
st_jss_sample0
   3-bit busses from sample0 to sample 15. They were switched so that the 48 bit bus
got
   the individual 3 bit busses from 15 down to 0.  This was done to match the compare
values
   from the C sim.

Change 47581 on 2002/08/22 by smoss@smoss_crayola_linux_orl_regress

   added sc_pix_vec_grp_out.cmp

Change 47417 on 2002/08/21 by viviana@viviana_crayola_linux_orl

The jss sample state variables (samples 0-15) were being incorrectly indexed from
   the qpp_proc.  The index was changed to iQPP_SV_INDX for all 16 samples.

Change 47126 on 2002/08/20 by kmeekins@kmeekins_r400_win

Increased z_min and z_max bit widths from 14 to 18 bits each. The
new format leading into the sc_z_interp is now s3.14 2's comp.

Added macros to define the bit positions of the PA to SC interface.

Connected z_min, z_max, and clipped_prim in the test bench.

Change 47123 on 2002/08/20 by kmeekins@kmeekins_crayola_unix_orl

Increased z_min and z_max bit widths from 14 to 18 bits each.
s3.14 2's comp. format.

Change 47080 on 2002/08/20 by donaldl@donaldl_crayola_unix_orl

Created state_var_indx_out version.

Change 46996 on 2002/08/20 by viviana@viviana_crayola_linux_orl

Added an include for output compares from the packer.

Change 46992 on 2002/08/20 by viviana@viviana_crayola_linux_orl

This is the compare file for the output of the packer.  It uses sc_pix_vec_grp_out.dmp
for comparison.

Change 46936 on 2002/08/20 by mmantor@mmantor_r400_win
```

```
This set of changes with previous enabled multi-context to work and wrap around.

tb_sc.v
  1. changed width of SC_RC_coarse_covered from 1 bit to 16 to remove warning
  2. updated buf and cntr counter stuff for SQ/SC interface control
  3. turned on random SX_SC random RTR
sc_packer.v
   1. fixed bug in load_prim_data determination
   2. added eov setting in the oneclkcommand outside a vector for csim match and
counter compliance
   3. Force data to be zero's in the one clk command
   4. Fixed pkr_fpos to be modified on register output of packer
sc_iterator.v
   1.  increased size of sent_sq_cntl_cnt to allow events to work properly
   2.  updated fpos and singleclk leaving signals as well as the pv_cnt and cntr_cnt
sc_interp.cpp
   1.  changed default quads from PRIM_QUAD to CLEAR_QD to remove packer mismatches
with hardware
sc_block_model.cpp
   1.  added a note for clarity
sc_interp.h
   1.  added CLEAR_QD definition.

Change 46868 on 2002/08/19 by donaldl@donaldl_crayola_unix_orl

Updated sc_pipe (to match csim) --
1.  derived x_min, x_max, y_min, y_max
2.  Removed st_max_minus_1.  Not needed anymore.

Change 46867 on 2002/08/19 by donaldl@fl_donaldl_p4

Updated sc_pipe (to match csim) --

1.  derived x_min, x_max, y_min, y_max

2.  Removed st_max_minus_1.  Not needed anymore.

Change 46818 on 2002/08/19 by donaldl@donaldl_crayola_unix_orl

Expanded e0y, e1x, e2x inputs from 29.3 to 29.8 format.
Piped state_id[2:0] and st_max_sample_dist_in[3:0] through.

Change 46668 on 2002/08/17 by smoss@smoss_crayola_linux_orl_regress

   New results directory

Change 46591 on 2002/08/16 by kmeekins@kmeekins_r400_win
```

```
Added the changes to zmin and zmax for polyoffset.
Decoding the state variable MSAA_ENABLE and pipeing it to the RC.
Adjusted the compare points on the z data bus.
Expanded the covered signal to a 16 bit bus to handle the quad covered mask.

Change 46588 on 2002/08/16 by kmeekins@kmeekins_crayola_unix_orl

Added the logic to modify the zmin and zmax for polyoffset.
Expanded the covered signal to a 16 bit bus to carry the quad covered
mask.

Change 46362 on 2002/08/15 by donaldl@fl_donaldl_p4

Before expanding lsbs of edge distances and piping stateid, x_major, and
st_max_sample_dist.

Change 46359 on 2002/08/15 by smoss@smoss_crayola_linux_orl_regress

   Removed stop() from VGT used finish

Change 46264 on 2002/08/15 by rramsey@RRAMSEY_P4_r400_win

Changes for tb_sc to better support multi-context tests

Change 45755 on 2002/08/13 by kmeekins@kmeekins_crayola_unix_orl

Corrected clamping and sign extension problems.

Change 45753 on 2002/08/13 by kmeekins@kmeekins_crayola_unix_orl

Corrected clamping and sign extension problems

Change 45611 on 2002/08/13 by rramsey@FL_RAMSEY_r400_win

Fix some issues with multi-state
Fix a bug with dealloc out of packer

Change 45461 on 2002/08/12 by kmeekins@kmeekins_crayola_unix_orl

Initial release.

Change 45460 on 2002/08/12 by kmeekins@kmeekins_crayola_unix_orl

Initial release.

Change 45387 on 2002/08/12 by rramsey@FL_RAMSEY_r400_win

1. Change sc_sp dump to leave out lclk transfers to the sq
```

```
2. Remove temp drivers for cliprects in sc.v
3. Temp fix to coarse_walker to only pop zfifo when a valid end_of_prim is leaving

Change 45276 on 2002/08/09 by rramsey@RRAMSEY_P4_r400_win

Mask off compares for one-clock-transfers
Ignore lower bit of CenterZ until RTL is updated

Change 45264 on 2002/08/09 by rramsey@RRAMSEY_P4_r400_win

Clean up some code for multi-state tests

Change 45204 on 2002/08/09 by kmeekins@kmeekins_crayola_unix_orl

Added one bit to rel_exp to act as sign bit to get correct clamping
when comparing sign.

Change 45140 on 2002/08/09 by rramsey@RRAMSEY_P4_r400_win

SC_STANDALONE
1. Update msaa alg calc to handle rects (bbfractbits)
2. Change names for provok_vert, stateId to match emu code
3. Add checks for covered bits
4. Add ability to ignore Z-compares when running standalone tests in tb_sc
   I can't get these to match up yet

Change 45044 on 2002/08/08 by kmeekins@kmeekins_r400_win

Connected the Polymode bit from the SuScan.dmp file within the PA_SC interface.

Change 44754 on 2002/08/07 by rramsey@RRAMSEY_P4_r400_win

Put z fifo depth back to 8

Change 44425 on 2002/08/06 by kmeekins@kmeekins_r400_win

Connected provoking vertex signal in testbench.

Change 44390 on 2002/08/06 by smoss@smoss_crayola_linux_orl_regress

redistribution of tests

Change 44346 on 2002/08/06 by rramsey@RRAMSEY_P4_r400_win

1. Temporarily disable xmajor compare at qmask output (not in RTL yet)
2. Add ../TB_PIPE_CW_QM/out_compare.v to file list in tb_sc/Makefile
3. Don't count sc_rcc transfers for events
4. Fix SC_ZDATA depth in sc_header.v
```

```
5. Add SC/SQ primtype remapping to sc_iter.v
6. Add some conditions to detail_accum signals in sc_packer.v
7. Move line stipple state out of context space in sc_rbiu.v

Change 44306 on 2002/08/05 by ctaylor@ctaylor_crayola_unix_orl

       Fixed typo bug using wrong sample y location for frac bb determination.

Change 43900 on 2002/08/02 by smoss@smoss_crayola_linux_orl_regress

removed stop

Change 43702 on 2002/08/01 by rramsey@RRAMSEY_P4_r400_win

Remove unused inputs from sc_pipe instance

Change 43669 on 2002/08/01 by donaldl@fl_donaldl_p4

Removed null_prim_flag since no longer needed in csim.  Also removed inputs associated
with null_prim_flag:  iFIRST_PRIM_OF_SLOT, iDEALLOC_SLOT, and iEND_OF_PKT.

Change 43667 on 2002/08/01 by donaldl@donaldl_crayola_unix_orl

Removed null_prim_flag since no longer needed in csim.  Also removed inputs
associated with null_prim_flag:  iFIRST_PRIM_OF_SLOT, iDEALLOC_SLOT, and
iEND_OF_PKT.

Change 43641 on 2002/08/01 by rramsey@RRAMSEY_P4_r400_win

Update sc_pipe.bvrl to match emulator change
Always set passEmptyPrim if input prim is flipped or null

Change 43604 on 2002/07/31 by mmantor@mmantor_r400_win

temp comment out zminmx comparison until the suscan.cdmp dumps these values.

Change 43552 on 2002/07/31 by kmeekins@kmeekins_crayola_unix_orl

Added a bit of precision to the rel_exp signal as a sign bit to prevent
a large positive number from activating the zero clamp. (sc_zgrad_flt2fix)

Change 43541 on 2002/07/31 by kmeekins@kmeekins_r400_win

Added another bit of percision to rel_exp to account for the sign bit. This prevents
the zero clamp from acting on a large positive number.

Change 43512 on 2002/07/31 by grayc@grayc_crayola_linux_orl
```

udpates for vcs compile

Change 43495 on 2002/07/31 by smoss@smoss_crayola_linux_orl_regress

new path

Change 43462 on 2002/07/31 by smoss@smoss_crayola_linux_orl_regress

modified for cron

Change 43458 on 2002/07/31 by kmeekins@kmeekins_r400_win

Split z_dx and z_dy into msb and lsb parts to permit proper assignment in the GetVec PLI call. GetVec will only handle a maximum of 32 bits per field.

Change 43346 on 2002/07/31 by kmeekins@kmeekins_r400_win

Recompiled sc_z_interp to pickup the changes made to sc_ztc_flt2fix, sc_zflt5_add, and sc_zgrad_flt2fix.

Change 43224 on 2002/07/30 by mmantor@mmantor_r400_win

sc_rc coarse interface dump file and tracker checking

Change 43176 on 2002/07/30 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Undo change to script to keep dump files

Change 43127 on 2002/07/30 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Updated coarseCompare, scripts and cfg files to run AA rands.

Change 43108 on 2002/07/30 by rramsey@FL_RAMSEY_r400_win

Update sc rand script

Change 43069 on 2002/07/30 by kmeekins@kmeekins_r400_win

Resulting files from changes in respective .mc files. Simulations now passing initial test vectors.

Change 43067 on 2002/07/30 by kmeekins@kmeekins_crayola_unix_orl

Increased precision on signals used to determine the 2^3 bit position in order to handle the worst case condition.

Change 42956 on 2002/07/29 by kmeekins@kmeekins_crayola_unix_orl

```
Moved the 1's complement operation to after the shift to remove the need for a
shifter that will perform a sign extention while shifting right.

Change 42954 on 2002/07/29 by kmeekins@kmeekins_crayola_unix_orl

Added a zero clamp on delta_lnsb_m1. Added a check for all leading zero bits
when determining the bit position of the 2^3 bit.

Change 42869 on 2002/07/29 by rramsey@RRAMSEY_P4_r400_win

Clean up some more csim/rtl mismatches to get multi-prim rands to work
  Need to send_row if (qds_accepted OR row_xfer_qdcnt) instead of (qds_accepted AND
row_xfer_qdcnt)
  Change condition for load_prim_data
  Add reset for nxt_pkr_fill_partial_vector

Change 42868 on 2002/07/29 by rramsey@FL_RAMSEY_r400_win

Change Makefile include of register_addr.v to use client relative path

Change 42730 on 2002/07/26 by rramsey@RRAMSEY_P4_r400_win

Change run_vsim_rand.pl to take a "-f" arg for specifying the config file

Change 42644 on 2002/07/26 by rramsey@RRAMSEY_P4_r400_win

Fix concatenate order problem in sc_iter.v
Fix logic in sc_packer.v "pkr_curr_qds_per_vector, case 0" to match emulator

Change 42631 on 2002/07/26 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Changed MSAA_NUM_SAMPLES to be a 3-bit field (instead of 4).
Fix bug in sc_sample_mask_in dump for jss_sample_sel field
Fix bug in sc_samplemask test bench for jss_sample_sel field
Update sc tests which set num_samples to 8.

Change 42630 on 2002/07/26 by rramsey@RRAMSEY_P4_r400_win

Get rid of parameters for memory sizes

Change 42614 on 2002/07/26 by rramsey@RRAMSEY_P4_r400_win

Update dumps/rtl for mod3 comparing in sc_quadmask

Change 42586 on 2002/07/26 by smoss@smoss_crayola_linux_orl_regress

     add
```

```
Change 42515 on 2002/07/25 by mmantor@mmantor_r400_win

finished sample mask change for aa and 1 clk increase latency

Change 42513 on 2002/07/25 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Randy fixed script file for XP

Change 42506 on 2002/07/25 by mmantor@mmantor_r400_win

added the latest baryc code and routed new state data

Change 42478 on 2002/07/25 by rramsey@RRAMSEY_P4_r400_win

Add random script for sc blocks

Change 42469 on 2002/07/25 by rramsey@RRAMSEY_P4_r400_win

Hook up tilex/y mod3 signals to quadmask outputs

Change 42468 on 2002/07/25 by rramsey@rramsey_crayola_unix_orl

Add tilex/y mod3 support

Change 42450 on 2002/07/25 by rramsey@rramsey_crayola_unix_orl

Add tilex/y mod3

Change 42351 on 2002/07/25 by smoss@smoss_crayola_linux_orl

        Modified for Linux

Change 42244 on 2002/07/24 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Updated sc_samplemask and sc_baryc MC code for all new AA methodology.
Added state vars to sc_baryc_in.dmp
Fixed JSS mask bug in emulator.
Updated baryc test bench for new I/F

Change 42242 on 2002/07/24 by rramsey@RRAMSEY_P4_r400_win

Fix for pkr_curr_qds_per_vector=3 case when we see a last_qdpair_of_prim with no valid
quads from the qpp

Change 42176 on 2002/07/24 by donaldl@fl_donaldl_p4

Try previous fix again.
```

Change 42174 on 2002/07/24 by smoss@smoss_crayola_linux_orl

       build for sc

Change 42167 on 2002/07/24 by donaldl@fl_donaldl_p4

Mem stub for Z fifo.

Change 42143 on 2002/07/24 by donaldl@fl_donaldl_p4

Fixed bug for oSTATE_VAR_INDX_ZFF.

Change 42142 on 2002/07/24 by donaldl@fl_donaldl_p4

Created mem_stub for Z fifo.

Change 42122 on 2002/07/24 by kmeekins@kmeekins_r400_win

Corrected mantissa by including the sign bit and implied 1 prior to the 2's complement.

Change 42120 on 2002/07/24 by kmeekins@kmeekins_crayola_unix_orl

Fixed the mantissa to include the sign bit and the implied 1 prior to
taking the 2's complement.

Change 41997 on 2002/07/23 by grayc@grayc_crayola_linux_orl

   files needed for modelsim

Change 41985 on 2002/07/23 by grayc@grayc_crayola_linux_orl

   should have checked in to TB_SC

Change 41950 on 2002/07/23 by rramsey@rramsey_crayola_unix_orl

Add xmajor to sc_quadmask and connect it to qpp inputs

Change 41947 on 2002/07/23 by mmantor@mmantor_r400_win

change out baryc for Dan's split implementation to reduce compilation time and reduce
area and increase speed to make Stevie happy.

Change 41879 on 2002/07/22 by mmantor@mmantor_r400_win

hack for now

Change 41821 on 2002/07/22 by mmantor@mmantor_r400_win

```
* added pipe stages in sc_qdpr_proc and sc_iter for increased latency of module
compiler code.
* switch interconnect between samplemask and barc logic to be sample_id's instead of
offsets
* connected lod_correct values completely
* connected new state data
* rewired sc_sq interface and widened to handle larger lod_correct terms
*misc test bench and signal connections through the sc

Change 41783 on 2002/07/22 by dclifton@dclifton_r400

Wrapper for split sc_baryc block.

Change 41765 on 2002/07/22 by dclifton@dclifton_r400

Split the sc_baryc.mc into two files.

Change 41761 on 2002/07/22 by donaldl@fl_donaldl_p4

Initial

Change 41747 on 2002/07/22 by donaldl@donaldl_crayola_unix_orl

Adjusted idly for reset.

Change 41739 on 2002/07/22 by donaldl@fl_donaldl_p4

Removed comparison of x_major; no longer in dumps.

Change 41611 on 2002/07/19 by donaldl@fl_donaldl_p4

Added sc_zflt5_add

Change 41610 on 2002/07/19 by donaldl@fl_donaldl_p4

Added fanned out pipe_freeze_b_dly to go directly to prim fifo write enable.

Change 41609 on 2002/07/19 by donaldl@fl_donaldl_p4

Resulting bvrl after moving parameters from dps to mc file.

Change 41608 on 2002/07/19 by donaldl@donaldl_crayola_unix_orl

Resolve latencies of data from sc_quadmask.

Change 41576 on 2002/07/19 by mmantor@mmantor_r400_win

adjusted latencies for mc code changes.
```

Change 41574 on 2002/07/19 by ctaylor@ctaylor_crayola_unix_orl

Updated for new interfaces. Should work for all non-AA cases.

Change 41572 on 2002/07/19 by ctaylor@fl_ctaylor_r400_win_marlboro

Update baryc TB for new interfaces.

Change 41538 on 2002/07/19 by mmantor@mmantor_r400_win

fixed sensitivity list problems

Change 41536 on 2002/07/19 by ctaylor@fl_ctaylor_r400_win_marlboro

Test Bench changes for new interfaces.

Change 41514 on 2002/07/19 by ctaylor@ctaylor_crayola_unix_orl

Fixed undefined deriv_jss_enable so this code now seems to work for non-aa tests.

Change 41502 on 2002/07/19 by ctaylor@ctaylor_crayola_unix_orl

Post I/F change for new AA

Change 41501 on 2002/07/19 by ctaylor@ctaylor_crayola_unix_orl

bvrl file corresponding to pre-change working .mc

Change 41498 on 2002/07/19 by donaldl@fl_donaldl_p4

Initial

Change 41469 on 2002/07/19 by ctaylor@fl_ctaylor_r400_win_marlboro

Fixed issues in tb. Regressions work with pre-7/19 changes

Change 41466 on 2002/07/19 by ctaylor@ctaylor_crayola_unix_orl

Fixed dependent latencies

Change 41440 on 2002/07/19 by ctaylor@fl_ctaylor_r400_win_marlboro

Adding new test bench directory

Change 41385 on 2002/07/18 by donaldl@fl_donaldl_p4

Has new latencies due to clock period change and technology lib change.

Change 41382 on 2002/07/18 by donaldl@donaldl_crayola_unix_orl

Initial

Change 41380 on 2002/07/18 by donaldl@donaldl_crayola_unix_orl

Removed dps parameters for latency, clk period, input delay, and output delay.
Placed them in the mc files as definitions.

Change 41368 on 2002/07/18 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

fix to use .bvrl extension

Change 41339 on 2002/07/18 by ctaylor@ctaylor_crayola_unix_orl

       Adding sc baryc testbench

Change 41270 on 2002/07/18 by smoss@smoss_crayola_win

modified for tb_sc

Change 41241 on 2002/07/18 by smoss@smoss_crayola_win

more stuff

Change 41234 on 2002/07/18 by smoss@smoss_crayola_win

missed dump

Change 41197 on 2002/07/18 by grayc@grayc_crayola_unix_orl

added 'u' to instance names

Change 41077 on 2002/07/17 by mmantor@mmantor_r400_win

fixed latch problem

Change 40920 on 2002/07/16 by donaldl@fl_donaldl_p4

Added support for Z functions.

Change 40862 on 2002/07/16 by donaldl@fl_donaldl_p4

Initial

Change 40861 on 2002/07/16 by donaldl@donaldl_crayola_unix_orl

```
Initial

Change 40675 on 2002/07/15 by grayc@grayc_r400_win

initial release for sc regressions

Change 40590 on 2002/07/15 by rramsey@RRAMSEY_P4_r400_win

One more fix for rb_split

Change 40548 on 2002/07/15 by mmantor@mmantor_r400_win

added rb_id and split though the sc and fixed some bugs associated with it.  Renamed
all RC_SC_heir_xx signals to RC_SC_hier_xxx

Change 40304 on 2002/07/13 by rramsey@rrhome_r400_win

fix for fifo pop to stage 0

Change 39965 on 2002/07/12 by rramsey@RRAMSEY_P4_r400_win

Update sc rtl to work with new block file defs
Clean up sc Makefile

Change 39958 on 2002/07/12 by mmantor@mmantor_r400_win

fixed sensitivity list

Change 39897 on 2002/07/12 by mmantor@mmantor_r400_win

fixed singleclk bug

Change 39895 on 2002/07/12 by mmantor@mmantor_r400_win

fixed sensitivity list problem for synthesis

Change 39780 on 2002/07/11 by donaldl@fl_donaldl_p4

Separated declaration and initialization of integers from one line into two due to
syntax problems with older Modelsim version.

Change 39772 on 2002/07/11 by rramsey@RRAMSEY_P4_r400_win

Updates to tb_sc
  Add new pa_sc dump fields
  Add rand_int function, and randomization of rc_sc data
Add temp hack for sc_sq primtype compare until hw can be updated to match new emulator
```

```
Change 39740 on 2002/07/11 by rramsey@RRAMSEY_P4_r400_win

Fix parameters for primfifo

Change 39587 on 2002/07/10 by mmantor@mmantor_r400_win

enable basic random handshaking on all output interfaces and fixed multiple bugs to
pass simple traingle and test case #2

Change 39549 on 2002/07/10 by rramsey@RRAMSEY_P4_r400_win

Fix bug in stage management in qpp
Fix packer to match csim

Change 39493 on 2002/07/10 by grayc@grayc_r400_win

missed one signal in interface_regs block :-(

Change 39363 on 2002/07/10 by grayc@grayc_crayola_unix_orl

added mem_stub for synthesis

Change 39311 on 2002/07/10 by mmantor@mmantor_r400_win

made primitive data out know all times and prevented data from going to the z
accumulate if the iterator is stalled and the packer is ready to send data,

Change 38973 on 2002/07/09 by grayc@grayc_r400_win

okay ... another fix for clock names

Change 38971 on 2002/07/09 by grayc@grayc_r400_win

one more fix

Change 38970 on 2002/07/09 by grayc@grayc_r400_win

added ports for new named connections

Change 38969 on 2002/07/09 by grayc@grayc_r400_win

fixed port connections

Change 38922 on 2002/07/08 by grayc@grayc_r400_win

moved most top level registers into a block sc_interface_regs

Change 38639 on 2002/07/08 by donaldl@fl_donaldl_p4
```

```
Updated en_ph1_ph3 to use clip_prim (instead of clip_prim_in).  This is a temporary
behavioral code change.  This fix will be done later in sc_stage_reg.mc.

Change 38292 on 2002/07/05 by rramsey@RRAMSEY_P4_r400_win

Add connection for event flag in sc_packer
Kill valids to sx and sp for events in sc_iter

Change 37867 on 2002/07/03 by rramsey@RRAMSEY_P4_r400_win

Add some support for events to tb_sc
Fix an error report msg in sc_sp compare

Change 37748 on 2002/07/02 by mmantor@mmantor_r400_win

changes to get primlib_template_simple_triangle to pass with no back pressure.

Change 37084 on 2002/06/28 by rramsey@RRAMSEY_P4_r400_win

Fix some more issues with pa_sc inputs in tb_sc.v
Fix bug in qpp that happens when there are single quad tiles in r0 and r1, but no new
tile in the result fifo.

Change 36476 on 2002/06/26 by rramsey@RRAMSEY_P4_r400_win

Clean up SC dumps
  Remove pa_sc.dmp since it is redundant
  Add sc_rbbm.dmp which only contains sc relevant reg writes so tb_sc runs faster
  Rearrange dump levels so only block level interfaces are dumped at level 1,
    hw accurate internals are dumped at level 2, and non-hw accurate are dumped
    at level 3
Update emu_dumps block diagram to reflect changes

Change 36430 on 2002/06/26 by rramsey@RRAMSEY_P4_r400_win

Update tb_sc (specifically pa_sc inputs) to work with new GetVec PLI routine

Change 36397 on 2002/06/26 by rramsey@RRAMSEY_P4_r400_win

Change comma to or in sensitivity list

Change 36257 on 2002/06/25 by donaldl@fl_donaldl_p4

Set output busy signals also when incrementing busy counters.

Change 36256 on 2002/06/25 by donaldl@donaldl_crayola_unix_orl
```

Set output busy signals also when incrementing busy counters.

Change 36235 on 2002/06/25 by rramsey@RRAMSEY_P4_r400_win

Fix some internal signal names, no functional change

Change 36233 on 2002/06/25 by mmantor@mmantor_r400_win

first full pass at the sc_busy is done.

Change 36227 on 2002/06/25 by donaldl@fl_donaldl_p4

Cleaned up anti-alias state variable names.

Change 36226 on 2002/06/25 by donaldl@donaldl_crayola_unix_orl

Removed iFREEZE_B term for decrement of busy counters.
Extended busy output signals for 2 clks.
Changed input busy signals names from pkr_iterator.

Change 36225 on 2002/06/25 by donaldl@fl_donaldl_p4

Updated with latest csim changes (except line stipple)

Change 36223 on 2002/06/25 by donaldl@donaldl_crayola_unix_orl

Updated with latest csim changes (except line stipple)

Change 36194 on 2002/06/25 by donaldl@fl_donaldl_p4

Removed iFREEZE_B term for decrement of busy counters. Extended busy output signals
for 2 clks. Changed input busy signals from pkr_iterator.

Change 36193 on 2002/06/25 by donaldl@fl_donaldl_p4

Changed signal names on input busy signals from pkr_iter to sc_stage_reg.

Change 36148 on 2002/06/25 by mmantor@mmantor_r400_win

adding the sc busy determination logic, there will be an update

Change 36099 on 2002/06/25 by rramsey@RRAMSEY_P4_r400_win

Add rb_id and split to tb_sc instance of sc

Change 35920 on 2002/06/24 by rramsey@RRAMSEY_P4_r400_win

Reformat sc_sx dump for rb_id/split/tilex/tiley change

```
Change sc_primfifo to use memory based fifo and modify qpp to
  remove a reg stage and pop the fifo one clk later
Add cntx0_dec and cntx17_dec signals to qpp for front-pipe
  busy count decrementing
Add RC_SC_rb_id and RC_SC_split signals to sc top and pipe
  those sigs all the way to the qpp outputs
Update sc_sx tracker to handle new emu dump file format
  rb_id and split are not being compared yet since RC drivers
  are not in RTL yet

Change 35836 on 2002/06/24 by mmantor@mmantor_r400_win

added pkr busy signals

Change 35834 on 2002/06/24 by mmantor@mmantor_r400_win

out_compare - tmp fix to work around split and rbid on sx interface
sc_detail_mask_accum - tmp fix for infinite loop
sc_iter and sc_packer -  clean up and some packer busy stuff

Change 35758 on 2002/06/24 by rramsey@rramsey_crayola_linux_orl

Mods to support VCS sims

Change 35650 on 2002/06/21 by donaldl@donaldl_crayola_unix_orl

Added context busy logic.  Removed pipestall directive to allow free running count
registers.  Other regs had to qualify enable directly with iFREEZE_B.

Change 35649 on 2002/06/21 by donaldl@fl_donaldl_p4

Added initial logic support for context0 and context1to7 busy signals.

Change 34962 on 2002/06/19 by rramsey@rramsey_crayola_linux_orl

Add .tab file for vcs compiles
Update InitVec function to execute on REASON_CALLTF
Update sc_qdpr_proc tb to run with VCS

Change 34685 on 2002/06/18 by rramsey@RRAMSEY_P4_r400_win

Move SC_SQ outputs from front of delay pipe to the back so transfers
line up with SX and SP data

Change 34465 on 2002/06/17 by donaldl@fl_donaldl_p4

Called coarse_walker and quadmask compare routines as functions and use them as
internal trackers.
```

Change 34460 on 2002/06/17 by donaldl@fl_donaldl_p4

Added x_major quadmask compare.

Change 34440 on 2002/06/17 by donaldl@fl_donaldl_p4

Tests sc_pipe, sc_coarse_walker, and sc_quadmask blocks.

Change 34332 on 2002/06/15 by donaldl@donaldl_crayola_unix_orl

Clear the valid signal from sc_coarse_dly during SRST.

Change 34331 on 2002/06/15 by donaldl@fl_donaldl_p4

Clear the valid signal from sc_coarse_dly during SRST.

Change 34323 on 2002/06/14 by mmantor@mmantor_r400_win

fixed a bug with iter_phase_dll

Change 34168 on 2002/06/14 by rramsey@RRAMSEY_P4_r400_win

Increase num chars in compare strings

Change 34152 on 2002/06/14 by rramsey@RRAMSEY_P4_r400_win

Fix out of range warning in vcs

Change 34050 on 2002/06/14 by grayc@grayc_crayola_linux_orl

macro now defined with new emulator build

Change 34044 on 2002/06/14 by grayc@grayc_crayola_unix_orl

tmp fix for undefined register macro

Change 33898 on 2002/06/13 by mmantor@mmantor_r400_win

enabled the sq and sx interfaces with the sc. passes the first triangle test case

Change 33628 on 2002/06/12 by mmantor@mmantor_r400_win

got sc to sp interface working in the sc

Change 33543 on 2002/06/12 by donaldl@fl_donaldl_p4

Added SC_SQ tracker.

Change 33373 on 2002/06/11 by donaldl@fl_donaldl_p4

Added support for SC_SP and SC_SX trackers.

Change 33372 on 2002/06/11 by donaldl@fl_donaldl_p4

Added SC_SP and SC_SX output trackers.

Change 33371 on 2002/06/11 by donaldl@fl_donaldl_p4

Added sc_iter

Change 33370 on 2002/06/11 by donaldl@fl_donaldl_p4

Forced iterator send state variables as a temporary fix.

Change 33369 on 2002/06/11 by donaldl@fl_donaldl_p4

Added iterator block (ie. sc_iter).

Change 33368 on 2002/06/11 by donaldl@fl_donaldl_p4

Added iterator block (ie. sc_iter).

Change 33367 on 2002/06/11 by donaldl@donaldl_crayola_unix_orl

Clear I0 and J0 terms if processing an unclipped prim.

Change 33344 on 2002/06/11 by donaldl@fl_donaldl_p4

Clear I0 and J0 terms if processing an unclipped prim.

Change 33153 on 2002/06/11 by mmantor@mmantor_r400_win

added initial incomplete sc_iter.v and test bench

Change 33104 on 2002/06/10 by donaldl@fl_donaldl_p4

Registered RC_SC_HEIR_MASK, RC_SC_HEIR_SEND, and SC_RC_HEIR_RTR using ati_dff flops.

Change 33103 on 2002/06/10 by donaldl@fl_donaldl_p4

Removed registering of hier_fifo_we and heir_mask_wd. Already done at the sc top
level.

Change 33097 on 2002/06/10 by donaldl@fl_donaldl_p4

```
Removed temporary state variables.

Change 33096 on 2002/06/10 by donaldl@fl_donaldl_p4

Clear last_tile_of_prim and z_ff_read_en during reset.

Change 33094 on 2002/06/10 by donaldl@donaldl_crayola_unix_orl

Clear last_tile_of_prim and z_ff_read_en during reset.

Change 33091 on 2002/06/10 by donaldl@fl_donaldl_p4

Add HW_SCREEN_OFFSET_TILE to tilex and tiley

Change 33090 on 2002/06/10 by donaldl@donaldl_crayola_unix_orl

Add HW_SCREEN_OFFSET_TILE to tilex and tiley

Change 32995 on 2002/06/10 by rramsey@RRAMSEY_P4_r400_win

And delete from tb_sc

Change 32993 on 2002/06/10 by rramsey@RRAMSEY_P4_r400_win

This time really remove unused state inputs

Change 32985 on 2002/06/10 by rramsey@RRAMSEY_P4_r400_win

Add aa_mask to sc_rbiu decode and sc_state block
Add state index selects for qdpr_proc and iterator blocks
Fix problem with testbench rc_sc driver
Remove temp state inputs from sc.v

Change 32891 on 2002/06/10 by donaldl@fl_donaldl_p4

Changed for state variables .o work with rbiu

Change 32843 on 2002/06/08 by rramsey@RRAMSEY_P4_r400_win

Removing TB_SC/tbfiles from depot.

Change 32842 on 2002/06/08 by rramsey@RRAMSEY_P4_r400_win

add out_compare to TB_SC

Change 32841 on 2002/06/08 by rramsey@RRAMSEY_P4_r400_win

Try to get rid of lower case tb_sc
```

Change 32824 on 2002/06/07 by donaldl@fl_donaldl_p4

Removed input registers of state variables to time up with state_var_index from sc_stage_reg.

Change 32823 on 2002/06/07 by donaldl@fl_donaldl_p4

Added sc_rsel.

Change 32822 on 2002/06/07 by donaldl@donaldl_crayola_unix_orl

Increased idly from 500 to 800 to account a little for removing input state var registers.

Change 32821 on 2002/06/07 by donaldl@donaldl_crayola_unix_orl

Removed input registers of state variables to time up with state_var_index from sc_stage_reg.

Change 32699 on 2002/06/07 by rramsey@RRAMSEY_P4_r400_win

Add rc_sc inputs and sc_rc trackers to tb_sc
Add out_compare.v and ../tb_sc_qdpr_proc/out_compare.v to tb_sc and sc Makefile
Correct clk and rst inputs to usc_qdpr_proc in sc.v

Change 32617 on 2002/06/07 by donaldl@fl_donaldl_p4

Added simple rtr control.

Change 32607 on 2002/06/07 by rramsey@RRAMSEY_P4_r400_win

Make qdpr_proc deterministic
Update compare function to match new dumps
Add fifo name to sc_tilefifo parameters

Change 32517 on 2002/06/06 by donaldl@fl_donaldl_p4

Changed definition of SC_QD_DATA_WIDTH from "96:0" to "97"

Change 32511 on 2002/06/06 by donaldl@fl_donaldl_p4

Merge with latest version

Change 32497 on 2002/06/06 by mmantor@mmantor_r400_win

updated for packer changes and gc level compile

```
Change 32474 on 2002/06/06 by rramsey@RRAMSEY_P4_r400_win

Move qdpr_proc vector compare code into functions in new file (out_compare.v)
  so they can easily be ported to top level testbench
Update tb_sc_qdpr_proc and Makefile to include out_compare.v

Change 32460 on 2002/06/06 by mmantor@mmantor_r400_win

updated top level for gc integration issues and to work with latest packer

Change 32453 on 2002/06/06 by mmantor@mmantor_r400_win

conditioned detail z interface with zneeded

Change 32421 on 2002/06/06 by mmantor@mmantor_r400_win

updated the mti_pli.dll to handle 110 fields for getvec and cmpvec
fixed tilex,y width in sc_dumps
first working sc_packer code and associated files

Change 32322 on 2002/06/06 by rramsey@RRAMSEY_P4_r400_win

Update qdpr_proc testbench

Change 32302 on 2002/06/06 by fhsien@fhsien_r400_unix_marlboro

Check in to fix GC build

Change 32133 on 2002/06/05 by donaldl@fl_donaldl_p4

Added rbiu counters

Change 32131 on 2002/06/05 by donaldl@fl_donaldl_p4

Used 'or' instead of ',' when listing sensitivity list.

Change 32120 on 2002/06/05 by ctaylor@fl_ctaylor_r400_win_marlboro

Changed pipestall signal name to pipestall_b for active-low

Change 32102 on 2002/06/05 by mmantor@mmantor_r400_win

update

Change 32082 on 2002/06/05 by rramsey@RRAMSEY_P4_r400_win

Updates to sc rtl
Remove oQPP_Q0_VALID and oQPP_Q1_VALID from sc_qdpr_proc.v
```

```
Add event flag to primitive fifo
Update sc_qdpr_proc testbench

Change 31964 on 2002/06/05 by mmantor@mmantor_r400_win

added initial sc_packer code to the sc.v  and a test bench for it

Change 31936 on 2002/06/05 by donaldl@fl_donaldl_p4

Temporary pass-through of data for June milestone triangle.

Change 31934 on 2002/06/05 by donaldl@donaldl_crayola_unix_orl

Temporary pass-through of data for June milestone triangle.

Change 31933 on 2002/06/05 by donaldl@donaldl_crayola_unix_orl

Increased oDEALLOC_SLOT bits (from 1 to 3) and iCNTL bits.

Change 31931 on 2002/06/05 by donaldl@donaldl_crayola_unix_orl

Increased bit width of iDEALLOC_SLOT from 1 bit to 3 bits.

Change 31930 on 2002/06/05 by donaldl@donaldl_crayola_unix_orl

Added oZ_FF_RD_EN (Z fifo read enable) and iRC_RTR.

Change 31929 on 2002/06/05 by donaldl@fl_donaldl_p4

Removed SC_BUSY.

Change 31928 on 2002/06/05 by donaldl@fl_donaldl_p4

Increased oDEALLOC_SLOT bits (from 1 to 3) and iCNTL bits.

Change 31927 on 2002/06/05 by donaldl@fl_donaldl_p4

Added more state variable selects.

Change 31926 on 2002/06/05 by donaldl@fl_donaldl_p4

Increased bit width of iDEALLOC_SLOT from 1 bit to 3 bits.

Change 31925 on 2002/06/05 by donaldl@fl_donaldl_p4

Added oZ_FF_RD_EN (Z fifo read enable) and iRC_RTR.

Change 31924 on 2002/06/05 by donaldl@fl_donaldl_p4
```

```
Corrected some bit width signals while instantiating.

Change 31835 on 2002/06/04 by ctaylor@fl_ctaylor_r400_win_marlboro

Fix sc_samplemask MC bug with LRC E1,E2 edge calcs.

Change 31813 on 2002/06/04 by donaldl@fl_donaldl_p4

Added sc_coarse_dly and defined VLOG_INC.

Change 31809 on 2002/06/04 by donaldl@fl_donaldl_p4

Added GFX_DECODE definition

Change 31807 on 2002/06/04 by donaldl@fl_donaldl_p4

Added sc_coarse_dly

Change 31708 on 2002/06/04 by rramsey@rrhome_r400_win

Updates to sc_qdpr_proc instance

Change 31702 on 2002/06/04 by rramsey@rrhome_r400_win

Change sc_quad_select instance to sc_qdpr_proc and add associated signals
Add sc_qdpr_proc to Makefile

Change 31658 on 2002/06/04 by rramsey@RRAMSEY_P4_r400_win

Intermediate checkin for quad-pair processor

Change 31566 on 2002/06/03 by donaldl@fl_donaldl_p4

Created bit width definitions of z fifo data.

Change 31435 on 2002/06/03 by donaldl@fl_donaldl_p4

Changed SC_TILEDATA_SKIDW to 1 to create an almost full flag of tile data fifo.

Change 31356 on 2002/06/02 by rramsey@rrhome_r400_win

Add sc_qdpr_proc module

Change 31317 on 2002/06/01 by donaldl@fl_donaldl_p4

Removed sc_busy
```

```
Change 31170 on 2002/05/31 by ctaylor@fl_ctaylor_r400_win_marlboro

Adding .bvrl files for samplemask and baryc
Modified baryc for new full prec outputs.
Added cntrmost sample offset and id for antialiasing.

Change 31123 on 2002/05/31 by rramsey@RRAMSEY_P4_r400_win

Fixed to quad_select tb to get all data matching

Change 31068 on 2002/05/31 by bbuchner@fl_bbuchner_r400_win

Added detail mask accumulator module, test bench, and vis-studio
project to generate vectors.

Change 30833 on 2002/05/30 by rramsey@RRAMSEY_P4_r400_win

more stuff for sc_quad_select.v

Change 30825 on 2002/05/30 by rramsey@RRAMSEY_P4_r400_win

move tbmod_rand to top level sc dir

Change 30808 on 2002/05/30 by rramsey@RRAMSEY_P4_r400_win

adding sc_quad_select rtl, and updating sc.v to include it

Change 30253 on 2002/05/28 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Added centermost sample computation and lod sample id determination to Emu and Hw

Change 30194 on 2002/05/27 by ctaylor@fl_ctaylor_r400_dtwin_marlboro

Modify Emu and HW for new high precision SC->SP IJ data paths.
Fix HW accurate 3-input adder bug for baryc math.
Add official sc_bary_in/out dumps.
Fix HW to work in subpix instead of pix for gradients.

Change 28524 on 2002/05/16 by donaldl@fl_donaldl_p4

Added ati_1rp_state_storage, sc_rbiu, and sc_state.

Change 28521 on 2002/05/16 by donaldl@fl_donaldl_p4

Fixed errors when loading in vsim

Change 28419 on 2002/05/16 by sallen@sallen_r400_lin_marlboro
```

```
fix compile error

Change 28391 on 2002/05/16 by donaldl@fl_donaldl_p4

Added first cut of rbbm interface and state variables.

Change 28390 on 2002/05/16 by donaldl@fl_donaldl_p4

Initial

Change 27745 on 2002/05/13 by donaldl@fl_donaldl_p4

Added ati_fifo and sc_stage_reg.

Change 27743 on 2002/05/13 by donaldl@fl_donaldl_p4

Updated to match latest PA to SC interface changes.

Change 27740 on 2002/05/13 by donaldl@fl_donaldl_p4

Instantiated sc_stage_reg unit, primitive fifo, Z fifo, and tile fifo.

Change 27732 on 2002/05/13 by donaldl@fl_donaldl_p4

Behavioral verilog generated from Module Compiler.

Change 27728 on 2002/05/13 by donaldl@donaldl_crayola_unix_orl

Initial

Change 27727 on 2002/05/13 by donaldl@donaldl_crayola_unix_orl


Change 27725 on 2002/05/13 by donaldl@donaldl_crayola_unix_orl

Replaced oPIPE_FREEZE_B output with oPIPE_FREEZE_B_EARLY and oPIPE_FREEZE_B_DLY.
       oPIPE_FREEZE_B_EARLY is the freeze unregistered while oPIPE_FREEZE_B_DLY is used
       to freeze units internal to the scan converter.

Change 27722 on 2002/05/13 by donaldl@donaldl_crayola_unix_orl

Added null primitive input.
       Removed input registers; done in sc_stage_reg unit.

Change 27617 on 2002/05/13 by donaldl@donaldl_crayola_unix_orl

Removed references to any tech_lib or wireload.  Caused problems getting an MC license.
```

```
Change 27384 on 2002/05/10 by ctaylor@fl_ctaylor_r400_win_marlboro

Adding .dps files
sc_samplemask is done and moderately tested for regular rendering, MSAA, JSS, AA MASK.
Still missing line_stipple mask logic and centroid logic.

Change 27077 on 2002/05/08 by donaldl@fl_donaldl_p4

Added null prim input, renamed busy signals, and increased SC_SQ_data to 49 bits wide.

Change 27075 on 2002/05/08 by donaldl@fl_donaldl_p4

Added changes to clk gating logic.  Added null prim input to sc_pipe.

Change 25892 on 2002/05/01 by donaldl@fl_donaldl_p4

Initial testbench to test sc_pipe, sc_coarse_walker, and sc_quadmask.

Change 25875 on 2002/05/01 by donaldl@fl_donaldl_p4

simple random vectors

Change 25869 on 2002/05/01 by donaldl@fl_donaldl_p4

simple random vectors

Change 25866 on 2002/05/01 by donaldl@fl_donaldl_p4

Instantiated sc_pipe, sc_coarse_walker, & sc_quadmask blocks.

Change 25864 on 2002/05/01 by donaldl@fl_donaldl_p4

Added ati_dff_en_in

Change 25632 on 2002/04/30 by donaldl@fl_donaldl_p4

SC makefile for modelsim

Change 25324 on 2002/04/29 by mmantor@mmantor_r400_win

updated spec for PA_SC_su interface changes
updated sc.v and created tb directories

Change 25156 on 2002/04/26 by donaldl@donaldl_crayola_unix_orl

Initial

Change 25155 on 2002/04/26 by donaldl@donaldl_crayola_unix_orl
```

```
Initial

Change 23611 on 2002/04/17 by rramsey@RRAMSEY_P4_r400_win

Add qmask testbench

Change 23321 on 2002/04/15 by mmantor@mmantor_r400_win

seperated some sc_interp stuff for hardware modeling of output controllers

Change 23129 on 2002/04/12 by ctaylor@fl_ctaylor_r400_win_marlboro

check in sc interp mc

Change 21452 on 2002/04/02 by mmantor@mmantor_r400_win

removed sc_rbbm_nrtrtr

Change 20769 on 2002/03/27 by mmantor@mmantor_r400_win

updated for interface integration changes

Change 20474 on 2002/03/26 by mmantor@mmantor_r400_win

updated for spec changes

Change 20229 on 2002/03/22 by rramsey@RRAMSEY_P4_r400_win

add mc code for sc_quadmask in correct location

Change 19542 on 2002/03/18 by mmantor@mmantor_r400_win

initial top level for the pa and sc verilog files
```

```
Change 54213 on 2002/09/28 by hartogs@hartogs_crayola_unix_orl

Added missing signal to sensitivity list

Change 54186 on 2002/09/27 by hartogs@fl_hartogs2

Added multi-prim index buffer reset.

Change 53441 on 2002/09/24 by hartogs@hartogs_crayola_unix_orl

Deleted signals from old implementation.

Change 53436 on 2002/09/24 by hartogs@hartogs_crayola_unix_orl

Yet another attempt to make this change correctly.

Change 53430 on 2002/09/24 by hartogs@fl_hartogs

Second try to submit modified vgt_tess_output.v file.

Change 53421 on 2002/09/24 by hartogs@fl_hartogs

Converted vgt_tess_output block to a modified version of the bit-slice divider.

Change 53384 on 2002/09/24 by hartogs@fl_hartogs2

Fixed reg/wire problem.

Change 53363 on 2002/09/24 by hartogs@fl_hartogs

Added new 19-bit divide-by-3 module for vgt_tess_output module.
It remains to be seen if it's fast enough.

Change 53362 on 2002/09/24 by hartogs@hartogs_crayola_unix_orl

Converted 19-bit divide-by-3 into a module.

Change 53268 on 2002/09/24 by hartogs@fl_hartogs

Added missing sensitivity list signal.

Change 52889 on 2002/09/20 by hartogs@fl_hartogs2

Added null_primitive signal to the clip_p bus. Changed behavior so that events are no
longer transmitted over the clip_s interface.

Change 52861 on 2002/09/20 by hartogs@fl_hartogs2
```

```
Changed implementation of adder for divide-by-3 to meet timing.

Change 52702 on 2002/09/20 by smoss@smoss_crayola_linux_orl_regress

   VCS not VSC

Change 52665 on 2002/09/19 by hartogs@fl_hartogs2

Changed a signal that went from the rbiu -> grouper -> rbiu combinationally.
   Now it is completely contained in the grouper.

Change 52652 on 2002/09/19 by hartogs@hartogs_crayola_unix_orl

Added another directive to prevent resource sharing

Change 52596 on 2002/09/19 by hartogs@fl_hartogs2

Restructured a block to get control over resource sharing. No function change.

Change 52503 on 2002/09/19 by hartogs@fl_hartogs2

Replaced $finish with `ifdef VCS and $stop as the routine for Modelsim. This will
hopefully avoid the "Blocking channel driver" pop-up that occurs intermittently for a
$finish in modelsim.

Change 52405 on 2002/09/18 by hartogs@fl_hartogs2

Fixed sensitivity list

Change 52326 on 2002/09/18 by hartogs@fl_hartogs2

Another timing experiment.

Change 52260 on 2002/09/18 by hartogs@fl_hartogs

More changes for timing.

Change 52248 on 2002/09/18 by hartogs@fl_hartogs

Yet another change for timing.

Change 52118 on 2002/09/17 by hartogs@hartogs_crayola_unix_orl

Added some missing sensitivity list signals.

Change 52108 on 2002/09/17 by hartogs@fl_hartogs

Reorganized if statement to hopefully improve timing.
```

Change 52072 on 2002/09/17 by hartogs@fl_hartogs

vgt_grouper.v -- changed some false-triggering error detection logic. No functional change.
vgt_output.v -- modified to handle events that occur within a chain of packets.

Change 52005 on 2002/09/17 by hartogs@fl_hartogs

Fixed problem in default settings for major mode 0, 2D prim types 0x10 (16) thru 0x15 (21).
Fixed timing loop caused by evaluating two pseudo-unrelated groups of signals in the same always block.

Change 51850 on 2002/09/16 by hartogs@fl_hartogs

Added snooped enable bit for multi prim index buffer mode.

Change 51807 on 2002/09/16 by hartogs@fl_hartogs

Added multi-context register for multi_prim_ib_register (per Clay's vgt.blk file change).

Change 51744 on 2002/09/16 by hartogs@hartogs_crayola_unix_orl

Removed "infer_mix" directives. They were causing compiler syntax errors.

Change 51739 on 2002/09/16 by hartogs@fl_hartogs2

More timing changes.

Change 51553 on 2002/09/13 by hartogs@fl_hartogs2

Shuffled some stuff around, no intended functionality change.

Change 51421 on 2002/09/13 by hartogs@fl_hartogs2

Changed event type width from 4 to 5 bits.

Change 51335 on 2002/09/13 by hartogs@fl_hartogs

Reverted the computation of the extract vector signal.

Change 51242 on 2002/09/12 by hartogs@fl_hartogs2

Reverted back to version 16 (change 49011) because other timing changes probably made this one unnecessary.

Change 51232 on 2002/09/12 by hartogs@fl_hartogs2

Yet another change for timing.

Change 51216 on 2002/09/12 by hartogs@hartogs_crayola_unix_orl

Small change for synthesis.

Change 51002 on 2002/09/12 by hartogs@fl_hartogs2

Added shallow (2 word) fifo on dma_data path to buffer the read signal of the large dma data fifo from the logic in the grouper that generates the read signal.

Change 50947 on 2002/09/11 by hartogs@fl_hartogs

Fixed error in computation of second_pass_rl_q signal that was introduced in the last check-in.

Change 50881 on 2002/09/11 by grayc@grayc_crayola_linux_orl

   removed hard coded path

Change 50878 on 2002/09/11 by grayc@grayc_crayola_linux_orl

   text files used to run leda

Change 50851 on 2002/09/11 by hartogs@fl_hartogs2

expedited the determination of shift_vect_rtr.

Change 49870 on 2002/09/05 by hartogs@fl_hartogs

Reverted back to revision 51; however, kept the d/pre_d split for possible use later.
Also kept the right_max_no_extract and right_max_extract signals; however, they're not registered.
From this starting point, pre-computed and registered the terms for the creation of "extract_vector".
This registered precomputation is called "extract_vector_if_rtr_q"

Change 49647 on 2002/09/05 by hartogs@hartogs_crayola_unix_orl

Re-fixed timing loop.

Change 49583 on 2002/09/04 by bbuchner@fl_bbuchner_r400_win

change unused tri data/types to match EMU.

Change 49570 on 2002/09/04 by hartogs@fl_hartogs2

```
Attempt to fix timing problem.

Change 49562 on 2002/09/04 by bbuchner@fl_bbuchner_r400_win

removed unused interfaces.
fixed output unit data types for don't care data.

Change 49485 on 2002/09/04 by hartogs@fl_hartogs2

Added synthesis stubs for Virage memories.

Change 49475 on 2002/09/04 by hartogs@fl_hartogs2

Fixed typo in signal name that has existed for months (the Verilog compiler sucks!)

Change 49064 on 2002/08/30 by hartogs@hartogs_crayola_unix_orl

Added missing signal to sensitivity list.

Change 49012 on 2002/08/30 by hartogs@fl_hartogs2

Should have been part of change 49001

Change 49011 on 2002/08/30 by hartogs@fl_hartogs2

Implemented the following functions:
    1) Soft reset combined with hard reset
    2) Register readback via the RBBM
    3) Finished implementing ati_dff modules on I/O
    4) Added random reg readback test to vgt_rbiu_tb
    5) regress_vgt_rtl.tcsh now indicates test that are skipped
       by request or because the dump files were missing
    6) Consolidated the calculation of the number of acive pipes
       in the vgt_vtx_reuse block and passed to the vgt_output block.

Other code changes:
    1) Deleted indx fifo in the vgt_vtx_reuse block
    2) Converted indx fifo in the vgt_out_indx block
       to Virage based memory (was register based)

Change 48621 on 2002/08/28 by bbuchner@fl_bbuchner_r400_win

added pipe stage to vertex path in walker unit for timing.
swap s/t logic moved to walker unit to offload output timing path.

Change 48349 on 2002/08/27 by hartogs@fl_hartogs2
```

```
Changed signal name VGT_PA_clip_p_null_prim to VGT_PA_clip_p_event_flag.

Change 48292 on 2002/08/27 by bbuchner@fl_bbuchner_r400_win

major rewrite of setup for timing

Change 48138 on 2002/08/26 by hartogs@fl_hartogs2

Changed makefile so that the compile macro "DEBUSSY" is set be default.
   Changed testbench to enable Debussy dumps only when the command line +VGT_DEBUSSY=1
is supplied to vsim.

Change 47830 on 2002/08/23 by hartogs@fl_hartogs2

Modified to ignore lines in test_list that start with a #.

Change 47565 on 2002/08/22 by hartogs@fl_hartogs2

Changes to accmodate Chris Gray's hacks of MY testbench.

Change 47532 on 2002/08/22 by grayc@grayc_crayola_linux_orl

   updates for vgt_tb

Change 47040 on 2002/08/20 by bbuchner@fl_bbuchner_r400_win

modify usage of vtx_reuse_depth to improve timing.

Change 46887 on 2002/08/19 by bbuchner@fl_bbuchner_r400_win

break delta calculation over two clocks to meet timing.
modify mux select of tess. level for timing.

Change 46669 on 2002/08/17 by smoss@smoss_crayola_linux_orl_regress

   changed vgt resutls dir

Change 46613 on 2002/08/16 by hartogs@fl_hartogs

Changed so that the VGT_RBBM_nrtrtr is registered with ati io dff module.

Change 46602 on 2002/08/16 by hartogs@fl_hartogs2

Updated

Change 46597 on 2002/08/16 by hartogs@fl_hartogs2

Created new script for re-running tests with a given seed.
```

```
   Increased timeout clock count in testbench.

Change 46474 on 2002/08/16 by bbuchner@fl_bbuchner_r400_win

updated test bench to reflect tessellator I/O changes

Change 46370 on 2002/08/15 by bbuchner@fl_bbuchner_r400_win

modification for state machine timing
modification for delta calculation timing

Change 46359 on 2002/08/15 by smoss@smoss_crayola_linux_orl_regress

   Removed stop() from VGT used finish

Change 46254 on 2002/08/15 by hartogs@fl_hartogs2

Fixed a problem with the RBBM state stall logic.

Change 46142 on 2002/08/14 by hartogs@fl_hartogs2

Modified rbbm stall logic in the testbench for new multi-context stuff.

Change 46100 on 2002/08/14 by bbuchner@fl_bbuchner_r400_win

corrected undeclared wire
walker_busy signal is now asserted when walker is holding
valid prim data at its output.

Change 45976 on 2002/08/14 by hartogs@fl_hartogs2

Fixed error detection code.

Change 45860 on 2002/08/13 by hartogs@hartogs_crayola_unix_orl

Added missing wire declaration.

Change 45835 on 2002/08/13 by hartogs@fl_hartogs2

Fixed event type bug.

Change 45827 on 2002/08/13 by hartogs@fl_hartogs

Removed mod_in argument from vgt_7_bit_div_3 function (and renamed it) to avoid
warnings from the synthesizer.

Change 45825 on 2002/08/13 by smoss@smoss_crayola_linux_orl_regress
```

```
   Files for VGT VCS

Change 45769 on 2002/08/13 by hartogs@fl_hartogs

Re-coded the vgt_rbiu sub-block to use common modules for FIFOs

Change 45741 on 2002/08/13 by smoss@smoss_crayola_linux_orl_regress

   Added files for VCS VGT

Change 45737 on 2002/08/13 by smoss@smoss_crayola_linux_orl_regress

   Modified for VGT in VCS

Change 45542 on 2002/08/12 by hartogs@hartogs_crayola_unix_orl

Disabled some pragmas that were attempting to force certain designware implementations.

Change 45511 on 2002/08/12 by hartogs@hartogs_crayola_unix_orl

Delete even more `ifdef MODELTECH macros.

Change 45481 on 2002/08/12 by hartogs@hartogs_crayola_unix_orl

Removed 'ifdef MODELTECH

Change 45479 on 2002/08/12 by hartogs@hartogs_crayola_unix_orl

vgt_dma -- deleted unused variable
vgt_grouper, vgt_vtx_reuse -- may each loop index unique and changed from integer to
reg.

Change 45427 on 2002/08/12 by grayc@grayc_r400_win

tmp fix to rbbm daisy chain reads for chip simulation

Change 45412 on 2002/08/12 by hartogs@fl_hartogs

Fixed typo.

Change 45409 on 2002/08/12 by hartogs@fl_hartogs

Reverted the vgt_grouper.v file back to version 41 because fix in 42 for timing made
timing worse.
Simple changed to one 'if' statement in vgt_grouper to hopefully make it faster.
Reduce verilog "memories" to a single entry in the timing control list for the presto
reader.
Added `ifdef MODELTECH in timing control lists that have split-out memory entries.
```

```
Change 44736 on 2002/08/07 by hartogs@fl_hartogs

Re-organized previous change to ensure that latches are not infered.

Change 44715 on 2002/08/07 by hartogs@fl_hartogs

Added ati modules for VGT Block I/O

Change 44706 on 2002/08/07 by hartogs@fl_hartogs2

Put in a stop check.

Change 44691 on 2002/08/07 by hartogs@fl_hartogs

Converted i/o flops to ati modules.

Change 44662 on 2002/08/07 by hartogs@fl_hartogs2

Fixed yet again.

Change 44661 on 2002/08/07 by hartogs@fl_hartogs

Fixed selection of current_shift_d and current_stride_d

Change 44654 on 2002/08/07 by hartogs@fl_hartogs

Moved some computations over to the previous clock cycle for timing.
Hopefully improve the timing of right_shift_max.

Change 44508 on 2002/08/06 by hartogs@fl_hartogs2

Genericized.

Change 44507 on 2002/08/06 by hartogs@fl_hartogs2

Backpressure bug fix.

Change 44487 on 2002/08/06 by hartogs@fl_hartogs2

Fixed bug.

Change 44474 on 2002/08/06 by hartogs@fl_hartogs2

   Enhanced for running regression in loop with random backpressure.

Change 44433 on 2002/08/06 by hartogs@fl_hartogs
```

Made random seed and random backpressure into vsim command line arguments

Change 44281 on 2002/08/05 by hartogs@fl_hartogs

Added random backpressure generation to the testbench. Fixed some errors in the backpressure logic.

Change 44275 on 2002/08/05 by hartogs@fl_hartogs

More signals.

Change 44166 on 2002/08/05 by hartogs@fl_hartogs

Moved grp_decr and grp_fist_decr to access one clock earlier.

Change 44142 on 2002/08/04 by hartogs@fl_hartogs

Moved grp_decr and grp_first_decr register one clock early for timing.

Change 43877 on 2002/08/01 by hartogs@fl_hartogs

Fixed a bug in previous timing fix.

Change 43846 on 2002/08/01 by hartogs@fl_hartogs

Yet another attempt.

Change 43825 on 2002/08/01 by hartogs@fl_hartogs

Attempted to fix timing loop introduced in previous check-in.

Change 43764 on 2002/08/01 by hartogs@fl_hartogs

Fixed sensitivity list errors.

Change 43747 on 2002/08/01 by hartogs@fl_hartogs

Yet another change to meet timing.

Change 43722 on 2002/08/01 by hartogs@fl_hartogs

Added test counter and total test count to the output.

Change 43556 on 2002/07/31 by hartogs@fl_hartogs

Several changes aimed at fixing timing problems.

Change 43508 on 2002/07/31 by bbuchner@fl_bbuchner_r400_win

```
timing modifications:
1 -- move OFLAG and SWAP_S_T Calculation to prior pipeline stage
2 -- calculate partial DELTA terms in prior pipeline stage.

Change 43232 on 2002/07/30 by bbuchner@fl_bbuchner_r400_win

generate delta values a clock earlier for timing (setup)
generate s/t comparision values a clock earlier for timing (walker)

Change 43222 on 2002/07/30 by hartogs@fl_hartogs

Still trying to get synopsys to do what I want.

Change 43192 on 2002/07/30 by hartogs@fl_hartogs

Second attempt at synopsys directive.

Change 43166 on 2002/07/30 by hartogs@fl_hartogs

Added synopsys directives to cause selection of carry-look-ahead components.

Change 43144 on 2002/07/30 by hartogs@fl_hartogs

Deleted grp_te_valid from TE_SETUP_BUSY

Change 42986 on 2002/07/29 by hartogs@fl_hartogs

Fixed sensitivity list errors.

Change 42984 on 2002/07/29 by hartogs@fl_hartogs

Changed grouper from mask-based control to left/right indx tracking control
in attempt to improve worst case timing.

Change 42982 on 2002/07/29 by hartogs@fl_hartogs

Updated for changes to grouper.

Change 42603 on 2002/07/26 by hartogs@hartogs_crayola_unix_orl

Fixed blocking assignment to 'shift_reg_mask_d' to resolve a problem with mixed
blocking/non-blocking assignments to this register (synopsys error).

Change 42551 on 2002/07/25 by efong@efong_crayola_linux_cvd

fixed syntax error
```

```
Change 42494 on 2002/07/25 by hartogs@fl_hartogs2

Added some new signals

Change 42493 on 2002/07/25 by hartogs@fl_hartogs2

Recoded a process to (hopefully) improve timing.

Change 42490 on 2002/07/25 by bbuchner@fl_bbuchner_r400_win

removed vertex data fifo.

Change 42449 on 2002/07/25 by bbuchner@fl_bbuchner_r400_win

fixed incorrect error message in setup
and a few mods for synthesis

Change 42256 on 2002/07/24 by hartogs@fl_hartogs

Fixed sensitivity list errors.

Change 42243 on 2002/07/24 by bbuchner@fl_bbuchner_r400_win

modified calculation of 1-s-t and 1-s-1/3(t) to improve timing.

Change 42237 on 2002/07/24 by hartogs@fl_hartogs

Fixed problem with reset of auto index counter (or lack thereof).

Change 42185 on 2002/07/24 by bbuchner@fl_bbuchner_r400_win

stop simulation on illegal prim type

Change 42184 on 2002/07/24 by bbuchner@fl_bbuchner_r400_win

fixed bug in mux select of DATA_Z

Change 42162 on 2002/07/24 by bbuchner@fl_bbuchner_r400_win

fix sensitivity and latch errors

Change 42077 on 2002/07/23 by hartogs@fl_hartogs

Debugged the event code. This code passes a test case with several events
interleaved with normal 3D packets.

Change 42076 on 2002/07/23 by hartogs@fl_hartogs
```

```
Updated signals for events.

Change 42023 on 2002/07/23 by hartogs@fl_hartogs

Fixed width of the output FIFO. Fixed transmission of the event type field. Fixed
detection of "unknowns".

Change 41964 on 2002/07/23 by hartogs@fl_hartogs

Transmission of event is coded (untested) in this version except for the output block.
This version does not affect the non-event transactions.

Change 41888 on 2002/07/22 by hartogs@fl_hartogs2

Aded pipelined event_flag bit which goes to the passthru block.
Moved the derived state one register earlier.

Change 41668 on 2002/07/19 by hartogs@fl_hartogs

vgt_output.v -- made out_pt_prim_read signal NOT qualified by pt_out_prim_valid
vgt_out_indx.v -- made out_pt_data_read signal NOT qualified by pt_out_indx_valid
vgt.v -- passed all four bits of prim type to the passthru block to handle VGT_TE_QUAD
type.
vgt_passthru.v -- coded.

Change 41613 on 2002/07/19 by hartogs@hartogs_crayola_unix_orl

Fixed sensitivity list problem.

Change 41252 on 2002/07/18 by hartogs@fl_hartogs

Replaced '/ 3' operator in vgt_tess_output with a bit-slice divider.
This divide by three technique is due to the fact that the synopsys (V)HDL Reader
cannot
infer a '/' operator unless both operands are constants. In the vgt_tess_output block,
one of the
operands is a constant, but the other is a wire.

Change 41053 on 2002/07/17 by efong@efong_crayola_linux_cvd

removed the _hacked files

Change 40834 on 2002/07/16 by hartogs@hartogs_crayola_unix_orl

Fixed error in sensitivity list.

Change 40733 on 2002/07/15 by bbuchner@fl_bbuchner_r400_win
```

typo .. change wire to reg

Change 40724 on 2002/07/15 by bbuchner@fl_bbuchner_r400_win

fixed synthesis errors

Change 40711 on 2002/07/15 by bbuchner@fl_bbuchner_r400_win

fixed sensitivity list omissions

Change 40706 on 2002/07/15 by hartogs@fl_hartogs2

Fixed some inferred latches.

Change 40696 on 2002/07/15 by hartogs@fl_hartogs

Renamed clocks in the tessellation engine to be compatible with synthesis scripts.

Change 40656 on 2002/07/15 by hartogs@fl_hartogs

Fixed sensitivity list errors.

Change 40651 on 2002/07/15 by hartogs@fl_hartogs

Fixed sensitivity list error.

Change 40648 on 2002/07/15 by hartogs@fl_hartogs

Fixed sensitivity list error.

Change 40643 on 2002/07/15 by hartogs@fl_hartogs

Fixed sensitivity list error.

Change 40640 on 2002/07/15 by hartogs@fl_hartogs

Fixed some sensitivity list errors.

Change 40636 on 2002/07/15 by hartogs@fl_hartogs

Fixed sensitivity list errors.

Change 40622 on 2002/07/15 by hartogs@fl_hartogs2

Added more signals.

Change 40621 on 2002/07/15 by hartogs@fl_hartogs2

Fixed some sensitivity list errors.

Change 40113 on 2002/07/12 by hartogs@fl_hartogs

Added a 2 word fifo in the prim path to break the backpressure path.

Change 40079 on 2002/07/12 by hartogs@fl_hartogs

Added synthesis-compatible stub instead of real memory macros.

Change 40070 on 2002/07/12 by hartogs@fl_hartogs

Set file type to binary to prevent the line ends from being changed.

Change 40069 on 2002/07/12 by hartogs@fl_hartogs

Set exec file type bit (+w).

Change 40061 on 2002/07/12 by hartogs@fl_hartogs2

Put the vgt_reg.v and pa_reg.v include statements into the vgt_common.v file.

Change 40017 on 2002/07/12 by hartogs@fl_hartogs

Add include "pa_reg.v" to the top of the file

Change 40003 on 2002/07/12 by hartogs@fl_hartogs2

Changed out_indx block to accept indx data into a FIFO independent it related
primitive. Removed the input sel field between the output block and the out_indx block.

Change 39970 on 2002/07/12 by hartogs@fl_hartogs

Changed VGT grouper to force unused components to zero to aide in RTL/EMU vector
checking.

Change 39966 on 2002/07/12 by hartogs@fl_hartogs2

Fixed a bug with quotes in an echo statement.

Change 39933 on 2002/07/12 by hartogs@fl_hartogs2

Changed from SQ_PROVOKING_VTX to PA_SU_SC_MODE_CNTL_PROVOKING_VTX_LAST

Change 39655 on 2002/07/11 by hartogs@fl_hartogs

Added passthru block signals

```
Change 39396 on 2002/07/10 by hartogs@fl_hartogs2

Modified testbench for changes in dumpfiles.

Change 37850 on 2002/07/03 by hartogs@fl_hartogs2

Debussy wave file for vgt testbench

Change 37848 on 2002/07/03 by hartogs@fl_hartogs2

Fixed case where output block was null-terminating a vertex vector that has no entries
in it.

Change 37837 on 2002/07/03 by hartogs@fl_hartogs2

vgt.v & Makefile -- Removed COMPILE_TESS macros.
   regress_vgt_rtl.tcsh -- Improved behavior when files are in use.

Change 37836 on 2002/07/03 by bbuchner@fl_bbuchner_r400_win

fixed typo in test bench
edge flags for pass-through and tess modes are forced to "111"
for triangles, "000" for anything else

Change 37735 on 2002/07/02 by hartogs@fl_hartogs2

Fixed typo.

Change 37732 on 2002/07/02 by hartogs@fl_hartogs2

More small changes

Change 37730 on 2002/07/02 by hartogs@fl_hartogs2

Change that shouldn't matter at all.

Change 37700 on 2002/07/02 by hartogs@fl_hartogs2

Added pass/fail summary file.

Change 37669 on 2002/07/02 by hartogs@fl_hartogs2

Scripts for RTL simulation automation.

Change 37641 on 2002/07/02 by hartogs@fl_hartogs2

Added a "I'm alive" statement that prints every 100,000 clocks.
   Added a timeout detection that occurs if all of the vgt internal interfaces are idle
```

for more than 1000 clocks.

Change 37617 on 2002/07/02 by hartogs@fl_hartogs2

vgt_grouper -- fixed auto_group_counter_q. It was reseting while the pipeline was frozen.
fixed polygon edge flags. Did not previously consider case with one triangle polygon.
vgt_output -- fixed logic for new_vtx_vector flag. Previously allowed generation of new_vtx_vector flag
when prim had no new indices.

Change 37443 on 2002/07/01 by hartogs@fl_hartogs2

Changed code that determines when to dealloc in the output block.

Change 37399 on 2002/07/01 by hartogs@fl_hartogs2

vgt_grouper -- fixed a default assignment to prevent inferred latch.
vgt.v -- fixed the wiring of the HOS state select signal.
vgt_rbiu.v -- fixed the order of the individual fields in the read and write bus of several state registers.

Change 37398 on 2002/07/01 by hartogs@fl_hartogs2

Added logic to cause the vgt testbench to stall the RBBM bus instead of overwritting
state data while it is in use. (This is analogous to the "WAIT_UNTIL" logic in the RBBM in the emulator.)

Change 37381 on 2002/07/01 by bbuchner@fl_bbuchner_r400_win

update TE instantiation names
makefile had a line continuation bug

Change 37206 on 2002/06/28 by hartogs@fl_hartogs2

Fixed a bug in the reuse depth calculation.

Change 37193 on 2002/06/28 by hartogs@fl_hartogs2

Reordered the min/max index clamping test to be consistent with the emulator (and R300).

Change 37146 on 2002/06/28 by hartogs@fl_hartogs2

Fixed a bus width error on the ejection detect logic.

Change 37110 on 2002/06/28 by hartogs@fl_hartogs2

```
vgt_tb -- changed requirements for stoping the simulation
   vgt_grouper -- fixed several bugs in the "load data" decision of the shifter

Change 36934 on 2002/06/27 by hartogs@fl_hartogs

Added Debussy compile flag

Change 36933 on 2002/06/27 by hartogs@fl_hartogs

Added routines to cause Debussy dump files.

Change 36899 on 2002/06/27 by hartogs@fl_hartogs

Changed Makefile to be dependency based. Also can compile for Debussy now.

Change 36874 on 2002/06/27 by hartogs@fl_hartogs

Re-added these files with a lowercase 'v' name.

Change 36873 on 2002/06/27 by hartogs@fl_hartogs

Deleted these files to change their names to lowercase 'v'.

Change 36754 on 2002/06/27 by hartogs@fl_hartogs

Fixed vector checking on the VgtSq interface.

Change 36434 on 2002/06/26 by hartogs@fl_hartogs

vgt_vtx_reuse.v -- coded the force vertex vector ejection (deadlock avoidance) logic.
vgt.v -- wired the ROM_SPx_disable to the vgt_vtx_reuse block.
vgt_tb.v -- broke out the compare for the VgtSq interface to handle the case when the
indx_valid bit is false.

Change 36393 on 2002/06/26 by hartogs@fl_hartogs

Changed VGT_VTX_TIMEOUT_REG to VGT_VTX_VECT_EJECT_REG and wired the
PRIM_COUNT field over to the vertex reuse block.

Change 36263 on 2002/06/25 by hartogs@fl_hartogs

Modified VGT RTL testbench to stop automatically when the RBBM stimulus file
is exhausted and the VGT is no longer busy. Also added checks for compare
files that empty too early or that are not empty at the end of the test.

Change 36249 on 2002/06/25 by hartogs@fl_hartogs
```

```
Fixed a bad typo in the index offset/clamp function.

Change 35937 on 2002/06/24 by hartogs@fl_hartogs

Wired up the busy chain.

Change 35904 on 2002/06/24 by hartogs@fl_hartogs

Removed misleading comment.

Change 35903 on 2002/06/24 by hartogs@fl_hartogs

vgt_rbiu.v -- hooked up state select for vertex_reuse_block_cntl renderstate register
vgt.v -- reduced grp_components_valid signal going into vertex reuse block from 4 bits
to 3 bits.
hooked up vertex_reuse_depth renderstate register and its state select signal.
vgt_out_indx.v -- Fixed up the logic to correctly handle an "invalid indx" for sending
the
end-of-vertex-vector information. This includes getting the index count right on
the VgtPa_clip_v interface.
Renamed the indx (per prim) count for clarity.
vgt_output.v -- Fixed up the logic to correctly handle an "invalid indx" for sending
the
end-of-vertex-vector information.
Put a fifo full check prior to writing the "indx side" fifo.
vgt_vtx_reuse.v -- Removed stub, added real block.

Change 35137 on 2002/06/20 by hartogs@fl_hartogs

Added VGT_RBBM_no_dma_busy signal to the RTL. This
This signal is used by the CP post-fetch parser to perform wait-on instructions
       It deliberately excludes the VGT DMA engine busy signals which are initiated by
the
       CP pre-fetch parser.

Change 35022 on 2002/06/19 by hartogs@fl_hartogs

Made changes to $InitVec() routine calls to accomodate changes in the PLI DLL.

Change 34966 on 2002/06/19 by hartogs@fl_hartogs

Wired up state select for deallocate distance.
Fixed error in static_deallocate_distance signal.

Change 34915 on 2002/06/19 by sallen@sallen_r400_lin_marlboro

remove -Mlib from vcsbuild.pl
   use whatever vcsbuild.pl you find in the lib path
```

```
   ferret: state tweak

Change 34890 on 2002/06/19 by hartogs@fl_hartogs

Added file based interface for DMA interface to MH to the vgt block-level testbench.

Change 34255 on 2002/06/14 by hartogs@fl_hartogs

New version of vgt_dma block. This code has been substantially validated with
random data and random backpressure.

Change 33881 on 2002/06/13 by hartogs@fl_hartogs

Added VGT_DEBUG to vgt_common.v.

Change 33850 on 2002/06/13 by hartogs@fl_hartogs

Deleted tess_input_mode state signal from the design.

Change 33809 on 2002/06/13 by hartogs@fl_hartogs

Changed `DEBUG macros to `VGT_DEBUG macros to facilitate full chip integration.

Change 33801 on 2002/06/13 by rbell@rbell_crayola_sun_cvd

Fixes/hacks to get the first chip integration compile to work.

Change 32510 on 2002/06/06 by hartogs@fl_hartogs

VGT DMA engine is substantially code complete and passes simple, single DMA test.

Change 31493 on 2002/06/03 by hartogs@fl_hartogs

Fixed some inaccurate comments.

Change 31477 on 2002/06/03 by hartogs@fl_hartogs

Fixed the GFX_COPY_STATE register per e-mail dated 5/30/02.
Fixed vgt_rniu module to use correct description of GFX_COPY_STATE register.
Delete GFX_PIPE_CNTL register per the same e-mail.
Added VGT_SQ_event and VGT_PA_clip_p_event signals per e-mail also dated 5/30/02.
Converted entire VGT to "named module ports".

Change 29898 on 2002/05/24 by bbuchner@fl_bbuchner_r400_win

added variable (random) timing on unit inputs
added tracking and dump of state utilization.
```

```
Change 29895 on 2002/05/24 by bbuchner@fl_bbuchner_r400_win

fixed "diamond-rule" bug with lines.  Quad 1 line vertices are now
presented in opposite order.

Change 29758 on 2002/05/23 by hartogs@fl_hartogs

Updated some of the global system signals.
Deleted the vgt_fifo_ctrl code (now using ati_fifo_ctrl).
Added some of the VGT busy tree.
Some progress on the vgt_dma code.

Change 29622 on 2002/05/23 by hartogs@fl_hartogs

Deleting autoreg file.

Change 29479 on 2002/05/22 by bbuchner@fl_bbuchner_r400_win

added non-stubbed version of tessellation engine.
makefile has compile_tess option now to compile just tess engine
default is still to compile with stubbed tess engine, but option
to compile with full tess engine is available.

Change 29477 on 2002/05/22 by bbuchner@fl_bbuchner_r400_win

error message was incorrectly generated for invalid data

Change 29289 on 2002/05/21 by bbuchner@fl_bbuchner_r400_win

fixed bug with null vert

Change 29288 on 2002/05/21 by bbuchner@fl_bbuchner_r400_win

test bench

Change 28827 on 2002/05/17 by hartogs@fl_hartogs

Deleted auto-reg files.

Change 28523 on 2002/05/16 by bbuchner@fl_bbuchner_r400_win

TE passes all functional tests, and 1000K random vectors.
Not yet tested with backpressure

Change 28473 on 2002/05/16 by hartogs@fl_hartogs

Added some error checking code.
```

```
Change 28361 on 2002/05/16 by hartogs@fl_hartogs

Fixed vgt_vtx_reuse stub to operate a peak throughput.
Fixed bug in vgt_output.v block.

Change 28197 on 2002/05/15 by hartogs@fl_hartogs

Added ati_rbbm_intf module to the vgt_rbiu.
This version passes the basic_3d test vectors.

Change 28071 on 2002/05/15 by hartogs@fl_hartogs

Updated for block file changes.

Change 28043 on 2002/05/15 by hartogs@fl_hartogs

Updated for reorganization of the GFX register block files.

Change 27898 on 2002/05/14 by hartogs@fl_hartogs

Deleted unused signal.

Change 27883 on 2002/05/14 by hartogs@fl_hartogs

Updated.

Change 27790 on 2002/05/13 by hartogs@fl_hartogs

Coded the vgt_output block (which now includes a sub block called vgt_out_indx).
The VGT now simulates and passes triangles. The vgt_vtx_reuse stub seems
to have a throttling problem which introduces a clock between triangles.

Change 27144 on 2002/05/09 by bbuchner@fl_bbuchner_r400_win

setup working well with randoms
basic funtionality for lines through entire TE
All funtionality coded.

Change 27067 on 2002/05/08 by hartogs@fl_hartogs

Register field name change.

Change 26780 on 2002/05/07 by hartogs@fl_hartogs

Added macros for the vgt_out_fix2flt module readability.

Change 26777 on 2002/05/07 by hartogs@fl_hartogs
```

```
Added hold signal and changed the interface.

Change 26619 on 2002/05/06 by hartogs@fl_hartogs

Fixed bug in point location adjustment.

Change 26604 on 2002/05/06 by hartogs@fl_hartogs

Added float to fix module and assocated testbench.

Change 25726 on 2002/05/01 by hartogs@fl_hartogs

Switch GFX state registers from the state_storage_reg module to the
ati_rpl_state_storage module.

Change 25627 on 2002/04/30 by bbuchner@fl_bbuchner_r400_win

update all TE units

Change 25551 on 2002/04/30 by hartogs@fl_hartogs

This version compiles and runs the test "rbbm.dmp" file up to
the vgt_output block (which has yet to be written).

Change 25401 on 2002/04/29 by hartogs@fl_hartogs

Yet more changes to the tessellator i/o list.

Change 25373 on 2002/04/29 by hartogs@fl_hartogs

Fixed some sloppy errors in the last change.

Change 25359 on 2002/04/29 by hartogs@fl_hartogs

Updated some signals between the tessellator and the output block

Change 25342 on 2002/04/29 by hartogs@fl_hartogs

Added signals to the grouper common interface bus.

Change 24954 on 2002/04/25 by hartogs@fl_hartogs

Updated to reflect changes in auto_gen files

Change 24697 on 2002/04/24 by fhsien@fhsien_r400_unix_marlboro

Rearrange the order of 'include for mktree
```

```
Change 24548 on 2002/04/23 by hartogs@fl_hartogs

Added index offset and clamp pipe stage and strip/loop/fan/polygon
conversion stage to the grouper.

Change 24452 on 2002/04/23 by hartogs@fl_hartogs

Added another autoreg file.

Change 24449 on 2002/04/23 by hartogs@fl_hartogs

Added auto reg files so that vgt can be built without entire
emulator setup. These files must be kept upto date with the auto
reg versions.

Change 24415 on 2002/04/22 by hartogs@fl_hartogs

New testbench for the grouper

Change 24414 on 2002/04/22 by hartogs@fl_hartogs

The core of the shifter works and the vgt_grouper testbench works.

Change 24110 on 2002/04/20 by hartogs@fl_hartogs

Added GFX state registers to the rbiu.

Change 21027 on 2002/03/29 by hartogs@fl_hartogs

Mantor is trying to establish a naming convention for the
Verilog code. Therefore, a "vector" of indices sent from the VGT to the
Sequencer shall henceforth be known as a "vertex vector"
(analogous to a "pixel vector"). I have changed the following
two signals in the vgt.v file. So it is written so shall it be done.

changed VGT_SQ_end_of_vector to VGT_SQ_end_of_vtx_vect
changed VGT_PA_clip_p_start_vector to VGT_PA_clip_p_new_vtx_vect

Change 20938 on 2002/03/28 by hartogs@fl_hartogs

Added these signals to the VGT_PA_clip_p interface
   VGT_PA_clip_p_edge_flags,      // Edge flags
   VGT_PA_clip_p_null_prim,       // Null primitive flag
   VGT_PA_clip_p_start_vector,    // Start vector bit

Deleted these signals from the VGT_MH interface
   VGT_MH_clientid,            // Client id (always 7 for VGT)
   VGT_MH_write,               // Read/write request (always read for VGT)
```

```
   VGT_MH_phase,               // Command phase (always address phase for vgt)
```

```
Change 20509 on 2002/03/26 by hartogs@fl_hartogs

Fixed VGT_MH_tabbe signal name for top-level integration.

Change 19190 on 2002/03/15 by hartogs@fl_hartogs

Fixed non-conforming signal names

Change 19179 on 2002/03/15 by hartogs@fl_hartogs

Fixed non-conforming signals names.

Change 19161 on 2002/03/15 by hartogs@fl_hartogs

Fixed non-conforming signal names in Verilog

Change 18266 on 2002/03/08 by hartogs@fl_hartogs

Makefile for compiling vgt blocks and test benches.

Change 18262 on 2002/03/08 by hartogs@fl_hartogs

Coded the RBBM input skid fifo, address decode, draw initiator
fifo, dma_request fifo, and the immediate data fifo. The non-fifo
state register writes are NOT coded. The decode for the event
initiator is also NOT coded.

The existing features have been tested with random vectors in
a block level testbench specifically for the vgt_rbiu module.

Change 18254 on 2002/03/08 by hartogs@fl_hartogs

Made some interface changes to the vgt top level.

Change 18253 on 2002/03/08 by hartogs@fl_hartogs

Added register directives (macros) to the vgt_common.v file.

Change 18252 on 2002/03/08 by hartogs@fl_hartogs

Added vgt_tb. This version does not work.

Change 18247 on 2002/03/08 by hartogs@fl_hartogs

Added vgt_fifo_ctrl module and testbench.
This module has been tested with random vectors.
```

```
Change 18031 on 2002/03/07 by bbuchner@fl_bbuchner_r400_win

added tessellation engine hierarchy

Change 17881 on 2002/03/07 by bbuchner@fl_bbuchner_r400_win

updated tessellator interface to include (already muxed) state data.
deleted the state select.

Change 16181 on 2002/02/21 by hartogs@fl_hartogs

Added some missing signals

Change 15677 on 2002/02/15 by mmantor@mmantor_r400_win

Empty module files for first pass wiring. (rsh)

Change 15672 on 2002/02/15 by hartogs@fl_hartogs

First-pass wiring of vgt top level.

Change 13414 on 2002/01/21 by mmantor@mmantor_crayola_sun_orl

       Created the vgt.v shell to get started
```

Change 54189 on 2002/09/27 by viviana@viviana_crayola_unix_orl

Added the virage memory.

Change 54137 on 2002/09/27 by dclifton@dclifton_r400

Added actual rams for synthesis

Change 54130 on 2002/09/27 by dclifton@dclifton_r400

Instantiated the real rams into the fifos.

Change 54107 on 2002/09/27 by dclifton@dclifton_r400

Swapped out pa_ccg_vgt_to_ccgen_fifo, pa_cl_ccgen_to_clipcc_fifo, and
pa_cl_primic_to_clprim_fifo with ati_fifo.

Change 54084 on 2002/09/27 by dclifton@dclifton_r400

Added SC bits for readback of pa_su_sc_mode_cntl register.

Change 54077 on 2002/09/27 by dclifton@dclifton_r400

Added read-back capability to pa_ag and updated tbmod_rbbm_pa to check any reads.

Change 54041 on 2002/09/27 by bhankins@fl_bhankins_r400_win

remove redundant line

Change 54019 on 2002/09/27 by bhankins@fl_bhankins_r400_win

fixed potential bug in clip_vertex_fifo control logic

Change 54008 on 2002/09/27 by bhankins@fl_bhankins_r400_win

Eliminate separate primic_event fifo.

Rename primic_state fifo to vgt_to_clips.

Add null_prim to vgt p bus.

Fix state select bug in pa_cl_vert_store_nopos.

Fix fifo depths to match csim.

Remade tbmod_vgttoclip from scratch.

Change 53928 on 2002/09/26 by dclifton@dclifton_r400

```
Increased input delay of deltas

Change 53567 on 2002/09/25 by dclifton@dclifton_r400

Fixed bit assignment of sv readback.

Change 53403 on 2002/09/24 by dclifton@dclifton_r400

Tightened up clock to improve timing.

Change 53101 on 2002/09/23 by bhankins@fl_bhankins_r400_win

initialized full and empty signals of sx_pending_fifo

Change 53047 on 2002/09/23 by bhankins@fl_bhankins_r400_win

renamed pa_cl_primic_state_fifo

Change 52655 on 2002/09/19 by dclifton@dclifton_r400

Changes for timing improvement

Change 52466 on 2002/09/19 by bhankins@fl_bhankins_r400_win

try to improve on timing.  no functional change.

Change 52390 on 2002/09/18 by dclifton@dclifton_r400

Updated for cumulative changes.

Change 52255 on 2002/09/18 by bhankins@fl_bhankins_r400_win

removed unused signals in clipper-su interface

Change 52104 on 2002/09/17 by dclifton@dclifton_r400

Combined pa_su_ieee_mult32 into a pa_su_ge to make pa_su_ge_mult32 for timing.

Change 52095 on 2002/09/17 by dclifton@dclifton_r400

Fixed bug introduced by timing improvements.

Change 52092 on 2002/09/17 by bhankins@fl_bhankins_r400_win

try to improve timing.  no functional change.

Change 51863 on 2002/09/16 by dclifton@dclifton_r400
```

```
More timing improvements

Change 51836 on 2002/09/16 by dclifton@dclifton_r400

Another small change to improve timing

Change 51814 on 2002/09/16 by dclifton@dclifton_r400

Improvements for timing.

Change 51686 on 2002/09/16 by bhankins@fl_bhankins_r400_win

fixed ifdef SIM for declaration of current_state_edt debug signal

Change 51484 on 2002/09/13 by dclifton@dclifton_r400

Increased width of event_id to 5 bits

Change 51474 on 2002/09/13 by bhankins@fl_bhankins_r400_win

removed unused bit from primic state fifo

Change 51437 on 2002/09/13 by dclifton@dclifton_r400

Increased input delay on init_point_prim input

Change 51432 on 2002/09/13 by bhankins@fl_bhankins_r400_win

increased event id through clipper from 4 to 5 bits

Change 51416 on 2002/09/13 by bhankins@fl_bhankins_r400_win

fix logic error introduced with attempt to improve timing

Change 51407 on 2002/09/13 by dclifton@dclifton_r400

Increased input delay of state variables

Change 51401 on 2002/09/13 by dclifton@dclifton_r400

Increased input delay on input coming from ge0.

Change 51397 on 2002/09/13 by dclifton@dclifton_r400

Increased input delay of inputs coming from mux.

Change 51353 on 2002/09/13 by dclifton@dclifton_r400
```

Ditto.

Change 51351 on 2002/09/13 by dclifton@dclifton_r400

fixed leda error

Change 51338 on 2002/09/13 by dclifton@dclifton_r400

Fixed LEDA errors

Change 51103 on 2002/09/12 by bhankins@fl_bhankins_r400_win

fixed two drivers on one signal

Change 51089 on 2002/09/12 by dclifton@dclifton_r400

Fixed a bunch of leda errors

Change 51045 on 2002/09/12 by bhankins@fl_bhankins_r400_win

sensitivity list fixes

Change 51043 on 2002/09/12 by bhankins@fl_bhankins_r400_win

fix sensitivity lists

Change 50997 on 2002/09/12 by bhankins@fl_bhankins_r400_win

sensitivity list fixes.

rename variable with var_ prefix

Change 50981 on 2002/09/12 by bhankins@fl_bhankins_r400_win

fix sensitivity list

Change 50977 on 2002/09/12 by bhankins@fl_bhankins_r400_win

try to improve on timing. no functional changes.

Change 50959 on 2002/09/12 by bhankins@fl_bhankins_r400_win

removed check of ps_expand

Change 50958 on 2002/09/12 by bhankins@fl_bhankins_r400_win

fix an overzealous fix

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Change 50956 on 2002/09/12 by bhankins@fl_bhankins_r400_win

change erroneous blocking assignments to non blocking

Change 50955 on 2002/09/12 by bhankins@fl_bhankins_r400_win

change erroneous blocking assignments to non blocking

Change 50954 on 2002/09/12 by bhankins@fl_bhankins_r400_win

change erroneous blocking assignments to non blocking

Change 50953 on 2002/09/12 by bhankins@fl_bhankins_r400_win

changed erroneous blocking signals to non blocking

Change 50882 on 2002/09/11 by grayc@grayc_crayola_linux_orl

   file needed for leda

Change 50817 on 2002/09/11 by dclifton@dclifton_r400

SX request also resets timeout count.

Change 50787 on 2002/09/11 by bhankins@fl_bhankins_r400_win

make changes per clip.cpp; issues that Mang encountered while working on the new
clipper design.  this shouldn't break anything.

Change 50777 on 2002/09/11 by bhankins@fl_bhankins_r400_win

try to improve on timing.  no functional changes.

Change 50773 on 2002/09/11 by dclifton@dclifton_r400

Increased input delay of state variables.  Increased AREA_LATENCY to accomodate.

Change 50771 on 2002/09/11 by dclifton@dclifton_r400

fixed lint warnings

Change 50770 on 2002/09/11 by dclifton@dclifton_r400

Fixed lint warnings, added vte_busy to pa_rbbm_busy output

Change 50768 on 2002/09/11 by bhankins@fl_bhankins_r400_win
```

```
fix lint warnings.  no functional change.

Change 50763 on 2002/09/11 by bhankins@fl_bhankins_r400_win

try to improve on timing.  no functional changes.

Change 50492 on 2002/09/10 by bhankins@fl_bhankins_r400_win

add unchecked clipper outputs

Change 50424 on 2002/09/10 by bhankins@fl_bhankins_r400_win

change fifo instance names to align with convention

Change 50214 on 2002/09/09 by bhankins@fl_bhankins_r400_win

fixed sensitivity list

Change 50204 on 2002/09/09 by dclifton@dclifton_r400

Eliminated differences seen between different sim setups with similar vectors.

Change 50180 on 2002/09/09 by bhankins@fl_bhankins_r400_win

bug fix

Change 49945 on 2002/09/06 by bhankins@fl_bhankins_r400_win

removed unused bit from clip_to_arb bus

Change 49941 on 2002/09/06 by dclifton@dclifton_r400

Disabled w sort on clipped points

Change 49896 on 2002/09/06 by dclifton@dclifton_r400

Added trackers for ccg and clipper to arb signals

Change 49763 on 2002/09/05 by dclifton@dclifton_r400

Turned off CLSA flag

Change 49751 on 2002/09/05 by dclifton@dclifton_r400

Added trackers for ve input and output

Change 49645 on 2002/09/05 by bhankins@fl_bhankins_r400_win
```

increased IDLE_CLOCKS

Change 49637 on 2002/09/05 by bhankins@fl_bhankins_r400_win

increased IDLE_CLOCKS

Change 49628 on 2002/09/05 by bhankins@fl_bhankins_r400_win

try to improve on timing. no functional change.

Change 49612 on 2002/09/05 by bhankins@fl_bhankins_r400_win

added two more inputs into the generation of the clipper_busy signal:

current_state_empty from the clipper state machine, and

sx_pending_fifo_empty, from the shader export interface module.

Change 49504 on 2002/09/04 by bhankins@fl_bhankins_r400_win

replace instances of ati_fifo_top with unique modules.

modified Makefile to reflect changes.

Change 49492 on 2002/09/04 by bhankins@fl_bhankins_r400_win

try and improve on timing. no functional changes.

Change 49490 on 2002/09/04 by bhankins@fl_bhankins_r400_win

initial checkin of renaming ati_fifo_top instances to individual names, and setting
default parameters to actual values.

Change 49382 on 2002/09/03 by dclifton@dclifton_r400

Fixed missing 'Done' at end of test

Change 49372 on 2002/09/03 by dclifton@dclifton_r400

A few fixes

Change 49371 on 2002/09/03 by dclifton@dclifton_r400

Fixed w latency in veu

Change 49339 on 2002/09/03 by dclifton@dclifton_r400

Added trackers for vte inputs

Change 49326 on 2002/09/03 by dclifton@dclifton_r400

Fixed these to work

Change 49280 on 2002/09/03 by dclifton@dclifton_r400

Created separate trackers for clip and ccg streams out of vte.

Change 49269 on 2002/09/03 by bhankins@fl_bhankins_r400_win

replace vgt_to_clips fifo with primic_element_fifo and primic_state_fifo.

Change 49256 on 2002/09/03 by bhankins@fl_bhankins_r400_win

fix some memset problems that show up on null prims, where the csim outputs 0's.

Change 49117 on 2002/08/30 by dclifton@dclifton_r400

Trackers for internal clipper data buses.

Change 49116 on 2002/08/30 by dclifton@dclifton_r400

Fixed test bench for turn key switch to clipper stand-alone dumps.

Change 49057 on 2002/08/30 by bhankins@fl_bhankins_r400_win

stop some hangs

Change 49009 on 2002/08/30 by dclifton@dclifton_r400

Integrated pa_vte_seu into pa_vte_veu to reduce critical paths in synthesis.

Change 48767 on 2002/08/29 by bhankins@fl_bhankins_r400_win

fix bug to force another vertex path write sequence when the number of unique verts exceeds 64.

Change 48710 on 2002/08/29 by bhankins@fl_bhankins_r400_win

move state select back one clock

Change 48709 on 2002/08/29 by bhankins@fl_bhankins_r400_win

modify to more closely match when csim does memset 0 to positions

Change 48650 on 2002/08/28 by dclifton@dclifton_r400

Changed I/O timing requirements for seu to veu I/O to eliminate critical path.

Change 48543 on 2002/08/28 by bhankins@fl_bhankins_r400_win

remove some commented lines

Change 48514 on 2002/08/28 by dclifton@dclifton_r400

Removed all state locking for events.

Change 48493 on 2002/08/28 by dclifton@dclifton_r400

Not locking state for cache flush

Change 48492 on 2002/08/28 by bhankins@fl_bhankins_r400_win

changed state variable index used by vert_store from that coming from ccg to that coming from primic interface, and removed state_var_indx from ccg to clip interface.

Change 48460 on 2002/08/28 by bhankins@fl_bhankins_r400_win

Make change to match clip.cpp changelist #48374

Change 48459 on 2002/08/28 by bhankins@fl_bhankins_r400_win

change the way we count unique verts in the primitive path to decide when it's time to force another write down the vertex path.

Change 48390 on 2002/08/27 by dclifton@dclifton_r400

Fixed test bench and I/O for active high CG_PA_pm_en

Change 48356 on 2002/08/27 by bhankins@fl_bhankins_r400_win

rename vgt p bus null_prim signal to event_flag

Change 48354 on 2002/08/27 by bhankins@fl_bhankins_r400_win

rename null_prim on vgt p bus to event_flag

Change 48348 on 2002/08/27 by sallen@sallen_r400_lin_marlboro

update _pm_enb to use positive sense of clock

Change 48332 on 2002/08/27 by bhankins@fl_bhankins_r400_win

change array preprocessor switch name to be less generic

```
Change 48300 on 2002/08/27 by dclifton@dclifton_r400

Fixed w sort for degenerate triangles

Change 48209 on 2002/08/27 by bhankins@fl_bhankins_r400_win

removed commented line.

Change 48120 on 2002/08/26 by dclifton@dclifton_r400

Update to file name for clipper stand alone

Change 47996 on 2002/08/26 by bhankins@fl_bhankins_r400_win

connect clip_state_var_indx_r0

Change 47822 on 2002/08/23 by dclifton@dclifton_r400

File name hocus-pocus

Change 47817 on 2002/08/23 by bhankins@fl_bhankins_r400_win

remove testing for rtr on vertex path before doing write to primitive path.

Change 47810 on 2002/08/23 by bhankins@fl_bhankins_r400_win

fix bug where state machine wasn't sourcing point size value.

Change 47808 on 2002/08/23 by bhankins@fl_bhankins_r400_win

enable clipper vert_store to access point size memory when the ccg isn't.

Change 47801 on 2002/08/23 by dclifton@dclifton_r400

Updated input data definition for clipper stand-alone

Change 47736 on 2002/08/23 by bhankins@fl_bhankins_r400_win

try to improve on timing.  no functional change.

Change 47735 on 2002/08/23 by bhankins@fl_bhankins_r400_win

revert to 8-14 version

Change 47505 on 2002/08/22 by bhankins@fl_bhankins_r400_win

mod to support pa_cl_vert_store.v split into
```

pa_cl_vert_store_nopos.v and pa_cl_vert_store_pos.v

Change 47504 on 2002/08/22 by bhankins@fl_bhankins_r400_win

initial checkin of splitting up pa_cl_vert_store.v

Hierarchy:

  pa_cl_vert_store.v

    pa_cl_vert_store_nopos.v

    pa_cl_vert_store_pos.v

Change 47490 on 2002/08/22 by bhankins@fl_bhankins_r400_win

fix to support vertex reuse. re-do the way we count unique vertices sent on the primitive bus.

Change 47280 on 2002/08/21 by bhankins@fl_bhankins_r400_win

modify previous fix to try to prevent introducing a problem when

the vgt_to_ccgen fifo is full, of overwriting the fifo.

Change 47218 on 2002/08/21 by bhankins@fl_bhankins_r400_win

remove vertex fifo rtr qualifier for reading from prim file.

Not sure if this will cause problems later, but fixes a test

that hangs when vertex fifo fills - clipper waits on new

prims to be received, while tbmod_vgttoclip waits for vertex rtr

before sending prims.

Change 46668 on 2002/08/17 by smoss@smoss_crayola_linux_orl_regress

   New results directory

Change 46608 on 2002/08/16 by dclifton@dclifton_r400

Fixed w sort for degenerate triangles-

Change 46494 on 2002/08/16 by dclifton@dclifton_r400

fixed expand_line_width bit position

Change 46449 on 2002/08/16 by dclifton@dclifton_r400

Added checking clipped bit

Change 46359 on 2002/08/15 by smoss@smoss_crayola_linux_orl_regress

   Removed stop() from VGT used finish

Change 46047 on 2002/08/14 by dclifton@dclifton_r400

Updated pa testbench to use dmp files for multiple contexts

Change 45964 on 2002/08/14 by bhankins@fl_bhankins_r400_win

add support for tbmod_vgt_event

Change 45963 on 2002/08/14 by bhankins@fl_bhankins_r400_win

connected tbmod_vgt_event to output port

Change 45930 on 2002/08/14 by dclifton@dclifton_r400

Fix bit position of expand_lw_enable bit in sc_line_cntl

Change 45909 on 2002/08/14 by bhankins@fl_bhankins_r400_win

bug fixes

Change 45698 on 2002/08/13 by bhankins@fl_bhankins_r400_win

add some debug signals

Change 45626 on 2002/08/13 by dclifton@dclifton_r400

Changes to fix tbmod_rbbm_wait

Change 45603 on 2002/08/13 by bhankins@fl_bhankins_r400_win

output state_var_indx for clipped prims per clip.cpp, changelist 44700.

Change 45497 on 2002/08/12 by dclifton@dclifton_r400

Doubled max sim length

Change 45488 on 2002/08/12 by dclifton@dclifton_r400

Added checking for write to VGT_EVENT_INITIATOR register although it doesn't do

anything yet

Change 45450 on 2002/08/12 by dclifton@dclifton_r400

Disabled clip bit on culled null prims.

Change 45400 on 2002/08/12 by dclifton@dclifton_r400

Removed bit range for single bit signals

Change 45381 on 2002/08/12 by dclifton@dclifton_r400

Enabled checking of zmin/zmax.

Change 45373 on 2002/08/12 by grayc@grayc_r400_win

temp fix for read data bus

Change 45371 on 2002/08/12 by dclifton@dclifton_r400

Added statements that can be uncommented to run clipper stand-alone tests.

Change 45185 on 2002/08/09 by mmang@fl_mmang_r400_win

Added logic to support state based point size ucp clipping in clipper.

Change 44985 on 2002/08/08 by dclifton@dclifton_r400

Stand-alone testbench for pa_cl_ve

Change 44969 on 2002/08/08 by dclifton@dclifton_r400

Fixed multiplier table for expanded line width.

Change 44956 on 2002/08/08 by bhankins@fl_bhankins_r400_win

implement latest changes - nan discard, bad pipe support, and state

based point size during ucp clipping.

Change 44885 on 2002/08/08 by dclifton@dclifton_r400

Widened zmin/zmax to allow clamp -8 to +8, forced backfacing to zero for normal lines
and points.

Change 44390 on 2002/08/06 by smoss@smoss_crayola_linux_orl_regress

redistribution of tests

Change 44371 on 2002/08/06 by bhankins@fl_bhankins_r400_win

remove multi-dimensional access to please synopsys

Change 44298 on 2002/08/05 by dclifton@dclifton_r400

Fixed bug introduced when deleting inputs that were tied hi/low.

Change 44226 on 2002/08/05 by bhankins@fl_bhankins_r400_win

add comments for number of flops/process

Change 44221 on 2002/08/05 by bhankins@fl_bhankins_r400_win

removed unused vte_positions_vte_orig_nxt flops

Change 44214 on 2002/08/05 by bhankins@fl_bhankins_r400_win

don't reset prim_back_point_valid if we're being stalled by the su.

Change 44124 on 2002/08/03 by bhankins@fl_bhankins_r400_win

fix bug to hold off from starting until receiving the first init

Change 44082 on 2002/08/02 by dclifton@dclifton_r400

Connected su_busy to su_status read.

Change 44078 on 2002/08/02 by dclifton@dclifton_r400

Deleting unused i/o between blocks.

Change 44075 on 2002/08/02 by dclifton@dclifton_r400

One of the buffered selects was not attached.

Change 44073 on 2002/08/02 by dclifton@dclifton_r400

Removed srst and vte_vpipe_rts connections to pa_vte_veu since they were not being used.

Change 44069 on 2002/08/02 by dclifton@dclifton_r400

Removed iEXP_BIASED input and associated logic from pa_su_rcpeng32 to eliminate synthesis warnings.

Change 44036 on 2002/08/02 by dclifton@dclifton_r400

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Removed en input from pa_vte_pipe

Change 44034 on 2002/08/02 by dclifton@dclifton_r400

Changed default depth to 2 to eliminate synthesis warning about loop not executed.

Change 44015 on 2002/08/02 by dclifton@dclifton_r400

Corrected a few mismatches with polymode.

Change 43965 on 2002/08/02 by bhankins@fl_bhankins_r400_win

bug fix in state variable indx output

Change 43949 on 2002/08/02 by bhankins@fl_bhankins_r400_win

bug fix

Change 43928 on 2002/08/02 by bhankins@fl_bhankins_r400_win

bug fix to stop inits when pa fifos are full

Change 43843 on 2002/08/01 by dclifton@dclifton_r400

..

Change 43840 on 2002/08/01 by dclifton@dclifton_r400

Reverting to rev 30

Change 43832 on 2002/08/01 by dclifton@dclifton_r400

Reverted previous changes--they were invalid

Change 43821 on 2002/08/01 by dclifton@dclifton_r400

Replaced zmin/zmax logic changes that had somehow been deleted.

Change 43733 on 2002/08/01 by bhankins@fl_bhankins_r400_win

removed debug signal

Change 43725 on 2002/08/01 by bhankins@fl_bhankins_r400_win

fixed some synopsys warnings

Change 43686 on 2002/08/01 by bhankins@fl_bhankins_r400_win
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remove point size from check

Change 43660 on 2002/08/01 by bhankins@fl_bhankins_r400_win

fix bugs and make closer to csim

Change 43659 on 2002/08/01 by bhankins@fl_bhankins_r400_win

add point size to check

Change 43657 on 2002/08/01 by bhankins@fl_bhankins_r400_win

separate position and point size write addresses

Change 43584 on 2002/07/31 by grayc@grayc_crayola_linux_orl

   removed checking of zmin and zmax

Change 43542 on 2002/07/31 by grayc@grayc_r400_win

moved pli source to new location in src/common/mti_pli

Change 43514 on 2002/07/31 by dclifton@dclifton_r400

Fixed a problem with polymode where front and back sides drew the same prim.

Change 43506 on 2002/07/31 by grayc@grayc_crayola_linux_orl

   point to new location for pli code

Change 43495 on 2002/07/31 by smoss@smoss_crayola_linux_orl_regress

new path

Change 43462 on 2002/07/31 by smoss@smoss_crayola_linux_orl_regress

modified for cron

Change 43442 on 2002/07/31 by dclifton@dclifton_r400

Fixes for polymode clipped lines.

Change 43351 on 2002/07/31 by bhankins@fl_bhankins_r400_win

removed unused signals

Change 43338 on 2002/07/31 by bhankins@fl_bhankins_r400_win
```

removed provoking_vertex output from pa_clipper.v

Change 43326 on 2002/07/31 by bhankins@fl_bhankins_r400_win

fixed sensitivity list

Change 43324 on 2002/07/31 by bhankins@fl_bhankins_r400_win

sensitivity list fix

Change 43319 on 2002/07/31 by bhankins@fl_bhankins_r400_win

bug fix in selection of point size memory read address

Change 43307 on 2002/07/31 by bhankins@fl_bhankins_r400_win

fixed primic_to_clprim width; removed point size.

Change 43304 on 2002/07/31 by bhankins@fl_bhankins_r400_win

increased pa s-bus input prim_type from 3 to 4 bits

Change 43136 on 2002/07/30 by dclifton@dclifton_r400

Made all margins and tabs uniform

Change 42967 on 2002/07/29 by dclifton@dclifton_r400

Optimizations for polymode.

Change 42896 on 2002/07/29 by dclifton@dclifton_r400

Disabled polymode if front and back types are triangles. Enabled "one side fits all" polymode if front and back types are both lines or points.

Change 42747 on 2002/07/26 by dclifton@dclifton_r400

Fixed polymode zmin, zmax to give limits on just the z values used. Fixed problem with polymode & no edge flags set.

Change 42692 on 2002/07/26 by dclifton@dclifton_r400

Corrected ram depth values

Change 42624 on 2002/07/26 by dclifton@dclifton_r400

Added zmin, zmax checking.

Change 42621 on 2002/07/26 by dclifton@dclifton_r400

Fixed zmin, zmax and added checking to tb

Change 42594 on 2002/07/26 by dclifton@dclifton_r400

Update to cull clipped polymode points and sort baryc values of clipped polymode lines so that k values are always zero.

Change 42585 on 2002/07/26 by smoss@smoss_crayola_linux_orl_regress

        added

Change 42412 on 2002/07/25 by dclifton@dclifton_r400

Removed reset from pa_rbiu

Change 42410 on 2002/07/25 by dclifton@dclifton_r400

Updated sensitivity lists.

Change 42406 on 2002/07/25 by bhankins@fl_bhankins_r400_win

undo previous change. hangs some tests. will investigate.

Change 42377 on 2002/07/25 by grayc@grayc_r400_win

files needed for regressions

Change 42375 on 2002/07/25 by grayc@grayc_r400_win

files for tb_pa

Change 42353 on 2002/07/25 by bhankins@fl_bhankins_r400_win

updates to point size. still needs work to match csim.

Change 42352 on 2002/07/25 by bhankins@fl_bhankins_r400_win

updates

Change 42339 on 2002/07/25 by bhankins@fl_bhankins_r400_win

altered the priority of read access to pointsize memory

Change 42317 on 2002/07/25 by bhankins@fl_bhankins_r400_win

use point (not position) address, for writing to point and position memories, since it is updated last.

Change 42315 on 2002/07/25 by bhankins@fl_bhankins_r400_win

removed duplicate logic

Change 42297 on 2002/07/24 by dclifton@dclifton_r400

Put ram parameters in include file

Change 42293 on 2002/07/24 by dclifton@dclifton_r400

Added an ij0_pipe to pa_su. Put all memory size info in pa_su_lat_def.v.

Change 42286 on 2002/07/24 by dclifton@dclifton_r400

Actually added the xyz_pipe this time

Change 42283 on 2002/07/24 by dclifton@dclifton_r400

Added another ram-based pipeline to setup. changed name of pa_su_geom_pipe_cntl to pa_su_pipe_cntl

Change 42265 on 2002/07/24 by dclifton@dclifton_r400

Changes to improve and fix polymode. Also removed parameter definition for pa_su_geom_pipe in pa_su.v.

Change 42205 on 2002/07/24 by bhankins@fl_bhankins_r400_win

1. move event input from p to s bus

2. add in event and event_id

3. start to add in point size logic. still has bugs.

Change 42201 on 2002/07/24 by bhankins@fl_bhankins_r400_win

fix synthesis warning

Change 42161 on 2002/07/24 by bhankins@fl_bhankins_r400_win

added logic for clipper read access to point size memory

Change 42091 on 2002/07/23 by grayc@grayc_crayola_linux_orl

   changes for linux an dv vcs compiles

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Change 41997 on 2002/07/23 by grayc@grayc_crayola_linux_orl

   files needed for modelsim

Change 41853 on 2002/07/22 by dclifton@dclifton_r400

Added check for event and event_id

Change 41850 on 2002/07/22 by dclifton@dclifton_r400

Fixed tracker to check all 40 bits of PA_SC_P1 output

Change 41508 on 2002/07/19 by dclifton@dclifton_r400

Added syn_stub code

Change 41503 on 2002/07/19 by dclifton@dclifton_r400

Slight decrease in clock period to improve synthesis timing

Change 41472 on 2002/07/19 by dclifton@dclifton_r400

Fixed a problem with draw direction on rectangles

Change 41438 on 2002/07/19 by bhankins@fl_bhankins_r400_win

fix

Change 41392 on 2002/07/18 by dclifton@dclifton_r400

Turned register pipe into ram-based pipe

Change 41391 on 2002/07/18 by dclifton@dclifton_r400

Turned a register pipe into a ram-based pipe.  Fixed a problem with attr_indx2 on
points and lines.

Change 41305 on 2002/07/18 by bhankins@fl_bhankins_r400_win

add mechanism to keep sending input on vertex interface to pa for multiple (64-big)
groups of vertices.

Change 41286 on 2002/07/18 by dclifton@dclifton_r400

Fixed hang on send init at end of file

Change 41263 on 2002/07/18 by dclifton@dclifton_r400
```

Consolodating several module compiler blocks to speed synthesis.

Change 41207 on 2002/07/18 by bhankins@fl_bhankins_r400_win

add readback of VTX_KILL_OR state bit

Change 41199 on 2002/07/18 by grayc@grayc_crayola_unix_orl

changed component name for Stub'd memory

Change 41186 on 2002/07/17 by efong@efong_crayola_linux_cvd

fixed syntax error on the parameter line

Change 41177 on 2002/07/17 by dclifton@dclifton_r400

Fixed precision issue with pa_su_rcpeng32. Enabled checking 32 bit mantissa in tb_pa_su

Change 41152 on 2002/07/17 by dclifton@dclifton_r400

removed infer_mux directive

Change 41150 on 2002/07/17 by dclifton@dclifton_r400

Fixed 'for' loop bounds

Change 41047 on 2002/07/17 by dclifton@dclifton_r400

Fixed polymode operation to output facing triangle as a null prim so that scan converter can grab max Zx/Zy for polygon offset.

Change 41019 on 2002/07/17 by bhankins@fl_bhankins_r400_win

update to match dumps

Change 40997 on 2002/07/17 by bhankins@fl_bhankins_r400_win

moved srst to just after clock edge

Change 40996 on 2002/07/17 by dclifton@dclifton_r400

Replace updated version of pa_cl_ve.bvrl, reverted pa to use lower case I/O names in pa_cl_ve

Change 40989 on 2002/07/17 by grayc@grayc_r400_win

fixed syntax errors from previous checkin

```
Change 40988 on 2002/07/17 by grayc@grayc_crayola_unix_orl

removed defparam (not supported by synthesis) ... added dum_mem_syn_stub where needed

Change 40982 on 2002/07/17 by grayc@grayc_crayola_unix_orl

removed defparam (not supported by synthesis)

Change 40974 on 2002/07/17 by bhankins@fl_bhankins_r400_win

change to match pa_cl_ve i/o signal names

Change 40940 on 2002/07/16 by dclifton@dclifton_r400

pa_su_geom_prep uses sign bit in determining if all w's equal for force-w-to-one
function.  All other files have just had the parameter statements removed from input
list.

Change 40668 on 2002/07/15 by bhankins@fl_bhankins_r400_win

removed "===" from vhdl -> verilog translation utility

Change 40665 on 2002/07/15 by dclifton@dclifton_r400

Updated versions of bvrl's compiled with changes for synthesis.

Change 40652 on 2002/07/15 by mmang@fl_mmang_r400_win

Added AG logic for point sprite clipping states.

Change 40129 on 2002/07/12 by dclifton@dclifton_r400

Eliminated 28 bit versions of pa_su_ieee_mult and pa_su_rcpeng.
Removed dps files and updated mc files to use new synthesis flow.
Removed pa_rcpeng which is not being used.

Change 40040 on 2002/07/12 by dclifton@dclifton_r400

vgtpaclips file still has event flag in it.

Change 40037 on 2002/07/12 by dclifton@dclifton_r400

Delete several unused signals

Change 40010 on 2002/07/12 by dclifton@dclifton_r400

Fixed typo in for loop
```

```
Change 39973 on 2002/07/12 by dclifton@dclifton_r400

First check-in of new state variable design.

Change 39963 on 2002/07/12 by bhankins@fl_bhankins_r400_win

added support for event flag (needs to be uncommented)

Change 39950 on 2002/07/12 by bhankins@fl_bhankins_r400_win

decrease ccgen to clip fifo depth

Change 39913 on 2002/07/12 by bhankins@fl_bhankins_r400_win

add expect signals for debug

Change 39793 on 2002/07/11 by dclifton@dclifton_r400

Fixed continue signals so that eop can be reached.

Change 39783 on 2002/07/11 by dclifton@dclifton_r400

Fixed case where cid count is both incremented and decremented

Change 39751 on 2002/07/11 by dclifton@dclifton_r400

More fixes for stalling

Change 39713 on 2002/07/11 by bhankins@fl_bhankins_r400_win

minor bug fix

Change 39711 on 2002/07/11 by dclifton@dclifton_r400

Added delay to continue signals to eliminate double send from same trigger

Change 39500 on 2002/07/10 by dclifton@dclifton_r400

Update for 32-bit z precision

Change 39499 on 2002/07/10 by dclifton@dclifton_r400

Updates for Z precision and provoking vtx changes

Change 39449 on 2002/07/10 by bhankins@fl_bhankins_r400_win

change compare to use CompareVec
```

Change 39417 on 2002/07/10 by bhankins@fl_bhankins_r400_win

fix clip_su_st_indx checker

Change 39416 on 2002/07/10 by bhankins@fl_bhankins_r400_win

fix vgt i/f drivers (again)

Change 39413 on 2002/07/10 by bhankins@fl_bhankins_r400_win

increased IDLE_CLOCKS

Change 39358 on 2002/07/10 by grayc@grayc_r400_win

initial release of rand script for tb_pa_su

Change 39324 on 2002/07/10 by dclifton@dclifton_r400

Connected continue signals to read_data signals

Change 39301 on 2002/07/10 by bhankins@fl_bhankins_r400_win

bug fix

Change 39294 on 2002/07/10 by bhankins@fl_bhankins_r400_win

update

Change 39293 on 2002/07/10 by bhankins@fl_bhankins_r400_win

update

Change 39109 on 2002/07/09 by bhankins@fl_bhankins_r400_win

add test for context id

Change 39099 on 2002/07/09 by bhankins@fl_bhankins_r400_win

bug fix; state id not properly being passed to su interface

Change 39071 on 2002/07/09 by bhankins@fl_bhankins_r400_win

bug fix

Change 39026 on 2002/07/09 by bhankins@fl_bhankins_r400_win

cleanup baryc-su i/f, and add ability to get point size from ag.

```
Change 38733 on 2002/07/08 by dclifton@dclifton_r400

A few fixes

Change 38665 on 2002/07/08 by bhankins@fl_bhankins_r400_win

add separate cl/su baryc i/f

Change 38656 on 2002/07/08 by dclifton@dclifton_r400

32-bit precision on p1 output

Change 38651 on 2002/07/08 by bhankins@fl_bhankins_r400_win

add separate baryc i/f to su

Change 38413 on 2002/07/05 by dclifton@dclifton_r400

Speeded up sv interaction between sv and prims

Change 37851 on 2002/07/03 by bhankins@fl_bhankins_r400_win

bug fixes that show up when the su pushes back on the clipper

Change 37625 on 2002/07/02 by bhankins@fl_bhankins_r400_win

increase skid size for now

Change 37623 on 2002/07/02 by bhankins@fl_bhankins_r400_win

include su_clip_rtr as qualifier

Change 37405 on 2002/07/01 by dclifton@dclifton_r400

Fixed float to fixed conversion of clip_su_pt_size

Change 37375 on 2002/07/01 by dclifton@dclifton_r400

Fixed sv_load_cont getting dropped on frz

Change 37374 on 2002/07/01 by bhankins@fl_bhankins_r400_win

increase vector_latency by 1

Change 37207 on 2002/06/28 by dclifton@dclifton_r400

Fixed handling of rectangles
```

```
Change 37123 on 2002/06/28 by dclifton@dclifton_r400

bug fix for zero length lines

Change 37121 on 2002/06/28 by dclifton@dclifton_r400

Added unlimited prim capability

Change 37058 on 2002/06/28 by dclifton@dclifton_r400

Eliminated screening of user clip plane updates

Change 36931 on 2002/06/27 by dclifton@dclifton_r400

fixed another sort bug with degenerate triangles

Change 36923 on 2002/06/27 by dclifton@dclifton_r400

Increased prim capability

Change 36917 on 2002/06/27 by dclifton@dclifton_r400

bug fix for seeing degenerate triangles as right triangles

Change 36871 on 2002/06/27 by dclifton@dclifton_r400

increased primitive count capability

Change 36856 on 2002/06/27 by dclifton@dclifton_r400

Fixing use of getvec statements to account for pli_mti.dll changes.

Change 36827 on 2002/06/27 by dclifton@dclifton_r400

Makefile for tb_su

Change 36826 on 2002/06/27 by dclifton@dclifton_r400

Update for batch sims with su

Change 36790 on 2002/06/27 by bhankins@fl_bhankins_r400_win

fix rtrs to vgt

Change 36779 on 2002/06/27 by bhankins@fl_bhankins_r400_win

fix
```

Change 36756 on 2002/06/27 by bhankins@fl_bhankins_r400_win

add reset to remove unknowns

Change 36741 on 2002/06/27 by dclifton@dclifton_r400

Changes for new mti_pli and vgt interface

Change 36737 on 2002/06/27 by bhankins@fl_bhankins_r400_win

fix sensitivity lists

Change 36717 on 2002/06/27 by bhankins@fl_bhankins_r400_win

add tbtrk_clsu

Change 36710 on 2002/06/27 by bhankins@fl_bhankins_r400_win

wire in pa_cl_rei

Change 36461 on 2002/06/26 by bhankins@fl_bhankins_r400_win

extended reset by 2 clocks to remove some unknowns in pa_cl_rei.v

Change 36460 on 2002/06/26 by bhankins@fl_bhankins_r400_win

cleaned up vhdl to verilog translation

Change 36447 on 2002/06/26 by grayc@grayc_r400_win

added new functions GetLineNum GetMisCompareCnt

Change 36419 on 2002/06/26 by grayc@grayc_r400_win

modify random function more ...

Change 36417 on 2002/06/26 by grayc@grayc_r400_win

modify reporting of compareVec to return validvectorcnt

Change 36366 on 2002/06/26 by bhankins@fl_bhankins_r400_win

fix

Change 36365 on 2002/06/26 by grayc@grayc_r400_win

modify GetVec so that it returns a 0 when reading the last valid vector

```
Change 36255 on 2002/06/25 by rramsey@rramsey_crayola_linux_orl

Modify get and compare vec so correct number of compares happen
add maxargs to compare and get vec

Change 36172 on 2002/06/25 by bhankins@fl_bhankins_r400_win

fixes

Change 36155 on 2002/06/25 by bhankins@fl_bhankins_r400_win

fix

Change 36151 on 2002/06/25 by dclifton@dclifton_r400

Removed clk waits from both drivers

Change 35871 on 2002/06/24 by dclifton@dclifton_r400

Added capability to run batch mode

Change 35810 on 2002/06/24 by dclifton@dclifton_r400

removed defparam statements because of synthesis limitations

Change 35800 on 2002/06/24 by bhankins@fl_bhankins_r400_win

sensitivity list fix

Change 35774 on 2002/06/24 by dclifton@dclifton_r400

Updating latencies

Change 35771 on 2002/06/24 by grayc@grayc_r400_win

fix to only put valid data for call to GetVec()

Change 35740 on 2002/06/24 by bhankins@fl_bhankins_r400_win

used the right flop for busy signal

Change 35556 on 2002/06/21 by bhankins@fl_bhankins_r400_win

put some more logic behind PA_RBBM_busy to include clipper and

input and output dff's.
```

Change 35524 on 2002/06/21 by bhankins@fl_bhankins_r400_win

add mismatch signal for debug

Change 35100 on 2002/06/20 by bhankins@fl_bhankins_r400_win

add tracker for clipper-to-su interface

Change 35095 on 2002/06/20 by bhankins@fl_bhankins_r400_win

started to add event signal into pa. for now it pretty much passes through from vgt through 1-clk clipper to su.

Change 35055 on 2002/06/19 by dclifton@dclifton_r400

Fixed handshaking between tbmod_rbbm_pa and tbmod_vgttoclip

Change 34987 on 2002/06/19 by dclifton@dclifton_r400

Test bench update to add wait signal for tbmod_rbbm_pa block and to update InitVec routines.

Change 34962 on 2002/06/19 by rramsey@rramsey_crayola_linux_orl

Add .tab file for vcs compiles
Update InitVec function to execute on REASON_CALLTF
Update sc_qdpr_proc tb to run with VCS

Change 34912 on 2002/06/19 by bhankins@fl_bhankins_r400_win

added 3rd parameter for InitVec to match latest mti_pli.dll

Change 34889 on 2002/06/19 by bhankins@fl_bhankins_r400_win

replace tbmod_vgttoclipp/s/v.v with tbmod_vgttoclip.v

Change 34805 on 2002/06/18 by dclifton@dclifton_r400

fixed delay on vgt_init and vgt_cid output signals

Change 34785 on 2002/06/18 by dclifton@dclifton_r400

Fixed endless loop condition

Change 34707 on 2002/06/18 by bhankins@fl_bhankins_r400_win

fixed index to clip_disable state bit

```
Change 34697 on 2002/06/18 by dclifton@dclifton_r400

Align latency with vector engine

Change 34626 on 2002/06/17 by dclifton@dclifton_r400

Added capability to screen out inapplicable rbbm writes.

Change 34579 on 2002/06/17 by dclifton@dclifton_r400

Finishing multiple state variable capability in tb_pa.  Fixed bugs with copy in
pa_rbiu.

Change 34554 on 2002/06/17 by grayc@grayc_r400_win

fix for 0 valid vector files

Change 34526 on 2002/06/17 by bhankins@fl_bhankins_r400_win

add 1 to param_cache_indx state

Change 34517 on 2002/06/17 by dclifton@dclifton_r400

Fixing copy state

Change 34503 on 2002/06/17 by sallen@sallen_r400_lin_marlboro

ferret: use GUI_ACTIVE
   ferret: add help to construct files (cons -h)
   ferret: add idle counter reset when register driven

Change 34499 on 2002/06/17 by dclifton@dclifton_r400

Fixed bugs in state variable update

Change 34459 on 2002/06/17 by dclifton@dclifton_r400

fixed address bus shift

Change 34434 on 2002/06/17 by dclifton@dclifton_r400

Fixed test bench to handle multiple states

Change 34149 on 2002/06/14 by bhankins@fl_bhankins_r400_win

fix sensitivity list

Change 34052 on 2002/06/14 by bhankins@fl_bhankins_r400_win
```

dumps to match current executable and test bench

Change 34051 on 2002/06/14 by bhankins@fl_bhankins_r400_win

executable matches test bench and dumps in tbfiles

Change 34049 on 2002/06/14 by bhankins@fl_bhankins_r400_win

files to match current test bench and executable

Change 33822 on 2002/06/13 by bhankins@fl_bhankins_r400_win

executable used to test current version of

clipper and sxifccg

Change 33821 on 2002/06/13 by bhankins@fl_bhankins_r400_win

misc fixes

Change 33578 on 2002/06/12 by dclifton@dclifton_r400

Added new clipper/su baryc interface to SU, added VGT draw initiator state variable for SU

Change 33525 on 2002/06/12 by bhankins@fl_bhankins_r400_win

update shader export interface, clip code generator and

clipper to match csim ccgen.cpp and clip.cpp

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Change 33524 on 2002/06/12 by mmang@fl_mmang_r400_win

Added clipper decode support for SMC_T_BLEND_(PREV/CURR)_(0/1), SMC_CLIP_DIST_(VV/UCP), SMC_EDGE_DISTANCE_(0/1), and SMC_T_FACTOR_(PREV/CURR)_(0/1).

Change 33048 on 2002/06/10 by bhankins@fl_bhankins_r400_win

fixes

Change 32927 on 2002/06/10 by bhankins@fl_bhankins_r400_win

fix

Change 32698 on 2002/06/07 by bhankins@fl_bhankins_r400_win

```
updates

Change 32689 on 2002/06/07 by bhankins@fl_bhankins_r400_win

initial checkin

Change 32655 on 2002/06/07 by bhankins@fl_bhankins_r400_win

updates

Change 32637 on 2002/06/07 by bhankins@fl_bhankins_r400_win

initial checkin

Change 32636 on 2002/06/07 by bhankins@fl_bhankins_r400_win

deleted

Change 32635 on 2002/06/07 by bhankins@fl_bhankins_r400_win

updates

Change 32575 on 2002/06/07 by bhankins@fl_bhankins_r400_win

initial checkin

Change 32552 on 2002/06/07 by bhankins@fl_bhankins_r400_win

changed prim_type to 3 bits

Change 32548 on 2002/06/07 by bhankins@fl_bhankins_r400_win

changed prim_type to 3 bits

Change 32546 on 2002/06/07 by bhankins@fl_bhankins_r400_win

reversed order of xyzw from vte

Change 32421 on 2002/06/06 by mmantor@mmantor_r400_win

updated the mti_pli.dll to handle 110 fields for getvec and cmpvec
fixed tilex,y width in sc_dumps
first working sc_packer code and associated files

Change 32397 on 2002/06/06 by dclifton@dclifton_r400

Changed all internal signals in pa.v to lower case, carried change down into SU, VTE,
```

```
and VE

Change 32321 on 2002/06/06 by mmang@fl_mmang_r400_win

1.  Fix things lost in merge.
2.  Added register to be compatable with ati_1rp_state_storage.

Change 32308 on 2002/06/06 by mmang@fl_mmang_r400_win

1.  Increased src_vertex_indx from clip sm to 7 bits.
2.  Decreased ve_out_addr to 6 bits.
3.  Added decode for clip states SMC_OUTPUT_FIRST_BARYC_?,
    SMC_OUTPUT_FIRST_CLIP_POS_?, SMC_T_BLEND_PREV_ABC_?, and
    SMC_T_BLEND_CURR_ABC_?.

Change 32279 on 2002/06/06 by dclifton@dclifton_r400

Connected up some rcpeng signals

Change 32276 on 2002/06/06 by bhankins@fl_bhankins_r400_win

reversed interpretation of the order of xyzw from the vte

Change 32270 on 2002/06/06 by bhankins@fl_bhankins_r400_win

fix

Change 32262 on 2002/06/06 by bhankins@fl_bhankins_r400_win

reversed order of xyzw for side1, too

Change 32260 on 2002/06/06 by bhankins@fl_bhankins_r400_win

reversed order of xyzw

Change 32245 on 2002/06/06 by bhankins@fl_bhankins_r400_win

qualified decode on xfc

Change 32240 on 2002/06/06 by bhankins@fl_bhankins_r400_win

fix

Change 32239 on 2002/06/06 by bhankins@fl_bhankins_r400_win

changes

Change 32217 on 2002/06/06 by bhankins@fl_bhankins_r400_win
```

fixed deallocate_slot width

Change 32204 on 2002/06/06 by bhankins@fl_bhankins_r400_win

fix to match csim

Change 32148 on 2002/06/05 by dclifton@dclifton_r400

Connecting outputs of PA_SX

Change 32129 on 2002/06/05 by dclifton@dclifton_r400

Fixed pa_sx output register connections

Change 32100 on 2002/06/05 by dclifton@dclifton_r400

Fixed possible fall-through logic

Change 32081 on 2002/06/05 by dclifton@dclifton_r400

Fixed address shift

Change 32048 on 2002/06/05 by bhankins@fl_bhankins_r400_win

changed interface to arbiter:

removed high_priority

increased src_vertex_indx to 7 bits

Change 32031 on 2002/06/05 by bhankins@fl_bhankins_r400_win

increase deallocate_slot to 3 bits

Change 32019 on 2002/06/05 by dclifton@dclifton_r400

Turn off regclk_enable after file is read.

Change 32015 on 2002/06/05 by dclifton@dclifton_r400

Fixed so RBBM_we and other outputs go inactive once file is read

Change 32013 on 2002/06/05 by dclifton@dclifton_r400

RBBM_waddr wasn't being driven--fixed

Change 31991 on 2002/06/05 by bhankins@fl_bhankins_r400_win

don't start vgt to pa stimulus until rbbm finished

Change 31987 on 2002/06/05 by dclifton@dclifton_r400

Fixed tbmod_rbbm_pa to drive outputs

Change 31980 on 2002/06/05 by bhankins@fl_bhankins_r400_win

wait until reset is gone

Change 31978 on 2002/06/05 by bhankins@fl_bhankins_r400_win

minor change

Change 31962 on 2002/06/05 by dclifton@dclifton_r400

Connected up su_busy to PA_RBBM_busy and deleted PA_RBBM_ntrrtr from pa (tie hi at rbbm)

Change 31956 on 2002/06/05 by grayc@grayc_r400_win

increased number of fields parsed to 60

Change 31955 on 2002/06/05 by grayc@grayc_r400_win

increased num fields to be parsed in a line to 60

Change 31954 on 2002/06/05 by bhankins@fl_bhankins_r400_win

increased deallocate_slot to 3 bits

Change 31951 on 2002/06/05 by bhankins@fl_bhankins_r400_win

fix

Change 31943 on 2002/06/05 by bhankins@fl_bhankins_r400_win

added tbtrk_pasx

Change 31941 on 2002/06/05 by bhankins@fl_bhankins_r400_win

added tbtrk_pasx tracker

Change 31922 on 2002/06/05 by bhankins@fl_bhankins_r400_win

increased deallocate_slot to three bits

```
Change 31871 on 2002/06/04 by dclifton@dclifton_r400

connected up pa_rbbm_busy with su_busy

Change 31854 on 2002/06/04 by bbuchner@fl_bbuchner_r400_win

changed dump file names

Change 31801 on 2002/06/04 by bhankins@fl_bhankins_r400_win

Initial checkin of tracker for pasx0/1 interfaces.

Change 31761 on 2002/06/04 by bhankins@fl_bhankins_r400_win

added vgt and sx interface stimulus generators

Change 31744 on 2002/06/04 by dclifton@dclifton_r400

Updates to get rid of unknowns

Change 31741 on 2002/06/04 by bhankins@fl_bhankins_r400_win

added tbmod_sxpa

Change 31734 on 2002/06/04 by bhankins@fl_bhankins_r400_win

Initial checkin.  provide test stimulus to u)/1_SX_PA interfaces

Change 31697 on 2002/06/04 by bhankins@fl_bhankins_r400_win

added tbmod_vgttoclipv/s/p

Change 31692 on 2002/06/04 by bhankins@fl_bhankins_r400_win

initial checkin

Change 31666 on 2002/06/04 by bhankins@fl_bhankins_r400_win

Initial checkin

Change 31664 on 2002/06/04 by bhankins@fl_bhankins_r400_win

update to provide asynchronous send response to rtr from uut.

Change 31616 on 2002/06/03 by dclifton@dclifton_r400

Tracker for PA outputs
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Change 31615 on 2002/06/03 by dclifton@dclifton_r400

Debugging--intermediate check in

Change 31578 on 2002/06/03 by dclifton@dclifton_r400

Widened pa_su_cntl bus, temp fixed clip_su_dealloc_slot and ove_waddr mismatch.

Change 31557 on 2002/06/03 by dclifton@dclifton_r400

Changed commas in sensitivity lists to "or"

Change 31459 on 2002/06/03 by grayc@grayc_r400_win

updates for integration

Change 31278 on 2002/05/31 by dclifton@dclifton_r400

Functional for unclipped polygon, line, point, and polymode.

Change 31027 on 2002/05/31 by dclifton@dclifton_r400

Runs vectors with more than 8 state variable contexts

Change 30429 on 2002/05/28 by dclifton@dclifton_r400

testbench for setup unit

Change 30066 on 2002/05/24 by mmang@fl_mmang_r400_win

1. Added VteIn.dmp and AgVeOut.dmp compares.
2. Added #0.5 delay to input drives and output compares.
3. Added agve_dly_valid to help sync AgVeOut compare.
4. Increased clip to AG state_var_indx to 3 bits.
5. Increased Ag to Vte opcode to 3 bits.
6. Fixed y swizzle select bug.
7. Renamed AgState.dmp to RbiuAg.dmp.

Change 29952 on 2002/05/24 by bhankins@fl_bhankins_r400_win

Initial checkin

Change 29945 on 2002/05/24 by bhankins@fl_bhankins_r400_win

fix to send state var indx from ccg to arbiter with requests

Change 29935 on 2002/05/24 by bhankins@fl_bhankins_r400_win

up'd clip_to_arb_data_state_var_indx to 3 bits

Change 29933 on 2002/05/24 by bhankins@fl_bhankins_r400_win

up'd clip_to_arb_data_state_var_indx to 3 bits

Change 29913 on 2002/05/24 by bhankins@fl_bhankins_r400_win

updates

Change 29904 on 2002/05/24 by grayc@grayc_r400_win

modified DONE statements

Change 29903 on 2002/05/24 by grayc@grayc_r400_win

modified DONE statements

Change 29889 on 2002/05/24 by bhankins@fl_bhankins_r400_win

Initial checkin. Not much more than uut instantiation.

Change 29888 on 2002/05/24 by bhankins@fl_bhankins_r400_win

deleted

Change 29886 on 2002/05/24 by bhankins@fl_bhankins_r400_win

updates

Change 29877 on 2002/05/24 by bhankins@fl_bhankins_r400_win

Initial checkin. not much more than uut instantiation.

Change 29863 on 2002/05/24 by grayc@grayc_r400_win

added DONE statements

Change 29862 on 2002/05/24 by grayc@grayc_r400_win

Added DONE statement

Change 29845 on 2002/05/24 by bhankins@fl_bhankins_r400_win

added rbiu_ccg_expcntmd_sel

Change 29839 on 2002/05/24 by bhankins@fl_bhankins_r400_win

backed state io down to just the bits for pa_sxifccg.v

Change 29838 on 2002/05/24 by grayc@grayc_r400_win

fix for detecting END in compareVec

Change 29831 on 2002/05/24 by bhankins@fl_bhankins_r400_win

misc wiring fixes

Change 29830 on 2002/05/24 by bhankins@fl_bhankins_r400_win

support mods to pa_clipper.v and pa_sxifccg.v state i/o

Change 29827 on 2002/05/24 by bhankins@fl_bhankins_r400_win

fix on state i/o

Change 29825 on 2002/05/24 by bhankins@fl_bhankins_r400_win

mod to state i/o

Change 29705 on 2002/05/23 by fhsien@fhsien_r400_unix_marlboro

Update pa.v for GC core

Change 29699 on 2002/05/23 by dclifton@dclifton_r400

Updated vte interface with lowercase names

Change 29695 on 2002/05/23 by bhankins@fl_bhankins_r400_win

minor fix in i/o

Change 29694 on 2002/05/23 by bhankins@fl_bhankins_r400_win

minor fix in state_var_indx width to SU

Change 29689 on 2002/05/23 by grayc@grayc_r400_win

one more fix

Change 29685 on 2002/05/23 by grayc@grayc_r400_win

okay ... here's the real makefile

Change 29680 on 2002/05/23 by grayc@grayc_r400_win

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modified includes

Change 29655 on 2002/05/23 by grayc@grayc_r400_win

initial version

Change 29652 on 2002/05/23 by bhankins@fl_bhankins_r400_win

minor mod to state interfaces of pa_clipper and pa_sxifccg

Change 29648 on 2002/05/23 by dclifton@dclifton_r400

Changed extension.

Change 29627 on 2002/05/23 by bhankins@fl_bhankins_r400_win

minor fix for point sprite tests

Change 29615 on 2002/05/23 by bhankins@fl_bhankins_r400_win

minor state fix

Change 29614 on 2002/05/23 by bhankins@fl_bhankins_r400_win

minor derived state fix

Change 29583 on 2002/05/22 by dclifton@dclifton_r400

Fixed SQ_PROGRAM_CNTL id

Change 29521 on 2002/05/22 by bhankins@fl_bhankins_r400_win

updates

Change 29517 on 2002/05/22 by bhankins@fl_bhankins_r400_win

updates

Change 29516 on 2002/05/22 by bhankins@fl_bhankins_r400_win

updates on sxif state

Change 29497 on 2002/05/22 by bhankins@fl_bhankins_r400_win

deleted some unused signals, and initialized some 'variables'

Change 29486 on 2002/05/22 by bhankins@fl_bhankins_r400_win
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minor fixes

Change 29474 on 2002/05/22 by bhankins@fl_bhankins_r400_win

updates

Change 29473 on 2002/05/22 by bhankins@fl_bhankins_r400_win

updates

Change 29469 on 2002/05/22 by bhankins@fl_bhankins_r400_win

make fixes to pa_clipper/rbiu state interface.

added pa_cl_rei

Change 29468 on 2002/05/22 by bhankins@fl_bhankins_r400_win

removed debug-only signals from i/o

Change 29465 on 2002/05/22 by mmang@fl_mmang_r400_win

remove include of header.v in this package

Change 29459 on 2002/05/22 by bhankins@fl_bhankins_r400_win

updates to fix state i/o and use proper state_storage modules

Change 29389 on 2002/05/21 by dclifton@dclifton_r400

Added boilerplate header.

Change 29386 on 2002/05/21 by dclifton@dclifton_r400

Precision fixes

Change 29339 on 2002/05/21 by dclifton@dclifton_r400

vte testbench

Change 29338 on 2002/05/21 by dclifton@dclifton_r400

Interface between rcpeng and clipper translated from r300 vhdl

Change 29319 on 2002/05/21 by dclifton@dclifton_r400

A few updates
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Change 29299 on 2002/05/21 by bhankins@fl_bhankins_r400_win

renamed subblocks from pa_ to pa_ccg_

Change 29298 on 2002/05/21 by bhankins@fl_bhankins_r400_win

renamed pa_ subblocks to pa_cl_

Change 29261 on 2002/05/21 by bhankins@fl_bhankins_r400_win

started to add pa_clipper, pa_sxifccg

Change 29235 on 2002/05/21 by bhankins@fl_bhankins_r400_win

update (changed names of instantiated modules)

Change 29233 on 2002/05/21 by bhankins@fl_bhankins_r400_win

initial checkin (changed names)

Change 29232 on 2002/05/21 by bhankins@fl_bhankins_r400_win

obsolete (changing name)

Change 29118 on 2002/05/20 by dclifton@dclifton_r400

Fixes for various bugs discovered by random vectors.

Change 29064 on 2002/05/20 by bhankins@fl_bhankins_r400_win

comment out references to pa_clip_pkg.v

Change 29051 on 2002/05/20 by bhankins@fl_bhankins_r400_win

added pa_sxifccg.v and pa_clipper.v

Change 29046 on 2002/05/20 by bhankins@fl_bhankins_r400_win

obsolete

Change 29045 on 2002/05/20 by bhankins@fl_bhankins_r400_win

obsolete

Change 29044 on 2002/05/20 by bhankins@fl_bhankins_r400_win

update
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Change 29043 on 2002/05/20 by bhankins@fl_bhankins_r400_win

initial checkin

Change 29042 on 2002/05/20 by bhankins@fl_bhankins_r400_win

update

Change 29041 on 2002/05/20 by bhankins@fl_bhankins_r400_win

obsolete

Change 29040 on 2002/05/20 by bhankins@fl_bhankins_r400_win

updated dumps for latest csim/test bench combination

Change 29038 on 2002/05/20 by bhankins@fl_bhankins_r400_win

update test bench to instantiate pa_clipper.v, same as component in pa.v

Change 29036 on 2002/05/20 by bhankins@fl_bhankins_r400_win

updated hierarchy to flatten clipper to pa_clipper.v

Change 29033 on 2002/05/20 by bhankins@fl_bhankins_r400_win

obsolete

Change 29032 on 2002/05/20 by bhankins@fl_bhankins_r400_win

updates to support integration into pa.v

Change 29029 on 2002/05/20 by bhankins@fl_bhankins_r400_win

Initial checkin

Change 29010 on 2002/05/20 by dclifton@dclifton_r400

Changed GFX_SQ_IMPORT_EXPORT register to GFX_SQ_PROGRAM_CONTROL

Change 28520 on 2002/05/16 by bbuchner@fl_bbuchner_r400_win

CompareVec returns false when last vector is compared.

Change 28426 on 2002/05/16 by sallen@sallen_r400_lin_marlboro

add gc_test.tree (until gc stabilized enough to compile)
   use direct path to sq_register_addr.v
```

Change 28394 on 2002/05/16 by sallen@sallen_r400_lin_marlboro

gc testbench/ferret tweaks as we approach a usable testbench

Change 28343 on 2002/05/16 by grayc@grayc_r400_win

another wiring error

Change 28339 on 2002/05/16 by grayc@grayc_r400_win

fix wiring errors

Change 28328 on 2002/05/16 by grayc@grayc_crayola_unix_orl

added `include "header.v" on files

Change 27979 on 2002/05/14 by dclifton@dclifton_r400

Changed copy address compare to account for 2 LSB's

Change 27954 on 2002/05/14 by grayc@grayc_r400_win

additional mods for interfacing registers, adding common blocks, etc

Change 27879 on 2002/05/14 by dclifton@dclifton_r400

Fixed a few bugs with clip codes and ADD opcode.

Change 27877 on 2002/05/14 by bhankins@fl_bhankins_r400_win

Initial checkin. While functionally correct, this will need a lot of work on I/O for integration.

Change 27834 on 2002/05/14 by dclifton@dclifton_r400

More parts of increased z precision changes

Change 27800 on 2002/05/14 by grayc@grayc_r400_win

updates for clocks and reset ...

Change 27794 on 2002/05/13 by dclifton@dclifton_r400

Part of update for Z precision

Change 27390 on 2002/05/10 by dclifton@dclifton_r400

```
Update for SU I/O changes (event, provokingvtx)
A few changes to state register implementation
Added rbiu and su to pa top block

Change 27227 on 2002/05/09 by grayc@grayc_r400_win

mods for integration

Change 27226 on 2002/05/09 by dclifton@dclifton_r400

Initial revision of pa/rbbm interface unit

Change 27098 on 2002/05/08 by dclifton@dclifton_r400

These files have either been renamed or eliminated from the design.

Change 27097 on 2002/05/08 by dclifton@dclifton_r400

This update adds the state register and rbiu interface, increases the reciprocal
precision, removes area divide from all parameters but Z.

Change 26063 on 2002/05/02 by grayc@grayc_r400_win

fix to reading the last argument of a file

Change 26005 on 2002/05/02 by dclifton@dclifton_r400

This is the reciprocal engine that is shared by the vte and the clipper.

Change 25817 on 2002/05/01 by grayc@grayc_r400_win

change printf to io_printf so print msg will go to transcript

Change 24854 on 2002/04/24 by dclifton@dclifton_r400

Added fifo to front of su and removed it from middle

Change 24852 on 2002/04/24 by dclifton@dclifton_r400

polymode working in Setup Unit.
rounding working in vte.

Change 24826 on 2002/04/24 by grayc@grayc_r400_win

added capability to compare_vec routine to skip compares for field name = "xxx"

Change 24801 on 2002/04/24 by grayc@grayc_r400_win
```

```
fix for case of number of arguments of compare_vec() < number of arguments in file

Change 24394 on 2002/04/22 by mmantor@mmantor_r400_win

added initial pa_ag code and testbench

Change 23011 on 2002/04/12 by dclifton@dclifton_r400

Initial check-in of VTE and addition of prim fifo to SU

Change 23008 on 2002/04/12 by dclifton@dclifton_r400

Intermediate update

Change 23001 on 2002/04/12 by dclifton@dclifton_r400

First check-in of vte

Change 21844 on 2002/04/04 by bhankins@fl_bhankins_r400_win

Initial checkin

Change 21649 on 2002/04/03 by bhankins@fl_bhankins_r400_win

Initial checkin.

Change 21486 on 2002/04/02 by mmantor@mmantor_r400_win

old files

Change 21044 on 2002/03/29 by mmantor@mmantor_r400_win

added new signals from vgt and renamed two in the pa-> sx interface as a result of
reviews

Change 20769 on 2002/03/27 by mmantor@mmantor_r400_win

updated for interface integration changes

Change 20474 on 2002/03/26 by mmantor@mmantor_r400_win

updated for spec changes

Change 20329 on 2002/03/25 by dclifton@dclifton_r400

Fixed a few bugs with previous check-in.  Lines, points, and triangles mostly
functioning.
```

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Change 19599 on 2002/03/19 by grayc@grayc_r400_win

fixed crashing problem if file is missing

Change 19542 on 2002/03/18 by mmantor@mmantor_r400_win

initial top level for the pa and sc verilog files

Change 19230 on 2002/03/15 by dclifton@dclifton_r400

Added support for lines and points

Change 18210 on 2002/03/08 by dclifton@dclifton_r400

First revision of setup--passes unclipped prims and handles stalls from clipper or scan
converter

Change 14761 on 2002/02/06 by grayc@grayc_r400_win

fixed bug with InitVec when sim halts and resumes

Change 14736 on 2002/02/06 by dclifton@dclifton_r400

Initial rev.--main gradient calculation pipe

Change 14688 on 2002/02/05 by grayc@grayc_r400_win

fixed bug if dmp file only had one field
enhanced "END-OF-FILE" print statement

Change 14367 on 2002/01/31 by dclifton@dclifton_r400

Initial setup revision for sorting and area calculation

Change 14338 on 2002/01/31 by grayc@grayc_r400_win

clean-up

Change 14326 on 2002/01/31 by grayc@grayc_r400_win

additional changes for end-of-file detection

Change 14322 on 2002/01/31 by grayc@grayc_r400_win

changed to detect end of dump file

Change 14321 on 2002/01/31 by grayc@grayc_r400_win
```

```
changed to detect "END" at end of dump file

Change 14319 on 2002/01/31 by grayc@grayc_r400_win

added dependent file

Change 14298 on 2002/01/31 by grayc@grayc_r400_win

added new target 'verilog'

Change 14297 on 2002/01/31 by grayc@grayc_r400_win

moved

Change 14296 on 2002/01/31 by grayc@grayc_r400_win

moved dmp files

Change 14295 on 2002/01/31 by grayc@grayc_r400_win

PLI example code (for file IO)

Change 13941 on 2002/01/25 by dclifton@dclifton_r400

Initial version

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro

mv block dirs to gfx

Change 9586 on 2001/11/08 by dclifton@dclifton_r400

new specs

Change 9408 on 2001/11/07 by mmantor@mmantor_r400

moved the files from the re dir to the pa and then removed the pa directory

Change 6877 on 2001/09/25 by subad@MA_SUBA

fixed it

Change 6857 on 2001/09/24 by subad@MA_SUBA
```

```
scan converter block diagrams

Change 6846 on 2001/09/24 by subad@subad

added comments

Change 6743 on 2001/09/20 by subad@subad

checking it in as Orlando will work on it

Change 6535 on 2001/09/14 by subad@subad

completed pa_sc_walk_incee2.v; made relebant changes in other blocks

Change 6318 on 2001/09/11 by subad@subad

initial revision

Change 6262 on 2001/09/10 by subad@subad

initial revision of pa_sc_walk_incee1.v, renamed pa_sc_setup_bb to ..ee.

Change 6095 on 2001/09/05 by subad@subad

renaming files
```