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| 1 | $P R O C E E D I N G S$ |
| 2 | VIDEO OPERATOR: Good morning. We are now |
| 3 | recording and on the record. My name is Marissa |
| 4 | Demonte representing Veritext Mid Atlantic Region. |
| 5 | The date today is June 28, 2017. The time is 9:00 |
| 6 | a.m. This deposition is being held in the Office |
| 7 | of Mintz, Levin located at One Financial Center, |
| 8 | Boston, Massachusetts. |
| 9 | This deposition is being taken In the Matter |
| 10 | of: Certain Graphics Systems Components Thereof, |
| 11 | and Consumer Products Containing the Same, filed |
| 12 | with the United States Trade Commission. |
| 13 | The name of the witness is Laurent Lefebvre. |
| 14 | At this time, the attorneys will identify |
| 15 | themselves and the parties they represent, after |
| 16 | which our court reporter, Lisa Valdario, will |
| 17 | swear in the witness and we can proceed. |
| 18 |  |
| 19 | Richardson on behalf of the LG Respondents. |
| 20 | MR. LOWERY: Justin Lowery with McGuire |
| 21 | Woods on behalf of the MediaTek and Sigma |
| 22 | Respondents. |
| 23 | MR. RENAUD: Michael Renaud on behalf of the |
| 24 | Complainants, Advanced Micro Devices Inc. and ATI |
| 25 | Technologies along with Adam Rizk, both of Mintz, |

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| 1 |  | Levin. |
| 2 | LAURENT LEFEBVRE |  |
| 3 | A witness called for examination, having been |  |
| 4 | duly sworn, testified as follows: |  |
| 5 | DIRECT EXAMINATION |  |
| 6 | BY MR. ELENGOLD: |  |
| 7 | Q Good morning, Mr. Lefebvre. |  |
| 8 | A Good morning. |  |
| 9 | Q Could you please state your full name for the |  |
| 10 | record. |  |
| 11 | A Laurent Lefebvre. |  |
| 12 | Q | And I'll try my best to get that name correct |
| 13 |  | today as we go, sir. What is your current home |
| 14 |  | address? |
| 15 | A | My current home address is |
| 16 |  |  |
| 17 | 2 | Mr. Lefebvre, what is your current employment? |
| 18 | A | I am currently employed by ATI, a subsidiary of |
| 19 | AMD, as a hardware fellow. |  |
| 20 | Q | What is a hardware fellow? |
| 21 | A | It is a title we give to engineers at AMD. |
| 22 | Q | What is your current responsibilities in your |
| 23 | employment? |  |
| 24 | A | Currently, my responsibilities are to configure and plan the future products of AMD, and also |
| 25 |  |  |

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1 Q As we're going through the day, please ask for any 2 Clarification you have with regard to my question,
$6 \quad \mathbf{Q}$ And if at any time you need to take a break, don't
7 hesitate to ask. If there is a question pending,
8 I'll ask that you try to answer the question to
9 the best of your ability, but if you need a break
10
A $\quad$ will.
Q And finally, please try your best to answer my
questions audibly as we go through the day just so
the court reporter can get a clean record to your
responses to my questions.
A I understand.
Q Earlier, when we were talking about the products
that you're currently working with, you mentioned
I believe GPUs, APUs and SOC, is that correct?
A That's what $I$ remember my answer was, yes, but we
can go through the transcript if you want.
Q I'm just trying to bring you back to there so I
can ask a follow-up question if that's okay.
A That is okay.
Q And really what $I$ would like to ask you is what is

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|  |  | the difference between each of those three types |
| 2 |  | of products? |
| 3 |  | MR. RENAUD: Objection. |
| 4 | A | Can we restate the three types of products so I |
| 5 |  | get my answer as clear as possible? |
| 6 | 2 | Why don't we take them one at a time. What is |
| 7 |  | GPU? |
| 8 | A | Okay. So the GPU acronym stands for graphics |
| 9 |  | processing unit. This is typically a distinct |
| 10 |  | device that you put into a computer that is |
| 11 |  | responsible for performing graphics on the |
| 12 |  | computer, that is generating images that you see |
| 13 |  | on your computer. |
| 14 | Q | What is an APU? |
| 15 | A | APU is an internal acronym at AMD we use that |
| 16 |  | stands for accelerated processing unit. It's |
| 17 |  | similar to a GPU, but the main difference is that |
| 18 |  | all of the components of the computer are |
| 19 |  | integrated on a single chip; that is, the CPU and |
| 20 |  | the GPU are integrated on a single chip, which is |
| 21 |  | why we call it an APU versus a GPU. |
| 22 | Q | So GPU is dedicated to graphics processing, is |
| 23 |  | that right? |
| 24 |  | MR. RENAUD: Objection. |
| 25 | A | A GPU is a piece of hardware that performs |

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| 1 |  | graphics that does not contain a CPU. |
| 2 | Q | What is an SOC? |
| 3 | A | An SOC is the fabric, if you will, that allows us |
| 4 |  | to integrate multiple IPs on a single chip. The |
| 5 |  | acronym stands for system on chip, so it's the |
| 6 |  | fabric that allows to connect and integrate |
| 7 |  | everything on a single piece of silicon. |
| 8 | Q | Does an Soc contain a GPU? |
| 9 | A | SOC stands for system on a chip. It can contain |
| 10 |  | whatever you want it to contain. |
| 11 | Q | Can an APU contain a GPU? |
| 12 |  | MR. RENAUD: Objection. |
| 13 | A | An APU and a GPU are different products, so an APU |
| 14 |  | can contain graphics processing, a graphics core, |
| 15 |  | but it doesn't have to have all the capabilities |
| 16 |  | of a discrete GPU. |
| 17 | Q | Are they different chips, an APU and a GPU? |
| 18 | A | Can you define what you mean by chip? Do you mean |
| 19 |  | different pieces of silicon? |
| 20 | Q | Yes. |
| 21 | A | So yes, they would be specific different pieces of |
| 22 |  | silicon. |
| 23 | Q | And an SOC would be a different piece of silicon |
| 24 |  | or a different chip too? |
| 25 | A | An SOC is really the process by which we generate |

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| 1 |  | an APU, so it can be used by an APU, but it can |
| 2 |  | also be another piece of silicon if you want it to |
| 3 |  | be. |
| 4 | Q | And approximately how much of your current time is |
| 5 |  | spent working on graphics? |
| 6 | A | Can you define what you mean by graphics? It's a |
| 7 |  | pretty generic term. |
| 8 | Q | Sure. Why don't we come back to that, and first |
| 9 |  | let me ask you a couple questions about today. |
| 10 |  | So when did you find out you were going to |
| 11 |  | be deposed today? |
| 12 | A | So again, I'm speaking from memory here so excuse |
| 13 |  | if my dates are not exact. I remember late 2016 |
| 14 |  | or early 2017 receiving a call from Adam. |
| 15 |  | MR. RENAUD: And you can -- instruct you not |
| 16 |  | to provide any content of the call. |
| 17 |  | THE WITNESS: Sure. |
| 18 | A | And that made me aware of this pending litigation, |
| 19 |  | and then I met with counsel several times since |
| 20 |  | that date. |
| 21 | Q | Do you have an understanding of what this case is |
| 22 |  | about? |
| 23 |  | MR. RENAUD: Objection. You may answer so |
| 24 |  | long as you don't reveal any attorney/client |
| 25 |  | communications. |

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| 1 |  | please mark Exhibit 1. |
| 2 |  | (Document marked Exhibit 1 for |
| 3 |  | identification.) |
| 4 | Q | Mr. Lefebvre, have you seen Exhibit 1 before? |
| 5 | A | I believe I've seen this piece of paper or |
| 6 |  | collection of piece of paper in a bigger document |
| 7 |  | before, yes. |
| 8 | Q | Do you know what Exhibit 1 is? |
| 9 | A | It reads: Respondents' Notice of Deposition of |
| 10 |  | Laurent Lefebvre, so. |
| 11 | Q | Do you understand that you are noticed to be |
| 12 |  | deposed today in your personal capacity? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | Yes, I do understand that. |
| 15 |  | MR. ELENGOLD: And I'm going to ask the |
| 16 |  | court reporter to please mark Exhibit 2. |
| 17 |  | (Document marked Exhibit 2 for |
| 18 |  | identification.) |
| 19 | Q | Mr. Lefebvre, have you seen Exhibit 2 before? |
| 20 | A | I have seen a document that looks very much like |
| 21 |  | this. It was not exactly in the same form, but it |
| 22 |  | contains the same number of items than this |
| 23 |  | document. |
| 24 | Q | Do you know what Exhibit 2 is? |
| 25 | A | Again, it reads: Respondents' First Notice of |

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| 1 |  | on behalf of AMD and ATI? |
| 2 |  | MR. RENAUD: Objection, and you may answer, |
| 3 |  | but I'm just going to insert in the record that |
| 4 |  | all of those subjects are subject to objections |
| 5 |  | that have been made in writing, but sorry, please |
| 6 |  | answer the question. |
| 7 | A | Yes. I can testify to the facts related to those |
| 8 |  | patents with the understanding I'm not an attorney |
| 9 |  | so I can't really go, you know, beyond my |
| 10 |  | knowledge. |
| 11 | Q | You're prepared to testify today though on those |
| 12 |  | topics we just identified. |
| 13 | A | Yes. |
| 14 |  | MR. RENAUD: Same objection. He's prepared |
| 15 |  | subject to the objections. |
| 16 | Q | What did you do to prepare for today's deposition? |
| 17 | A | Okay. |
| 18 |  | MR. RENAUD: And you may answer that |
| 19 |  | question without revealing any attorney/client |
| 20 |  | communications. |
| 21 |  | THE WITNESS: Yes. |
| 22 | A | So I met with counsel in person, like I said |
| 23 |  | before, once in Montreal and then here in Boston |
| 24 |  | extensively for two days prior to this deposition, |
| 25 |  | and I reviewed a wealth of specifications, as well |

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| 1 | A | Again, speaking from memory here, I recall |
| 2 |  | reviewing at least the sequencer specification of |
| 3 |  | the R400 chip versions 0.4 and version 2.0. And I |
| 4 |  | believe for that particular deposition, the |
| 5 |  | specification that I reviewed, that was it. |
| 6 | Q | Those were the only two specifications you've |
| 7 |  | reviewed in preparation for your deposition today, |
| 8 |  | is that correct? |
| 9 | A | These are the depositions I recall being reviewed. |
| 10 |  | So I know for sure I reviewed those. I may have |
| 11 |  | reviewed other documents. There was a big binder. |
| 12 |  | At least those. |
| 13 | Q | You said you reviewed your depositions. Is that |
| 14 |  | referring to the two depositions we discussed |
| 15 |  | earlier? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | Yes, that is referring to the two depositions that |
| 18 |  | I did before, yes. |
| 19 | Q | And you reviewed both transcripts this week? |
| 20 |  | MR. RENAUD: Objection. |
| 21 | A | I read both transcripts, yes. |
| 22 | Q | You said you reviewed testimony. What testimony |
| 23 |  | did you review to prepare for today's deposition? |
| 24 | A | So as best I recall again, and if you have the |
| 25 |  | documents we can look at them, there were |

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| 1 |  | vertices. |
| 2 | Q | You mentioned reviewing some Exhibits this week. |
| 3 |  | Were you referring to the Deposition Exhibits from |
| 4 |  | your prior depositions? |
| 5 |  | MR. RENAUD: Objection. |
| 6 | A | Yes, I meant -- I was referring to some of the |
| 7 |  | Exhibits of my previous depositions. |
| 8 | Q | What presentations did you review to prepare for |
| 9 |  | your deposition? |
| 10 | A | While I don't recall the specifics, some of the |
| 11 |  | presentations I reviewed were part of the Exhibits |
| 12 |  | of my previous depositions, and I also reviewed |
| 13 |  | other presentations to refresh my memory and |
| 14 |  | prepare me to testify on behalf of $A M D$ on certain |
| 15 |  | topics. |
| 16 | Q | Do you recall any details regarding any |
| 17 |  | presentations you reviewed to prepare for today? |
| 18 |  | MR. RENAUD: Objection. |
| 19 | A | So I mean, I recall two specific presentations |
| 20 |  | that were new, at least not part of the Exhibits |
| 21 |  | before, that related about what Netlist 3 was in |
| 22 |  | terms of the R 400 product and how that particular |
| 23 |  | netlist was ported on a hardware simulator named |
| 24 |  | IKOS. |
| 25 | Q | Do you recall the author of that presentation? |

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| 1 | A | No, I do not. |
| 2 | Q | Were you already personally familiar with that |
| 3 |  | presentation before your review? |
| 4 | A | I must admit, I did not remember it. It was a |
| 5 |  | long time ago. I might have been familiar with it |
| 6 |  | way back when, but when it was re-presented to me, |
| 7 |  | it was new. It did not ring any bells, put it |
| 8 |  | that way. |
| 9 | Q | Do you recall the date of that presentation? |
| 10 | A | As I stated before, there were two presentations I |
| 11 |  | believe, and they were, one of them was in January |
| 12 |  | and the other one, February. I don't recall the |
| 13 |  | particular year unfortunately, but I'm sure if you |
| 14 |  | can -- these were produced, so if you can find |
| 15 |  | them, I can review them with you and can give you |
| 16 |  | more definition as to the date. |
| 17 | Q | How do you know they were produced? |
| 18 | A | Because counsel told me that they were produced. |
| 19 |  | MR. RENAUD: While that answer is fine, I |
| 20 |  | remind you, Laurent, any conversations with |
| 21 |  | counsel are off limits. Saying what was produced, |
| 22 |  | if you know it, I'll allow, but just be careful. |
| 23 |  | Okay. |
| 24 |  | THE WITNESS: Yes, sir. |
| 25 | Q | Did both presentations relate to the netlist for |

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|  |  | thick. And there might be more. Like I said, it |
| 2 |  | was a lot of documents that were browsed through. |
| 3 | Q | Did you speak with any AMD or ATI people to |
| 4 |  | prepare for your deposition today? |
| 5 | A | I recall having phone calls with a few people from |
| 6 |  | AMD. Yes. |
| 7 | Q | Who did you speak with from AMD? |
| 8 | A | I remember David Christie and a few other people |
| 9 |  | that I don't remember the names of. They are not |
| 10 |  | the -- I mean, I understand that they were |
| 11 |  | gathering information on behalf of AMD, and |
| 12 |  | documents, but I don't recall the specific names. |
| 13 |  | They are not people I work with very often. |
| 14 | Q | The only person you remember speaking with in |
| 15 |  | preparation for your deposition today at AMD is |
| 16 |  | David Christie, is that correct? |
| 17 |  | MR. RENAUD: Objection. |
| 18 | A | Yes, and but Pam Horn was also on the call. I |
| 19 |  | mean she always is typically. |
| 20 | Q | Who is David Christie? |
| 21 | A | My understanding is that he is a hardware engineer |
| 22 |  | that works for AMD legal teams to help accumulate |
| 23 |  | documents and reviews them for litigation purposes |
| 24 |  | and whatnot. I don't exactly know what he is |
| 25 |  | doing in that role though. |

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Q Why did you talk with David Christie to prepare for your deposition today?

MR. RENAUD: Instruct you not to answer that question if it can't be answered without revealing attorney/client communications.
A Yeah, I don't think I can answer that question directly.

Q Is Mr. Christie an attorney?
A He is, $I$ believe he is an engineer. Not an attorney.

Q Did you speak with him on the instruction of counsel?

MR. RENAUD: Instruct you not to answer that question.
A I can't answer that question.
MR. ELENGOLD: Why do you believe that his discussion with Mr. Christie is privileged?

MR. RENAUD: Because it is. Attorney/client communication. I was on the phone with him. I'm not going to pry into that. If you want to take a break and talk about it, we can.

MR. ELENGOLD: Okay.
MR. RENAUD: I'm also happy to ask the witness to go back and find out who the other AMD people are that he spoke with so you can get them

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| 1 | A | Either on the line or in the room, yes, because I |
| 2 |  | had these conversations from my counsel's office, |
| 3 |  | so -- |
| 4 | Q | In the last two days? |
| 5 | A | In the last two days, yes. |
| 6 | Q | Was your conversation with Mr. Christie in the |
| 7 |  | last two days? |
| 8 | A | Yes, it was. |
| 9 | Q | Other than the documents reviewed, you reviewed, |
| 10 |  | and your call with David Christie, is there |
| 11 |  | anything else you did to prepare for your |
| 12 |  | deposition today? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | I personally searched the Perforce database for |
| 15 |  | evidence of what Netlist 3 was, and you know, like |
| 16 |  | I said before, read documents, and I had another |
| 17 |  | call with other parties of AMD, like I already |
| 18 |  | stated, but that's the extent of what I remember. |
| 19 | Q | Was that a single other call with other people at |
| 20 |  | AMD that you're referring to? |
| 21 | A | Yes. That's what I remember, single other call. |
| 22 | Q | When did you search the Perforce database? |
| 23 |  | I did it in the last two days. |
|  | Q | Why did you search the Perforce database to |
| 25 |  | prepare for your deposition? |

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Q What is Netlist 3?
A So a netlist is a list of synthesis files, which
are the output of synthesis, so they're basically
a list of gate level files that implement a
hardware device.
Q What do you mean by "implement a hardware device"?
A I mean, it's the source file that is used to
generate silicon. So either the input of an $F P G A$
simulator or the input to the $P D$ team to generate
a chip, a silicon device.
Q So did you say FPGA simulator?
A FPGA.
Q What is an FPGA simulator?
A So FPGA is an acronym, and $I$ know it's present in
the IKOS User Manual, so we can go look there to
remind myself what the letters actually mean, but
it is a system of programmable gates that you can
program by pushing a netlist to it, to implement

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| 1 |  | clear, is that a computer program or is that a |
| 2 |  | hardware device? |
| 3 | A | So an FPGA simulator is a hardware device. It's a |
| 4 |  | big programmable hardware device which you can use |
| 5 |  | to simulate another product that, you know, would |
| 6 |  | become a chip in the end. It's a way to a means |
| 7 |  | to get a prototype early of the device that you |
| 8 |  | want to build. |
| 9 | Q | What is the PD team? |
| 10 | A | PD stands for physical device, so it's the team |
| 11 |  | that takes a netlist, or takes the output of |
| 12 |  | synthesis, and place and routes them in order to |
| 13 |  | make a floor plan of a chip that is going to be |
| 14 |  | built. |
| 15 | Q | Is there a name for that floor plan once the PD |
| 16 |  | team has completed its work? |
| 17 | A | Well, I believe a floor plan is a floor plan. I |
| 18 |  | mean, once everything is complete and done, I |
| 19 |  | believe the technical term is, we have a GDS |
| 20 |  | database, and that's what is used to do a tapeout. |
| 21 | Q | So when the PD team is done, that's -- the result |
| 22 |  | of their work is what would go to a tapeout, is |
| 23 |  | that correct? |
| 24 | A | Yes. The result of the work of the PD team would |
| 25 |  | result in a tapeout, yes. |

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| 1 | Q | And the PD team gets a netlist to start their |
| 2 |  | work? |
| 3 | A | The PD team gets a netlist to start their work, |
| 4 |  | yes. |
| 5 | Q | And at the same time, that netlist is also used |
| 6 |  | with an FPGA simulator, is that right? |
| 7 | A | Yes. So that same netlist that can be used by the |
| 8 |  | PD team can also be compiled or sent to an FPGA |
| 9 |  | simulator to establish a prototype of the chip. |
| 10 | Q | And is that for testing that you would do that at |
| 11 |  | the same time you're doing the tapeout? |
| 12 | A | Yes. Well, it is for testing, and it also is |
| 13 |  | used, as best I can tell -- and remember, it was a |
| 14 |  | long time ago, so forgive me for inaccuracies here |
| 15 |  | -- to bring up the software stack, the driver, |
| 16 |  | because it's a much more convenient machine to use |
| 17 |  | to run more extensive complete applications than |
| 18 |  | what you can run on an RTL simulator. |
| 19 | Q | Other than the conversations we've discussed and |
| 20 |  | the documents we've discussed, is there anything |
| 21 |  | else that you did to prepare for your deposition |
| 22 |  | today? |
| 23 | A | Not that I recall. |
| 24 | Q | Do you know what patent prosecution history is? |
| 25 | A | I am vaguely familiar with the term but I don't |

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| :---: | :---: | :---: |
| 1 | A | For the first one, probably nine to six. The |
| 2 |  | second one, somewhere more around nine to seven or |
| 3 |  | eight. So pretty long days. |
| 4 | Q | Were there any employees or documents that you |
| 5 |  | planned on reviewing but didn't before coming to |
| 6 |  | be deposed today? |
| 7 |  | MR. RENAUD: You may answer that yes or no. |
| 8 | A | No. |
| 9 | Q | Do you feel you're the most qualified person at |
| 10 |  | AMD to testify on their behalf for the corporate |
| 11 |  | topics you're discussing today? |
| 12 |  | MR. RENAUD: Objection. |
| 13 | A | I believe I qualified and I prepared adequately to |
| 14 |  | testify today, yes. |
| 15 | Q | Are you being paid for your testimony today? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | I am paid my normal salary by AMD. |
| 18 | Q | Do you get any additional compensation for |
| 19 |  | testifying? |
| 20 |  | MR. RENAUD: Objection. |
| 21 | A | No, I did not. |
| 22 | Q | Does AMD have any policies regarding employee |
| 23 |  | participation in litigation? |
| 24 |  | MR. RENAUD: Objection. You may answer that |
| 25 |  | yes or no. |

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| 1 | A | I don't know. |
| 2 | Q | For this investigation, did you personally search |
| 3 |  | for any documents in your files? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | So my understanding is that a team of people at |
| 6 |  | AMD did that investigation. That investigation |
| 7 |  | included my files, and like I stated before, I did |
| 8 |  | a Perforce search of documents yesterday and the |
| 9 |  | day before. |
| 10 | Q | Prior to those two searches in the last two days, |
| 11 |  | did you personally do any work collecting |
| 12 |  | documents for this investigation? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | No. I did not, but like I said, I had the |
| 15 |  | understanding a team at AMD did that work, and |
| 16 |  | that work included my documents. |
| 17 | Q | Did you discuss your deposition today with anyone |
| 18 |  | other than counsel? |
| 19 |  | MR. RENAUD: Objection. |
| 20 | A | I did not discuss the contents of my deposition |
| 21 |  | but, you know, at least my manager, Mike Mentor is |
| 22 |  | aware that I'm doing depositions today because I |
| 23 |  | had to get away from work for these days, so. |
| 24 | Q | And where is your work currently located? |
| 25 | A | I officially report to the Markham office of ATI, |

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|  |  | time. Is that what you mean by this question? |
| 2 | Q | I don't know. I don't know if you have a written |
| 3 |  | employment agreement or not. I'm just trying |
| 4 |  | to -- you said you -- I understand you're an |
| 5 |  | employee of AMD but through ATI, and I'm trying to |
| 6 |  | understand what that means. Who actually is your |
| 7 |  | employer? |
| 8 | A | Okay. So because I'm Canadian, to simplify tax |
| 9 |  | matters and everything, I'm paid through the |
| 10 |  | Toronto office, and so my paychecks and my actual |
| 11 |  | employer is the Markham office, which I understand |
| 12 |  | is ATI ULC because that's what it says on my |
| 13 |  | paychecks and tax records and what not. That's |
| 14 |  | pretty much the extent of what I know about this. |
| 15 |  | I don't know what relationship is, but as far as I |
| 16 |  | know, I work for AMD but it goes through this. |
| 17 |  | MR. RENAUD: And all of the answers |
| 18 |  | regarding corporate structure or purported |
| 19 |  | corporate structure are obviously outside the |
| 20 |  | scope of the designation, although you're free |
| 21 |  | pursue them. |
| 22 |  | MR. ELENGOLD: Yeah, that's fine. |
| 23 | Q | Your personal employment is not something you need |
| 24 |  | to be designated for right now. I was just trying |
| 25 |  | to understand who your employer is. |

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| 1 |  | MR. RENAUD: Yeah, and that corporate |
| 2 |  | structure relationships, I think there is a |
| 3 |  | witness coming up on that because I understand |
| 4 |  | that might be an area of inquiry. |
| 5 | Q | Yeah, I don't know if that's true or not, but |
| 6 |  | again, this is just limited to your employment |
| 7 |  | right now. |
| 8 |  | MR. RENAUD: Thank you. |
| 9 | Q | Can you please describe for me your education |
| 10 |  | since high school. |
| 11 |  | MR. RENAUD: Objection. |
| 12 | Q | Where did you go to college? |
| 13 | A | I went to the Ecole Polytechnique de Montreal |
| 14 |  | where I got an electronic engineering degree, and |
| 15 |  | I followed that immediately with a master's in |
| 16 |  | computer graphics from the University of Montreal. |
| 17 | Q | When did you get your initial engineering degree? |
| 18 | A | If memory serves, that would have been June 1998. |
| 19 | Q | When did you get your master's in computer |
| 20 |  | graphics? |
| 21 | A | That would have been somewhere in the summer of |
| 22 |  | 2000. Can't be exact on the date because it |
| 23 |  | involves, you know, giving the thesis and having |
| 24 |  | it reviewed and whatnot. |
| 25 | Q | What was the subject matter of your thesis? |

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| 1 |  | If I remember correctly, it was about the analysis |
| 2 |  | of and synthesis of textures through photograph |
| 3 |  | trying to get a procedural model for those. |
| 4 | Q | Do you have any other degrees? |
| 5 |  | MR. RENAUD: Objection. |
| 6 | A | I have a high school degree and primary school |
| 7 |  | diploma, but to my knowledge, that's it. |
| 8 | Q | That's it. |
| 9 |  | Did you attend any other schools after |
| 10 |  | receiving your master's degree? |
| 11 | A | No, I did not. I went to conferences and such but |
| 12 |  | not schools, that I remember. |
| 13 | Q | Where did you first work after obtaining your |
| 14 |  | master's degree? |
| 15 |  | MR. RENAUD: Objection. |
| 16 | A | I started working for ATI Technologies, the Boston |
| 17 |  | office. Or actually, to be more accurate, the |
| 18 |  | Marlborough office at the time. |
| 19 | Q | What was your initial title at ATI? |
| 20 |  | MR. RENAUD: Objection. |
| 21 | A | If I recall correctly, it was something like |
| 22 |  | engineering level one. |
| 23 | Q | What were your initial job responsibilities? |
| 24 | A | So again, thinking, talking from memory, 17 years |
| 25 |  | ago, it was, the very first thing I did was to |

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| 1 |  | MR. RENAUD: Objection. |
| 2 | A | You mean as I started working for ATI, right at |
| 3 |  | the beginning of my employment? |
| 4 | Q | Sure. Yeah. |
| 5 | A | As I recall, again it's a long time ago, that was |
| 6 |  | a fairly small team then. You know, maybe a few |
| 7 |  | architects and myself. So something like 10, 15 |
| 8 |  | people at the beginning. |
| 9 | Q | Is there a difference between an architect and an |
| 10 |  | engineer at ATI? |
| 11 | A | An engineer is a job title or job rank, if you |
| 12 |  | will. An architect means what you are doing. So |
| 13 |  | it specifies what the engineer is doing. It has |
| 14 |  | no real relationship with your rank within the |
| 15 |  | company. |
| 16 | Q | What does an architect do? |
| 17 | A | So my best understanding is that, and again at the |
| 18 |  | time, for the R400, an architect was responsible |
| 19 |  | to develop the specifications for the block that |
| 20 |  | he owned or the system that he owned, as well as |
| 21 |  | developing a model, which we call the C sim or |
| 22 |  | emulator, that would serve as a reference to the |
| 23 |  | designers. |
| 24 | Q | What is a block? |
| 25 | A | A graphics chip is composed of subsystems or |

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| 1 |  | with C sim? |
| 2 | A | What do you mean by "the code that's used with C |
| 3 |  | sim"? |
| 4 | Q | You just said the RTL is the source code that's |
| 5 |  | used, right? Earlier? Is that correct? |
| 6 | A | Yes. I said that it was the source -- that is the |
| 7 |  | source used by the synthesis tool to generate |
| 8 |  | gates. The C sim, as I refer to it, is the C code |
| 9 |  | which is C plus plus, it's a program, that serves |
| 10 |  | as a reference model to compare this RTL structure |
| 11 |  | against a golden model so to make sure that it |
| 12 |  | performs the right operation. |
| 13 | Q | What is a golden model? |
| 14 | A | I guess it depends, in the scope, I mean in AMD |
| 15 |  | and in the R400 project, for example, the golden |
| 16 |  | model is, you know, what is used to generate |
| 17 |  | pictures on the screen with the program that is |
| 18 |  | supposed to emulate the chip, and to make sure |
| 19 |  | that outputs the pictures we expect it to output. |
| 20 |  | It's a reference model if you will. |
| 21 | Q | It's a simulator or -- I'm sorry, strike that. |
| 22 |  | It's a simulated model programmed in $C$, is |
| 23 |  | that correct, or $C$ plus plus? |
| 24 | A | Yes. It's a behavioral model of the chip we want |
| 25 |  | to build that serves as a reference. |

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|  |  | MR. ELENGOLD: We've been going to about an |
| 2 |  | hour. Would you like to take a break? |
| 3 |  | MR. RENAUD: You know, in order to make the |
| 4 |  | day work, while I think later we'll need shorter |
| 5 |  | windows, maybe we go another 15 or so, if |
| 6 |  | everyone's comfortable with that? |
| 7 |  | MR. ELENGOLD: That's fine. |
| 8 |  | MR. RENAUD: But thank you for asking. |
| 9 | Q | What is the process that was used to design and |
| 10 |  | implement the R400 into the netlist, starting from |
| 11 |  | I guess the C model? |
| 12 | A | Okay. So let me rephrase the question, make sure |
| 13 |  | I understand correctly. What you are asking is, |
| 14 |  | the way AMD conceived or built the R 400 chip from |
| 15 |  | start to finish, in a general sense, is that what |
| 16 |  | you're asking? |
| 17 | Q | Yeah, was the R400 ever built? |
| 18 |  | MR. RENAUD: Objection. |
| 19 | A | The R400 was prototyped on the IKOS box, yes. |
| 20 | Q | What is IKOS? |
| 21 | A | It's the name and/or the company, I don't |
| 22 |  | remember, of the FPGA device. |
| 23 | Q | So yes, can you please describe for me the way AMD |
| 24 |  | or ATI conceived of the R 400 chip from start to |
| 25 |  | finish. |

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| 1 |  | initiate manufacturing of the silicon device. |
| 2 | Q | You mentioned doing the validation at the block |
| 3 |  | level. Is that done on the C model or the RTL? |
| 4 | A | Okay, some blocks, not all of them, have what we |
| 5 |  | call a block level test bench. And typically, |
| 6 |  | what this does is it's a closed environment around |
| 7 |  | the block that stimulates the block with inputs |
| 8 |  | and gets the output of the block, and then what we |
| 9 |  | do is we use the gold model or the C sim to |
| 10 |  | compare the outputs of the RTL against those we |
| 11 |  | get from the C sim. |
| 12 | Q | How do you know that the outputs from the C |
| 13 |  | simulator are correct? |
| 14 | A | So you'll know that for sure. The C sim, the way |
| 15 |  | we validate it is to use it to generate the final |
| 16 |  | pictures that we're expecting, and so the |
| 17 |  | assumption there is if you get the final picture |
| 18 |  | correct, then the interfaces in between will also |
| 19 |  | be correct. However, you know, as you run this |
| 20 |  | process, it's possible that you're going to get |
| 21 |  | mismatches between the RTL and the C sim and |
| 22 |  | sometimes, you know, the C sim is wrong and so you |
| 23 |  | just work on it until they agree, and you keep the |
| 24 |  | final image correct. |
| 25 | Q | So you mentioned you started your work originally |

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| 1 |  | on -- I'm probably going to get this wrong, but -- |
| 2 |  | I'm sorry, just to make sure I don't mess up |
| 3 |  | the -- I think you said pearl and noise, is that |
| 4 |  | correct? |
| 5 | A | Yes, that's what I said. |
| 6 | Q | What is pearl and noise? |
| 7 | A | Pearl and noise is a specific continuous noise |
| 8 |  | function that is used typically to introduce or |
| 9 |  | simulate natural environments, or like turbulence |
| 10 |  | or such. So if you want to do a cloud, cloud |
| 11 |  | doesn't have a very definite form, and so some |
| 12 |  | kind of noise needs to be introduced to create the |
| 13 |  | randomness. |
| 14 |  | So pearl and noise is a procedural manner to |
| 15 |  | generate said turbulence so that you can then |
| 16 |  | introduce it into graphic models. |
| 17 | Q | Was your work on pearl and noise at a |
| 18 |  | specification level or were you already working in |
| 19 |  | $C$ and/or RTL? |
| 20 | A | It's been a long, long time, but I believe I did |
| 21 |  | both, a model of the pearl and noise on $C$, as well |
| 22 |  | as specifications of what it would have been. So |
| 23 |  | both. Again, kind of an architect role on it too. |
| 24 | Q | What about RTL? |
| 25 |  | MR. RENAUD: Objection. |

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| 1 | A | At AMD, we tried not to have the same person that |
| 2 |  | defines the architecture and writes the C model |
| 3 |  | also writes the RTL, for the obvious reason that |
| 4 |  | if you have one person doing that, if he does an |
| 5 |  | error on one, he's likely to do the error on the |
| 6 |  | other. So we try to have the architect do the C |
| 7 |  | sim and another person under the direction write |
| 8 |  | the RTL, so that you have more chances of finding |
| 9 |  | errors and issues. |
| 10 | Q | You said your next role I believe was with the |
| 11 |  | scan converter, is that correct? |
| 12 | A | Yes, that is correct. |
| 13 | Q | What is a scan converter? |
| 14 |  | MR. RENAUD: Objection. |
| 15 | A | The scan converter in the R400 is the hardware |
| 16 |  | block that takes triangles or primitives and |
| 17 |  | rosterizes them. So it creates pixels or |
| 18 |  | identifies which pixels on the screen would belong |
| 19 |  | to that primitive, whether it's a triangle or some |
| 20 |  | other primitive. That's what we call scan |
| 21 |  | converting. |
| 22 | Q | Were you an architect for the scan converter? |
| 23 | A | I worked on the scan converter in both the |
| 24 |  | specification and the C sim. I don't know if I |
| 25 |  | was given, you know, formally the architect title, |

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| 1 |  | at least in development by the time I switched |
| 2 |  | over to the sequencer work. |
| 3 | Q | What do you mean by "in development"? |
| 4 | A | Well, as you may or may not know, the graphics |
| 5 |  | processers are not done in one day, so takes an |
| 6 |  | extensive time to build a GPU, and so what I mean |
| 7 |  | by "in development," I mean it was in that |
| 8 |  | development period. |
| 9 | Q | The R300 was still in development is what you're |
| 10 |  | saying, is that right? |
| 11 | A | At the time I switched to the R400 sequencer, yes, |
| 12 |  | I believe that was the case, but talking from |
| 13 |  | memory. Again, I'm sure we can find public |
| 14 |  | records or what not to put the dates on the |
| 15 |  | calendar, but that is my recollection. |
| 16 | Q | Did the R300 ever get commercialized? |
| 17 |  | MR. RENAUD: Objection. |
| 18 | A | Yes, I believe it did. |
| 19 | Q | What was the name of the commercial chip? |
| 20 | A | I am very bad with commercial names. I have no |
| 21 |  | idea. I only know the internal names. Even today |
| 22 |  | actually, so. I'm terrible with these. They have |
| 23 |  | these weirdest nomenclatures. |
| 24 | 2 | What public records would you look at to determine |
| 25 |  | when the R300 was finished with development? |

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|  |  | This is the beginning of tape 2. We're back on |
| 2 |  | the record. |
| 3 | 2 | Mr. Lefebvre, before the break we were talking |
| 4 |  | about the unified shader and the R400, do you |
| 5 |  | recall that? |
| 6 | A | I recall conversations about the R400 unified |
| 7 |  | shared, yes. I mean, if you want to talk about |
| 8 |  | specifics, we can pull back my previous answers |
| 9 |  | and discuss about them. |
| 10 | Q | What is a shader? |
| 11 |  | MR. RENAUD: Objection. |
| 12 | A | In the context of the R400, a shader is the block |
| 13 |  | that runs the pixel in all the vertex programs. |
| 14 | 2 | What is a pixel program? |
| 15 | A | So again, in the context of the R 400 , the R 400 is |
| 16 |  | what we call the programmable device, so you can |
| 17 |  | start running small programs on the pixels that |
| 18 |  | the chip generates to perform effects. This is |
| 19 |  | what I referred to as a program, these small, |
| 20 |  | well, programs, shaders; programmable pieces of a |
| 21 |  | GPU . |
| 22 | $Q$ | Is a program in that context a set of |
| 23 |  | instructions? |
| 24 | A | In the R400 was a set of ALU, control flow and |
| 25 |  | memory operations of some kind. |

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| 1 | Q | What is an ALU operation? |
| 2 | A | An ALU operation in the R 400 context is an |
| 3 |  | arithmetic operation. Can be anything you want; |
| 4 |  | an add, subtract, multiply, any kind of an |
| 5 |  | arithmetic operation. |
| 6 | Q | Were there logical operations that were supported |
| 7 |  | in the R400? |
| 8 | A | If you give me the specification, I can answer |
| 9 |  | decisively, but my memory, according to my memory, |
| 10 |  | yes, there were logical operations in the R400 |
| 11 |  | supported. |
| 12 | Q | By the ALU. |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | If memory serves, it was more done by what we call |
| 15 |  | the scalar unit. |
| 16 | Q | What is a scalar unit? |
| 17 | A | So the scalar unit is the unit that does anything |
| 18 |  | that the ALU unit could not do; so more involved |
| 19 |  | functions like exponentials, and you know, bit |
| 20 |  | manipulation and logical operations of sort. And |
| 21 |  | typically, not all the time, scalar operations |
| 22 |  | apply to a whole vector of elements versus ALU |
| 23 |  | operations that operate on a specific thread |
| 24 |  | within that vector of elements. |
| 25 | Q | When you say scalar, is that scalar with an A or |

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|  |  | scalar with an E at the end? Actually, strike |
| 2 |  | that. Can you spell scalar in this context, |
| 3 |  | please? |
| 4 | A | To me, that would be S C A L A R. |
| 5 | Q | When you say "to me," have you seen it both ways |
| 6 |  | before? |
| 7 |  | MR. RENAUD: Objection. |
| 8 | A | I vaguely remember having seen it both ways, but |
| 9 |  | English is my second language and I get some words |
| 10 |  | wrong, and so I'm not your best reference in the |
| 11 |  | English literature. |
| 12 | Q | So you say scalar operations apply to a vector |
| 13 |  | versus ALU operations on a specific thread; are |
| 14 |  | you just talking about the number of either |
| 15 |  | vertices or pixels that are getting affected by |
| 16 |  | the operation? |
| 17 | A | The R400 is operating on -- typically, a single |
| 18 |  | instruction applies to multiple elements, and so |
| 19 |  | when I say a vector, I mean -- I'm representing |
| 20 |  | the elements on which each thread or sub element |
| 21 |  | of that vector can have different data, but then |
| 22 |  | the instruction is the same for all of them. |
| 23 | Q | And for a scalar operation, the data would be the |
| 24 |  | same for all of them? |
| 25 | A | Yes. For the scalar operation, my understanding |

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| :---: | :---: | :---: |
| 1 |  | MR. RENAUD: Objection. |
| 2 | A | Processer. Yeah, you have -- I mean, if you give |
| 3 |  | me the specification -- I don't recall exactly |
| 4 |  | what this word was used for in the R400 |
| 5 |  | specification itself, but talking from memory, a |
| 6 |  | processer to me would mean the collection of ALU's |
| 7 |  | that perform arithmetic operations. |
| 8 | Q | Does that include the scalar? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | Again, I'm not seeing the specs and it's been a |
| 11 |  | long time, but thinking from memory, yes, it would |
| 12 |  | include -- it could include scalar operations as |
| 13 |  | well. |
| 14 | Q | What is a control flow operation? |
| 15 |  | MR. RENAUD: Objection. |
| 16 | A | Control flow operation is an operation that |
| 17 |  | prevents the executions of -- conditionally, |
| 18 |  | prevents the execution of some instructions in the |
| 19 |  | shader. It can be a loop, an if then else |
| 20 |  | condition. |
| 21 | Q | Is a branch a control flow operation? |
| 22 | A | Yes. Branch is typically the operation you use to |
| 23 |  | implement an if then else condition. |
| 24 | Q | In the R400, where were the control flow |
| 25 |  | operations executed? |

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| :---: | :---: | :---: |
| 1 |  | MR. RENAUD: Objection. |
| 2 | A | Again, it would be helpful if $I$ had the spec over |
| 3 |  | me, but best I recall, the operations were |
| 4 |  | executed by the sequencer itself. |
| 5 | Q | What spec would be helpful? |
| 6 | A | Any kind of R400 sequencer spec would be fine with |
| 7 |  | version two. |
| 8 | Q | This is part of the sequencer logic? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | Can you say what do you mean by this? |
| 11 | Q | Sure. Our discussion right now about the three |
| 12 |  | different types of operations that you identified, |
| 13 |  | is that part of the sequencer logic in the R400 |
| 14 |  | and that's why the sequencer specification would |
| 15 |  | have the information? |
| 16 | A | So the scalar processer -- well the scalar unit, |
| 17 |  | the L unit, they're in the SP, the shader pipe. |
| 18 |  | The sequencer controls the control flow operations |
| 19 |  | mostly, especially those that are applying to the |
| 20 |  | whole vector. The reason why I'm asking for a |
| 21 |  | sequencer spec is that I don't remember at what |
| 22 |  | level and at what point we implemented a possible |
| 23 |  | data dependent control flow instructions. |
| 24 | Q | I will try and find that spec for you in a little |
| 25 |  | bit. Just to follow-up on the last one, what is a |

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they're not the ones that pertain to what I
described as the memory operations. When I was talking about memory operations, I was really talking about the memories that are outside the chip on the board.

Q And what in the R 400 is responsible for processing those types of memory operations?

A That's an ambiguous question. I would like you to be more precise. I don't understand what you mean by processing.

Q How is a memory operation performed in the R400?
A Do you mean in the context of the shader of the R400 or -- because there is many blocks on the R400 device and some of these blocks have memory connections. So what are you asking about?

Q In the context of the shader of the R400, how are memory operations performed?

A Okay. The R400 shader contains options to, or instructions that allows either a pixel or a vertex shader to read data from memory, and so these instructions would be issued by the sequencer and executed by the $S B$ to read the source GPRs, and then they could go through what we call the texture unit and then to the memory controller, and eventually the memory system.

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| 1 | Q | Okay. There was a lot there so I'm going to ask |
| 2 |  | you some follow-up questions. |
| 3 |  | What is the difference between instructions |
| 4 |  | and operations? |
| 5 |  | MR. RENAUD: Objection. |
| 6 | A | An instruction is the control that is in the |
| 7 |  | program that tells the hardware how to -- what to |
| 8 |  | fetch and how to fetch it, and the operation, |
| 9 |  | again in my own definition and in the R400, is how |
| 10 |  | this instruction gets executed on the hardware, |
| 11 |  | the steps. |
| 12 | Q | What is the role of the sequencer with regard to |
| 13 |  | instruction execution? |
| 14 |  | MR. RENAUD: Objection. |
| 15 | A | So in the R 400 , the sequencer had the role to |
| 16 |  | choose which instructions would be executed next |
| 17 |  | between pixels and vertices because of the unified |
| 18 |  | nature of the shader as well as the ordering of |
| 19 |  | the instruction within each shader type. |
| 20 | Q | Does shader type refer to vertex and pixel? |
| 21 | A | When I say "shader type" in the R400, I refer to |
| 22 |  | pixels and vertices, yes. |
| 23 | Q | Are there any other kinds of shader types with |
| 24 |  | regard to the R400? |
| 25 | A | At the time, those were the only two types that I |

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| 1 |  | remember. |
| 2 | $Q$ | How did the sequencer order the instructions? |
| 3 | A | What is your question? Can you repeat the |
| 4 |  | question, please. |
| 5 |  | (Question read back.) |
| 6 | A | The instruction order per type is defined by the |
| 7 |  | program itself which is written by the programmer, |
| 8 |  | and the sequencer has to follow that order. So it |
| 9 |  | then forces that order per shader type, but it |
| 10 |  | also gets to pick where to apply the machine |
| 11 |  | between vertex and pixels, and that, that can be |
| 12 |  | done many different ways. |
| 13 | Q | What different ways are you referring to? |
| 14 | A | So in the R400 again, remember we have a shader |
| 15 |  | that is able to operate both pixels and vertices, |
| 16 |  | and so depending on the workload that a chip gets, |
| 17 |  | you can do more pixel work and less vertex work, |
| 18 |  | or vice versa, or have a mix of the two types. |
| 19 |  | That's what I mean by any type. |
| 20 | Q | Did the sequencer order which instruction will get |
| 21 |  | executed within each shader type? |
| 22 | A | I think I already answered that question. I said |
| 23 |  | that the execution was fixed by the programmer, |
| 24 |  | and the sequencer is enforcing the instruction |
| 25 |  | order within each shader type. |

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$1 \quad$ \& So the sequencer can only handle one instruction
set per shader type at a time, is that correct?
MR. RENAUD: Objection.
A I am not clear on your question. I don't
understand what you're asking.
Q I think what you said was that the sequencer did
not have any responsibilities with regard to
determining which instruction was next within,
say, the possible set of pixel instructions. Is
that correct?
MR. RENAUD: Objection.
A So in the R400, you can have, potentially, several
pixel vectors all at once in a shader. Within a
pixel vector, you have to use the ordering as
instructed by the program, but you can choose to
execute the next instruction of any of the pixel
vectors that are on the system.
Q And is the sequencer responsible for that
decision?
MR. RENAUD: Objection.
A The R400 sequencer is responsible for making that
decision, and the decision of whether or not it
wants to execute a vertex or a pixel execution,
yes.
Q You said that within each, let's say pixel vector,
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|  |  | proposal. I mean, must have been around the |
| 2 |  | creation date. I remember having discussions with |
| 3 |  | Steve about this particular spec, but as to |
| 4 |  | exactly when I first saw this, I don't recall the |
| 5 |  | specifics. |
| 6 | Q | Who is Steve? |
| 7 | A | Steve Morein is or was an architect at ATI and is |
| 8 |  | also the author of the spec as stated here on the |
| 9 |  | first page. |
| 10 | Q | What was the purpose of the R 400 Architecture |
| 11 |  | Proposal? |
| 12 | A | I believe the purpose is stated on the page and |
| 13 |  | I'm going to read, "This is a proposal for the |
| 14 |  | overall architecture of the R400. It's just a |
| 15 |  | proposal and nothing is decided yet." So it's to |
| 16 |  | initiate discussions about the R400 project. |
| 17 | Q | Do you know when this document was created? |
| 18 | A | I don't have memories as to when it was created, |
| 19 |  | but it states an originate date of 2000-11-13. |
| 20 |  | And I have no reason to believe those are wrong. |
| 21 | Q | And you started working on the R400 you said in |
| 22 |  | September of 2000, is that correct? |
| 23 | A | I said that I started working on pearl and noise, |
| 24 |  | which you know, we were investigating for the |
| 25 |  | R400, yes, around that timeframe. |

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| 1 | Q | Do you know if ATI searched for those documents |
| 2 |  | for this investigation? |
| 3 |  | MR. RENAUD: Objection. |
| 4 | A | I know that a team of people searched for it, but |
| 5 |  | I also know that this time period, we were using a |
| 6 |  | separate source revision control than Perforce, |
| 7 |  | which made the search much harder for that time |
| 8 |  | period because of it being antiquated and not |
| 9 |  | available. |
| 10 | Q | When did Perforce start being used? |
| 11 | A | I don't remember exactly but, you know, we could |
| 12 |  | go back to the logs, and obviously, the first |
| 13 |  | submissions to the depot would point as to a |
| 14 |  | pretty good idea of when the date was established, |
| 15 |  | effectively. |
| 16 | Q | So you're not sure whether there were or were not |
| 17 |  | other documents in this time period regarding the |
| 18 |  | R400 architecture, is that right? |
| 19 |  | MR. RENAUD: Objection. |
| 20 | A | Like I said, I recall at least diagrams from |
| 21 |  | Steve. There's definitely this one. Whether or |
| 22 |  | not there are others available, I don't know. |
| 23 | Q | Do you recall any others? |
| 24 | A | Well, I was working on the pearl and noise, so you |
| 25 |  | know, I have every reason to believe there would |

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|  |  | remember. I mean, I did discuss this before in my |
| 2 |  | previous testimonies and deposition. We could go |
| 3 |  | grab the records, but that's my recollection. I |
| 4 |  | had discussions with Steve. |
| 5 | Q | Whose idea was it to combine the vertex and pixel |
| 6 |  | shaders into a unified shader? |
| 7 |  | MR. RENAUD: Objection. |
| 8 | A | So Steve came up, as best I can understand, came |
| 9 |  | up with the original concept, but both myself and |
| 10 |  | Andy Gruber all worked on blocks and issues and |
| 11 |  | systems within that unified shader, so as such, |
| 12 |  | it's a collective effort, I would say. |
| 13 | Q | Are you referring to the patented invention now, |
| 14 |  | the patents, or are you talking about the idea of |
| 15 |  | putting a unified shader into the R 400 ? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | Q | Strike that. You said, just so it's clear for the |
| 18 |  | record, you said Andy -- sorry, what was his last |
| 19 |  | name? |
| 20 | A | So there were two Andys, Andi Skende and Andy |
| 21 |  | Gruber. Or Andy Gruber also goes by Andrew |
| 22 |  | Gruber, and Skende is Andi with an I. |
| 23 | Q | So Exhibit 3, which is in front you, discusses the |
| 24 |  | idea of using a unified shader for vertex and |
| 25 |  | pixel operations in the R400, is that correct? |

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| 1 | Q | Do you know who first suggested the idea of |
| 2 |  | combining vertex and pixel operations into a |
| 3 |  | single shader? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | Like I previously stated in my prior depositions, |
| 6 |  | I believe I said that I thought that Steve Morein |
| 7 |  | came up with the original idea, or the original |
| 8 |  | concept, and then we worked collectively to |
| 9 |  | further the idea into a design. |
| 10 | Q | Do you recall having contributed to this document, |
| 11 |  | the R400 Architecture Proposal that's Exhibit 3? |
| 12 |  | MR. RENAUD: Objection. |
| 13 | A | Can you define what you mean by "contributed"? |
| 14 |  | You mean typing words into the spec or do you mean |
| 15 |  | having -- |
| 16 | Q | Did you write any parts of Exhibit 3? |
| 17 | A | I don't recall writing personally any part of |
| 18 |  | Exhibit 3, no. |
| 19 | Q | When did you first start working with Mr. Skende |
| 20 |  | on the R400? |
| 21 |  | MR. RENAUD: Objection. |
| 22 | A | So best I can recall, Mr. Skende was working on |
| 23 |  | the R200 at the very, very onset of my beginning |
| 24 |  | to work at ATI. And again, if I recall correctly, |
| 25 |  | and I'm talking from very, very long time memory, |

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|  |  | the interactions really started in earnest when we |
| 2 |  | were developing the sequencer and the shader pipe |
| 3 |  | for the unified shader, so would have been |
| 4 |  | somewhere around the september 2001 timeframe. |
| 5 | Q | What is the R200? |
| 6 | A | The R200 is the chip that preceded the R300 in |
| 7 |  | nomenclature and was developed by the, in part by |
| 8 |  | the Orlando -- not the Orlando office -- well, the |
| 9 |  | Orlando office, yes, but also the Marlborough |
| 10 |  | office, which I was part of. |
| 11 | Q | Was the R200 ever manufactured into a chip? |
| 12 | A | Yes, my recollection is that it was, yes. |
| 13 | Q | Do you recall the name of that chip? |
| 14 | A | I don't recall the name. I know the internal |
| 15 |  | project name was Chaplain, and probably was called |
| 16 |  | something like Radeon, but like I said, I'm |
| 17 |  | terrible with marketing names. We never use them |
| 18 |  | in engineering. |
| 19 | Q | When did you first start working with Mr. Gruber? |
| 20 | A | Can you refine the question please because |
| 21 |  | Mr. Andy Gruber was my manager right from the |
| 22 |  | onset, so -- |
| 23 | Q | When did you start working on the R400 with |
| 24 |  | Mr. Gruber? |
| 25 | A | On the R -- I mean I've been always working on the |

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| 1 |  | R400 project, so Andy Gruber was my manager and |
| 2 |  | engaged in technical discussions right from the |
| 3 |  | beginning on the various topics that were assigned |
| 4 |  | to me, so as far as I know, I've been working with |
| 5 |  | Mr. Gruber for the whole time that I was employed |
| 6 |  | in the Boston office. |
| 7 | Q | September 2000? |
| 8 |  | MR. RENAUD: Objection. |
| 9 | A | From my initial employment day, yeah; September |
| 10 |  | 2000 to, until I moved back to Montreal. |
| 11 | Q | What was Mr. Gruber's title at the time you worked |
| 12 |  | with him on the unified shader? |
| 13 | A | I believe I already answered that question in a |
| 14 |  | previous deposition, so you must already know the |
| 15 |  | answer to that, but I don't recall what his title |
| 16 |  | was. I didn't recall it then, I don't recall it |
| 17 |  | now. |
| 18 | Q | What was Mr. Skende's title when you worked with |
| 19 |  | him on the unified shader? |
| 20 |  | MR. RENAUD: Objection. |
| 21 | A | Some kind of engineer. Again, I don't recall |
| 22 |  | exactly. |
| 23 | Q | Do you recall Mr. Morein's title when you worked |
| 24 |  | with him on the unified shader? |
| 25 |  | MR. RENAUD: Objection. |

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| 1 | A | No, not directly either. Again, these are all |
| 2 |  | questions that I'm pretty sure I answered |
| 3 |  | previously in depositions. |
| 4 | Q | You understand this is a different case from your |
| 5 |  | prior depositions, correct? |
| 6 | A | I do understand, and you have every right to ask |
| 7 |  | your questions, but I also understand you have all |
| 8 |  | that documentation, so it is available to you and |
| 9 |  | they are the exact same questions. As far as I |
| 10 |  | remember. |
| 11 | Q | Is all of your prior testimony, do you believe, |
| 12 |  | correct as you sit here today? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | So as I read through them, I found a few typos and |
| 15 |  | filed a errata sheet for both, and could not find |
| 16 |  | other discrepancies as best as I can tell, but if |
| 17 |  | you want to bring them up and discuss them, I'm |
| 18 |  | more than welcome to comment on them if you want |
| 19 |  | to. |
| 20 | Q | To your point, it seems rather than walk through |
| 21 |  | some of the stuff you believe you already |
| 22 |  | answered, do you still stand behind all of your |
| 23 |  | prior deposition testimony as being accurate and |
| 24 |  | correct? |
| 25 |  | MR. RENAUD: Objection. |

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|  |  | offering you an opportunity to say that you |
| 2 |  | believe that this deposition transcript is still |
| 3 |  | true and accurate with regard to your answers. Is |
| 4 |  | that the case? Is this deposition transcript true |
| 5 |  | and accurate to your knowledge? |
| 6 |  | MR. RENAUD: Objection. |
| 7 | A | To the best of my knowledge. I mean, there could |
| 8 |  | be dates here and there that I got wrong or |
| 9 |  | anything, but the generic sense when I read |
| 10 |  | through it yesterday -- it was yesterday, it was |
| 11 |  | not just now -- looked to be accurate. Yeah. |
| 12 |  | MR. ELENGOLD: I'll ask the court reporter |
| 13 |  | to please mark Exhibit 5. |
| 14 |  | (Document marked Exhibit 5 for |
| 15 |  | identification.) |
| 16 | Q | Before we turn to Exhibit 5, one more question for |
| 17 |  | you, Mr. Lefebvre, what was the subject matter of |
| 18 |  | your deposition in Exhibit 4? |
| 19 |  | MR. RENAUD: Objection. |
| 20 | A | Well, the first date -- the first page, sorry, |
| 21 |  | states that this was related to case |
| 22 |  | IPR-2015-00325, Patent 7,742,053 B2; Case |
| 23 |  | IPR-2015-00326, Patent 6,897,871, and Case |
| 24 |  | IPR-2015-00330, Patent 7,327,369 B2. So I don't |
| 25 |  | know. |

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| 1 | $Q$ | You just read the case caption, correct? |
| 2 | A | Yes. |
| 3 | Q | Do you recall what the subject matter was of the |
| 4 |  | deposition -- or strike that. Do you recall why |
| 5 |  | you were deposed in that case? |
| 6 |  | MR. RENAUD: Objection. |
| 7 | A | I recall talking in this deposition about the R400 |
| 8 |  | sequencer and multi-threaded patent which was -- |
| 9 |  | and also the unified shader patent, but |
| 10 |  | specifically, what was the purpose, I don't recall |
| 11 |  | exactly. |
| 12 | Q | When you say the "unified shader patent," is that |
| 13 |  | your understanding of the same family of patents |
| 14 |  | that's at issue in this investigation? |
| 15 |  | MR. RENAUD: Objection. |
| 16 | A | So my recollection is one of these patents, yes, |
| 17 |  | was from that family. |
| 18 | Q | Turning now to Exhibit 5, which is Bates stamped |
| 19 |  | AMD1044_0175035 through 175187. |
| 20 |  | Mr. Lefebvre, have you seen Exhibit 5 |
| 21 |  | before? |
| 22 | A | Yes, I have seen this Exhibit before. |
| 23 | Q | What is Exhibit 5? |
| 24 | A | This is the videotape deposition that I did on |
| 25 |  | December 9, 2016. |

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| :---: | :---: | :---: |
| 1 | A | There is also an errata sheet. |
| 2 |  | MR. RENAUD: We're going to confirm it's |
| 3 |  | either been produced or produce it. |
| 4 |  | MR. ELENGOLD: That would be great. Thank |
| 5 |  | you. |
| 6 | Q | So, you know, just to make sure the record is |
| 7 |  | clear then on that point, so other than the two |
| 8 |  | errata sheets, is there anything in Exhibits 4 and |
| 9 |  | Exhibit 5 that you wish to correct today for this |
| 10 |  | deposition? |
| 11 | A | Again, I'm human, but from reading through those, |
| 12 |  | they sound correct. So they sounded correct when |
| 13 |  | I read through them. |
| 14 |  | MR. ELENGOLD: I'll ask the court reporter |
| 15 |  | to please mark Exhibit 6. |
| 16 |  | (document marked Exhibit 6 for |
| 17 |  | identification.) |
| 18 |  | MR. ELENGOLD: For the record, Exhibit 6 is |
| 19 |  | Bates stamped AMD1044_0011617 through 11682. |
| 20 | Q | Mr. Lefebvre, have you seen Exhibit 6 before? |
| 21 | A | Yes, I have seen Exhibit 6 before. |
| 22 | Q | What is Exhibit 6? |
| 23 | A | This is, and I quote "Declaration of Inventor |
| 24 |  | Laurent Lefebvre Regarding the Invention Date of |
| 25 |  | U.S. Patent 6897871. |

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| :---: | :---: | :---: |
| 1 | Q | Did you author Exhibit 6? |
| 2 | A | I prepared Exhibit 6 with the help of counsel, |
| 3 |  | yes. |
| 4 | Q | Who wrote Exhibit 6? |
| 5 |  | MR. RENAUD: Objection. |
| 6 | A | Exhibit 6 was written by counsel upon my |
| 7 |  | instructions and guidance. |
| 8 | Q | And not your counsel here today, but prior counsel |
| 9 |  | you worked with, is that correct? |
| 10 | A | Yes. This is what I remember, correct. |
| 11 | Q | Why did you work with counsel to prepare the |
| 12 |  | declaration in Exhibit 6? |
| 13 |  | MR. RENAUD: And I'll instruct you not to |
| 14 |  | answer if that calls for revealing any |
| 15 |  | attorney/client communication. |
| 16 | A | My understanding is that this declaration was |
| 17 |  | created to establish a date of invention, or of |
| 18 |  | creation, if you will, of the R400. |
| 19 | Q | Do you mean a date of invention of creation for |
| 20 |  | the patent at issue that's on the front page, or |
| 21 |  | for the R400? |
| 22 |  | MR. RENAUD: Objection. |
| 23 | A | I meant establish an earlier date than the patent |
| 24 |  | was issued. |
| 25 | Q | An earlier date for what? |

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| 1 | A | This is correct. I mean, there is my electronic |
| :---: | :---: | :---: |
| 2 |  | signature here on the last page. I have no reason |
| 3 |  | to believe it's wrong. |
| 4 | Q | Do you still believe that the statements you made |
| 5 |  | in your declaration are true and accurate? |
| 6 |  | MR. RENAUD: Objection. |
| 7 | A | At best I can recall, yes. I mean, I did not see |
| 8 |  | any inaccuracies as I browsed through this |
| 9 |  | document for preparing to this deposition. |
| 10 | Q | Is there anything you wish to correct in this |
| 11 |  | document? |
| 12 | A | No. Not that I know of. |
| 13 | Q | So I'll ask you to turn to paragraph 6, please, on |
| 14 |  | page 3. And do you see where it says in the |
| 15 |  | second sentence, "We collectively conceived of the |
| 16 |  | graphics-processing system claimed in the '871 |
| 17 |  | patent no later than early 2002, while working on |
| 18 |  | the R400"? |
| 19 | A | Yes. I see. |
| 20 | Q | What did you mean by that statement? |
| 21 | A | So again, the specific wording is not mine. It |
| 22 |  | was written by counsel, but reading this, to me it |
| 23 |  | means that the -- we conceived or we made a |
| 24 |  | product called the R400, and it was operating to |
| 25 |  | perform pixel and vertex functions, no later than |

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| 1 |  | early 2002. |
| 2 | Q | What did you mean by the graphics-processing |
| 3 |  | system claimed in the '871 patent? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | So again, these are not my words. They're the |
| 6 |  | words of my counsel, but the graphics-processing |
| 7 |  | system is the graphics core of a GPU. So the |
| 8 |  | whole graphics infrastructure. |
| 9 | Q | And did you intend to offer testimony regarding |
| 10 |  | when you conceived of the actual claimed system in |
| 11 |  | the patent, or were you trying to just refer to |
| 12 |  | the R400 in your statement? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | Q | You can strike that. |
| 15 |  | And I know I'm going to ask you some general |
| 16 |  | question, but I wanted to have these documents in |
| 17 |  | front you, so please feel free to reference them |
| 18 |  | if you would like to as we go through the day |
| 19 |  | since I know you mentioned that you wanted to |
| 20 |  | ensure your accuracy across the documents so -- |
| 21 | A | I appreciate that. |
| 22 | Q | Is that helpful to have those in front you now? |
| 23 | A | Yes. I will, as, if I remember more, refer to |
| 24 |  | these documents. |
| 25 | Q | So now -- and I'll tell you, looking at your |

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|  |  | operation that you can do in a pixel shader that |
| 2 |  | does not affect color. |
| 3 | 2 | Any others? |
| 4 | A | Offhand, not that I can remember from the pixel |
| 5 |  | shader side, no. |
| 6 | Q | What is a vertex operation? |
| 7 |  | MR. RENAUD: Objection. |
| 8 | A | In the R400 context, and assuming by "vertex |
| 9 |  | operation" you mean vertex shader operation, that |
| 10 |  | would be the instructions executed on the vertex |
| 11 |  | shader. |
| 12 | Q | What types of operations are instructed on -- |
| 13 |  | sorry, strike that. |
| 14 |  | What types of operations are executed on a |
| 15 |  | vertex shader? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | On the R400, the vertex shader supported, I |
| 18 |  | believe -- again, you give me the R400 sequencer |
| 19 |  | specification I can be more precise, but my |
| 20 |  | recollection is that it allowed for memory fetch |
| 21 |  | operations as well as scalar operations, ALU |
| 22 |  | operations, and control flow. |
| 23 | Q | What were the benefits of using a unified shader |
| 24 |  | in the R400? |
| 25 | A | Okay, so that's one I know I answered already. |

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| 1 |  | the R400? |
| 2 | A | Okay. The benefits of the R 400 unified shader are |
| 3 |  | two fold. The first one is that it is an area |
| 4 |  | reduction benefit by which you can only have one |
| 5 |  | shader instead of two. So it's by definition |
| 6 |  | smaller. |
| 7 |  | The second benefit is that it can operate on |
| 8 |  | both pixels and vertices dynamically and assign |
| 9 |  | the shader to either or both pixels and vertices |
| 10 |  | depending on the workload, and the third benefit |
| 11 |  | is that having only one shader core to validate, |
| 12 |  | it simplifies the validation purposes. |
| 13 | Q | By "validation," you mean testing for |
| 14 |  | commercialization? |
| 15 | A | By validation, I mean testing, yes. |
| 16 | Q | What kind of validation is done to make sure that |
| 17 |  | GPU works successfully? |
| 18 |  | MR. RENAUD: Objection. |
| 19 | A | Do you mean the classes of verification? I am |
| 20 |  | not -- this is a pretty broad question. I want to |
| 21 |  | make sure that I answer it very directly. |
| 22 | Q | That's fine. |
| 23 | A | So what are you concerned about? |
| 24 | Q | Well, you mentioned that validation is a benefit |
| 25 |  | of using unified shared, correct? |

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| 1 |  | discussed before, is relatively, |
| 2 |  | relatively-speaking, fast. |
| 3 |  | The RTL simulation itself, when you run the |
| 4 |  | RTL code, then you're trying to compare it with |
| 5 |  | the golden C simulator. That is the thing that |
| 6 |  | takes a lot of time. |
| 7 | Q | Is it -- does it take a lot of time because you're |
| 8 |  | fixing errors in the RTL, or does it take a lot of |
| 9 |  | time because it's just slow to run tests? |
| 10 |  | MR. RENAUD: Objection. |
| 11 | A | It takes a lot of time because it's just very slow |
| 12 |  | to run anything. I mean, for example, you can't |
| 13 |  | imagine running a few frames of a game on an RTL |
| 14 |  | simulator. It just -- it would take months. |
| 15 | Q | And the FPGA simulator lets you run those tests |
| 16 |  | faster? |
| 17 |  | MR. RENAUD: Objection. |
| 18 | A | Yes, the FPGA device, hardware device lets you run |
| 19 |  | tests much, much faster. |
| 20 | Q | Why is that? |
| 21 | A | In part, because it is a hardware device, so it's |
| 22 |  | not an emulation of the system. It is the system |
| 23 |  | in some hardware form and it can run the system -- |
| 24 |  | it doesn't have to emulate the system. It just, |
| 25 |  | you know, runs as if it was a chip just at a much |

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|  |  | something obviously you can commercialize because |
| 2 |  | it's very expensive, it's very big. |
| 3 | Q | And so in order to do that, it's already been laid |
| 4 |  | out at that point, like the F -- I'm sorry, I keep |
| 5 |  | getting the -- P -- |
| 6 | A | FPGA. |
| 7 | Q | No, no, I'm sorry, the team we were talking about |
| 8 |  | earlier. |
| 9 | A | PD. |
| 10 | Q | The PD team. So it's already been laid out in |
| 11 |  | order to see how all those interconnections will |
| 12 |  | work by the PD team? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | Not being on the IKOS, you know, team, I don't |
| 15 |  | have the, in great details exactly how that |
| 16 |  | process works, and AMD can bring in the experts if |
| 17 |  | you want more details on that. We have some |
| 18 |  | people, but I don't know to what extent it needs |
| 19 |  | to be floor plan to be able to operate on the |
| 20 |  | FPGA. |
| 21 | Q | Did you -- sorry, go ahead. |
| 22 | A | It starts from the same netlist, that is what I |
| 23 |  | was wanting to say. |
| 24 | Q | Did you work on the netlist? |
| 25 |  | MR. RENAUD: Objection. |

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1 A Can you define what you mean by "work on the netlist"? I mean --

Q Did you have any responsibilities with regard to creation of the netlist?

MR. RENAUD: Objection.
A The creation of the netlist is an automated process by which we call synthesis. It takes in the RTL and, you know, outputs the netlist. So that would have been the responsibility of the RTL designer, but effectively, it's our design, so I'm not directly connected to the netlist, but in a sense, I've worked on the netlist. I mean --

Q Your specification results in a netlist.
MR. RENAUD: Objection.
A The work that I've done in specifying the R400 sequencer, as well as the models that we created, the $C$ sim model to validate the RTL, they all turn into eventually the netlist because they are used to generate that netlist, indirectly.

Q Some of this is new because I don't think you described the FPGA simulator in your declaration, is that correct?

MR. RENAUD: Objection.
A That is correct. I don't think that $I$ described these in my previous declarations because I was

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| :---: | :---: | :---: |
| 1 |  | not aware at the time that we did FPGA |
| 2 |  | simulations, or I did not recall at the time that |
| 3 |  | we did FPGA simulation, or FPGA prototyping would |
| 4 |  | be a better word, on the R400. I mean, it is |
| 5 |  | common practice, but again, it's been so long, I |
| 6 |  | was not aware when exactly we started doing that |
| 7 |  | process. |
| 8 | Q | And when did you start looking into that? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | The legal -- I mean not the legal team, but the |
| 11 |  | team at AMD that collected the document brought to |
| 12 |  | me evidence that the IKOS machine was used in the |
| 13 |  | R400 project. |
| 14 |  | MR. RENAUD: I don't want you to give any |
| 15 |  | communications with that team, but you can |
| 16 |  | continue your answer. |
| 17 |  | THE WITNESS: Yes, sir. |
| 18 | A | And so those were the two presentations that I |
| 19 |  | divulged before that, you know, describe the |
| 20 |  | netlist, what they were, and the progress on IKOS, |
| 21 |  | and so that is when I got aware of the IKOS |
| 22 |  | prototyping effort. |
| 23 | Q | When was that? |
| 24 | A | These documents were disclosed to me over the last |
| 25 |  | two days. |

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Q And were they disclosed to you by counsel or someone from AMD?

MR. RENAUD: You can answer that with either of those answers, counsel or AMD.

A Counsel.
Q Were you involved in any work with the FPGA system?

MR. RENAUD: Objection.
A Again, in the R400 it's the same thing. I was not directly involved into the work of pushing the netlist on the FPGA prototype, but $I$ was involved in the design of the R400, so indirectly, you know, you can involve me with any given step of the way, but I did not directly work on the IKOS machine, no.

Q Who did?
A So during the break, I browsed through some documents we had, and at least there was a person named Colin Stuart that was named in the logs, and by the way, he is the one that I spoke on the phone with for preparation.

There was another name, but unfortunately, I lost it again. But it's in --

MR. RENAUD: I can tell you what that name is if it's helpful.

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| :---: | :---: | :---: |
|  |  | MR. ELENGOLD: That's okay. Let's let him |
| 2 |  | testify. |
| 3 | A | I forgot about it. I knew the names coming in but |
| 4 |  | then we discussed things. |
| 5 | Q | Did you talk to your counsel about the substance |
| 6 |  | of your deposition during the break? Just a yes |
| 7 |  | or no question. |
| 8 | A | No. |
| 9 | Q | You reviewed these documents on your own? |
| 10 |  | MR. RENAUD: You can answer that yes or no. |
| 11 | A | Yes. |
| 12 | Q | What documents did you review during the break? |
| 13 | A | There was an IKOS log file document that listed |
| 14 |  | all the interactions and steps involving IKOS. I |
| 15 |  | mean, it's probably not an all inclusive document, |
| 16 |  | but at the very least, it had a few names and |
| 17 |  | information that were helpful into establishing |
| 18 |  | the IKOS work. |
| 19 | Q | What do you mean by "establishing the IKOS work"? |
| 20 | A | I mean which netlist was ported to the IKOS and |
| 21 |  | when that netlist was pushed on the IKOS machine. |
| 22 | Q | Is a netlist tied to a version of RTL? |
| 23 |  | MR. RENAUD: Objection. |
| 24 | A | Okay. This is a tricky answer. A netlist is a |
| 25 |  | collection of synthesis files, and the collection |

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| 1 | Q | What is the driver? |
| :---: | :---: | :---: |
| 2 | A | For the R 400 GPU , in order to connect an |
| 3 |  | application which is, you know, a game or anything |
| 4 |  | to the hardware system, the application goes |
| 5 |  | through what we call an API which defines the |
| 6 |  | operations that the application can perform, but |
| 7 |  | that API defines broadly what applications can do, |
| 8 |  | and has to be vendor independent so that |
| 9 |  | applications can work on any graphics device. |
| 10 |  | What sits under that API is a driver which |
| 11 |  | is a software piece of code that interprets the |
| 12 |  | API commands and translates them to hardware |
| 13 |  | commands. |
| 14 | Q | So do you know when the driver first ran on the |
| 15 |  | FPGA system? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | From what I could gather at this point, I |
| 18 |  | couldn't -- I don't have a conclusive date. I |
| 19 |  | mean $I$ see, like I said, see some projection dates |
| 20 |  | in these program reviews. This is all very fresh. |
| 21 |  | Like I said, I'm sure if you want to dig into that |
| 22 |  | more, AMD can provide more information, but at |
| 23 |  | this point I cannot give you any dates. |
| 24 | Q | And is all your information regarding the IKOS |
| 25 |  | system from the documents you've reviewed in the |

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| :---: | :---: | :---: |
| 1 |  | past two days? |
| 2 |  | MR. RENAUD: Objection. |
| 3 |  | MR. ELENGOLD: Sorry, strike that. |
| 4 | Q | Is all your knowledge regarding the IKOS system in |
| 5 |  | the R400 from the documents you've reviewed in the |
| 6 |  | past two days? |
| 7 |  | MR. RENAUD: Objection. |
| 8 | A | I would say most of my knowledge, you know, as I |
| 9 |  | stated, there are some indications in the program |
| 10 |  | reviews about some IKOS dates in there which I |
| 11 |  | didn't pay attention to before, but the |
| 12 |  | information was there. So to be fair, it was |
| 13 |  | there, not to a great extent though. |
| 14 | Q | Is all your knowledge regarding the IKOS system |
| 15 |  | from documents that you have reviewed, or do you |
| 16 |  | have any personal recollections regarding any of |
| 17 |  | the IKOS testing? |
| 18 |  | MR. RENAUD: Objection. |
| 19 | A | No, not having worked directly on the IKOS |
| 20 |  | prototype device, I don't have any personal |
| 21 |  | recollection of such. |
| 22 | Q | Did you talk to anyone about the FPGA system in |
| 23 |  | the IKOS testing? |
| 24 | A | One of the phone calls that we had yesterday or |
| 25 |  | the day before, I don't remember, was about that |

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| :---: | :---: | :---: |
| 1 |  | topic, yes. |
| - | Q | Who did you talk to? |
| 3 | A | That Colin Stuart, and that other person which my |
| 4 |  | counsel can give you the name to. It's also in |
| 5 |  | that, in the documents so -- |
| 6 | Q | Who is Colin Stuart? |
| 7 | A | Colin Stuart, as I understand it, is a manager; at |
| 8 |  | least at the time, he was managing the IKOS |
| 9 |  | effort. |
| 10 | Q | Is Mr. Stuart still at AMD or ATI? |
| 11 | A | To the best of my knowledge, since I talked to him |
| 12 |  | yesterday or the day before, yes. |
| 13 | Q | So he was still when you talked to him? |
| 14 | A | Yes. |
| 15 | Q | Do you know Mr. Stuart's current position? |
| 16 | A | No. Unfortunately not, but I can find that out if |
| 17 |  | you want to. |
| 18 | Q | How long did you talk to Mr. Stuart for? |
| 19 | A | My recollection was in the vicinity of half an |
| 20 |  | hour to 45 minutes. |
| 21 | Q | What did you learn with regard to the FPGA system |
| 22 |  | and the IKOS testing from Mr. Stuart? |
| 23 | A | Mostly the timelines and what was on the IKOS |
| 24 |  | machine at the time. That kind of information. |
| 25 | Q | What timelines did you learn? |

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| :---: | :---: | :---: |
| 1 | A | So again, I don't recall the specifics, but |
| 2 |  | Mr. Stuart is named into file log and that file |
| 3 |  | log that the dates of the entries, and so while I |
| 4 |  | don't remember the exact dates and stuff, I could |
| 5 |  | tell, you know, what was going on, and that file |
| 6 |  | log also was stating which netlist -- because each |
| 7 |  | netlist has a number -- was used for IKOS. |
| 8 |  | So you know, we just had the opportunity to |
| 9 |  | discuss that and make sure we were aligned. |
| 10 | Q | What do you mean? What do you mean aligned? |
| 11 | A | Aligned on the, that the data that I was seeing in |
| 12 |  | the log was consistent with his memory because, |
| 13 |  | you know, he was much more hands-on than I would |
| 14 |  | have been on the IKOS machine. |
| 15 | Q | So what timelines do you recall learning from |
| 16 |  | Mr. Stuart? |
| 17 | A | I mean corroborating evidence that the work on |
| 18 |  | IKOS was, you know, at least done to some extent |
| 19 |  | prior to that presentation. |
| 20 | Q | February 2000? |
| 21 | A | February 2000, yeah, making sure the presentation |
| 22 |  | and the logs were consistent. |
| 23 |  | So I wouldn't say that I learned any new |
| 24 |  | dates from the discussion. It was more to, as |
| 25 |  | best as we could, make sure that everything was |

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|  |  | back then, but, you know, that should give you -- |
| 2 |  | those are the guidelines I can provide. |
| 3 | Q | You're not aware of any frozen set of RTL that |
| 4 |  | represents what was put on the IKOS machine, |
| 5 |  | correct? |
| 6 |  | MR. RENAUD: Objection. |
| 7 | A | So I am aware of Netlist 3, and that there is |
| 8 |  | evidence that these files are -- eventually came |
| 9 |  | from a branch, and so the question is, yes, there |
| 10 |  | is evidence of freezing the RTL. What we could |
| 11 |  | not assess yet is what RTL files were pulled into |
| 12 |  | that branch and eventually pushed onto the Netlist |
| 13 |  | 3. That's the part what we're missing right now. |
| 14 | Q | Why do you refer to it as Netlist 3? Was there a |
| 15 |  | Netlist 2? |
| 16 | A | There is evidence on the Perforce server of many |
| 17 |  | netlist numbers; some poorly named, some well |
| 18 |  | named, but the reason why I'm referring to Netlist |
| 19 |  | 3 is that this is a number that we could find that |
| 20 |  | is consistent across netlist generation and |
| 21 |  | documentation and presentation, so that we can |
| 22 |  | establish a link on what went on when, where. |
| 23 | Q | When was the first netlist created? |
| 24 |  | MR. RENAUD: Objection. |
| 25 | A | I don't recall directly, but I believe it's in one |

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A So I said that the RTL code gets stable when --
    and I don't remember if I called it first tri or
    one tri, but there is this one test which is a
    single triangle that we tried to run first, and
    that establishes proof of life, and once that test
    gets working, we keep it working, and we make sure
    that all the designers have to run it after they
    make any change to make sure they did not break
    anything. And so, you know, I think in this --
    where is it.
    Q Are you looking at your declaration?
    A I am looking at Exhibit No. 6, page 30, where you
        have an example of that first triangle. And in
        this particular declaration, it is labeled that,
        for the successful first triangle. This is what I
        am referring to.
    Q Just make sure I heard you correctly and the court
        reporter got it too. First triangle, not first
        try? Or does it mean the same thing?
    A First tri is a contraction of first triangle. So
        when we -- when I said first tri, I meant first
        triangle, and it's just a contraction.
    Q Which is fine, but you understand, just for
        purposes of the records, that's why I'm asking you
        to clarify to make sure your testimony is
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| 1 |  | accurate. |
| 2 | A | Okay. |
| 3 | Q | So earlier you were referring to the first |
| 4 |  | triangle test that's on page 30 of Exhibit 6, is |
| 5 |  | that right? |
| 6 | A | That is correct. Yes. |
| 7 | Q | And what type of work is done on the RTL after |
| 8 |  | it's stable? |
| 9 | A | So the first triangle test establishes what we |
| 10 |  | call a proof of life, meaning that the hardware |
| 11 |  | can operate from top to bottom on what it's |
| 12 |  | supposed to do, but as you can imagine, to have a |
| 13 |  | commercial product, you need to test all the sub |
| 14 |  | features and, you know, various instructions and |
| 15 |  | what not that might not be needed for first |
| 16 |  | triangle. |
| 17 |  | So from that point on, all the work that |
| 18 |  | goes through is really to verify and complete all |
| 19 |  | the sub feature work to make sure you have a |
| 20 |  | commercial product, and there's also performance |
| 21 |  | testing that comes along after that point. |
| 22 | Q | How is performance testing done on the RTL? |
| 23 |  | MR. RENAUD: Objection. |
| 24 | A | So on the R400 project, what we have is the set of |
| 25 |  | tests, and we measure the number of clocks it |

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|  |  | takes to process, you know, a triangle, two |
| 2 |  | triangles, 10 triangles and what not, and knowing |
| 3 |  | the through-put that the chip is capable of, let's |
| 4 |  | say that the chip can do four pixels per clock, |
| 5 |  | I'm making up a configuration, then we make sure |
| 6 |  | that if you have a triangle that is 10,000 pixels, |
| 7 |  | then the chip does not take more than 10,000 |
| 8 |  | divided by four, that kind of performance testing. |
| 9 | Q | And is that kind of testing done on an IKOS |
| 10 |  | machine, or is it done on the C sim, or is it done |
| 11 |  | on, I think you said VCS simulator for the RTL? |
| 12 |  | MR. RENAUD: Objection. |
| 13 | A | What we did for the R 400 , that type of testing on |
| 14 |  | that project occurred on the VCS simulator because |
| 15 |  | this is representation of the hardware. It did |
| 16 |  | not occur on the IKOS machine as far as I know, |
| 17 |  | which was more used for software bringing up |
| 18 |  | purposes, and it can also -- it cannot really |
| 19 |  | occur on the C sim because the C sim is a |
| 20 |  | functional model. It doesn't have a good |
| 21 |  | understanding of the clocks. |
| 22 | Q | Okay. Let's go off the record. |
| 23 |  | VIDEO OPERATOR: The time is 12:27 p.m. |
| 24 |  | This concludes tape two. Off the record. |
| 25 |  | (Lunch recess taken.) |

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| 1 |  | VIDEO OPERATOR: The time is 1:11 p.m. This |
| 2 |  | is the beginning of tape three. We are back on |
| 3 |  | the record. |
| 4 | A | Before you ask a question, do you want me to go on |
| 5 |  | the record? I went downstairs and did find the |
| 6 |  | name of the person that I talked to over the phone |
| 7 |  | for the IKOS, and his name is Ron White, and both |
| 8 |  | he and Colin Stuart are SMTS's. You asked me for |
| 9 |  | their titles so I went and looked it up. |
| 10 | Q | What's SMTS? |
| 11 | A | SMTS is senior member of technical staff. |
| 12 | Q | Do they work for AMD or ATI? |
| 13 | A | They now work for AMD and they are employed by the |
| 14 |  | Toronto office, so they must have -- their work |
| 15 |  | employment is probably through ATI Technologies |
| 16 |  | ULC as well. |
| 17 | Q | And you mentioned Mr. Christie as well earlier? |
| 18 | A | David Christie, yeah. |
| 19 |  | That was the other conversation I had. |
| 20 | Q | And those are the only three people you've talked |
| 21 |  | to, to prepare for today, is that correct? |
| 22 | A | Along with Pam Horn, but yes, this is my |
| 23 |  | recollection, correct. |
| 24 | Q | Earlier there were some people you couldn't |
| 25 |  | remember their names. I just want to make sure |

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|  |  | we're done with the sort of list of people you |
| 2 |  | can't remember. So are those the three people |
| 3 |  | that you spoke with, other than counsel and Pam |
| 4 |  | Horn, to prepare for your deposition today? |
| 5 | A | As best as I can remember, this is correct. |
| 6 | Q | Okay. And during the break, your counsel located |
| 7 |  | some errata sheets I presume from you, is that |
| 8 |  | correct, with regard to your prior depositions? |
| 9 | A | Yes, I did provide two errata sheets for my |
| 10 |  | previous two depositions. |
| 11 | Q | And so I believe they were just Bates stamped and |
| 12 |  | produced right now, so to put them into the |
| 13 |  | record, we will mark them as Exhibit 7 and |
| 14 |  | Exhibit 8. |
| 15 |  | (Documents marked Exhibit 7 and Exhibit 8 |
| 16 |  | for identification.) |
| 17 |  | MR. ELENGOLD: For purposes of the record, |
| 18 |  | Exhibit 7 is Bates stamped AMD1044_0252730 through |
| 19 |  | 733, and Exhibit No. 8 is Bates stamped |
| 20 |  | AMD1044_0252728 through 729. |
| 21 | Q | Starting with Exhibit 7, Mr. Lefebvre, have you |
| 22 |  | seen this before? |
| 23 | A | Yes. |
| 24 | Q | What is Exhibit 7? |
| 25 | A | As best I can tell, this is the errata list that I |

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|  |  | provided after my first deposition on November 13, |
| 2 |  | 2015. |
| 3 | Q | And did you just provide this to your counsel |
| 4 |  | during the lunch break? |
| 5 | A | I signed and provided that errata to the counsel |
| 6 |  | that did the -- that helped me with this |
| 7 |  | testimony, but counsel came with -- I don't know |
| 8 |  | who gave them to him. |
| 9 | Q | So putting aside that you gave this to your |
| 10 |  | counsel in that case back in 2015, did you just |
| 11 |  | provide it to your counsel in this case during the |
| 12 |  | lunch break? |
| 13 | A | No. I did not. |
| 14 | Q | Okay. Other than this errata sheet for your |
| 15 |  | deposition, which I believe, and let me make sure |
| 16 |  | I get it clear for the record, is Exhibit 4, other |
| 17 |  | than this errata sheet, are there any other |
| 18 |  | corrections or changes you would want to make to |
| 19 |  | Exhibit 4 to make it complete and accurate |
| 20 |  | testimony? |
| 21 | A | Not that I'm aware of. |
| 22 | Q | Okay. And what is Exhibit -- sorry, strike that. |
| 23 |  | Mr. Lefebvre, have you seen Exhibit 8 before? |
| 24 | A | Yes. |
| 25 | Q | What is Exhibit 8? |

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A Best $I$ can tell, this is the errata sheet for the deposition that I did on December 9, 2016.

Q And did you just provide this errata sheet to your counsel that's sitting here today during the lunch break?

A No, I did not.
Q Other than the errata sheet in Exhibit 8, are there any other changes, corrections or additions to your testimony in Exhibit 5 that you would want to make in order to make it a complete, true and accurate set of testimony?

A Not that I'm aware of.
Q Okay. And before the break for lunch, we were talking about the first triangle test. Do you recall that?

A Yes. Let me bring back the relevant document to make sure.

Okay. I brought back Exhibit 6 and I'm now at page 30 .

Q Is the first triangle test an industry standard test for graphics processing?

MR. RENAUD: Objection.
A I can't speak about the industry. I mean I've only been employed through AMD, but I can tell you that this is a very standard process at AMD, and

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|  |  | even to this day we still do it. That is still |
| 2 |  | the test we use. I mean, obviously, we changed it |
| 3 |  | slightly to adapt to the newer chips which need |
| 4 |  | more pixel, but still the same concept. |
| 5 | Q | What's involved in the first triangle test from an |
| 6 |  | actual emulation perspective? |
| 7 | A | Can you refine what you mean by emulation? |
| 8 | Q | Sure. |
| 9 | A | You talking about the C sim or the RTL? |
| 10 | Q | Which is the first triangle test performed on, the |
| 11 |  | C sim or the RTL? |
| 12 | A | Okay. So in R400 and other chips that I worked |
| 13 |  | on, this test is first performed on the C sim to |
| 14 |  | bring up the reference model to a level to which |
| 15 |  | it is able to support the RTL development, and |
| 16 |  | then we run the test on both the RTL and VCS and |
| 17 |  | the C sim, compare the output image to make sure |
| 18 |  | they match. |
| 19 | Q | Is the first triangle test also run on the IKOS |
| 20 |  | machine? |
| 21 | A | Nothing precludes it from being run. I don't know |
| 22 |  | if it was run, but certainly, if it can work on |
| 23 |  | the RTL, it should also work on the IKOS machine. |
| 24 | Q | But it's not part of the standard. I believe you |
| 25 |  | suggested it was sort of the standard procedure |

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|  |  | every time a change is made with regard to the |
| 2 |  | RTL; is that true, to then run the first triangle |
| 3 |  | test again? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | So it is standard procedures for the developers |
| 6 |  | and the architects to run this test prior to |
| 7 |  | making any changes to the RTL; however, the thing |
| 8 |  | that is being applied to the IKOS prototype is a |
| 9 |  | netlist, and that doesn't get refreshed on every |
| 10 |  | change list. It only gets refreshed at fixed |
| 11 |  | periods. |
| 12 | Q | How many netlists were there for the R 400? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | At least three, given that we have a netlist |
| 15 |  | number three. There is evidence that there were |
| 16 |  | more, but I can't tell you conclusively how many |
| 17 |  | iterations that project went through so -- |
| 18 | Q | Approximately how many? Earlier you mentioned |
| 19 |  | there were a bunch that didn't have correct |
| 20 |  | naming, and some that did have correct naming? |
| 21 |  | Are we talking dozens, hundreds? |
| 22 |  | MR. RENAUD: Objection. |
| 23 | A | I've seen evidence of up to, you know, maybe eight |
| 24 |  | or nine but without deeper search, I can't give |
| 25 |  | you a better answer than that. |

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| :---: | :---: | :---: |
| 1 |  | reporter to please mark Exhibit 9. |
| 2 |  | (Document marked Exhibit 9 for |
| 3 |  | identification.) |
| 4 |  | MR. ELENGOLD: For the record, Exhibit 9 is |
| 5 |  | Bates labeled AMD1044_0175191 through 196. |
| 6 | Q | Mr. Lefebvre, have you seen Exhibit 9 before? |
| 7 | A | Yes, I have. |
| 8 | Q | What is Exhibit 9? |
| 9 | A | This is a presentation by Peter Pellerite that |
| 10 |  | occurred on August 30, 2002, and I am reading from |
| 11 |  | the presentation to say that, that is called the |
| 12 |  | R400 August Program Review, which also |
| 13 |  | incidentally happened to be an Exhibit for my |
| 14 |  | previous depositions. |
| 15 | Q | Is this the program review you were just referring |
| 16 |  | to? |
| 17 | A | This is one of such presentations, yes. |
| 18 | Q | Do you know if there's others that exist? |
| 19 | A | Yes, there are others that exist. |
| 20 | Q | What other program review summaries are you aware |
| 21 |  | of for the R400? |
| 22 | A | I don't recall the specifics but I know, I mean at |
| 23 |  | least in the preparation there were several other |
| 24 |  | program reviews, and these program reviews are |
| 25 |  | typically held at regular time intervals. This |

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|  |  | one is August. I'm expecting there's going to be |
| 2 |  | others earlier, later. |
| 3 | Q | Do you recall any that you've looked at that -- in |
| 4 |  | preparing for today's deposition, other than the |
| 5 |  | August? |
| 6 | A | I recall reviewing other presentations, yes, where |
| 7 |  | probably would have been a later one because the |
| 8 |  | actual column on page Bates number AMD1044_0175196 |
| 9 |  | had a more complete actual description. |
| 10 | Q | Is the IKOS emulation start what you were |
| 11 |  | referring to with regard to the FPGA and IKOS |
| 12 |  | machine? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | The IKOS simulation start is, yes, the process by |
| 15 |  | which we are starting prototyping, if you will, |
| 16 |  | the netlist on the IKOS machine. |
| 17 | Q | And when, to your knowledge, do you know when that |
| 18 |  | occurred, that prototyping or emulation occurred? |
| 19 | A | Like I said before, there's a very similar program |
| 20 |  | review presentation that has a lot more actual |
| 21 |  | dates, and that would state the record properly. |
| 22 |  | I think, if my memory serves, that it occurred |
| 23 |  | slightly after the plan date, but you know, we can |
| 24 |  | find for sure because that information is readily |
| 25 |  | available. |

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| 1 | $Q$ | But you don't know yourself? |
| 2 |  | MR. RENAUD: Objection. |
| 3 | Q | You're just saying you have to look at a document |
| 4 |  | to tell you, is that correct? |
| 5 | A | I said I don't remember. Correct. |
| 6 | Q | What does "begin early block delivery" mean? |
| 7 | A | Begin early block delivery? |
| 8 | Q | It's right under "IKOS emulation start." |
| 9 | A | Yeah. I believe this has to deal with initial |
| 10 |  | efforts to deliver blocks to physical design, so |
| 11 |  | through the PD team, so they can start as early as |
| 12 |  | possible the floor plan effort, so that when they |
| 13 |  | get the later blocks, they can focus their effort |
| 14 |  | on those. |
| 15 | Q | Then what is an IKOS emulation with software? |
| 16 | A | This is exactly the topic that we broached on a |
| 17 |  | little bit earlier where I said the hardware |
| 18 |  | emulator would be running with the software |
| 19 |  | infrastructure. This is what this line refers to. |
| 20 | Q | The RTL freeze/Final Netlist, what does that step |
| 21 |  | represent? |
| 22 | A | In the R 400 , as with many other silicon devices, |
| 23 |  | at some point you have to freeze the design in |
| 24 |  | order to submit the GDS or the netlist to the |
| 25 |  | manufacturing process. So this date is the date |

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|  |  | by which we were intending to freeze the design |
| 2 |  | completely for fabrication. |
| 3 | Q | What is "base layers tapeout"? |
| 4 | A | Silicon chip contains several layers. The first |
| 5 |  | layer is the silicon layer in which the gates are |
| 6 |  | etched in, and then it follows by several metal |
| 7 |  | layers, which are the wires that connect the gates |
| 8 |  | together. |
| 9 |  | So that base layer tapeout is taping out |
| 10 |  | that baseline, the first layer of where the gates |
| 11 |  | are etched, and then the metal layers are the |
| 12 |  | subsequent layers that you lie on top of that base |
| 13 |  | layer to establish the connections. |
| 14 | Q | What is the "First Samples for Engineering" step? |
| 15 | A | This, again, in the R400 concept is when we expect |
| 16 |  | to get the first chips back from the manufacturer. |
| 17 | Q | How many samples are usually returned for |
| 18 |  | engineering purposes? |
| 19 |  | MR. RENAUD: Objection. |
| 20 | A | I don't recall the number specifically for the |
| 21 |  | R400, but you know, for product like we would do |
| 22 |  | today, we just do a few wafers, which would be, I |
| 23 |  | don't know, around a thousand chips or so. I |
| 24 |  | mean, that vicinity. We're not talking millions |
| 25 |  | of parts. It's really a small number of parts. |

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| 1 | Q | Then what occurs between the first Samples of |
| :---: | :---: | :---: |
| 2 |  | Engineering and the A12 Tapeout? |
| 3 | A | So the samples are going to go to the software |
| 4 |  | team for what the process we call bring-up, which |
| 5 |  | is, you know, starting to run applications on the |
| 6 |  | chip. Sometimes you have issues and, you know, |
| 7 |  | small problems that you have to reconnect the |
| 8 |  | gates differently. This is what we call an ECO or |
| 9 |  | an A12. It's just a -- so A12 means it's -- a |
| 10 |  | metal mask is just released. So you don't change |
| 11 |  | the base layer, just one of the metal layers, |
| 12 |  | which is a much faster turnaround time to fix any |
| 13 |  | possible issues that one might have encountered in |
| 14 |  | one application. |
| 15 | Q | And then is that same sort of thing done with the |
| 16 |  | A12 samples for engineering, are they then also |
| 17 |  | tested for minor or other problems? |
| 18 | A | So in this R400 concept, the A12 Samples for |
| 19 |  | Engineering is really -- so we were -- this |
| 20 |  | program was planning for one -- was expecting or |
| 21 |  | planning for one metal layer in the schedule, and |
| 22 |  | so this is just testing again to make sure the |
| 23 |  | chip works before the production is, you know, |
| 24 |  | enlarged to millions and millions of parts, at |
| 25 |  | which point you can't fix anything anymore. |

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|  |  | was very transparent. It's really the same kind |
| 2 |  | of product. So I don't exactly recall when I |
| 3 |  | stopped working on one and started working on the |
| 4 |  | other because they're one, one and the same kind |
| 5 |  | of blur in my memory. |
| 6 | Q | Is it approximately fall 2002, based on these |
| 7 |  | dates? |
| 8 | A | These dates are stating, like, the back end |
| 9 |  | blocks, the back end efforts, or the PD efforts |
| 10 |  | which I'm not really involved in. I can't tell |
| 11 |  | from this when the front end designers and |
| 12 |  | architect would have transitioned from one program |
| 13 |  | to the other. I mean -- |
| 14 | Q | So it could have been before August 2002, is that |
| 15 |  | right? |
| 16 | A | Could have been before August -- so August 2002, |
| 17 |  | that was the first synthesis date, is that the |
| 18 |  | point you're referring to or? |
| 19 | Q | Well, that's when this is from, right? |
| 20 |  | The program schedule is dated August 2002, I |
| 21 |  | believe -- |
| 22 | A | So -- |
| 23 | Q | -- according to your testimony? |
| 24 | A | So at the time of this presentation, because |
| 25 |  | people were still, you know, inactive, this is the |

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|  |  | first synthesis, so it's still undergoing active |
| 2 |  | RTL development. So I have every belief that at |
| 3 |  | that time, I probably would still have been |
| 4 |  | involved in the R400 program itself. Maybe the |
| 5 |  | Xenos program also started, but there would still |
| 6 |  | be work on the R400 at that time. |
| 7 | Q | Was there overlap between the R400 program and the |
| 8 |  | Xenos program? |
| 9 | A | To the best of my memory, yes, there was, and so |
| 10 |  | that's why it contributed to making it even more |
| 11 |  | of a blur. |
| 12 | Q | What kind of overlap? |
| 13 | A | So at AMD, we use Perforce server and |
| 14 |  | depositories, so the depositories are directories, |
| 15 |  | and you can integrate files from one depot to the |
| 16 |  | other. Typically, a depository has the name of a |
| 17 |  | given project, and so you can start working on the |
| 18 |  | Xenos program and then start back integrating |
| 19 |  | changes as you see fit to the R400 and back and |
| 20 |  | forth. It's like, it kind to working with two |
| 21 |  | different directories. |
| 22 | Q | Are you talking about changes to specifications, |
| 23 |  | or changes to C code, or changes to RTL, or all of |
| 24 |  | the above? |
| 25 | A | Any kind of changes can be back integrated, but |

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Page 135 of 312 programs versus the GPUs so that people know what they are working on. Typically, the -- our names, at the time, we reserved for our GPU line of products, our PC products, whereas, whenever you had a -- an SCBU program, or a dedicated piece of silicon for, dedicated for a specific customer, it would have a program name to obfuscate also who the customer might have been.

Q Xenos was specifically being designed for Microsoft, is that right?

MR. RENAUD: Objection.
A The Xenos chip was specifically designed for Microsoft, but the RTL, at least during the overlap, was -- at least a portion of the RTL for the graphics core existed on both the R400 and Xenos program, as was very similar if not the same in some respect.

MR. RENAUD: Just so the record is clear, the Xenos subject matter, you're testifying in your personal capacity.

MR. ELENGOLD: Okay.
So this witness is only testifying on the R400 on behalf of AMD and ATI.

MR. RENAUD: No, he's testifying consistent
with the subjects, but $I$ don't believe the Xenos

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| 1 |  | is within to the scope of the subject matters. Do |
| 2 |  | you have a different point of view on that? |
| 3 |  | MR. ELENGOLD: I don't know. That's why I'm |
| 4 |  | trying to clarify your objection -- |
| 5 |  | (Court reporter interruption of overlapping colloquy) |
| 6 |  | MR. ELENGOLD: -- trying to understand where |
| 7 |  | you're trying to draw the line with your objection |
| 8 |  | so I make sure it's clear for the record. |
| 9 |  | MR. RENAUD: My memory is, the Xenos is |
| 10 |  | outside the scope, but I would be happy to go back |
| 11 |  | and take a second look at it during a break. |
| 12 |  | MR. ELENGOLD: It's up to you. |
| 13 | Q | For now, we're going to treat this testimony as |
| 14 |  | personal testimony, just for yourself, as far as |
| 15 |  | your recollection regarding Xenos. |
| 16 |  | So I think the last question -- I'm sorry, I |
| 17 |  | think we got a little derailed there, was just |
| 18 |  | regarding whether or not this was specifically |
| 19 |  | designed for Microsoft, and I believe you said the |
| 20 |  | chip was specifically designed for Microsoft, is |
| 21 |  | that correct? |
| 22 | A | So if I remember correctly my statement, I said |
| 23 |  | that the Xenos chip itself was a product |
| 24 |  | specifically designed for Microsoft, but then a |
| 25 |  | lot of the graphics blocks and infrastructures, at |

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| 1 |  | overlap. |
| 2 | Q | And at some point, everyone stopped working on the |
| 3 |  | R400 program and either were working on Xenos or |
| 4 |  | other projects at ATI, is that correct? |
| 5 | A | So at some point, yeah, the R400 program got |
| 6 |  | cancelled, and so everyone who was working on R400 |
| 7 |  | at the time transitioned to Xenos and possibly |
| 8 |  | some other program. I mean -- but -- |
| 9 | Q | Did everybody transition to Xenos, is that |
| 10 |  | correct? |
| 11 | A | Are you asking me -- |
| 12 |  | MR. RENAUD: Objection. |
| 13 | A | -- everyone at AMD transitioned? |
| 14 | Q | Well, I think you just said, at some point |
| 15 |  | everyone stopped working on the R400 program and |
| 16 |  | were either working on Xenos and possibly other |
| 17 |  | projects at ATI. I just wanted to make sure I |
| 18 |  | understood your testimony for both of us to make |
| 19 |  | sure it's accurate. |
| 20 |  | So was everyone that was working on R400 |
| 21 |  | project when it was cancelled, transitioned to the |
| 22 |  | Xenos program? |
| 23 | A | Yeah, when I meant everyone, I didn't mean |
| 24 |  | everyone at ATI because there were another team |
| 25 |  | working on the R300. That team never worked on |

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| 1 |  | the R400 or the Xenos program. |
| 2 |  | But once we transitioned to the Xenos |
| 3 |  | program, and the project got, the R 400 project got |
| 4 |  | cancelled, I can't say for sure if everyone that |
| 5 |  | was working on the R400 transitioned to the Xenos |
| 6 |  | program, but my recollection is that at least most |
| 7 |  | of the people transitioned over. |
| 8 | Q | Was there an R500 program? |
| 9 | A | Again, to the best of my recollection, the R500 |
| 10 |  | program was a derivative from the R300, so the |
| 11 |  | team that was working on the R 500 was actually the |
| 12 |  | R300 team. |
| 13 | Q | What was the next computer chip -- sorry, strike |
| 14 |  | that. What was the next general purpose computer |
| 15 |  | chip program to follow the R 400? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | So to the best of my knowledge, that would have |
| 18 |  | been the R600, also known as Pele. |
| 19 | Q | P E L E? |
| 20 | A | Like the football person, yes. P E L E, yes. |
| 21 |  | I think it has an accent, but let's not get |
| 22 |  | picky. |
| 23 | Q | Approximately, when did the R600 program start? |
| 24 | A | I really don't recall. I mean after the R500 and |
| 25 |  | then the Xenos program, and there could also be, |

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memory is only five gigabytes because of the bus
width and so forth, you need a cache to amplify
that so that in most cases, the clients that need
10 gigabytes of bandwidth can operate inside the
chip without having to always use the small narrow
bus going to system memory or $D$ rams onboard.
Q Are there any other differences between the R400
and the xenos chip that you recall?
A Without going into specifics that $I$ can't divulge
because of customer relationships, I mean
proprietary information from Microsoft, the only
other difference that $I$ can remember is that Xenos
had a slightly different configuration than the
R400 program.
Q So we're under a protective order in this case
which keeps things confidential, so I believe you
can speak freely to the extent that you want to
testify to this issue on behalf of AMD or ATI.
MR. RENAUD: We may need to take a break on
that. Let me just see if $I$ can solve it quickly,
counsel.
Is this something, Laurent, that you think
you need specific permission from Microsoft to
disclose that we don't have?
A So this subject matter came up in one of my
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| 1 |  | previous testimonies and we had this issue where 145 |
| :---: | :---: | :---: |
| 2 |  | would -- I was not able to divulge Microsoft |
| 3 |  | proprietary information, and so we can read the |
| 4 |  | transcript. I mean, I sent most of the |
| 5 |  | information in that. I mean, it's really just a |
| 6 |  | configuration difference between the two chips, |
| 7 |  | and last time I could not tell you what the Xenos |
| 8 |  | configuration was because of these protective, or |
| 9 |  | I don't know how you call them in English. I |
| 10 |  | can't tell you how many pixels the Xenos can |
| 11 |  | process per clock, but I can tell you, it is a |
| 12 |  | different number than on the R400, but my |
| 13 |  | understanding is everything else is the same. |
| 14 | Q | How much additional work was done on the Xenos |
| 15 |  | chip from when the integration started from the |
| 16 |  | R400 into the Xenos chip becoming commercialized? |
| 17 | A | How much work? |
| 18 | Q | Let me rephrase that. How much time did it take |
| 19 |  | to make the Xenos chip into a customer-ready chip? |
| 20 |  | MR. RENAUD: Objection. |
| 21 | Q | From when the R 400 program was ported over. |
| 22 | A | Is your question pertaining to the Xenos chip as a |
| 23 |  | whole or on the shader section? |
| 24 | Q | Let's start with the Xenos chip as a whole. |
| 25 | A | So on the Xenos chip as a whole, like I said, most |

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of the work had to deal with the render back ends
which were brand new pieces of hardware. I don't
recall exactly how long they took, but that was
the bulk of the effort. Everything else kind of
followed right through.
Q Were any changes required to the other hardware
blocks?
MR. RENAUD: Objection.
A Because the configuration was different, we had to
tweak a few parameters, but $I$ don't recall the
extent of any of the changes, but you know, I can
tell you that the two chips are very similar, and
the only main difference that $I$ can remember,
again, is the render back ends and then the
configuration to change a number of pixels.
Q So you're not sure of any other differences that
might exist? That's not something you prepared
for, for today's deposition?
MR. RENAUD: Objection.
A I did not prepare, you know, or review the Xenos
program extensively. So no, I'm not -- I don't
remember any other changes.
Q Did you review any Xenos documents in preparing
for today's deposition?
MR. RENAUD: Objection. Let me make one

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clarification just because $I$ refreshed my memory. Xenos is outside the scope for any domestic industry stuff, but to the extent it's within the reduction of practice, it would be within the scope, so.

MR. ELENGOLD: I don't think it is. Well, I don't know, you said it's not, so I don't want to put words in your mouth.

MR. RENAUD: But I just looked at a record here that says the scope objection was to the extent it was related to domestic industry since we're not relying on it, but that to the extent it was related to reduction of practice, it is. So whether that makes sense to you or not, I just wanted to make sure $I$ wasn't leaving you ambiguous.

So the questions about the Xenos, to the extent they reflect the reduction of the practice, he will be the designee, but he's not going to be a designee as to domestic industry use.

MR. ELENGOLD: Okay. So all of our questions then with respect to Xenos, and then we might have to go back, I apologize, now to revisit those if you are being designated, questions with respect to Xenos to the extent it's relevant to

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|  |  | production or not reduction to practice -- |
| 2 |  | MR. RENAUD: He will be the designee. |
| 3 |  | MR. ELENGOLD: -- you're saying he is |
| 4 |  | designated, right? |
| 5 |  | MR. RENAUD: And apologies for the |
| 6 |  | ambiguity. |
| 7 |  | Sorry. Do you want to read the question |
| 8 |  | back? |
| 9 |  | MR. ELENGOLD: No, I can ask the question. |
| 10 |  | Thank you. |
| 11 | Q | Did you review any Xenos documents in preparing |
| 12 |  | for your deposition today? |
| 13 | A | I recall there was this source code computer that |
| 14 |  | counsel had, and there were some files of Xenos on |
| 15 |  | there. I browsed through them. That's the extent |
| 16 |  | of it. |
| 17 | Q | Do you know when the Xenos program passed the |
| 18 |  | first triangle test for the first time? |
| 19 | A | I don't recall that information. I mean we can - |
| 20 |  | if you have Xenos specific documents with you, we |
| 21 |  | can review them, but unfortunately, I don't know. |
| 22 | Q | Do you know if it passed it? |
| 23 |  | MR. RENAUD: Objection. |
| 24 | A | So the Xenos was made into a commercial program, |
| 25 |  | and so it's in millions of consoles, or was at |

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|  |  | least, so yes, I have a very good feeling that it |
| 2 |  | passed it. |
| 3 | Q | Do you know when the Xenos chip went into IKOS |
| 4 |  | emulation? |
| 5 | A | No, I do not know. |
| 6 | Q | Do you know if it did? |
| 7 | A | No, I don't. |
| 8 | Q | Do you know when the tapeout was for the IKOS |
| 9 |  | chip? |
| 10 | A | There is no tapeout. |
| 11 | Q | Sorry, strike that. I apologize. I said it |
| 12 |  | wrong. Do you know when the tapeout was for the |
| 13 |  | Xenos chip? |
| 14 | A | Okay. Again, having not reviewed anything, I can |
| 15 |  | talk from memory. I recall it vaguely being |
| 16 |  | around 2004, but this is very vague. |
| 17 | Q | Do you know when the first products were delivered |
| 18 |  | to customers for the Xenos chip? |
| 19 | A | No, I don't recall any specific dates, no. |
| 20 | Q | So turning back to the first triangle test that we |
| 21 |  | were discussing earlier, which you're free to |
| 22 |  | reference either the presentation in Exhibit 9 or |
| 23 |  | your declaration, which I believe is Exhibit 6, |
| 24 |  | how was the first triangle test performed? |
| 25 | A | On the R400, you mean how this test is being run? |

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1 Q I assume it's the same for all of the programs
since you said it's sort of part of standard for
ATI.
A Okay. Yes. So the base process by which we run
functional test on hardware at AMD, and at the
time on the R400, was that we create, like, a low
level API which allows us to write small C
programs that describe the test and what it's
supposed to do, and by such, energize the hardware
in a similar manner of which it would have been
stimulated by the driver.
I know, you know, again, upon my review to
prepare for this deposition, that in the source
computer, there is the source code for such a
test, which we can walk through so you can get
appreciation of exactly what is being driven to
the hardware, but effectively, it is a small C
program that describes what you want the test to
do.
Q Is it a static image of the triangle? Is it a
single picture?
A In this particular case, it is a single picture of
a triangle, yes. The test is render, triangle,
and terminate. Finish.
Q I believe in your declaration, you said it's a
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| 1 |  | Gouraud shaded triangle, is that correct? |
| 2 |  | MR. RENAUD: Objection. |
| 3 | A | It is a Gouraud shaded triangle, yes. |
| 4 | Q | I thought maybe counsel was objecting to my |
| 5 |  | pronunciation on that one. |
| 6 |  | What is Gouraud shading? |
| 7 | A | So a Gouraud shaded triangle is a triangle that |
| 8 |  | has three different colors for each of the |
| 9 |  | vertices of the triangle. So in this case, if you |
| 10 |  | had a color picture for this triangle, one of the |
| 11 |  | vertex, which is one of the extremities of the |
| 12 |  | triangle, would be blue, the other one would be |
| 13 |  | red, and the third one would be green, and then |
| 14 |  | the inside of the triangle varies slowly from one |
| 15 |  | color to the next, and it is to ensure that the |
| 16 |  | interpolation structure that determines the color |
| 17 |  | for each of the pixels within the triangle is |
| 18 |  | working effectively. |
| 19 | Q | Is it just one set of vertices that are used for |
| 20 |  | the test? |
| 21 | A | For this test because it was one triangle, it is, |
| 22 |  | yes. It's three vertices and one primitive, which |
| 23 |  | we call the triangle. |
| 24 | Q | And how many pixels are used? |
| 25 | A | If your picture was better, we could count them, |

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but the pixels in this case are the big squares that you see here. It's not a very big triangle.

Q The picture is a little better here. This is how it gets produced to us, so I apologize.

A It is hard to see, especially at the top, but you can see these big squares are the pixels, so I mean, there are one, two, three, four, five, six, seven, eight, nine, 10, 11; 11 by 11 divided by two.

Q So to draw the triangle in the triangle test, you would make sure all the vertices shaded correctly, and then you would rosterize the pixels and make sure the pixels are shaded correctly, is that correct?

MR. RENAUD: Objection.
A So the way the API works is that the test sends the three vertices and the connectivity information, say, by this vertex connected to this one and to this one to form the triangle. The hardware does the rest.

So the hardware makes sure that the vertices are first passed through the shader, operates the right positions, as well as the attributes, which are the color in this case, and then subsequently runs the pixel shader on those attributes.

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A In fact, I was hoping to get Version 2.0, which
    had the control flow structures, to answer any of
    your questions about the control flow, but this is
    one version of the sequencer, yes.
Q I think I have that one too and I'll bring that
    out next, but I wanted to ask you a couple
    questions about this first.
    So do you remember approximately the date of
    when this document was completed in the current
    form that it is in Exhibit 10?
    MR. RENAUD: Objection.
    A So the date, I have no reason to believe that it
        would be wrong. This document, by myself, if you
        look at the revision changes on page 3 of 20, or
        Bates number AMD1044_0175218, it's dated by
        myself, or what appears to be me, on August 24,
        2001.
    Q Do you recall making that entry in this document?
    A I don't recall directly having made that entry,
        but I have no reason to believe that it's
    incorrect. I mean --
    Q Do you know why the Edit Date on the document says
        September 4, 2015?
    A I don't know why, but I can tell you that these
        fields up there are usually automatic fields, and
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Q You don't know how those dates got there, is that right?

MR. RENAUD: Objection.
A Well, I told you that $I$ know that these dates here on page 3 of 20 are typed in. So these are typed in by the author, which just happens to be me. So I'm confident in these. How these on the first page got changed or not, yeah, I don't remember exactly what form we used at the time.

Q Did you create Exhibit 10?
MR. RENAUD: Objection.
A By "create," you mean did I write this specification?

Q Did you write Exhibit 10?
A I am the author, at least according to this document, of this specification, and this is also my recollection, yes.

Q Did anyone make edits to Exhibit 10 other than you, to your knowledge, other than the date field we're talking about?

MR. RENAUD: Objection.
A According to this log, which is on, again, page 3 of this Exhibit, I'm the sole contributor to this specification.

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1 Q So the management of the dates and the revision changes is left to the authors and may not be a hundred percent accurate, but the Perforce logs you believe are always maintained to be accurate, is that correct?

MR. RENAUD: Objection.
A That is my understanding, yes.
Q Do you know approximately the date of Exhibit 10?
A Well, like stated before, this is dated on the page 3 by myself as of August 24, 2001. No reason to believe it not to be accurate.

Q Is that because you, every time you made a change to a document, put a note in the Revision Change log?

MR. RENAUD: Objection.
A It is because $I$ personally, whenever $I$ change a revision number on the first page, try to put a revision change list in the Revision Changes. So I know I have not been a hundred percent accurate, and I could have made changes to this document without changing the rev number, but if $I$ change the rev number, again, it's my recollection and my work practice, I would make an entry in the Revision Change.

Q So this could have some changes that occurred

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|  |  | after August 24, 2001 in this document, but any of |
| 2 |  | those changes would have occurred prior to you |
| 3 |  | creating Version .5, is that correct? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | That is a possibility, yes, and if we go to the |
| 6 |  | Perforce log, we can say conclusively whether it |
| 7 |  | is the case here or not. |
| 8 | Q | Why did you create this document that's Exhibit |
| 9 |  | 10? |
| 10 | A | This document is the architecture document that is |
| 11 |  | meant to describe the way the sequencer is |
| 12 |  | supposed to operate in the R 400 unified pixel and |
| 13 |  | vertex shader. |
| 14 | Q | Whose idea was it to put a sequencer in the R 400 |
| 15 |  | shader? |
| 16 | A | Everyone, at least of the architecture team, knew |
| 17 |  | that a sequencer was needed because you need, |
| 18 |  | maybe not the name sequencer, but you need a |
| 19 |  | module that controls the operation of the shader, |
| 20 |  | and so, you know, I can't tell you -- I don't know |
| 21 |  | that anyone had an idea to put a sequencer in the |
| 22 |  | R400. The idea is how to make it work in that |
| 23 |  | context. |
| 24 | Q | Was the R400 the first ATI program to use a |
| 25 |  | sequencer in a shader? |

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|  |  | Page 160 |
| :---: | :---: | :---: |
| 1 |  | MR. RENAUD: Objection. |
| 2 | A | To my knowledge, the R300 had a pixel shader |
| 3 |  | sequencer, meaning the sequencer was only |
| 4 |  | operative on the pixel shader side of things, and |
| 5 |  | this is, to my knowledge, the first time ATI |
| 6 |  | created a sequencer that able to operate on either |
| 7 |  | or both pixels or vertices. |
| 8 | Q | Do you know when the R300 sequencer was created? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | So your question is when it was created? |
| 11 | Q | Do you know when? |
| 12 | A | No, I don't know the date, I mean, and I recalled |
| 13 |  | it being named into the overview, and so I just |
| 14 |  | went to read back through it to see if there was |
| 15 |  | any date, but there's no date. It just states |
| 16 |  | that the sequencer is based on the R300 design, |
| 17 |  | where we used it as a baseline and then modified |
| 18 |  | it in order to operate in a unified vertex and |
| 19 |  | pixel shader environment. |
| 20 | Q | Is that a true statement, that the R400 sequencer |
| 21 |  | is based on the R300 sequencer? |
| 22 |  | MR. RENAUD: Objection. |
| 23 | A | This is what page 4 of 20 of this specification is |
| 24 |  | stating. I mean, it is to the best of my |
| 25 |  | knowledge, we use some concepts of the R300. We |

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|  |  | use the clause concepts. But the R 400 sequencer |
| 2 |  | is still significantly different than the R300 |
| 3 |  | sequencer. It has to deal with the two types of |
| 4 |  | elements, which the R300 did not have to deal |
| 5 |  | with, and I also know we upgraded it to have more |
| 6 |  | clauses or more flexibility. |
| 7 | Q | What are clauses? |
| 8 | A | If you refer to the figure which is not named on |
| 9 |  | page 5, or Bates number AMD1044_0175220, you have |
| 10 |  | a Top Level Diagram of the Version 0.4 sequencer. |
| 11 |  | The clauses are effectively the trips between the |
| 12 |  | various reservation stations. So the more clause |
| 13 |  | you have, the more opportunities you have to do |
| 14 |  | what we call dependent fetches, which is go to |
| 15 |  | memory, fetch an element, do some ALU map on them, |
| 16 |  | and then do another fetch based on that, so forth. |
| 17 | Q | Can each clause support one instruction? |
| 18 |  | MR. RENAUD: Objection. |
| 19 | A | Each clause supports a number of instructions, but |
| 20 |  | they have to be all of the same type; so either |
| 21 |  | all textures or all ALU. Whenever you had to |
| 22 |  | transition from an ALU to a texture or fetch |
| 23 |  | operation, you had to go to a new clause. |
| 24 | Q | What is the purpose of supporting ALU clauses and |
| 25 |  | eight texture clauses? |

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1 A Like I just stated, it's to support what we call 2 dependent fetches. So let's say in the first 3 texture clause, you go to memory, you fetch a


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| :---: | :---: | :---: |
|  |  | sequencer without a constant store if you want it, |
| 2 |  | but it's a nice tool in your tool box. |
| 3 | Q | Could you have a sequencer without an instruction |
| 4 |  | store? |
| 5 |  | MR. RENAUD: Objection. |
| 6 | A | You can have a sequencer without an instruction |
| 7 |  | store, yes. |
| 8 | Q | How would that work? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | The way I would envision this to work is to have a |
| 11 |  | sequencer coupled to system memory and it fetching |
| 12 |  | the instructions as needed. |
| 13 | Q | So it would be slow but it would work? |
| 14 |  | MR. RENAUD: Objection. |
| 15 | A | It can be as fast as you want it to be because if |
| 16 |  | you imagine instead, you have an instruction |
| 17 |  | cache, then you can make it very fast and very |
| 18 |  | flexible. It's a more complex design than having |
| 19 |  | a buffer, an instruction store. |
| 20 | Q | You could do a cache instead of a store, would be |
| 21 |  | one way to do it? |
| 22 |  | MR. RENAUD: Objection. |
| 23 | A | So like I said before, you can do a cache, you can |
| 24 |  | do nothing at all and couple it to memory, you can |
| 25 |  | do a store. There are many ways one can do it. |

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| :---: | :---: | :---: |
| 1 | Q | Could you have a sequencer without the |
| 2 |  | vertex/pixel vector arbitrator block? |
| 3 |  | MR. RENAUD: Objection. |
| 4 | A | Can you be more precise in your question because |
| 5 |  | sequencer generically is very generic, so what is |
| 6 |  | the scope of your question? |
| 7 | Q | Sure, as far as I understand your R 400 sequencer, |
| 8 |  | the components included vertex/pixel vector |
| 9 |  | arbitrator, and instruction store, and a constant |
| 10 |  | store based on our discussion so far of this |
| 11 |  | specification. Is that right? |
| 12 | A | So the R400 sequencer included all of these |
| 13 |  | modules, yes. You don't have to have all of these |
| 14 |  | modules to have a unified shader. It's just an |
| 15 |  | implementation of, and it just happened to have |
| 16 |  | these blocks. |
| 17 | Q | Are any of these necessary to have a unified |
| 18 |  | shader? |
| 19 |  | MR. RENAUD: Objection. |
| 20 | A | One could envision having a unified shader with, |
| 21 |  | you know, for example, an instruction store |
| 22 |  | dedicated to vertices, and instruction store |
| 23 |  | dedicated to pixels, and then just shared |
| 24 |  | resources on the GPRs which are the SPs. You can |
| 25 |  | do any level of unification that you want. This |

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designs.
Q And to that point, what I'm trying to understand
is what is required in order to build a unified
shader of what you claim you invented?
MR. RENAUD: Objection.
A Unified shader means unification of some degree,
and so $I$ think at a minimum, to have a unified
shader, you would need to have unification of the
most expensive part of the shader, which is the
GPRs and the ALUs. The rest is not, not
necessary. You can build it with or without it,
but you would lose most of the benefits of the
unified shader if you did not have a unified ALU
coupled with GPRs.
Q What are GPRs?
A The GPRs are the general purpose registers. These
are the small embedded memories that serve as
source and destinations for $A L U$ operations or
fetches. They're the stored -- the data, the
intermediate data as you run your shader.
Q Why are they called general purpose registers?
A Because they can store any data you want. They're
generic memories that you can use as source or
destination and they store any information you
want to store.

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1 Q So unification of GPRs and ALUs, you believe, is
all that's required in order to have the unified
shader that you believe was invented and as part
of the R400 project, is that right?
MR. RENAUD: Objection.
A I believe that in order to get benefits great
enough to go to the burden of unifying everything
and, you know, have the area and savings, that is,
you know, the one piece you need to have.
Obviously, the more you add on top of that, the
more you can maximize your savings, but you know,
they're not strictly necessary.
MR. RENAUD: Good time for a break, counsel?
MR. ELENGOLD: Sure, let's take a break. Go
off the record.
VIDEO OPERATOR: The time is $2: 31 \mathrm{p} . \mathrm{m}$. This
is the end of tape 3. We are off the record.
(Off the record.)
VIDEO OPERATOR: The time is 12:51 p.m.
This is the beginning of tape four. We are back
on the record.
Q Mr. Lefebvre, before the break we were talking
about Exhibit 10. Do you recall that?
A Yes.
Q And I'd like to turn to page 175232 which at the

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| :---: | :---: | :---: |
|  |  | top says: 13. Examples of program executions. |
| 2 |  | What is this section of the document used for? |
| 3 | A | This section of the spec, as best I can tell, in |
| 4 |  | the R400 is meant to provide an example of an |
| 5 |  | execution of a vertex shader program so that the |
| 6 |  | designer can refer to it and understand with an |
| 7 |  | example the kind of steps expected to be run when |
| 8 |  | we are running an exemplary program on vertices. |
| 9 | Q | Okay. In step 2 -- you see step 2? What does |
| 10 |  | that say? |
| 11 | A | Step 2 reads as follows, "SEQ arbitrates between |
| 12 |  | the Pixel FIFO and the Vertex FIFO - basically the |
| 13 |  | Vertex FIFO always has a priority. At this point, |
| 14 |  | the vector is removed from the Vertex FIFO; the |
| 15 |  | arbiter is not going to select a vector to be |
| 16 |  | transformed if the parameter cache is full unless |
| 17 |  | the pipe has nothing else to do (i.e. no pixels |
| 18 |  | are in the pixel fifo)." |
| 19 | Q | And is that the operation of the pixel/vertex |
| 20 |  | arbiter block we were talking about earlier? |
| 21 |  | MR. RENAUD: Objection. |
| 22 | Q | That's on page 220. |
| 23 | A | You mean the R400 vertex/pixel arbiter -- |
| 24 |  | arbitrator? |
| 25 | Q | We can use the terms interchangeably, that's fine. |

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| 1 |  | always make sure that the parameter cache, which 175 |
| :---: | :---: | :---: |
| 2 |  | is the storage for the attributes of the vertex |
| 3 |  | shader, was always full or as full as possible, |
| 4 |  | enabling the pixel flow to be as continuous as |
| 5 |  | possible, and in that sense, have as good |
| 6 |  | performance as possible. |
| 7 | Q | Because vertices always have to get processed |
| 8 |  | before pixels? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | In the R400 program, yes, that was the case. The |
| 11 |  | vertices, since they are the input to the pixel |
| 12 |  | flow, they had to be processed before the pixels. |
| 13 | Q | When you say "in the R400 program," is that not |
| 14 |  | the case for graphics processing in general, that |
| 15 |  | you do your vertices before you do your pixels? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | Q | Sorry, strike that. Is it not the case in |
| 18 |  | graphics processing in general that you shade your |
| 19 |  | vertices before you shade your pixels? |
| 20 |  | MR. RENAUD: Objection. |
| 21 | A | It is my understanding that in all the AMD |
| 22 |  | products, that is the way we are doing it, and in |
| 23 |  | some other products that I'm aware of in the |
| 24 |  | literature, that is also the case, but I can't |
| 25 |  | talk to everything that I may or may not know. I |

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|  |  | mean, that is, in my opinion, a generic way of |
| 2 |  | doing things, but if someone finds a way to do it |
| 3 |  | otherwise. |
| 4 | Q | Do you know of a way to do it otherwise? |
| 5 |  | MR. RENAUD: Objection. |
| 6 | A | No. I basically cannot think of another way of |
| 7 |  | doing it. That's the way I would have done it, |
| 8 |  | vertices first. |
| 9 |  | MR. ELENGOLD: Going to ask the court |
| 10 |  | reporter to please mark Exhibit 11. |
| 11 |  | (Document marked Exhibit 11 for |
| 12 |  | identification.) |
| 13 | Q | Mr. Lefebvre, have you seen Exhibit 11 before? |
| 14 | A | I don't think I've seen this Exhibit, no. |
| 15 | Q | Do you know what Exhibit 11 is? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | It reads, and I quote: The Complainants Notice of |
| 18 |  | Patent Priority Dates, In the Matter of Certain |
| 19 |  | Graphics Systems, Component Thereof, and Consumer |
| 20 |  | Products Containing the Same. |
| 21 | Q | I'm going to ask you to turn to page 2 and look at |
| 22 |  | Section C. Can you read the title of section c of |
| 23 |  | this document? |
| 24 | A | U.S. Patent No. 8, 760,454. |
| 25 | Q | Mr. Lefebvre, are you familiar with that patent |

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| :---: | :---: | :---: |
| 1 |  | number? |
| 2 | A | I have seen this patent number in the past. I |
| 3 |  | believe this is one of the unified shader patents. |
| 4 | Q | Do you understand you've been designated to |
| 5 |  | testify today about the conception and reduction |
| 6 |  | to practice regarding the patent 8,760,454? |
| 7 |  | MR. RENAUD: Objection. |
| 8 | A | Yes. |
| 9 | Q | If I call that the '454 patent moving forward, |
| 10 |  | will you understand what I'm referring to? Is |
| 11 |  | that okay? |
| 12 | A | Yes. It would be even better if you had it so |
| 13 |  | that, you know, we would know what exactly you're |
| 14 |  | talking about. |
| 15 | Q | I do have it. Do you not know what I'm talking |
| 16 |  | about right now? |
| 17 |  | MR. RENAUD: Objection. |
| 18 | A | I know it's one of the unified shader patent, but |
| 19 |  | exactly what -- which one it was, I mean, I can't |
| 20 |  | remember these patents by numbers only. |
| 21 | Q | Okay. Sure. Can you look at Section D, please. |
| 22 |  | Can you read section D. |
| 23 | A | The title? |
| 24 | Q | Yes. |
| 25 | A | U.S. Patent No. 9,582,846. |

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| 1 | Q | Do you know what that patent number is? |
| :---: | :---: | :---: |
| 2 |  | MR. RENAUD: Objection. |
| 3 | A | '846. Yeah. I think that's another one of these |
| 4 |  | unified shader patents. |
| 5 | Q | Do you know if you've been designated to testify |
| 6 |  | today on complainants' behalf for conception and |
| 7 |  | reduction to practice regarding that 9,582,846 |
| 8 |  | patent? |
| 9 | A | So the assignment for the -- sorry, the first |
| 10 |  | notice of deposition says that I am assigned to |
| 11 |  | testify on the reduction to practice to any |
| 12 |  | alleged acts of diligence in reduction of practice |
| 13 |  | of each of the asserted claims and asserted |
| 14 |  | patents. However, not being a lawyer, I don't |
| 15 |  | exactly remember which patents were asserted and |
| 16 |  | which were not. |
| 17 | Q | Okay, I'll ask the court reporter to please mark |
| 18 |  | Exhibit 12. |
| 19 |  | ('454 Patent marked Exhibit 12 for |
| 20 |  | identification.) |
| 21 | Q | Mr. Lefebvre, have you seen Exhibit 12 before? |
| 22 |  | While you're looking, I'll note for the |
| 23 |  | record, it is AMD1044_0000165 through 176. |
| 24 |  | And I'm sorry, Mr. Lefebvre, have you seen |
| 25 |  | Exhibit 12 before? |

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|  |  | discussing earlier that's identified in Section D |
| 2 |  | of Exhibit 11? |
| 3 | A | Section B? |
| 4 | Q | D. |
| 5 | A | D. Yes. With the same caveat as before, that it |
| 6 |  | has a B2 at the end, which this Section D does |
| 7 |  | not. |
| 8 | Q | If we refer to this as the l 846 patent going |
| 9 |  | forward, is that okay with you? |
| 10 | A | That is okay with me, yes. |
| 11 | Q | Okay. So turning back now to Exhibit 11, if you |
| 12 |  | look at Section $C$, can you read the first full |
| 13 |  | sentence on page 3 in that, beginning with, "The |
| 14 |  | Asserted claims." |
| 15 | A | "The asserted claims of the '454 Patent were |
| 16 |  | conceived at least as early as August 24, 2001." |
| 17 | Q | Mr. Lefebvre, do you understand that to be AMD and |
| 18 |  | ATI's contention in this case? |
| 19 |  | MR. RENAUD: Objection. |
| 20 | A | I am not a lawyer, so I don't even -- I can't |
| 21 |  | interpret contention for you. I can read the |
| 22 |  | English, and it says, "asserted claims of the '454 |
| 23 |  | Patent," which appears to be this one, and "were |
| 24 |  | conceived at least as early as August 24, 2001." |
| 25 | Q | Do you agree with that statement? |

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|  |  | point, which was about the contentions of this |
| 2 |  | document, are outside the scope on a question by |
| 3 |  | question -- |
| 4 |  | MR. ELENGOLD: So you're objecting to the |
| 5 |  | prior questions. |
| 6 |  | MR. RENAUD: That's right. On a question by |
| 7 |  | question basis, I think facts related to any |
| 8 |  | contentions are fair game, although he may know |
| 9 |  | one way or another whether they support or don't |
| 10 |  | support contentions. |
| 11 |  | MR. ELENGOLD: Are you objecting to the |
| 12 |  | question, "What did the R400 do as of August 24, |
| 13 |  | 2001"? |
| 14 |  | MR. RENAUD: To the extent you're relating |
| 15 |  | it to the contentions, I am. To the extent it's |
| 16 |  | standing alone, I'm not. |
| 17 | A | Okay. So the August 24, 2001 is a date that is |
| 18 |  | after the date of this specification here, Exhibit |
| 19 |  | 10, that says -- well, actually, it's the date of |
| 20 |  | that specification. So if by "conception," you |
| 21 |  | mean writing the specification of the sequencer |
| 22 |  | that describes how the R400 unified shader works, |
| 23 |  | then yes, I agree with this statement. |
| 24 | Q | So I think my question was, just so we're clear |
| 25 |  | for the record, because I'm not sure you answered |

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my question at all, my question said, "What did
the R400 do as of August 24, 2001."
MR. RENAUD: Objection.
A Okay. I don't recall what the actual $R 400$ did at
that time. The one thing that I can point to is
the fact that the specification, which I wrote,
was available on that date and described the
functioning of the sequencer or -- of the R400.
Q Do you know if that specification by itself
supports conception of the claims of the '454
patent on August 24, 2001?
MR. RENAUD: Objection.
A I am not a patent attorney, again. I don't have
any law background. I can attest to the facts,
and the facts are that the specification existed
at that date according to the entries in the file.
Q Are you aware of any facts other than that
document to support conception of your unified
shader invention on August 24, 2001?
MR. RENAUD: Objection.
A I am aware of at least that other specification,
which is Exhibit 3, that you gave me, that is the
proposal for the R400 architecture that is also
dated well ahead of the August 24, 2001 date. So
that would be another proof or fact behind the
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|  |  | fact that this chip or this idea was conceived on |
| 2 |  | or before that date. |
| 3 | $Q$ | Anything else? |
| 4 | A | Sure. We can go to the Perforce server again and |
| 5 |  | do a search of the files that existed then. I |
| 6 |  | must have written some portion of the C simulator |
| 7 |  | which described the R400 functions. That would be |
| 8 |  | another thing we can look at. |
| 9 | Q | Do you know if that exists? Have you reviewed |
| 10 |  | that code to see if it exists? |
| 11 | A | I know that I reviewed the Perforce submission as |
| 12 |  | part of doing this Declaration, which has a |
| 13 |  | calendar, and so if we look at this calendar and |
| 14 |  | pinpoint August 24, unless it goes all the way |
| 15 |  | down -- yes, 1 think it does. |
| 16 |  | So by August 24, 2001, the only entry in |
| 17 |  | this calendar on page 33 is the sequencer |
| 18 |  | specification, and from that point on, there is a |
| 19 |  | list of code and changes that occurred that showed |
| 20 |  | that we worked on the R400 project from that point |
| 21 |  | on. |
| 22 |  | MR. RENAUD: Just so the record is clear, |
| 23 |  | all of the documents that he's referring to |
| 24 |  | regarding Perforce have been either produced or |
| 25 |  | made available to respondents. |

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|  |  | MR. ELENGOLD: When you say "made |
| 2 |  | available," I'm not sure what you're referring to. |
| 3 |  | MR. RENAUD: The source code is on a source |
| 4 |  | code computer. |
| 5 |  | MR. ELENGOLD: Yeah, and the documents have |
| 6 |  | been produced? |
| 7 |  | MR. RENAUD: Yes. |
| 8 | Q | So I believe you discussed this August 24 th date |
| 9 |  | in your Declaration as well. Do you recall that? |
| 10 |  | MR. RENAUD: Objection. |
| 11 | Q | I'll direct you to page 8. |
| 12 |  | MR. RENAUD: Can you just state the Exhibit |
| 13 |  | number because there are multiple declarations in |
| 14 |  | the case? |
| 15 |  | MR. ELENGOLD: I think there is only one |
| 16 |  | that we're using today, but it is Exhibit 6 . |
| 17 |  | MR. RENAUD: Thank you. |
| 18 | A | Yes. So in this Declaration -- sorry, making sure |
| 19 |  | I get the words right. I did describe that the |
| 20 |  | Version 0.4 of the R400 Sequencer Specification |
| 21 |  | was dated on August 24, 2001. |
| 22 |  | And furthermore, to qualify our previous |
| 23 |  | discussions, it says here that this date was |
| 24 |  | corroborated by the Perforce log. So I think it |
| 25 |  | is a true and accurate date because you had some |

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|  |  | contention to the day before, you said it could be |
| 2 |  | this or after. This can conclusively prove that |
| 3 |  | it is actually this date and not another one. |
| 4 | Q | The documents that are cited in your Declaration |
| 5 |  | prove that? |
| 6 | A | The fact that the log entry meant that, when I did |
| 7 |  | this Declaration, and I do remember reviewing the |
| 8 |  | calendar events against the Perforce logs, so I'm |
| 9 |  | confident that this is a true and accurate date, |
| 10 |  | and it came from the Perforce log and not only the |
| 11 |  | written version on page 3 of Exhibit 10. |
| 12 | Q | And the purpose of your Declaration was to |
| 13 |  | similarly establish a conception date and to a |
| 14 |  | reduction of practice date with regard to the |
| 15 |  | prior proceeding, is that correct? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | Can you rephrase your question? I got confused. |
| 18 | Q | Sure. When you put together this Declaration, it |
| 19 |  | was to try to talk about your work on the R400 |
| 20 |  | with regard to the unified shader patents, |
| 21 |  | correct? |
| 22 |  | MR. RENAUD: Objection. |
| 23 | A | I believe this Declaration that I did was to show |
| 24 |  | work on the R400 project and when each of the |
| 25 |  | elements occurred. I mean, it is obviously, the |

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| 1 | R400 is an implementation of the patent, so by |
| :--- | :--- |
| 2 | extension, it is loosely related to the patent, |
| 3 | but this is really more a collection of facts |
| 4 | about the R400. |
| 5 | Q |

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|  |  | has been done by AMD. I'm only human. I mean, |
| 2 |  | there's probably more things, but I can't offhand |
| 3 |  | think of anything else. |
| 4 | Q | And that's the IKOS system we talked about with |
| 5 |  | regard to Exhibit 9? |
| 6 |  | MR. RENAUD: Objection. |
| 7 | Q | Is that correct? |
| 8 | A | Yes. This is the similar -- this is the same |
| 9 |  | IKOS, and we did touch on this subject when this |
| 10 |  | Exhibit was brought up. |
| 11 | Q | Are there any other facts you're aware of beyond |
| 12 |  | those in your Declaration and the IKOS device |
| 13 |  | regarding the R400? |
| 14 |  | MR. RENAUD: Objection. |
| 15 | A | Can you describe, like, what facts -- |
| 16 | Q | Sure. |
| 17 | A | -- you want me to, because this is a very, very |
| 18 |  | broad subject on a very broad -- |
| 19 | Q | You told me earlier that you're here to testify |
| 20 |  | about facts related to topics including conception |
| 21 |  | and reduction to practice, is that correct? |
| 22 | A | Yes, that is correct. |
| 23 | Q | Beyond the facts that you put into your written |
| 24 |  | testimony and what we've discussed regarding the |
| 25 |  | IKOS device, are there any other facts that you're |

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| 1 |  | aware of to support those topics? |
| 2 | A | I see. |
| 3 |  | MR. RENAUD: Objection. |
| 4 | A | No, as of today, there are no other facts that I |
| 5 |  | can remember being aware of. |
| 6 | Q | For conception and for reduction to practice. |
| 7 | A | Again, I'm not an attorney. I don't know what |
| 8 |  | conception, reduction to practice means. I can |
| 9 |  | speak about the dates of the R400, and timeline, |
| 10 |  | and the specifications. If this was your |
| 11 |  | question, then yeah. |
| 12 | Q | Okay. Turning back to Exhibit 11. |
| 13 | A | Yes. |
| 14 | Q | Staying in the same paragraph we were in, the |
| 15 |  | third full sentence begins, "The asserted claims |
| 16 |  | of the '454 patent were actually also reduced to |
| 17 |  | practice," do you see that sentence? |
| 18 | A | The asserted claims. Yeah, so you're referring to |
| 19 |  | page 3, line five? |
| 20 | Q | Yes. |
| 21 | A | Okay, "Asserted claims of the ' 454 Patent were |
| 22 |  | also actually reduced to practice, in the form of |
| 23 |  | physical embodiments, at least as early as April |
| 24 |  | 20, 2003 and June 26, 2003." Yes, I see those |
| 25 |  | lines. |

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1 Q What happened with regard to the R 400 project on
April 20, 2003?
MR. RENAUD: Objection.
A I don't recall this exact date. It might be the
date on which the -- there was some evidence of
IKOS implementation, but let me check the calendar
to see if this date is present in the calendar to
refresh my memory.
April 28, 2003.
So I see some check-ins on that date from
the calendar, I don't know, some RTL check-ins and
a test. I don't know why that date got picked up
in this notice here, but, you know -- "form of
physical embodiment."
I don't quite understand the physical
embodiment nomenclature, if you will. But so I
don't know.
Q What happened with regard to the R 400 program on
June 26, 2003?
MR. RENAUD: Objection.
A June 26, 2003. Again, from the calendar there
were some check-ins to the Perforce depot. And
the first synthesis of the R400, at least
according to Exhibit 9, page AMD1044_0175196 said
that the first synthesis occurred on, I guess it

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| 1 |  | is August 3, 2003, or on or before August 3, 2003. |
| 2 |  | Other than that, I can't really remember or tell |
| 3 |  | from the documentation that you have here in front |
| 4 |  | of me what actually occurred on that date. I |
| 5 |  | don't recall. |
| 6 | Q | For the R 400 program, what activities were |
| 7 |  | occurring between August 24, 2001 and the third |
| 8 |  | quarter of 2002? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | Can you restate the question, please. |
| 11 |  | (Question read back.) |
| 12 | A | August 24. So that's initial. |
| 13 |  | And the third quarter of? |
| 14 | Q | 2002. |
| 15 |  | MR. RENAUD: Objection. |
| 16 | A | And by "third quarter," you mean up until what, |
| 17 |  | August? September? What do you mean by third |
| 18 |  | quarter? |
| 19 | Q | Let's go with July. |
| 20 | A | July. |
| 21 | Q | What was occurring with regard to the R400 program |
| 22 |  | between August 24, 2001 and July 2002? |
| 23 |  | MR. ELENGOLD: Objection. |
| 24 | A | Again, I am referring to my Declaration, which is |
| 25 |  | Exhibit No. 6, calendar, Diligence Calendar. On |

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Page 193 of 312 environment, which is the graphics core; that is, all the blocks of the graphics domain to be working and energizing. And so all of these persons are all, as far as $I$ can tell, and again, a lot of them left AMD, but at the time were all graphics designers or graphics architects; might not have directly worked on the unified shader blocks per se, but all their work was relevant to the unified shader because of the reason that in order to enable testing of the unified shader, and the sequencer and the $S P$, we needed the whole graphics core block to be working.

Q So is it true then that the sequencer was never tested until November 2003?

MR. RENAUD: Objection.
A I fail to understand why you're making that comment.

Q Well, your Diligence Calendar shows work occurring on R400 through November 2003, is that correct, and that's on page 175547.

A 175. Which date did you say, sorry?
Q November 2003. So is it correct that your Diligence Calendar that you put into your Declaration shows work occurring on the R400 until November 2003?

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| 1 |  | MR. RENAUD: Objection. |
| 2 | A | This Diligence Calendar shows that there is work, |
| 3 |  | yes, occurring on either the tests infrastructure, |
| 4 |  | which are used to test the sequencer or the |
| 5 |  | emulator or the RTL. But it doesn't mean that the |
| 6 |  | SQ, or the sequencer, the R400 Sequencer, was not |
| 7 |  | tested before then. It means that the testing or |
| 8 |  | the, you know, the work progressed all the way to |
| 9 |  | that November 20 th date. |
| 10 | Q | When was the sequencer first tested? |
| 11 | A | So you can say that effectively the sequencer |
| 12 |  | and again, it depends on your definition of |
| 13 |  | "tested." Can you refine exactly what you mean by |
| 14 |  | tested? |
| 15 | Q | Well, you just said there was no block level test |
| 16 |  | bench, so everything affected the sequencer |
| 17 |  | because it couldn't be tested until the other |
| 18 |  | people did their work, is that correct? |
| 19 |  | MR. RENAUD: Objection. |
| 20 | A | I did say there was no sequencer test bench, and |
| 21 |  | thus by definition, the sequencer was affected by |
| 22 |  | the other blocks. That is correct. |
| 23 |  | So for example, if one of the other blocks |
| 24 |  | were to break or stop working, this would affect |
| 25 |  | temporarily at least the sequencer because the |

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|  |  | test would be broken momentarily. It doesn't mean |
| 2 |  | that the sequencer was not tested and, you know, |
| 3 |  | in fact of the matter is, if you find that a given |
| 4 |  | change to another block broke the graphics core |
| 5 |  | test bench, you could just revert that locally on |
| 6 |  | your machine so that work can continue on the |
| 7 |  | sequencer on the R400. |
| 8 | Q | And those kinds of changes were occurring at least |
| 9 |  | through November, 2003, is that correct? |
| 10 |  | MR. RENAUD: Objection. |
| 11 | A | From this calendar of event, I can't really tell |
| 12 |  | you what kind of changes occurred. We would need |
| 13 |  | to go to the Perforce depot and look at each and |
| 14 |  | every change and see what was modified. |
| 15 |  | This just says that some work occurred all |
| 16 |  | the way up until November 20, 2003. And this |
| 17 |  | Exhibit here, which is Exhibit No. 9, shows that |
| 18 |  | by August 30 of 2002, the single triangle test was |
| 19 |  | working on the sequencer, and this was a GC test |
| 20 |  | bench, which is the same test bench that we are |
| 21 |  | referring to here. |
| 22 | Q | And additional problems were getting fixed until |
| 23 |  | November 2003, is that correct? |
| 24 | A | Additional issues, or problems or, you know, new |
| 25 |  | features requested by Microsoft or whatnot, were |

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|  |  | the Sequencer Version 2.5 at least on or before |
| 2 |  | that date. |
| 3 | Q | Were there any revisions to the sequencer |
| 4 |  | specification after 2.0? |
| 5 | A | Yes, there were. In fact, if you refer to again |
| 6 |  | Exhibit 6, page AMD1044_0011679, you're going to |
| 7 |  | see a table there that lists a collection, and I |
| 8 |  | don't think if it's an exhaustive list of all the |
| 9 |  | specifications ever released, but you can clearly |
| 10 |  | see that beyond 2.0, we went to 2.1, and then all |
| 11 |  | the way to revision number 2.11, all of which I |
| 12 |  | believe were provided as part of this written |
| 13 |  | testimony as Exhibits. |
| 14 | Q | Do you know if the 2.11 sequencer specification |
| 15 |  | was the last version of the specification? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | I do not recall that information, no. |
| 18 | Q | When did you stop working on the R400 sequencer? |
| 19 | A | Again, the work for me from the R 400 to Xenos |
| 20 |  | transition was seeming -- I mean, it was very |
| 21 |  | fluid, and so I don't really remember how and when |
| 22 |  | I transitioned to Xenos, and how and when |
| 23 |  | documents got imported over. |
| 24 |  | The fact of the matter is the Xenos program, |
| 25 |  | as far as the sequencer and the unified shader is |

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|  |  | concerned, is the R400 program, and such, you |
| 2 |  | know, it was just one big continuous for me. |
| 3 | Q | So the R400 sequencer could have continued |
| 4 |  | changing even after version 2.11 was complete, is |
| 5 |  | that right? |
| 6 |  | MR. RENAUD: Objection. |
| 7 | A | So it could. What it could also mean is by that |
| 8 |  | time the R400 program got cancelled and we started |
| 9 |  | working on the specification in the Xenos depot, |
| 10 |  | but like I said, to me it's just a location for a |
| 11 |  | file, and so I would have continued working on the |
| 12 |  | sequencer, almost as if it was the R400 because |
| 13 |  | they were so similar. |
| 14 | Q | Was the sequencer always getting modified up until |
| 15 |  | when Xenos chip was netlisted for production? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | So while I know a lot about what's inside Xenos |
| 18 |  | because it's the same design for me as the R400, |
| 19 |  | I'm not as familiar with the Xenos dates, and so I |
| 20 |  | don't know and remember how this would line up |
| 21 |  | with my work on the R400, or my work on Xenos per |
| 22 |  | se. |
| 23 | Q | Was the R400 sequencer constantly being changed |
| 24 |  | until the end of the R 400 program? |
| 25 |  | MR. RENAUD: Objection. |

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1 A I can tell you. Let me look at the calendar 2 again. So the R400 -- so the calendar is not 3 precise enough because the -- the R400 sequencer

Q Is that what would have been in the Arch folder?
A Yes, it would have been an Arch change, so for example here, the last Arch change that $I$ see in this calendar occurred on Monday, October 6, 2003, unless I missed an entry.

Q So outside of what we've discussed with regard to the calendar in your Declaration, which is Exhibit 6, are there any other activities you're aware of

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|  |  | that were going on with regard to the R400 program |
| 2 |  | from August 2001 to July, 2002? |
| 3 |  | MR. RENAUD: Objection. |
| 4 | A | Again, there was this IKOS activity, which is the |
| 5 |  | hardware prototype, which was, you know, at least |
| 6 |  | planned, and if you give me another presentation |
| 7 |  | which has more complete dates, we could get a |
| 8 |  | better refine date on this, but it was at least |
| 9 |  | planned to be occurring around 11, October 11 of |
| 10 |  | 2002. |
| 11 | Q | And you think that took place before July 2002? |
| 12 | A | Sorry, so July 2000 -- no, of course. Well, I |
| 13 |  | mean, it was planned to be. Whether or not, you |
| 14 |  | know, things got started on that machine before |
| 15 |  | that, you know, I would have to -- |
| 16 | Q | That's the IKOS emulation start you're talking |
| 17 |  | about that's in Exhibit 9? |
| 18 | A | Yes. That is it. |
| 19 | Q | So if that emulation had started before the |
| 20 |  | August 30, 2002 presentation, do you think it |
| 21 |  | would have said it in the presentation? |
| 22 |  | MR. RENAUD: Objection. |
| 23 | A | So this is saying whether or not we were -- so |
| 24 |  | effectively, my understanding of this IKOS |
| 25 |  | emulation start line is that we would have been |

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Q Is that the IKOS emulation with software date, when you start running things on it?

MR. RENAUD: Objection.
A No. The IKOS emulation with software, in my opinion, refers to trying to use the IKOS hardware with the driver versus trying to energize it manually, if you will, with simple tests.

Q Okay. So other than what's identified in Exhibit 9 and the calendar in your Declaration, what other activities are you aware of that were going on with regard to the R 400 program from August 2001 to July of 2002?

MR. RENAUD: Objection.
That is the extent of what $I$ remember.

Other than your Declaration, Exhibit 6, and Exhibit 9, what activities are you aware of that occurred from July 2002 to April 2003 with regard to the R400 program?

MR. RENAUD: Objection.
A I mean there's a bunch of other presentations that we have as Exhibit that I've seen. Without seeing them again to refresh my memory, $I$ can't really

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| 1 |  | his answer. |
| 2 |  | MR. ELENGOLD: I'm not intending to |
| 3 |  | interrupt. I just want to make sure he understood |
| 4 |  | my question. I don't have to strike his answer, |
| 5 |  | but -- |
| 6 | A | Your question pertained to the IKOS program, and |
| 7 |  | the IKOS program as I understand -- |
| 8 | Q | What you learned from Mr. White with regards to |
| 9 |  | the IKOS program. |
| 10 |  | MR. RENAUD: Are you going to let him |
| 11 |  | answer? |
| 12 | A | I learned from Mr. White -- we tried to record |
| 13 |  | from Mr. White the amount of recollection he had |
| 14 |  | on the IKOS program. What I'm trying to tell you |
| 15 |  | is that on that subject matter, which is the whole |
| 16 |  | implementation of the R400 on a hardware machine, |
| 17 |  | looking at the other documentation that was |
| 18 |  | present in the room, I saw that there was a bunch |
| 19 |  | of document that were likely not in the Exhibit 6 |
| 20 |  | agenda because they were in directories that were |
| 21 |  | not covered by this particular investigation, and |
| 22 |  | they were, you know, provided, as I understand, by |
| 23 |  | Pam Horn in AMD, and Dave Christie, to you to |
| 24 |  | describe the amount of work that went in, into the |
| 25 |  | IKOS server, as well as other activities of AMD |

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|  |  | during that timeframe, and these include, like, |
| 2 |  | extensive Perforce logs as I understand, and |
| 3 |  | extensive presentations that are not covered in |
| 4 |  | this detailed agenda that only covers a subsection |
| 5 |  | of the directories of the Perforce server and not |
| 6 |  | the whole database. |
| 7 |  | And furthermore, I also saw some other Xenos |
| 8 |  | presentations that were laying on the table, and |
| 9 |  | that reminded myself that this is, although not -- |
| 10 |  | also, sorry, not covered by Exhibit No. 6, and I |
| 11 |  | understand, because it was on the table down |
| 12 |  | there, that it was provided as information to you |
| 13 |  | guys. |
| 14 |  | So there is a wealth of document that are |
| 15 |  | available that show work that are not covered by |
| 16 |  | the scope of this particular agenda which is |
| 17 |  | definitely inclusive -- well, not inclusive, but |
| 18 |  | it's -- all the work here is included in the |
| 19 |  | document, but this is not exhaustive as to the |
| 20 |  | amount of information that AMD has on the work |
| 21 |  | that went in. |
| 22 | Q | The documents you're referring to, did you review |
| 23 |  | them yesterday? |
| 24 | A | They were on the table all day but, you know, |
| 25 |  | honestly, the table is covered with documents so |

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| 1 | Q | So you reviewed them Monday, yesterday, and today, |
| :---: | :---: | :---: |
| 2 |  | is that correct, these Perforce logs that you're |
| 3 |  | talking about? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | So the logs were on the table. I saw them. I did |
| 6 |  | not, you know, go through them one by one on |
| 7 |  | Monday and Tuesday. I did go and look at them |
| 8 |  | today after I talked to Pam because, you know, she |
| 9 |  | reminded me we have all these logs, and so you |
| 10 |  | make sure that you explain to them that this is |
| 11 |  | more than just what you did on the sequencer. |
| 12 |  | There's all of the MAS, so they are not just the |
| 13 |  | sequencer and the SP. All of the presentations |
| 14 |  | that we provided are not in these directories that |
| 15 |  | you have in your Declaration because some of them |
| 16 |  | are on servers, and she told me -- and Dave |
| 17 |  | actually told me that we also provided, you know, |
| 18 |  | tests, and test descriptions, and test logs, which |
| 19 |  | would also not be on the, on these particular |
| 20 |  | directories in Perforce. |
| 21 | Q | When did you talk to Pam Horn? |
| 22 | A | I just did during the break with Dave Christie as |
| 23 |  | well. |
| 24 | Q | How long did you talk for? |
| 25 | A | If memory serves, about 10 minutes or so. 10 |

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| 1 |  | Page 212 |
| :---: | :---: | :---: |
|  |  | minutes with Pam, maybe six minutes with Dave |
| 2 |  | Christie because he joined in after she had her -- |
| 3 |  | she called him basically to complement her |
| 4 |  | answers. |
| 5 | Q | Was it your idea to call Pam Horn during the |
| 6 |  | break? |
| 7 | A | So it was after I sought wealth of document on the |
| 8 |  | table and realized that I was not talking here on |
| 9 |  | my behalf but on behalf of AMD, that I decided to |
| 10 |  | go forward and make sure that I was covering |
| 11 |  | everything because this particular declaration is |
| 12 |  | somewhat -- well, it's exhaustive, but it only |
| 13 |  | pertains to the sequencer, which is not the whole |
| 14 |  | R400, so I wanted to make sure that, because I'm |
| 15 |  | not talking in my name, I got all the bases |
| 16 |  | covered. |
| 17 | Q | Was it your idea to call Pam Horn during the |
| 18 |  | break? |
| 19 | A | Well, I mean, again, I was looking at the |
| 20 |  | specification, and so that was my idea to look |
| 21 |  | more and then find more, but the actual idea of |
| 22 |  | calling came from counsel. |
| 23 | Q | Which counsel? |
| 24 | A | The present counsel. |
| 25 | Q | Do you know their names? |

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| 1 | A | Well, I mean the counsel Adam Rizk and |
| :---: | :---: | :---: |
| 2 | Q | So Adam and Michael suggested that you call Pam, |
| 3 |  | is that correct? |
| 4 | A | Well, they called her and put her on the line, |
| 5 |  | yeah, but -- |
| 6 | Q | So they just called her. |
| 7 | A | They opened the line to Pam, is all they did. |
| 8 | Q | Did you ask Pam questions? |
| 9 | A | Yes. |
| 10 | Q | What was the first question you asked Pam? |
| 11 | A | I asked Pam to tell me if the Perforce log on the |
| 12 |  | table that was sitting next to me was part of the |
| 13 |  | evidence that was sent to the counsel team and if |
| 14 |  | there were more, because I was concerned that, you |
| 15 |  | know, there was not enough information here to |
| 16 |  | cover everything or every activity that occurred |
| 17 |  | at the AMD. I'm only human. I can only know so |
| 18 |  | much. |
| 19 | Q | What was the name of the Perforce log? |
| 20 | A | That Perforce log did not have a name. It's just |
| 21 |  | a thick book of paper with all of the Perforce |
| 22 |  | entries in both the Xenos repository and the R400 |
| 23 |  | repository. It's just a big stack of paper with a |
| 24 |  | big paper binder attached to it. |
| 25 | Q | Did you ask Pam any other questions? |

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| 1 | A | I'm sure there will be some kind of document that |
| :---: | :---: | :---: |
| 2 |  | show the communications, and from those documents, |
| 3 |  | we can infer which was the first, you know, |
| 4 |  | discussion to Microsoft, but I can't remember all |
| 5 |  | of these dates on all this wealth of documents. |
| 6 |  | If you want to talk about these, I mean, just |
| 7 |  | bring the documents on the table and we can sort |
| 8 |  | them and look which one is the first one. |
| 9 | Q | Do you know if the first discussion of the Xenos |
| 10 |  | chip between Microsoft and ATI has been produced |
| 11 |  | in this case? |
| 12 | A | I don't know if the first one got produced or not, |
| 13 |  | but I know that from discussions with Dave and |
| 14 |  | from the document I saw, that presentations were |
| 15 |  | disclosed, and so you know, I can't say |
| 16 |  | conclusively from those presentations whether or |
| 17 |  | not the first presentation would have been here or |
| 18 |  | not, but there were a wealth of presentations, and |
| 19 |  | some of these presentations were to Microsoft. |
| 20 | Q | Did you do any investigation as to when the first |
| 21 |  | offer of the Xenos chip to Microsoft was? |
| 22 | A | Can you rephrase the question, please. |
| 23 | Q | Sure. |
| 24 | A | When you say "first" -- |
| 25 | Q | In preparing for your deposition, did you do any |

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| 1 | A | I believe it -- I mean, the purpose of the shader, |
| :---: | :---: | :---: |
| 2 |  | the unified shader, unified pixel and vertex |
| 3 |  | shader is to process pixels and vertices, and so I |
| 4 |  | think that the one triangle, admittedly, it -- |
| 5 |  | sorry, it is a fairly simple test, but it shows |
| 6 |  | that the shader is able to process both vertex and |
| 7 |  | pixels, and as such, it shows that it can work in |
| 8 |  | the simplest form. It doesn't mean that all the |
| 9 |  | corner cases are, you know, figured out and |
| 10 |  | everything, but to me, the test passes, the test |
| 11 |  | worked. The hardware generates a picture, the |
| 12 |  | right picture. |
| 13 | Q | Can you please turn to Exhibit 12. |
| 14 | A | Yes. I am on Exhibit 12. |
| 15 | Q | Do you know what a patent claim is? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | Pardon me, can you repeat? |
| 18 | Q | Do you know what a patent claim is? |
| 19 | A | I know where to find the patent claims. I know |
| 20 |  | how to read them in English. I can't really |
| 21 |  | interpret them in the sense of the law because, |
| 22 |  | you know, I'm not equipped to really tell you what |
| 23 |  | they mean in the sense of the law. |
| 24 | Q | Were you involved in drafting the claims of the |
| 25 |  | ' 454 patent? |

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```
A The way I recall it working at AMD is what we
    filed, what we call an IDF, which is Invention
    Disclosure Form to the attorneys, or an attorney
    in that particular case, and we describe and work
    with the attorney to describe the machine, in that
    case, the R400, and then the claims are -- were
    worded by the attorney retained to write this
    patent, and that's my understanding on how it
    went.
Q Do you have an opinion on whether or not the R400
    uses claim 2 of the '454 patent?
        MR. RENAUD: Objection.
    A So not being an attorney, I don't have an opinion
        on the claims per se. I can't break down the
        product down to a set of claims. I have not done
        the regression, the, you know, the study to see
        what exists and what not. What I can tell you is
        I believe the R400 and the unified shader in that
        R400 are implementing in the general sense what is
        described in this patent, yes.
    Q Can you look at Figure 4A please on page 171.
        Have you looked at this figure before?
    A Yes, I have looked at this figure. This is a
        figure in the patent, so having read the patent,
        I've seen this figure before, yes.
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|  |  | Page 225 |
| :---: | :---: | :---: |
| 1 | Q | Have you done that? |
| 2 | A | I have not done that personally, but you know, put |
| 3 |  | the code on and we can do it right now. |
| 4 | Q | Has anyone at AMD to your knowledge compared the |
| 5 |  | RTL code of the R400 to the Figures of the '454 |
| 6 |  | patent? |
| 7 |  | MR. RENAUD: Objection. |
| 8 | A | So I know the code got produced. I don't know if |
| 9 |  | anyone at AMD did or did not do it. I mean, I |
| 10 |  | know there is a lot of evidence that was produced, |
| 11 |  | and somewhere in there, there is probably a |
| 12 |  | mapping of that nature. It's just -- you know, |
| 13 |  | again, I can't, I can't remember, if you don't put |
| 14 |  | the -- it's too far away. You have to put some |
| 15 |  | documents in front of me for me to conclusively |
| 16 |  | say one way or another. |
| 17 | Q | What about Figure 5. Can you turn to Figure 5, |
| 18 |  | please. It's on page 172. Does Figure 5 look |
| 19 |  | like an accurate representation of the R400 |
| 20 |  | architecture? |
| 21 |  | MR. RENAUD: Objection. |
| 22 | A | By "R400 architecture," what do you mean exactly? |
| 23 |  | Can you refine your question? |
| 24 | Q | Sure. Do you remember any documents that referred |
| 25 |  | to the R400 architecture that we looked at |

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|  |  | Page 226 |
| :---: | :---: | :---: |
| 1 |  | earlier? |
| 2 | Q | And you don't have to look. I'm asking if you |
| 3 |  | remembered, but I'm taking it you don't, so let me |
| 4 |  | ask it a different way. Looking at Figure 5, does |
| 5 |  | Figure 5 look like the R400? |
| 6 | A | Figure 5 looks like, yes, something we would have |
| 7 |  | implemented in a similar fashion from the R400. I |
| 8 |  | mean, assuming the GPRs would be block 92, and |
| 9 |  | then the sequencer would be block 99, it looks, |
| 10 |  | you know, fairly familiar as to what the R400 |
| 11 |  | unified shader would have looked like. |
| 12 | Q | Why do you say that block 99 looks like the |
| 13 |  | sequencer? |
| 14 | A | Well, for one, it contains the instructions store |
| 15 |  | in the constant, which is where these things are |
| 16 |  | located in the R400, and for two, in the |
| 17 |  | specifications, column 4, line 52, it states, "The |
| 18 |  | sequencer 99 includes constants block 91 and |
| 19 |  | instructions store 98," so. |
| 20 | Q | Anything else? |
| 21 | A | Anything else about what? |
| 22 | Q | Why you say block 99 looks like the sequencer. |
| 23 |  | Any other reason? |
| 24 | A | Well, I mean, it's connected to the SP, or the ALU |
| 25 |  | unit by line 94. And I can go and read the spec |

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So you know, the whole paragraph here describes it in some detail.

Q So turning back to claim 2, having now looked at the figures and the specification, do you know whether the R 400 practices claim 2 of the '454 patent?

MR. RENAUD: Objection.
A Again, I mean, claims are patent verbiage for me, and I'm not equipped to discuss the claims. I'm not an attorney. I can tell you again that this patent, like the Exhibit 12, the patent '454, is based on the R400 design, and as such, I think the R400 is an implementation of this patent.

But further than that, I mean, can't really tell you.

Q So you don't have an opinion with respect to whether the R 400 practices any claims of the ' 454 patent, is that correct?

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|  |  | Page 230 |
| :---: | :---: | :---: |
| 1 |  | document? |
| 2 |  | MR. RENAUD: Objection. |
| 3 | A | No. The reason why I referred to this |
| 4 |  | specification is to try to be precise in my answer |
| 5 |  | in terminology. My understanding is, in the R400, |
| 6 |  | in the pipeline, and the chip in general, the |
| 7 |  | shader is the part that executes the ALU |
| 8 |  | instructions. |
| 9 | Q | So the shader is inside of the shader pipeline; is |
| 10 |  | that what you're trying to say in that |
| 11 |  | distinction? |
| 12 |  | MR. RENAUD: Objection. |
| 13 | A | In the R 400 , the shader pipeline contains the ALU |
| 14 |  | modules and it is the block that executes the ALU |
| 15 |  | operation. |
| 16 | Q | The shader pipeline is the block, is that what |
| 17 |  | you're saying? |
| 18 | A | The shader pipeline, or I mean, in one -- it's |
| 19 |  | terminology, but the shader pipeline can be seen |
| 20 |  | as a block, yes. That includes the GPRs and the |
| 21 |  | ALU units. |
| 22 | Q | Are shader pipeline and the shader synonymous for |
| 23 |  | purposes of the R400 documents? |
| 24 |  | MR. RENAUD: Objection. |
| 25 | A | So again, in the scope of the R400, I believe I've |

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| 1 |  | Page 231 |
| :---: | :---: | :---: |
|  |  | said before that shader is the program that you |
| 2 |  | run on your vertex or pixel shaders, and the |
| 3 |  | shader pipeline is the block that operates on the |
| 4 |  | ALU instructions. |
| 5 | Q | Is the sequencer inside of the shader pipeline? |
| 6 |  | MR. RENAUD: Objection. |
| 7 | A | The sequencer is inside the shader complex, I |
| 8 |  | would call it, so but it's outside of the shader |
| 9 |  | pipeline. So if you go to Exhibit 10, the |
| 10 |  | Sequencer Specification, there is a picture on |
| 11 |  | page 11 that shows the shader pipe, and so you can |
| 12 |  | see that the docs states, "the grey area |
| 13 |  | represents blocks," and I read, "that are |
| 14 |  | replicated four times per shader pipe." |
| 15 |  | So this is what I would refer to as the |
| 16 |  | shader pipe, and you can see that from that |
| 17 |  | picture, the sequencer is just sitting next to it |
| 18 |  | and ordering instructions into the shader pipe. |
| 19 | Q | And this started with us discussing where the |
| 20 |  | processor unit was in the R 400 , do you recall |
| 21 |  | that? |
| 22 | A | Correct. And started with the fact that, you |
| 23 |  | know, we don't really use the term processor unit |
| 24 |  | in the R400. So I was trying to map that word on |
| 25 |  | our terminology to better understand your |

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|  | Page 233 |  |
| :---: | :---: | :---: |
| 1 |  | MR. RENAUD: Objection. |
| 2 | A | The R400 is a GPU, or was a GPU, so it's a |
| 3 |  | graphics processor, but it's not -- I mean, it's a |
| 4 |  | graphics engine. It's not limited to a GPU. This |
| 5 |  | graphics processor can be used in APUs, and in |
| 6 |  | fact, it's being used in the Xenos program, which |
| 7 |  | is a specialized piece of silicon as well, and |
| 8 |  | those are all the same product, as far as I'm |
| 9 |  | concerned, the same entity of graphics, if you |
| 10 |  | will. |
| 11 | Q | So the 400 can be used in a variety of different |
| 12 |  | kinds of chips. |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | I'm saying -- the 400 -- the R 400 is a project |
| 15 |  | name. The graphics core inside the 400 can be |
| 16 |  | applied to, could be applied to any kind of other |
| 17 |  | chips, whether it is an APU, or semi-custom unit, |
| 18 |  | or any kind of device that uses graphics in any |
| 19 |  | way. |
| 20 | Q | Is there a unified shader in the R400? |
| 21 |  | MR. RENAUD: Objection. |
| 22 | A | In the R400, there is what we like to call a pixel |
| 23 |  | and vertex unified shader, which is a unified |
| 24 |  | shader that shares the load or shares the work |
| 25 |  | between pixels and vertices. |

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$1 \quad \mathbf{Q}$ And we talked about that a lot earlier with regard
to the sequencer specification, correct?
MR. RENAUD: Objection.
Q And other R400 documents that we discussed.
MR. RENAUD: Objection.
A So restate the question, please?
Q Sure. Strike that.
Is there a arbiter circuit in the R400?
A There are multiple arbiter circuits in the R400.
Some of them are in the unified shader
pixel/vertex of the R400, and I'm sure there's
many others elsewhere.
Q So the pixel/vertex arbiter is in the unified
shader in the R400?
MR. RENAUD: Objection.
A The pixel/vertex shader input arbiter is in the
R400 design. Correct. That's the way we
implemented it.
Q And that was what you worked on inside the
sequencer, is that correct?
MR. RENAUD: Objection.
A I worked on the R400 sequencer as a whole, not
only the input arbiter, and I defined the way the
sequencer was supposed to be working as a whole.
This is just a subsection of the $R 400$ sequencer.
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| :---: | :---: | :---: |
|  |  | the whole code files so that I can look at it, |
| 2 |  | because without context it's hard to say whether |
| 3 |  | or not if it's the input arbiter or some other |
| 4 |  | arbiter. |
| 5 | Q | How many arbiters in the sequencer were |
| 6 |  | responsible for arbitrating between vertex and |
| 7 |  | pixel? |
| 8 |  | MR. RENAUD: Objection. |
| 9 | A | In the -- well, are you referring -- what version |
| 10 |  | of the sequencer are you referring to when you ask |
| 11 |  | that question? |
| 12 | Q | Did it change across versions of the sequencer? |
| 13 |  | MR. RENAUD: Objection. |
| 14 | A | The arbitration points changed slightly. I think |
| 15 |  | the concepts stayed the same, but in order for me |
| 16 |  | to give you an accurate answer, I would like to |
| 17 |  | phrase it in terms of a specific version of the |
| 18 |  | sequencer. Is it 0.4 that you want to address? |
| 19 | Q | Do you know which version this RTL code came from? |
| 20 |  | MR. RENAUD: Objection. |
| 21 | A | This here says that the RTL code file in question |
| 22 |  | is on page 63 of the Declaration, the SQ thread |
| 23 |  | arbiter, which would indicate to me that this is |
| 24 |  | not the input sequencer. This is some kind of |
| 25 |  | other arbiter further down in the RTL that chooses |

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| 1 |  | Page 239 |
| :---: | :---: | :---: |
|  |  | one ALU winner, and in order to do that, it needs, |
| 2 |  | in this particular design, which is .4, pick a |
| 3 |  | winning clause of all of the texture clauses, and |
| 4 |  | a winning clause of all of the ALU clauses, and |
| 5 |  | this is showing the hierarchy of how it could do |
| 6 |  | this, but you know, you could presumably also look |
| 7 |  | at all the texture clauses in parallel, and pick |
| 8 |  | one of them, and that would give you the same |
| 9 |  | winner. |
| 10 | Q | Was this -- I'm sorry, strike that. Earlier you |
| 11 |  | mentioned the Sequencer Version 2.0, is that |
| 12 |  | correct? |
| 13 | A | I believe I mentioned it quite a few times, yes. |
| 14 | Q | Is the Sequencer Version 2.0 the same with regard |
| 15 |  | to this arbitration scheme? |
| 16 |  | MR. RENAUD: Objection. |
| 17 | A | Sequencer Version 2.0 had -- has the same goal. |
| 18 |  | It has to pick a winner out of the pixels and the |
| 19 |  | vertices for both the ALU and the texture. The |
| 20 |  | arbitration, however, as you can see in |
| 21 |  | Declaration Exhibit 6, page 19, was done in one |
| 22 |  | arbiter, at least according to this diagram, that |
| 23 |  | was looking at the collection of the reservation |
| 24 |  | stations at the time, and picked an ALU and a |
| 25 |  | texture winner amongst the waves that are on the |

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1 A Yes. This is one of the specifications that would
2 be very helpful.
3 Q Did the Xenos chip use the same sequencer


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| 1 |  | Page 243 |
| :---: | :---: | :---: |
|  |  | depot or otherwise in the Perforce server of the |
| 2 |  | company. |
| 3 | Q | Is it hard to tape out from a netlist? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | Can you -- what -- I don't understand. |
| 6 | Q | Is it a lot of work to complete a tapeout once you |
| 7 |  | have a netlist? |
| 8 | A | I see. |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | In order to do a tapeout from a netlist, you need |
| 11 |  | to have a PD team in place and floor plan the |
| 12 |  | chip. |
| 13 |  | There is work involved definitely, but it |
| 14 |  | is -- I wouldn't say it's easy, but it's like |
| 15 |  | common in silicon devices. That work is no |
| 16 |  | different for GPUs or for any other kinds of |
| 17 |  | access device, so it's common knowledge as to how |
| 18 |  | to take a netlist and make it into a GDS tapeout |
| 19 |  | file. |
| 20 | Q | Do you know approximately how long it would take |
| 21 |  | to tape out product from a netlist? |
| 22 | A | What product are you -- |
| 23 | Q | The R400? |
| 24 | A | The R400. So it again, you have all the Perforce |
| 25 |  | logs so you have all the informations back and |

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$1 \quad \mathrm{Q}$ When did you first learn of the idea of using a unified shader for both vertex and pixel?

MR. RENAUD: Objection.
A I stated before, $I$ don't recall the exact date. I know discussion took place between myself Andy Gruber, Andi Skende, and Steve Morein, and there is evidence of the first specification proposal produced by Steve around November 13, 2000 or thereabouts.

So again, there's probably a lot more documents that we could dig to refine these dates, but that would have been around these dates that a discussion occurred on the subject.

Q What was the first company or person that you were aware of outside of ATI to discuss the idea of having a unified shader for both pixel and vertex shading?

MR. RENAUD: Objection.
A What do you mean? Can you say what you mean by "discuss"?

Q Sure. Are you aware of anyone outside of ATI having had an idea to use a unified shader for both vertex and pixel?

A Having ideas. I know, for example, that Qualcomm has a unified shader because they license it from

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| 1 | A | The flag used to say Date and Patent Granted, |
| :---: | :---: | :---: |
| 2 |  | white flag, and then black flag said Date and |
| 3 |  | Patent Issued. They don't issue the flags |
| 4 |  | anymore, as far as I know. |
| 5 | Q | Are you a named inventor on any patents other than |
| 6 |  | the unified shader patents? |
| 7 | A | Yes. |
| 8 | Q | How many other patents approximately? |
| 9 | A | Do you count all of the derivatives and -- because |
| 10 |  | for example, this patent, which we -- the initial |
| 11 |  | patent was the '871, then it turned into the |
| 12 |  | 486 -- the '846. It turned into another number |
| 13 |  | here, the '454. So what -- |
| 14 | Q | So if we broadly classify all of the ones that |
| 15 |  | share the '871 specification -- |
| 16 | A | As one? |
| 17 | Q | -- as the unified shader patents, are you a named |
| 18 |  | inventor on any other patents? |
| 19 | A | Yes. Quite a few of them. |
| 20 | Q | Have any of them been involved in litigation? |
| 21 | A | I'm not typically aware, but I can say that at |
| 22 |  | least another one of mine was involved in |
| 23 |  | litigation because I was deposed on it by |
| 24 |  | Mr. Nese. It was the patent -- let me find the |
| 25 |  | actual. |

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| :---: | :---: | :---: |
|  |  | I believe, if my memory serves, I think it |
| 2 |  | was the patent, as stated here on Exhibit 4, page |
| 3 |  | 3, the 7,742,053 patent. And I can go into the |
| 4 |  | deposition to make sure and to -- let me just |
| 5 |  | check that actually. |
| 6 | Q | Any other patents that you know of that you were a |
| 7 |  | named inventor on that have been in litigation |
| 8 |  | other than the ' 053 patent? |
| 9 |  | MR. RENAUD: Objection. |
| 10 | A | I only got deposed on that one other patent. I am |
| 11 |  | not -- I don't know if there is any other |
| 12 |  | litigation or otherwise on the other patents that |
| 13 |  | I have been named inventor on. |
| 14 | Q | When you first talked to Steve Morein about using |
| 15 |  | unified shader in the R400, did you think it was a |
| 16 |  | surprising idea to use a unified shader? |
| 17 |  | MR. RENAUD: Objection. |
| 18 | A | It was definitely new. I mean, that was the first |
| 19 |  | time that anybody would be trying to do something |
| 20 |  | like that, and actually, even inside AMD it caused |
| 21 |  | a lot of friction as to whether or not it was a |
| 22 |  | good idea or not, at the inception. |
| 23 | Q | Why? |
| 24 | A | Because it was so novel and so unusual basically. |
| 25 | Q | What were the down sides? |

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MR. RENAUD: Objection.
A So I mean the things I learned during the break were based on discussions with Pam and Dave Christie, not with counsel. Counsel was in the room, but $I$ did the discussion and I did the learning, and I looked at the specification. And I don't mean to cut you off, but $I$ believe earlier your counsel mentioned, when we were talking about your other conversations when Pam and/or David was involved, they were with the legal department and it was at the direction of counsel, is that correct? I just don't want to push you into a place where you're breaching a privilege.

MR. RENAUD: Yeah, let's put it simply. I allowed a lot of latitude to explore what was done to collect documents and to enhance his awareness today.

MR. ELENGOLD: During the break.
MR. RENAUD: During the break, but there are things that both Dave and Pam do that are privileged and confidential. Shouldn't say privileged and confidential. Privileged or work product.

In this instance, I made the decision that

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| 1 |  | Page 255 |
| :---: | :---: | :---: |
|  |  | document, and it does provide a view of the |
| 2 |  | Perforce depot, but not an exhaustive view, but I |
| 3 |  | was also made aware by Dave and Pam that there |
| 4 |  | were many more documents submitted that were |
| 5 |  | outside of the Perforce depot, such as the test |
| 6 |  | logs, the test names, the source code -- well, |
| 7 |  | actually, the source code was in the depot, but it |
| 8 |  | got provided in various snaps, presentations which |
| 9 |  | were not in the directories that I described in my |
| 10 |  | Exhibit 6 testimony, as well as all of the IKOS |
| 11 |  | initiative, which is definitely not in that |
| 12 |  | testimony. |
| 13 | Q | So I believe you've now testified about all those |
| 14 |  | things, correct? |
| 15 | A | Well, to the extent -- |
| 16 | Q | Is there anything else that we haven't talked |
| 17 |  | about today that you would like to add to |
| 18 |  | supplement your testimony? |
| 19 | A | There is probably way more, yes. There is a |
| 20 |  | wealth of documents, and I can't remember them |
| 21 |  | all. I mean, if you want to talk about them, I |
| 22 |  | know that there's hundreds and hundreds of |
| 23 |  | documents that were provided. There's also |
| 24 |  | hundreds and hundreds of people at AMD that worked |
| 25 |  | on the R400 project. So -- |

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```
    talk to, to get additional information to
    supplement your testimony today?
        MR. RENAUD: Objection.
A There's hundreds and hundreds of people at AMD
        that worked on this program, so you know, we can
        talk to each and every one of them. They would
        probably have each their own view of what occurred
        at any of these dates. You know, at this point, I
        could talk to everyone that was involved and that
        probably would help me, but in the interest of
        time, do you really want to do this? I mean --
            MR. ELENGOLD: Okay. Let's go off the
        record.
            MR. RENAUD: Sure.
            VIDEO OPERATOR: The time is 5:38 p.m.
        We're off the record.
                                (Off the record.)
            VIDEO OPERATOR: The time is 5:53 p.m.
        We're back on the record.
Q I'm going to hand the witness Exhibit No. 15.
            (Document marked Exhibit 15 for
        identification.)
    Q Mr. Lefebvre, have you seen this document before?
    A I don't remember having seen this document before,
        no.
```

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|  |  | Page 258 |
| :---: | :---: | :---: |
| 1 | Q | Do you know what Exhibit 15 is? |
| 2 | A | Can you point me to it? I mean where is it - |
| 3 | Q | Sure, if you look at the title, and if you read |
| 4 |  | the title into the record, that might help. |
| 5 | A | Yeah, okay. Complainants Advanced Micro Devices, |
| 6 |  | Inc. and ATI Technologies ULC's First Supplemental |
| 7 |  | Responses and Objections to Respondents LG and |
| 8 |  | Vizio's First set of Joint Interrogatories (Nos. |
| 9 |  | 5-8, 12, 18, 34, 49, 51-52, 55, 65-66, 70-71. |
| 10 | Q | Do you know what that means? |
| 11 | A | Talks about joint interrogatories, but further |
| 12 |  | than that -- |
| 13 | Q | Do you know what an interrogatory is? |
| 14 | A | Not really. Can you educate me? |
| 15 | Q | Sure. You were designated today on topic 86 which |
| 16 |  | is just respondent's -- responses, complainants' |
| 17 |  | responses, so ATI and AMD's responses to discovery |
| 18 |  | requests, written discovery from LG and the other |
| 19 |  | respondents, and so $I$ just wanted to ask you a |
| 20 |  | couple quick questions about this document |
| 21 |  | which -- let's try, if you can turn to page 95, |
| 22 |  | I'm going to ask you to look at Interrogatory |
| 23 |  | number 49. |
| 24 |  | Again, you are only designated, my |
| 25 |  | understanding is, this topic with regard to your |

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| 1 |  | Page 259 |
| :---: | :---: | :---: |
|  |  | other topics; so conception, reduction to |
| 2 |  | practice. |
| 3 | A | Okay. What part of the -- |
| 4 | Q | Look at Interrogatory number 49, do you see that? |
| 5 | A | Yes, I see that. |
| 6 | Q | And you're welcome to read it. But my question is |
| 7 |  | going to be, do you understand Interrogatory |
| 8 |  | number 49 to be asking for the information |
| 9 |  | regarding conception and reduction to practice for |
| 10 |  | the patents that are at issue in this case? |
| 11 | A | Okay. I read through it. |
| 12 | Q | Can you look at the response on pages, bottom of |
| 13 |  | page 96 and top of 97 which says, Response No. 49, |
| 14 |  | and then in parentheses (6/5/2017). I think you |
| 15 |  | just said you read that. Do you see that this is |
| 16 |  | the most recent response to Interrogatory number |
| 17 |  | 49? |
| 18 | A | So 6/5, okay. I did not read that paragraph, so |
| 19 |  | can I read that paragraph? |
| 20 | Q | Absolutely. Response no. 49. |
| 21 | A | You want me to read it out loud? |
| 22 | Q | No, you can just read it to yourself. |
| 23 | A | Okay. |
| 24 |  | Okay. I read through it. |
| 25 | Q | Okay, do you understand that response to be an |

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| 1 | A | Okay. |
| :---: | :---: | :---: |
| 2 | Q | Do you understand the Response no. 52 to be |
| 3 |  | accurate and complete? |
| 4 | A | I can't really comment on, again, on the |
| 5 |  | completeness of all this not knowing what is being |
| 6 |  | discussed here. It's way too summarized for me to |
| 7 |  | provide any kind of opinion. |
| 8 | Q | And you didn't do any preparation to testify today |
| 9 |  | with regard to those responses, is that correct? |
| 10 | A | Well, I mean, I prepared for today's testimony as |
| 11 |  | far as the steps or the amount of work that went |
| 12 |  | in on the R 400 to prove that it was, you know, |
| 13 |  | diligently working and trying to make a product |
| 14 |  | for a date, and talked about, you know, various |
| 15 |  | people which we discussed; Dave Christie and Pam |
| 16 |  | Horn, and reviewed the Perforce logs, the |
| 17 |  | documents. So this is the, the preparation that I |
| 18 |  | did for this, right. |
| 19 | Q | I meant specific to these discovery responses, did |
| 20 |  | you do any preparation to testify on those today? |
| 21 | A | I don't know what these are, so no. |
| 22 | Q | So if I represent to you that this is the most |
| 23 |  | recent set of discovery responses that we've |
| 24 |  | received from AMD and ATI, which is Exhibit 15, so |
| 25 |  | for Interrogatory number 49, 51 and 52, you have |

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| :---: | :---: | :---: |
|  |  | no reason to doubt that AMD and ATI's responses |
| 2 |  | are wrong, right, or I'm sorry, you have no reason |
| 3 |  | to doubt that they're accurate and correct, right? |
| 4 |  | MR. RENAUD: Objection. |
| 5 | A | These response -- I mean, I can't tell what these |
| 6 |  | are, so I mean, unless you put in front of me what |
| 7 |  | these documents are, and I can look at them, I |
| 8 |  | can't formulate an opinion either way. I don't |
| 9 |  | know what this is. |
| 10 | Q | Well, these are the documents that AMD and ATI |
| 11 |  | have represented that that list are relevant to |
| 12 |  | these topics as of today or, you know, until they |
| 13 |  | supplement it again, so as of 6/5/17. My question |
| 14 |  | was, do you understand or do you have any reason |
| 15 |  | to believe that these are incorrect, these |
| 16 |  | responses? |
| 17 |  | MR. RENAUD: Objection. |
| 18 | A | Well, I mean, if they were provided by AMD, and |
| 19 |  | you know, counsel reviewed them and appended them |
| 20 |  | to this document, I don't have any reason to |
| 21 |  | believe these are not correct and accurate, but I |
| 22 |  | really want to state that I have no idea what |
| 23 |  | these are, so I can't really formulate a personal |
| 24 |  | opinion on this. I mean, I'm relying on AMD and |
| 25 |  | counsel. |

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|  | Page 267 |
| :---: | :---: |
| 1 | addressed, we're happy to have that conversation. |
| 2 | MR. ELENGOLD: Well, that's my question, is |
| 3 | I don't know that it's necessary because again, I |
| 4 | think we have a complete record based on what has |
| 5 | been put in to date. I guess my point again is |
| 6 | just that, to the extent that we're trying to keep |
| 7 | it to seven hours, I'm just noting for the record |
| 8 | that we're doing that, and we're doing that in |
| 9 | light of your request and the parties' agreement |
| 10 | to do that with individual deponents, but you |
| 11 | know, again, I think you're mischaracterizing |
| 12 | things quite a bit there, but I appreciate if you |
| 13 | want to represent there was no change in |
| 14 | testimony, I think that's fine, and I'm happy to, |
| 15 | you know, let that go and we both said our piece. |
| 16 | MR. RENAUD: Okay. We're happy to take it |
| 17 | up off the record. Thank you. |
| 18 | VIDEO OPERATOR: The time is 6:08 p.m. This |
| 19 | concludes the deposition of Laurent Lefebvre. |
| 20 | We're off the record. |
| 21 | (Whereupon the deposition concluded at |
| 22 | 6:08 p.m.) |
| 23 |  |
| 24 |  |
| 25 |  |

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1
2
2 Laurent Lefebvre
INSTRUCTIONS TO THE WITNESS
    Please read your deposition over
    carefully and make any necessary corrections.
    You should state the reason in the
    appropriate space on the errata sheet for any
    corrections that are made.
    After doing so, please sign the errata
    sheet and date it.
    You are signing same subject to the
    changes you have noted on the errata sheet,
    which will be attached to your deposition.
    It is imperative that you return the
    original errata sheet to the deposing
    attorney within thirty (30) days of receipt
    of the deposition transcript by you. If you
    fail to do so, the deposition transcript may
    be deemed to be accurate and may be used in
    court.
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                                    In The Matter Of Certain Graphics Systems v.
                                    Laurent Lefebvre
                                    ERRATA
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Laurent Lefebvre
ACKNOWLEDGMENT OF DEPONENT
I,

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\(\qquad\)
``` , do
    hereby certify that I have read the foregoing
    pages and that the same is a correct
    transcription of the answers given by
    me to the questions therein propounded,
    except for the corrections or changes in form
    or substance, if any, noted in the attached
    Errata Sheet.
    ___-______
    DATE
    S IGNATURE
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| A | activity 201:4 | 240:23 | 16:15,17 18:4 | 3:13 |
| :---: | :---: | :---: | :---: | :---: |
| a.m 1:23 5:6 59:22 | 213:16 | agree 51:23 181:25 | 19:1 20:3,22 | AMD1044_0011. |
| 59:25 | acts | 183:23 | 24:14 28:3,6,7,11 | 193:1 - |
| A12 131:2,9,9,16 | actual 40:10 43:5 | agreed 182:16 | 28:15,22 29:24 | MD1044_0011... |
| 131:18 | 47:13 72:20 | Agreeing 182:2 | 31:17,20 37:10 | 204:16 |
| ability 9:9 268:10 | 92:10 99:14,19 | agreement 39:20 | 37:17,22 38:6,15 | AMD1044_0011... |
| able 22:25 69:15 | 99:24 123:6 | 39:21,23,24 40:3 | 39:6,8,11,18 40:5 | 204:1 |
| 99:1 100:19 | 128:8,9,20 | 266:1 267:9 | 40:16 48:14 | MD1044_0011... |
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| 138:7 143:15 | 184:4 212:21 | 184:24 210:5 | 57:3 100:16 | MD1044_0012... |
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| accelerated 10:16 | add 61:4 170 | alleged 17 | 135:25 136:23 | 86:1 |
| accent 140:21 | 252:23 254:19 | allow 25:22 45:23 | 139:13 144:18 | AMD1044_0175... |
| access 143:14,18 | 255 | 72: | 150:5 157:5 | 127:5 |
| 143:19 243:17 | addition 220:23 | allowed 9 | 168:12 175:21 | MD1044_0175 |
| access | additional 37:18 | 143:22 163 | 179:17 181:17 | 128:8 191:2 |
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