R400 Program Review

Marlborough – October 10, 2002

ATI Corporate Presentation

IP – Virage HD

- Virage is under control for now
- 2.14 bit cell is out; 2.8 bit cell is in the HD memories
  - Compilers are ready because of prior customer
  - Larger RAM and it will consume more power
  - Cells design rules are less aggressive
  - Cell is not approved at TSMC, but does not appear to be a formality
  - Test chip is in the October Shuttle, but we will not see silicon till January
  - Some customization to the compiler need to be made

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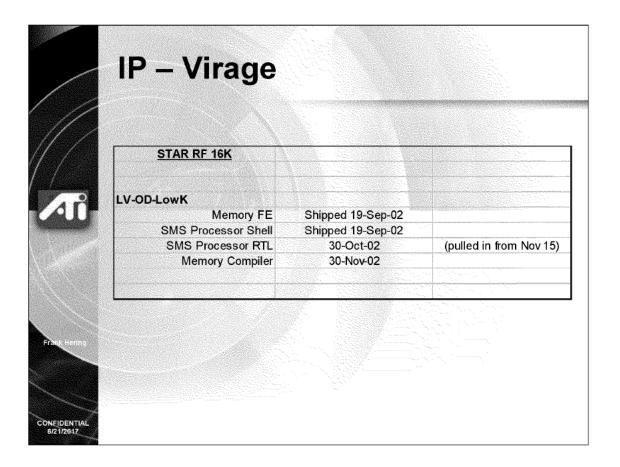6/21/2017

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IP – Virage RF

- Virage has delivered the logical views of the register file and fuse box.
- The Processor still has issues with the test and repair modes, but works in normal modes.
- Design team is beginning to enter the system into the Verilog
- We are still having issues with the compiler, but they seem to be addressed
- Virage is here tomorrow and we will review what our implementation
- Now need deal with the test and laser interface.

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IP – Virage

STAR RF 16K		
LV-OD-LowK		
Memory FE	Shipped 19-Sep-02	
SMS Processor Shell	Shipped 19-Sep-02	
SMS Processor RTL	30-Oct-02	(pulled in from Nov 15)
Memory Compiler	30-Nov-02	

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IP – Analog

- Work has started with Toronto team to make small modifications to the cell.
- MPLL should work at 600Mhz, but 700Mhz is scary.
- Thermal Sensor was over designed to nearly a medical instrument. Going to larger increment cause the design to half its area.
- TVDAC board muxing is the path we are going and adding a pin to control the chip.

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