```
Change 140380 on 2003/12/31 by vromaker@vromaker_r400_linux_marlboro

- fix for dropped real_time flag: moved export_pos bit into the "flags" field
  (it was using a bit that was set aside for the extra_in field)

Change 140350 on 2003/12/31 by rramsey@rramsey_xenos_linux_orl

Fix a bug that was allowing the texconst mem to be written when full (no phys addr
available)

Change 140331 on 2003/12/31 by mearl@mearl_xenos_linux_orl

Fixed bug; was using thread type instead of fetch type.

Change 140330 on 2003/12/31 by tien@tien_r500_emu

Bug fix for sec dim calcs

Change 140316 on 2003/12/31 by mmantor@FL_mmantorLT_r400_win

<special build with a sq_alu.h provided by tom to address dot lsb mismatches>

Change 140313 on 2003/12/31 by jcarroll@jcarroll_r400_win

added latest status; picked new test

Change 140284 on 2003/12/30 by dclifton@dclifton_xenos_linux_orl

Fixed scalar MOVA_FLOOR opcode;

Change 140270 on 2003/12/30 by danh@danh_r400_win

Status update.

Change 140266 on 2003/12/30 by smoss@smoss_crayola_linux_orl_regress

   changes for simple_register_indirect test (register read)

Change 140247 on 2003/12/30 by vbhatia@vbhatia_r400_linux_marlboro

Reverted fetch multisample test clamp, for the Team believes that it might be best to
support it

Change 140219 on 2003/12/30 by mdesai@mdesai_r400_linux

       During tfetch, using msb of texel_offset_pre

Change 140218 on 2003/12/30 by vbhatia@vbhatia_r400_linux_marlboro
```

Optimised away fetch multi sample tests to be overridded as tfetches, not supported

Change 140205 on 2003/12/30 by rramsey@RRAMSEY_P4_r400_win

update test status, pick another one

Change 140203 on 2003/12/30 by danh@danh_r400_win

Status update.

Change 140180 on 2003/12/30 by vbhatia@vbhatia_r400_linux_marlboro

Added clamp so as to test only point sampling when doing vertex fetches

Change 140174 on 2003/12/30 by rramsey@RRAMSEY_P4_r400_win

update status

Change 140155 on 2003/12/30 by rramsey@RRAMSEY_P4_r400_win

update with 12/30 regression results

Change 140117 on 2003/12/30 by danh@danh_r400_win

Status update.

Change 140102 on 2003/12/30 by mmantor@FL_mmantorLT_r400_win

<special build with sq_alu.h#79 for debug>

Change 140051 on 2003/12/29 by mearl@mearl_r400_win

update status

Change 140050 on 2003/12/29 by vromaker@vromaker_r400_linux_marlboro

status update - emulator fix was made for scalar const opcodes

Change 140036 on 2003/12/29 by jcarroll@jcarroll_r400_win

Updated jcarroll status

Change 139967 on 2003/12/29 by tien@tien_r400_devel_marlboro

Added another delay on compare to mirror added pipestage in RTL

Change 139957 on 2003/12/29 by tien@tien_r500_emu

```
Recoded log pitches going to TCF for better timing
Closing GetBorderColorFraction bug .. verified tests passing
Added stage to tp_addresser and refreshed .bvrls to be safe (tp_parameters dependency)

Change 139909 on 2003/12/28 by mmantor@mmantor_xenos_linux_orl

<timing fixes>

Change 139836 on 2003/12/24 by jayw@jayw_r400_linux_marlboro

Depth code clean up part 1/38103.  Fix for ignoring SX1 rtr.  Non-hiz depth still has
bug with expansion shown by rare gc r400rb_zwave failures.

Change 139795 on 2003/12/23 by danh@danh_r400_win

Status update.

Change 139793 on 2003/12/23 by vbhatia@vbhatia_r400_linux_marlboro

Added clamp for no lod grad when vertex fetches

Change 139789 on 2003/12/23 by mdesai@mdesai_r400_linux

       Fixed Addresser random test genRand11 (large denorms with offsets)

Change 139383 on 2003/12/23 by ctaylor@ctaylor_xenos_linux_orl

       Fixed bug in control flow sequencer where when thread was put back onto thread
buffer due to alloc cfi, the no-serialize bit was being taken from bit 40 of the cfs
opcode instead of the execute state machine opcode so it was the right bit from the
wrong instruction.  Things have been working mostly due to the fact that bit 40 of most
of the other CFI opcodes is reserved and therefore 0.

Change 139373 on 2003/12/23 by llefebvr@llefebvr_r400_emu_montreal

updated status for SX->PA missmatches.

Change 139356 on 2003/12/23 by bhankins@bhankins_xenos_linux_orl

Move some assignments out of process where they shouldn't be.  No functional change.

Change 139338 on 2003/12/23 by vromaker@vromaker_r400_linux_marlboro

- fix for scalar const ops: y and x swizzle fields used for gpr address bits [5:4]
  and [3:2] were swapped

Change 139327 on 2003/12/23 by rramsey@rramsey_xenos_linux_orl
```

```
add simd_id to sp_out mismatch message
make sx_rb_color tracker multi-threaded per sx/rb interface

Change 139310 on 2003/12/23 by vromaker@vromaker_r400_linux_marlboro

status update - took another test

Change 139296 on 2003/12/23 by tien@tien_r500_emu

Fixed GetBorderColorFraction DATA_FORMAT override

Change 139280 on 2003/12/23 by rmanapat@rmanapat_r400_release

Fix for bug 3126

Change 139223 on 2003/12/22 by llefebvr@llefebvr_r400_emu_montreal

Now working on SX->PA missmatches.

Change 139193 on 2003/12/22 by rramsey@RRAMSEY_P4_r400_win

update status

Change 139142 on 2003/12/22 by llefebvr@llefebvr_r400_emu_montreal

The SX->RB tracker is bad. Added a comment to explain the situation.

Change 139097 on 2003/12/22 by ctaylor@ctaylor_xenos_linux_orl

Fixed bug related to clamping of GPR addresses which are out of range.  Old code
clamped to absolute zero instead of the base for the current thread.

Change 139066 on 2003/12/22 by bhankins@bhankins_xenos_linux_orl

Add tbtrk_sx_bc_quad tracker (C1 version only)

Change 139057 on 2003/12/22 by rramsey@RRAMSEY_P4_r400_win

update more tests, pick another one

Change 139050 on 2003/12/22 by rramsey@RRAMSEY_P4_r400_win

Update with new regression results, pick a test

Change 139045 on 2003/12/22 by rramsey@rramsey_xenos_linux_orl

Fix phasing of thread_count in sq_ais_output.
```

```
Fix o_gprsm_busy from sq_vtx_ctl and change thread counter to only
reset on RST_VTX_CNT event.

Change 139044 on 2003/12/22 by bhankins@bhankins_xenos_linux_orl

Initial add to r400 branch

Change 138986 on 2003/12/20 by mmantor@mmantor_xenos_linux_orl

<changed csim to only make one pass for param gen and gen index and write the dump
files correctly, fixed a timing loop in pix tthread buffer >

Change 138964 on 2003/12/20 by donaldl@donaldl_xenos_linux_orl

Redundancy bug fixes --
1. Added RSP output muxes to TP_SP_data_valid[3:0] in tp_output.v.
2. Created I/O port TPC_TP_simd_id[1:0].  Needed so simd_id lines up
   with TP outputs going to SPs and RSP.

Change 138960 on 2003/12/20 by bhankins@bhankins_xenos_linux_orl

Forgot to make the same change to the BC1 side.  Has no affect on r400 version.

Change 138958 on 2003/12/20 by bhankins@bhankins_xenos_linux_orl

fix miswiring of quad_x and quad_y outputs of detailed quad fifo

Change 138921 on 2003/12/19 by tien@tien_r400_devel_marlboro

Man if this breaks anything I'll freak.
Changed the format_comp_* mux control for data_format=61 (FMT_...AS_1_1_1_1)

Change 138662 on 2003/12/19 by mearl@mearl_r400_win

update status

Change 138650 on 2003/12/19 by danh@danh_r400_win

Status update.

Change 138647 on 2003/12/19 by bhankins@bhankins_xenos_linux_orl

Add include of sx_defines.v.  No affect on r400 version.

Change 138609 on 2003/12/19 by tien@tien_r500_emu

Fixes location of ANISO_BIAS and DIM fields in emu and rtl
Closing out GetWeights bug, which I fixed last checkin
```

```
Change 138588 on 2003/12/19 by vromaker@vromaker_r400_linux_marlboro

- fixed a copy-paste error in the new code that generates src_c_sel for scalar const
ops

Change 138586 on 2003/12/19 by mearl@mearl_r400_win

update status

Change 138585 on 2003/12/19 by mearl@mearl_xenos_linux_orl

Fixed bug in tracker.

Change 138491 on 2003/12/18 by llefebvr@llefebvr_r400_emu_montreal

I'll leave the _const_add test to Vic since he is working on it with Dan. I'll focus
instead on coissue_frac_01.

Change 138489 on 2003/12/18 by mearl@mearl_r400_win

update status

Change 138486 on 2003/12/18 by danh@danh_r400_win

Status update.

Change 138469 on 2003/12/18 by cbrennan@cbrennan_r400_release

Try again to make a better performing miss_stall.

Change 138467 on 2003/12/18 by bhankins@bhankins_xenos_linux_orl

Increase detailed quad fifo skid size to account for input pipeline.  Only affects C1
version.

Change 138455 on 2003/12/18 by mearl@mearl_r400_win

update status

Change 138414 on 2003/12/18 by tien@tien_r400_devel_marlboro

Timing fix in tp_lod_aniso: put tri_juice in parallel with min/max clamp
  went from -0.3 to +0.4 slack coming out of MC (tp_lod_aniso)
GetWeights fix (tp_tsel)
Connected to vertex state bits properly (tp_lod_fifo/tp_input)

Change 138380 on 2003/12/18 by mearl@mearl_xenos_linux_orl
```

Updated the tracker to open all streams so a false PASS does not occur.

Change 138375 on 2003/12/18 by jayw@jayw_r400_linux_marlboro

Fix for hiz failures. Wrong hiz calculated. For Allen.

Change 138369 on 2003/12/18 by kevino@kevino_r400_release

      tcb_fetch_gen_walker timing fix

Change 138309 on 2003/12/18 by danh@danh_r400_win

Status update.

Change 138307 on 2003/12/18 by bhankins@bhankins_xenos_linux_orl

fix the way export memory is read in C1 mode

Change 138289 on 2003/12/17 by rramsey@rramsey_xenos_linux_orl

Fix a bug with pred_override that can occur when a clause starts
with two predicated alu instructions. pred_override needs to use
the isr version of the pred bits in this case because the pred register
can't be intit'ed until after the the last instr of the prev clause has
a chance to return its pred values and push them back to the thread buffer.
This fixes r400sc_sp_sample_cntl_47 and hopefully many more.

Change 138288 on 2003/12/17 by vromaker@vromaker_r400_linux_marlboro

- fix for scalar const opcodes: src_c_sel and gpr_read_en logic was updated

Change 138266 on 2003/12/17 by vbhatia@vbhatia_r400_linux_marlboro

       Standalone addresser testbench updates

Change 138212 on 2003/12/17 by mearl@mearl_r400_win

update status

Change 138152 on 2003/12/17 by danh@danh_r400_win

Status Update.

Change 138138 on 2003/12/17 by bhankins@bhankins_xenos_linux_orl

1. Modify detailed quad fifo to keep mrt quads and mem export quads together
2. Change NEW_BC defines to C1

```
Change 138120 on 2003/12/17 by mearl@mearl_xenos_linux_orl

Added ability to track exports that are not ordered.

Change 138119 on 2003/12/17 by cbrennan@cbrennan_r400_emu

Change to miss stall generation that may increase perf in worst latency case by about
5% up to 10%.
Basically after a miss stall cycle, the next stall is calculated off of more accurate
info which may let it go sooner.

Change 138105 on 2003/12/17 by mdesai@mdesai_r400_linux

       Resolved all hardware issues on bug3077.
       Fixed Y & Z overflow case

Change 138087 on 2003/12/17 by rramsey@RRAMSEY_P4_r400_win

latest regression status

Change 138053 on 2003/12/17 by chammer@chammer_r400_linux

Changed XENOS flag to C1 to correspond to the other blocks

Change 137864 on 2003/12/16 by rramsey@rramsey_xenos_linux_orl

Change emulator so param cache reads for params not exported by the VS
still show up in sq_sx_pcaddr.
Fix cf_resource_change logic in the cfs so it catches the clause boundary
where a cf instr with only tex instr gets sent to the alu cfs.

Change 137839 on 2003/12/16 by amys@amys_xenos_linux_orl

fix read_vc_cntl signal

Change 137833 on 2003/12/16 by vromaker@vromaker_r400_linux_marlboro

changed OR to AND on rb rtr inputs of sx_rb_if module

Change 137805 on 2003/12/16 by smoss@smoss_crayola_linux_orl_regress

   warnings for r400 too.

Change 137787 on 2003/12/16 by rmanapat@rmanapat_r400_release

Fix for bug3106
```

```
Change 137773 on 2003/12/16 by vromaker@vromaker_r400_linux_marlboro

- fixed a predicate override bug: pred_overide is driven from the done bits if
  the previous operation was a waterfall, but it must only be driven for the first
  instruction following a waterfall.  The bug occurred on back-to-back waterfalls
  where the pred_override was being driven for all cycles of the second waterfall.
- this fix caused r400sq_gpr_index_01 to pass

Change 137753 on 2003/12/16 by danh@danh_r400_win

Status update.

Change 137701 on 2003/12/15 by rramsey@rramsey_xenos_linux_orl

Add new _sf (single-file) versions of PLI routines that allow trackers
to only open their dump files one time.
Modify a few trackers and models to use the new _sf routines to verify
they are working.
Fix a problem with the cfsm not ignoring clause boundaries for unexecuted
predicate control flow instr.

Change 137604 on 2003/12/15 by dclifton@dclifton_xenos_linux_orl

Fixed scalar RSQ and RCP clamp to zero for -0 input.
Fixed scalar MUL clamp to one for exponent overflow.
Fixed scalar MUL sign on exponent underflow.
Fixed scalar FRACT for 1 < x < 2.
Fixed scalar FRACT for X all integer.
Fixed scalar SUB with shift of 24.
Fixed scalar ADD with clamp and exp underflow.
Fixed scalar SIN sign with input 0.
Enabled adder in sp_macc for vector PRED_SET ops.
Fixed more CUBE face_id cases in sp_comp_opcodes with ma = -0.
Fixed PRED_SETGT and PRED_SETGE conditions in sp_macc32 to account for nans.
Redefined data flow in sp_macc32 for PRED_SET ops.
Enabled denorms and -0 pass-thru in sp_macc32 on DST op.
Forced clearing of mantisa and sign in sp_macc32 for CUBE ma result.

Change 137569 on 2003/12/15 by donaldl@donaldl_xenos_linux_orl

Removed dependency of bp[15:0] bits on vc-to-sp valid bits.  Done so can
still track SP data even when the RSP is used during redundancy testing.

Change 137568 on 2003/12/15 by tien@tien_r400_devel_marlboro

Expanded gen100/101 for aniso testbench
Put in fix for Get/Set opcodes to completely match EMU...
  including don't care fields
```

Change 137566 on 2003/12/15 by donaldl@donaldl_xenos_linux_orl

Added tracker for RSP to SX data.

Change 137563 on 2003/12/15 by donaldl@donaldl_xenos_linux_orl

Fixed sensitivity list bug.

Change 137560 on 2003/12/15 by danh@danh_r400_win

Updated status.

Change 137474 on 2003/12/15 by hartogs@fl_hartogs_xenos_win

Integrated changes for addition of "VGT_MH_pglb_clear" from Xenos to R400.

Change 137470 on 2003/12/15 by rmanapat@rmanapat_r400_sun_marlboro

Changes for TCF, TCR, TCM chicken registers

Change 137425 on 2003/12/15 by cbrennan@cbrennan_r400_release

Changed ifndef to ifdef+else because v2k doesnt work in some environments.

Change 137415 on 2003/12/15 by jcarroll@jcarroll_r400_win

Picked tests

Change 137401 on 2003/12/15 by rramsey@RRAMSEY_P4_r400_win

update with weekend's results

Change 137386 on 2003/12/15 by mmantor@mmantor_xenos_linux_orl

<synchronize sx0 and sx1 paths to the rb's for xenos ordering within a tile>

Change 137363 on 2003/12/13 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 137313 on 2003/12/12 by mmantor@FL_mmantorLT_r400_win

<update for standalone vp test>

Change 137238 on 2003/12/12 by vromaker@vromaker_r400_linux_marlboro

took a few more tests

```
Change 137212 on 2003/12/12 by tien@tien_r400_devel_marlboro

Fix to sign determination for dni input sub (need to XOR sign of
       add result into input sign)
Enhancements to the deriv/aniso testbenches

Change 137206 on 2003/12/12 by cbrennan@cbrennan_r400_release

Revert this optimization..   Its too generous sometimes and causes a hang.  If it makes
any material difference a much more timing messy optimization could be put in place.

Change 137205 on 2003/12/12 by mearl@mearl_r400_win

updated status

Change 137203 on 2003/12/12 by kevino@kevino_r400_release

       Switched over to the low lat fifos in tca, fetch fifo , and tcd.
       Added tcd_ipbuf_fifo_top.v and switched overe to using 2 16x141 mems instead a 1
32x141 mems.
       Put latency params in for latency fifo prog depth testcases

Change 137188 on 2003/12/12 by rramsey@RRAMSEY_P4_r400_win

update with latest regression results

Change 137182 on 2003/12/12 by smburu@smburu_r400_linux_marlboro

Fix for 16_EXPAND border_color.

Change 137166 on 2003/12/12 by vromaker@vromaker_r400_linux_marlboro

- increased the depth of the sq-vc request fifo; this is a temporary fix while the
  mini and mega dec signals from the VC are added to the vc_rp_sp dump file

Change 137165 on 2003/12/12 by mearl@mearl_r400_win

updated status

Change 137146 on 2003/12/12 by vromaker@vromaker_r400_linux_marlboro

updated status

Change 137128 on 2003/12/12 by kevino@kevino_r400_release

       Removed extra debug fifo that was causing problems.
```

```
Change 137115 on 2003/12/12 by bhankins@bhankins_xenos_linux_orl

1. fix some bugs in sx-bc interface
   2. remove obsolete, commented code
   3. start to add support for grouping quads to bc

Change 137114 on 2003/12/12 by dclifton@dclifton_xenos_linux_orl

Fixed clamp on scalar LOG(inf).
Fixed sign on scalar RECIP(-inf) w/o clamp.
Fixed scalar FRACT of large negative (integer) nums
Fixed CUBE in sp_macc32 and sp_comp_opcodes with Y max at -0.
Fixed DST with -0 for output as w or z.

Change 137105 on 2003/12/12 by mmantor@mmantor_xenos_linux_orl

<fixed bug in the emu for redundancy control, added new input to the sq called
sx_sp_alloc_table_free  >

Change 137104 on 2003/12/12 by mmantor@mmantor_xenos_linux_orl

<This changed changed SQ and SX top level ports by added thread_type from sq_alloc
through the sx so tracker at sx_rb works correct and fixed some other minor bugs>

Change 137099 on 2003/12/12 by jayw@jayw_r400_linux_marlboro

For Allen and Rex; fixes for depth and increased quad FIFO depth.

Change 137079 on 2003/12/11 by mmantor@FL_mmantorLT_r400_win

<updated for Laurent's cube changes>

Change 137041 on 2003/12/11 by cbrennan@cbrennan_r400_release

Tiny cleanup of miss_stall condition.  Might save a cycle or two over a long test.

Change 137030 on 2003/12/11 by cbrennan@cbrennan_r400_emu

Flipped nibble order of DXT3A_AS_1_1_1_1 to really match dx spec this time.

Change 136926 on 2003/12/11 by cbrennan@cbrennan_r400_release

Changed C1 to map MCs to requestors differently than R400
Increased the length of the mh arb fifos from 8 to 24.

Change 136917 on 2003/12/11 by mearl@mearl_r400_win

updated status
```

```
Change 136910 on 2003/12/11 by bhankins@bhankins_xenos_linux_orl

Fix logic that adds hook for a write of a quad event/null indicator to the detailed
quad fifo.

Change 136909 on 2003/12/11 by dclifton@dclifton_xenos_linux_orl

Fixed scalar FRACT of negative all-integer number.
Fixed MOVA in sp_comp_opcodes to work like MAX.
Fixed MIN(0,0) in sp_comp_opcodes
Fixed CUBE in sp_comp_opcodes for ma = nan or inf

Change 136893 on 2003/12/11 by mearl@mearl_r400_win

updated status

Change 136888 on 2003/12/11 by bhankins@bhankins_xenos_linux_orl

Change defined "C1" switch to "NEW_BC" in sx rtl and related vcpp files

Change 136887 on 2003/12/11 by vhopkins@vhopkins_xenos_linux_orl

   added test_plusargs for deactivation of fsdb

Change 136871 on 2003/12/11 by mearl@mearl_r400_win

updated status

Change 136867 on 2003/12/11 by rramsey@rramsey_xenos_linux_orl

don't reset current_context at eo_rt load

Change 136854 on 2003/12/11 by dclifton@dclifton_xenos_linux_orl

Fix to sp_macc32 max clamp
Fix to sp_macc32 MULADD produce_ati_nan logic.
Fix to sp_macc32 TRUNC and FLOOR -denorms.
Fix to sp_comp_opcodes MIN(0,denorm)

Change 136832 on 2003/12/10 by mmantor@FL_mmantorLT_r400_win

<added all ops and provide pred opcode swizzle changes and kill in the standalone
vectpipetest>

Change 136805 on 2003/12/10 by kmeekins@kmeekins_xenos_linux_orl

Corrected logic that use to take advantage of the implied channel.
```

```
Change 136794 on 2003/12/10 by kmeekins@kmeekins_xenos_linux_orl

Added compile directives to make Xenos channel selection changes specific only
  to Xenos.

Change 136782 on 2003/12/10 by kmeekins@kmeekins_xenos_linux_orl

Changed the channel selection from bit 6 to bit 7 of the fetch address.

Change 136773 on 2003/12/10 by danh@danh_r400_win

Updated status.

Change 136758 on 2003/12/10 by bhankins@bhankins_xenos_linux_orl

fix ifdef/endif mismatch

Change 136749 on 2003/12/10 by smburu@smburu_C1_synth

Changed the reset going to TPC to be the hard reset.

Change 136733 on 2003/12/10 by dclifton@dclifton_xenos_linux_orl

Fixed FLOOR and FRACT of negative denorms.
Fixed 0*inf + -inf on MULADD

Change 136727 on 2003/12/10 by mmantor@FL_mmantorLT_r400_win

<added all vector ops>

Change 136713 on 2003/12/10 by vromaker@vromaker_r400_linux_marlboro

updated status

Change 136691 on 2003/12/10 by bhankins@bhankins_xenos_linux_orl

   1. Add ability for both r400 and xenos versions of sx to coexist
   2. Rewrite memory read mux select logic in sx_bc_if.v for better synthesis
   3. Add quad_x and quad_y signals to BC interface.
   4. Update 'copy_virage_' files to reflect memory updates
   5. Change 'ENABLE_SX_TO_BC' compile switch to 'C1'
   6. Remove obsolete code (sx_export_buffers_common.v logic is now in sx_rb_if.v)
   7. Update virage .cnt files

Change 136682 on 2003/12/10 by kevino@kevino_r400_release

       Added low latency fifo controllers to some fifos,  but have disabled them with
```

```
ifdefs until the controller works for all cases.   Added programmable depth for latency
fifos along with corresponding test cases

Change 136672 on 2003/12/10 by mearl@mearl_r400_win

updated status

Change 136616 on 2003/12/10 by dclifton@dclifton_xenos_linux_orl

Scalar compare ops getting ati nan if opposite sign inf input.
Scalar compare ops always output b input with nan input.
Removed mantissa clear on zero for scalar inputs.
Fixed scalar MAX(-0, 0);
Fixed scalar MAX(x, inf);
Fixed vector MIN
Fixed vector FLOOR, neg x > -1
Fixed inf and nan detect on dot product
Fixed ati nan for MULADD -inf + +inf
Fixed MULADD for 0 * inf or nan
Fixed final vector clamp logic

Change 136596 on 2003/12/09 by vromaker@vromaker_r400_linux_marlboro

- added a couple wire names for ppb read data in cfs
- added fsdb dump for tbtrk_sq_vtx_rs_input in tb_sqsp
- changed checking of predicate to registered version in above trk to fix false
mismatch
- bit 95 of vc/tp instruction was wired to 0 causing a mismatch, so
  I changed it to the actual instruction bit 95 (which is only used by the sq)

Change 136589 on 2003/12/09 by donaldl@donaldl_xenos_linux_orl

Bug fix - connected parameter cache write data from output of SX redundancy
input muxes (as opposed to directly from SP input registers).

Change 136574 on 2003/12/09 by danh@danh_r400_win

Updated r400sc_rts_* status

Change 136557 on 2003/12/09 by mmantor@mmantor_xenos_linux_orl

<fixed allocation counter for ea and cleaned up controls for rest of the counters and
fixed a bug in the spi_sp tracker by removing delay on sq_sp_simd_id because of
pipelining the vertex and pixel input data>

Change 136555 on 2003/12/09 by mmantor@FL_mmantorLT_r400_win

add VectPipeTest that test the vector pipe of the sp.
```

```
Change 136470 on 2003/12/09 by cbrennan@cbrennan_r400_emu

Fix a perfmon counter. Wasnt paying attention to the stall signal.

Change 136457 on 2003/12/09 by georgev@devel_georgev_r400_lin2_marlboro_coverage_tc

Put under perforce control.

Change 136442 on 2003/12/09 by kmeekins@kmeekins_xenos_linux_orl

randvc.pl
  ----------
  Created script for running random tests on the VC and recording the results.

  runvc
  ----------
  Corrected incomplete test detection.

Change 136424 on 2003/12/09 by mearl@mearl_r400_win

update status

Change 136403 on 2003/12/09 by jayw@jayw_r400_linux_marlboro

Fix for Rex performance fifo resizing!

Change 136398 on 2003/12/09 by rmanapat@rmanapat_r400_release

More changes to get the soft reset wire correctly

Change 136395 on 2003/12/09 by amys@amys_xenos_linux_orl

connect w0 output registers correctly

Change 136391 on 2003/12/09 by mmantor@FL_mmantorLT_r400_win

<src special swizz moved to the sq>

Change 136358 on 2003/12/09 by vromaker@vromaker_r400_linux_marlboro

updated status for r400sq_auto_wrapping_memories_01 (test issue)

Change 136336 on 2003/12/09 by smburu@smburu_C1_synth

Extraneous comma in module port list.

Change 136334 on 2003/12/09 by rramsey@RRAMSEY_P4_r400_win
```

update dot2add status, take more tests

Change 136332 on 2003/12/09 by mmantor@FL_mmantorLT_r400_win

<took test with >2 exports>

Change 136330 on 2003/12/09 by rmanapat@rmanapat_r400_release

Wired in soft reset for tcf tcr and tcm following the way Tien
did it for the tpc and tp

Change 136326 on 2003/12/09 by mearl@mearl_r400_win

took a few tests

Change 136235 on 2003/12/08 by cbrennan@cbrennan_r400_emu

Make fix for X's in comparitors for small rectangle shaped textures for mipmapped
stacks and cubes.

Change 136192 on 2003/12/08 by mearl@mearl_r400_win

Removed more SC pipe disable tests.

Change 136174 on 2003/12/08 by danh@danh_r400_win

Updated r400sc_* status

Change 136166 on 2003/12/08 by llefebvr@llefebvre_laptop_r400_emu

working on r400sp_coissue_add_01.cpp

Change 136158 on 2003/12/08 by mearl@mearl_xenos_linux_orl

IFDEFed ports TM1 and TM2 for XENOS.

Change 136153 on 2003/12/08 by vromaker@vromaker_r400_linux_marlboro

added my name by a few tests

Change 136141 on 2003/12/08 by mearl@mearl_r400_win

Removed pipe disable tests, renamed and moved to the ROM block

Change 136135 on 2003/12/08 by rramsey@rramsey_xenos_linux_orl

Add a bit to pix thread counter to handle larger thread buffer.

```
Change 136107 on 2003/12/08 by georgev@devel_georgev_r400_lin2_marlboro_coverage_tc

Streamlined TC for current directory.

Change 136102 on 2003/12/08 by rramsey@RRAMSEY_P4_r400_win

update 'sorted by type' page with latest results

Change 136070 on 2003/12/08 by dclifton@dclifton_xenos_linux_orl

Fixes to pass denorms on max or compare ops

Change 136063 on 2003/12/08 by mmantor@mmantor_xenos_linux_orl

<another synthesis issue>

Change 136048 on 2003/12/08 by mmantor@FL_mmantorLT_r400_win

<update for more ops>

Change 135995 on 2003/12/08 by danh@danh_r400_win

Updated r400sc_sp_sample_cntl* status

Change 135990 on 2003/12/08 by mmantor@FL_mmantorLT_r400_win

<added executable for vectorpipe test bench vector generation>

Change 135987 on 2003/12/08 by rramsey@RRAMSEY_P4_r400_win

update with status from 12/8/2003

Change 135984 on 2003/12/08 by mmantor@FL_mmantorLT_r400_win

<update for tb_vector>

Change 135983 on 2003/12/08 by dclifton@dclifton_r400

Updated for new sq rams

Change 135978 on 2003/12/08 by dclifton@dclifton_xenos_linux_orl

Fixed clamp of scalar mul with overflow.
Fixed trunc of neg numbers |x| < 1.
Reworked scalar fract of numbers |x| > 1.

Change 135975 on 2003/12/08 by mmantor@mmantor_xenos_linux_orl
```

```
<fixed leda errors for synthesis>

Change 135943 on 2003/12/07 by vromaker@vromaker_r400_linux_marlboro

- connected resource management register to thread buffers
  (programmable thread buffer size)
- fixed typo and leda error in sq_vtx_ctl

Change 135932 on 2003/12/07 by rramsey@rramsey_xenos_linux_orl

fix a problem with vizq_start events and how they cause state locks in the tb.
this should fix the vgt_event tests

Change 135879 on 2003/12/05 by mmantor@mmantor_xenos_linux_orl

<fixed a synthesis problem during elaboration in the sq_input_arb.v and fixed a problem
with redunancy so that both vertex and pixel input controllers would send simd_id with
there respective request to the spi.  This change renamed a top level port between the
sq and sp sq_sp_interp_simd_id changed to sq_sp_simd_id >

Change 135795 on 2003/12/05 by rmanapat@rmanapat_r400_release

Fixes a bug related to src address and l2sets and fetch3d

Change 135747 on 2003/12/05 by vbhatia@vbhatia_r400_linux_marlboro

       Added support for TP_Track_DisplayLog to suppress display logging in default
case
       for diskspace usage reasons.

Change 135715 on 2003/12/05 by mearl@mearl_xenos_linux_orl

Fixed a bug in the multi-pass logic.

Change 135678 on 2003/12/05 by kmeekins@kmeekins_xenos_linux_orl

buildtb
  tbasrt_rg.v
  -----------
  Added assertion testing for the RG.

  runvc
  -----------
  - Added more testing for incomplete tests
  - Collect the runvc command line arguments and write them to the FAIL file
    on failing tests.
  - Moving .dmp files from the random directory to the test directory to assist
```

```
    in file clean-up on passing tests.

  vc.v
  ------------
  Changed I/O definitions to prevent erroneous mis-compares in netlist generation
scripts.

  vcrg.cpp
  vcrg.v
  vcrg_tag_gen.v
  --------------
  Added exception logic to handle vertex buffer size of zero.

Change 135600 on 2003/12/05 by bhankins@bhankins_xenos_linux_orl

   1. add behavioral support for sx to bc interface.  Disabled.
   2. fixed bug in alloc/dealloc block to hold off resetting alloc bit until the last
bank of memory is read for a particular address.
   3. fixed bug in alloc/dealloc block where free logic was searching all 256 locations
of the buffer when only 128 are enabled.
   4. connect SX_SQ_free_export_address_buf to indicate last quad of memory export has
been created and written to the detailed quad fifo.
   5. fix minor bug in sx-rb interface logic that would have shown up with larger
export buffer.

Change 135598 on 2003/12/05 by smoss@smoss_crayola_linux_orl_regress

   removed reference to internal tracker

Change 135590 on 2003/12/05 by dclifton@dclifton_r400

Update for new rams

Change 135584 on 2003/12/05 by rramsey@rramsey_xenos_linux_orl

absolute address mode (const_addr_mode = 3'b001) should apply to all src constants

Change 135537 on 2003/12/04 by vromaker@vromaker_r400_linux_marlboro

- increased size of thread buffers: vtx from 16 to 32 threads, pix from 48 to 64 thread
- fixed gpr dealloc bug that resulted in reduced performance
- testbench and tracker changes were made to support the larger number of threads
- emualtor change (separate checkin) was also made for the bigger thread buffers

Change 135506 on 2003/12/04 by tien@tien_r500_emu

Added soft reset by OR-ing in with the sync'd version of hard reset
         (Timing issue? It adds and or to the tree of buffers on the reset)
```

```
       Not soft reset are:
         tp_register
  tp_perfmon_wrappper
         tp_cg
         tp_rf_stp
       and the equivalent tpc blocks
       TPC still only requires a hard recent from tcf
Refreshed the Makefiles.

Change 135471 on 2003/12/04 by viviana@viviana_xenos_linux_orl

Deleted old memories.

Change 135468 on 2003/12/04 by viviana@viviana_xenos_linux_orl

Memories replacing 10x96 and 12x104.

Change 135466 on 2003/12/04 by viviana@viviana_xenos_linux_orl

New PA memories.

Change 135460 on 2003/12/04 by dclifton@dclifton_xenos_linux_orl

Changed ram-based pipelines to prevent simultaneous read/write of same location.

Change 135435 on 2003/12/04 by cbrennan@cbrennan_r400_emu

Changed padding rules to always pad 32x32x4 on top of the 256Bytex1x1 for linear.  This
was to allow for bordersize=1 and mip packing when calculating mip offsets and
face/stack/3d slice offsets.

Change 135412 on 2003/12/04 by mdesai@mdesai_r400_linux

       Fixed bug3064, part I, adding offset causes texture int overflow
       Fixed bug in genRand11s, calculation of msb in texture_int_pre

Change 135403 on 2003/12/04 by mearl@mearl_xenos_linux_orl

Fixed a port bug for RT trackers.

Change 135392 on 2003/12/04 by dclifton@dclifton_xenos_linux_orl

Fix for cube with negative zero input vector.

Change 135347 on 2003/12/04 by mearl@mearl_xenos_linux_orl

Xenos specific change to take out the scan and test ports.
       In Xenos, they are defined at SC_A (SC, HZ) hierarchy level.
```

```
Change 135257 on 2003/12/04 by bhankins@bhankins_xenos_linux_orl

increase the tracker quad storage fifo depth to accomodate the larger color export
buffer

Change 135241 on 2003/12/04 by bhankins@bhankins_xenos_linux_orl

Fix bad checkin

Change 135238 on 2003/12/04 by dclifton@dclifton_xenos_linux_orl

Removed bits 1 and 0 of ROM_PIPE_SEL from I/O since they aren't used.

Change 135234 on 2003/12/04 by mmantor@mmantor_xenos_linux_orl

<1. wired simd2 and simd3 pipe_disable_vtx for proper vertex steering with 2 and 3
simds.
    2. Improved usaged of gpr input (Interp/Vtx data) port by pipline the vtx input
controller
       data and changing input arbiter.  Still need to make a changed in sq_pix_ctl to
remove
       busy signal on last 4clockcycle so interleaving can be tighter and in both
machines load
       to the thread buffer sooner once commmitted.
    3. changed SIMD2_PRESENT_TMP to SIMD2_PRESENT in sq code, still needs to be removed
from
       tb_sqsp and check other parts of the design such as the sp and rsp.>

Change 135151 on 2003/12/03 by mearl@mearl_xenos_linux_orl

Took out the SC_SP_last_quad signal from the top of the SC
         and SPI.

Change 135088 on 2003/12/03 by rramsey@rramsey_xenos_linux_orl

Add a unique vc/tp update for pending bits to the thread status regs
so they don't clobber each other.
Don't compare fetch constants for VC mini_fetches.
Change tex_instr_seq so fetch type (vc/tp) is determined based on the fetch opcode
rather than thread type.
Fix a problem in sx_export_control when a pos free_done happened on the same clk as a
pos_dec when exporting aux vectors.

Change 135061 on 2003/12/03 by jayw@jayw_r400_linux_marlboro

Fixed a minor issue with RBRC TB.
```

Change 135056 on 2003/12/03 by cbrennan@cbrennan_r400_emu

Cleaned up interface to tex_baddr_gen to facilitate a clean testbench.

Change 135037 on 2003/12/03 by bhankins@bhankins_xenos_linux_orl

fix signals that are checked

Change 135031 on 2003/12/03 by dclifton@dclifton_xenos_linux_orl

Fixed clamp on sin/cos.
Fixed sin(-0)
Fixed 0*Nan on dst.

Change 135028 on 2003/12/03 by bhankins@bhankins_xenos_linux_orl

fix how the index_op bit is obtained from the rb quad index to accomodate both 8 and 9
bit versions

Change 134965 on 2003/12/03 by rmanapat@rmanapat_r400_release

Fix that prevents height being shifted to 0x0 as it is adjusted
for a given mip level

Change 134866 on 2003/12/02 by donaldl@donaldl_xenos_linux_orl

Removed RB_SX0_quad_rtr and RB_SX1_quad_rtr as qualifiers for GetVec routines
(ie. only use SX0_RB_quad_send and SX1_RB_quad_send).

Change 134834 on 2003/12/02 by mdesai@mdesai_r400_linux

	Fixed Bordersize 1x1x1 mode

Change 134833 on 2003/12/02 by mdesai@mdesai_r400_linux

	Fixed Bordersize cases with 1x1x1 sizes.

Change 134818 on 2003/12/02 by llefebvr@llefebvr_r400_linux_marlboro

Now using the sq_aiq_bX_rts signal to drive the alu active counter. It used to be
driven by ais_busy which was also high when doing TP and VC fetches.

Change 134798 on 2003/12/02 by smburu@smburu_r400_linux_marlboro

Missing signals in sensitivity list.

Change 134797 on 2003/12/02 by smburu@smburu_r400_linux_marlboro

```
Fixed some tcr_register pins that were tied as "=0"; this was
causing synthesis problems.

Change 134796 on 2003/12/02 by donaldl@donaldl_xenos_linux_orl

Changed MC clock period and I/O delays to better meet synthesis timing.

Change 134768 on 2003/12/02 by dclifton@dclifton_xenos_linux_orl

Fixed problem with pass through of denorms on compare ops

Change 134699 on 2003/12/02 by mearl@mearl_xenos_linux_orl

1) Timing fixes.
            sc_packer.v
       2) Updated the real-time stream trackers and turned them on.
            sc_interp.cpp
            out_compare.v
            sc_defines.v
            tb_sc.v
            tbtrk_sc.v

Change 134697 on 2003/12/02 by smburu@smburu_xenos_netlist

Removed extra comma that appears when C1 is defined.

Change 134664 on 2003/12/02 by cbrennan@cbrennan_r400_release

Changed base addr gen and mh addr gen to happen in parallel to reduce latency and area.
 needs syn file changes to go with.

Change 134661 on 2003/12/02 by dclifton@dclifton_xenos_linux_orl

Fixed typo on new RETAIN_PREV opcode definition

Change 134660 on 2003/12/02 by dclifton@dclifton_xenos_linux_orl

 Fixed problem with clamp on infinity.

Change 134658 on 2003/12/02 by kevino@kevino_r400_release

       Fetch gen walker performance fix.   Note that some new modules were added and a
couple old ones removed.

Change 134653 on 2003/12/02 by bhankins@bhankins_xenos_linux_orl

- replace rf implementation of the quad buffer fifo from the sc with an implememtation
using hs ram
```

```
   - add new star processor to support hs ram

Change 134631 on 2003/12/02 by bhankins@bhankins_xenos_linux_orl

1. Fix wiring of high speed memory to star processor.
   2. Add high speed memory clock to pa test bench

Change 134573 on 2003/12/01 by smoss@smoss_crayola_linux_orl_regress

   removed random seed for the moment until I can get ncverilog happy again

Change 134460 on 2003/12/01 by smoss@smoss_crayola_linux_orl_regress

   removed bad path for sx_defines.v

Change 134411 on 2003/12/01 by kmeekins@kmeekins_xenos_linux_orl

Corrected the signal scforce port width for the Xenos build.

Change 134408 on 2003/12/01 by rramsey@rramsey_xenos_linux_orl

Fix HI/LO instruction split

Change 134404 on 2003/12/01 by bhankins@bhankins_xenos_linux_orl

   1. Added SX_INDEX_SIZE and SX_INDEX_SIZE_EQ_8 defines to the rtl, defined in
sx_defines.v and set equal t
   2. Moved sx_defines.v to parts_lib/src/common
   3. Renamed sx inputs that connect to the STAR processors to match the names in the
TST module

Change 134359 on 2003/11/30 by mmantor@mmantor_xenos_linux_orl

<removed delay in/outs from tb_sqsp>

Change 134302 on 2003/11/28 by mmantor@mmantor_xenos_linux_orl

<remove delay chain from sq>

Change 134278 on 2003/11/27 by jayw@jayw_r400_linux_marlboro

Fixed alpha for 1555 SINT format.

Change 134185 on 2003/11/26 by kmeekins@kmeekins_xenos_linux_orl

- Corrected logic for determining the invalidation window.
  - Edge detected the start of the invalidation cycle to prevent back-to-back
  invalidation cycles off the same start.
```

```
  - Moved the timing of the mux select for RAM invalidate commands.

Change 134180 on 2003/11/26 by kmeekins@kmeekins_xenos_linux_orl

runvc
  -------
  - Removed redundant shader pipe options. These are now automatically invoked
  unless explicitly disabled.
  - Changed the sim only option to accept a random seed to duplicate the block
  level testing performed by the test team.

  tb_vc.v
  --------
  Added logic to the FSDB dumping commands to automatically accommodate dump files
  larger than 2 Meg.

Change 134175 on 2003/11/26 by tien@tien_r400_devel_marlboro

Standalone testbench stuff

Change 134171 on 2003/11/26 by georgev@devel_georgev_r400_lin2_marlboro_coverage_tc

Updated script for tp and tc testbenches.

Change 134131 on 2003/11/26 by cbrennan@cbrennan_r400_emu

Fix stacks with bordersize=1.

Change 134126 on 2003/11/26 by donaldl@donaldl_xenos_linux_orl

Updated tbmod_fake_rb to create multiple file pointers based on thread_id[5:0] and
thread_type.  Needed because the quad_index[7:0] can come in out of order from the
SX.  The quad_index[7:0] and op bit are stored in a fifo and eventually sent back
to the SX.

Change 134100 on 2003/11/26 by donaldl@donaldl_xenos_linux_orl

Removed pred_kill_type and pred_kill_valid input signals since no longer used.
(ie. they are being delayed internally.

Change 133962 on 2003/11/25 by hartogs@fl_hartogs2

Changed emulator so that the simd counter resets in the same ways as the RTL (based on
a change in the number of pipes and specifically on a change in the pipe diable bits).
Also changed the RTL so that the pipe disable stuff is on a global clock.

Change 133920 on 2003/11/25 by tien@tien_r400_devel_marlboro
```

```
ifdef'd the delay chain out for C1

Change 133886 on 2003/11/25 by cbrennan@cbrennan_r400_emu

Removed delay chains for C1.

Change 133877 on 2003/11/25 by cbrennan@cbrennan_r400_emu

Cleaned up ports for C1.

Change 133855 on 2003/11/25 by mdesai@mdesai_r400_linux

        Fixed bug3014 & genRand11 issues with large exponents and offsets

Change 133853 on 2003/11/25 by mdesai@mdesai_r400_linux

        Fixed genRand11 issues with large exponents and offsets

Change 133852 on 2003/11/25 by mdesai@mdesai_r400_linux

        Fixed bug3014
        Fixed genRand11 cases (large exponents with offsets)

Change 133819 on 2003/11/25 by bhankins@bhankins_xenos_linux_orl

Add sx rf Virage files to perforce

Change 133815 on 2003/11/25 by bhankins@bhankins_xenos_linux_orl

Increase depth of color buffer to 256.  Only the first 128 locations are enabled for
now.

Change 133814 on 2003/11/25 by dclifton@dclifton_xenos_linux_orl

New RETAIN_PREV opcode replaces previous scalar stall for 3 operand vector ops.

Change 133755 on 2003/11/24 by jayw@jayw_r400_linux_marlboro

Changes to fix Alan's Fast Color Clear issue and to pave the way for more SX storage.

Change 133716 on 2003/11/24 by kmeekins@kmeekins_xenos_linux_orl

Replaced RTL memory models with the gate level versions.
  Added hooks for ncVerilog code coverage.

Change 133710 on 2003/11/24 by kmeekins@kmeekins_xenos_linux_orl

- Rewrote the vcmi_requestor.v to replace the single request FIFO with four FIFOs,
```

```
    one for each even/odd, 0/1 request.
  - Changed the performance monitor to monitior the new FIFO signals.
  - Removed old files no longer needed.
  - Corrected the sim build script to reference the correct files.
  - Corrected the register spec to reflect the new performance signals.

Change 133588 on 2003/11/24 by dclifton@dclifton_r400

Removed delay chain I/O from SP's

Change 133584 on 2003/11/24 by dclifton@dclifton_xenos_linux_orl

Changes to handle nans and infs in cube opcode.  Effects all compare ops.

Change 133582 on 2003/11/24 by dclifton@dclifton_xenos_linux_orl

Removed delay chains

Change 133580 on 2003/11/24 by chammer@chammer_r400_linux

 Fixed sc_quad_pair_proc internal tracker after removing zmask needed port.

Change 133568 on 2003/11/24 by chammer@chammer_r400_linux

Removal of sc_detail_accum block modified internal trackers.

Change 133461 on 2003/11/21 by kevino@kevino_r400_release

       Modified channel mask tests to put color in register than make sure texture
channel doens't overwrite it when masked out.  This way, the exported color has all
channels defined.

Change 133449 on 2003/11/21 by mmantor@mmantor_xenos_linux_orl

<Connected Parameter Cache register file input to the i/o register instead of the input
pins and pipe delayed write control >

Change 133426 on 2003/11/21 by smburu@smburu_r400_linux_marlboro

Fix for packed-formats border color.

Change 133425 on 2003/11/21 by chammer@chammer_xenos_linux_orl

Removed detail_mask_accum block.

Change 133300 on 2003/11/21 by vromaker@vromaker_r400_linux_marlboro

timing fix - stopped using any unregistered status read bits
```

```
Change 133296 on 2003/11/21 by tien@tien_r400_devel_marlboro

Put some noise on the reg grad/lod when not in use.

Change 133284 on 2003/11/21 by bhankins@bhankins_xenos_linux_orl

- remove delay chain from pa and vgt, and associated test benches

Change 133275 on 2003/11/21 by mearl@mearl_xenos_linux_orl

1. Took out delay chain in the SC and SC_B blocks.
            chip_sc.tree
            chip_sc_b.tree
            sc.v
            sc_b.v
            tb_sqsp_sc_iter.v
       2. Timing related changes.
            sc_packer.v
            sc_packer_pkg.v
       3. Real-Time tracker changes
            sc_block_model.cpp
            sc_interp.cpp
            sc_types.h
            out_compare.v
            tb_sc.v
            tbtrk_sc.v

Change 133264 on 2003/11/21 by bhankins@bhankins_xenos_linux_orl

1. Restructured sx to have an sx-rb interface block sx_rb_if, readying it for
      a similar sx_bc_if block for xenos.
   2. Removed delay chain
   3. Changed input quad fifo to dum_mem for now.
   4. Removed some unused signals.
   5. Changed pav.tree per Vivian's request to change test signal name.

Change 133221 on 2003/11/20 by tien@tien_r400_devel_marlboro

Resolved the lod_aniso_test testbench file
Fix for tp_opcodes GetWeights case

Change 133204 on 2003/11/20 by vbhatia@vbhatia_r400_linux_marlboro

       Updated interface dump bit width for the higher precision gradients
       (16 to 17 bit change, ie 5 bit exponent to 6 bit exponent)

Change 133191 on 2003/11/20 by rmanapat@rmanapat_r400_release
```

```
Had to update sensetivity list

Change 133094 on 2003/11/20 by tien@tien_r400_devel_marlboro

LOD gradient precision boost

Change 133084 on 2003/11/20 by bhankins@bhankins_xenos_linux_orl

Undid an inadvertent change that caused the tracker not to mask out compares of
uninitialized data

Change 133078 on 2003/11/20 by jayw@jayw_r400_linux_marlboro

Work to paramaterized in order to fix 16 bit URF.

Change 133076 on 2003/11/20 by cbrennan@cbrennan_r400_emu

Fix for stacks with border size set.

Change 133032 on 2003/11/20 by mdesai@mdesai_r400_linux

Fixed bug 2977
       Fixed large denorm coordinates

Change 133031 on 2003/11/20 by mdesai@mdesai_r400_linux

       Fixed bug 2977
       Fixed denorm coordinates (very large) by setting the texture_int to 2.

Change 133026 on 2003/11/20 by dclifton@dclifton_xenos_linux_orl

Optimizations for area:
Removed duplicate scalar_data register from sp_macc_gpr.
Removed 2-1 mux for scalar constant_address data from sp_macc--mux scalar
input data in sp_vector instead.

Change 133018 on 2003/11/20 by bhankins@bhankins_xenos_linux_orl

add scripts that fetch memory files

Change 133016 on 2003/11/20 by bhankins@bhankins_xenos_linux_orl

   1. Replace pa_cl_vte_out_orig_fifo memory with 24-deep.
   2. Change ccgen_to_clipcc and clipcode fifos to 24 deep.
   2. Increase pa_cl_vgt_to_clipp_fifo depth to 2K using 1kx56 hs memory and
pa_fifo_ctrl_mempl module.
   3  Remove old rf memory.
```

```
   4. Add test i/o, processor and fusebox for hs memory.
   5. Update tb_pa.v to accomodate new pa test i/o.

Change 132954 on 2003/11/19 by kevino@kevino_r400_release

      Several fixes for emu errors (mostly timeouts) in tp_multitexture_02_stress.
      Change to tcb_fetch_generator to make TF_PIPE1 a wire instead of a parameter.
Apparently synthesis has some difficulty with characterizing multiple instantiations of
the same module with different parameters.

Change 132940 on 2003/11/19 by georgev@devel_georgev_r400_lin2_marlboro_coverage

First revision.

Change 132934 on 2003/11/19 by rmanapat@rmanapat_r400_release

Pipeline fix

Change 132916 on 2003/11/19 by viviana@viviana_xenos_linux_orl

Memory model submitted for simulation.

Change 132904 on 2003/11/19 by vbhatia@vbhatia_r400_linux_marlboro

       Created a superset of the tp and vc testbenches, to deal with coverage tool
limitation,
       Also created a script to run various tests in parallel rather than in series.

Change 132894 on 2003/11/19 by rramsey@rramsey_xenos_linux_orl

Fix SQ_VC dec signals in tb_sqsp.
Change tbtrk_sqvc so it does not compare fetch addr for mini fetches.
Fix problem in tex_instr_seq that was allowing mini fetches to start
out of phase.
Add more info to msgs from pcdata tracker to tell which set of pc data
is mismatching. Also turn off sx1 compare since it is redundant now that
all the sx data comes from usx_0.

Change 132867 on 2003/11/19 by cbrennan@cbrennan_r400_emu

Fixed precision errors on stack maps.  Removed redundant code in addresser.  Updated rg
file with passing tests. DOWN TO 10!

Change 132864 on 2003/11/19 by bhankins@bhankins_xenos_linux_orl

delete obsolete files

Change 132853 on 2003/11/19 by cbrennan@cbrennan_r400_emu
```

```
Added two more stages to tp_addresser_test delay to match hw.

Change 132848 on 2003/11/19 by kevino@kevino_r400_release

      Added some error check signals to fetch_gen_out in an ifdef SIM.    Fixed some
dangling wires that were making it to the top of TCR in the C1 version of the tc.

Change 132842 on 2003/11/19 by chammer@chammer_xenos_linux_orl

Added changes for Xenos, enabled with `define XENOS
 Includes new rb_id, edram copy mode, zplane changes.

Change 132781 on 2003/11/19 by dclifton@dclifton_xenos_linux_orl

Duplicated clock gaters in sp.v for test.
Force_m12_zero forces in3_gte_in12 high in sp_macc32 (makes 'x' * 0 consistently 0)
Fixed sensitivity list for pv_SrcCNegate and pv_SrcCAbs in sp_macc.
Created scalar stall for three operand vector ops in sp_macc to preserve previous
scalar.

Change 132699 on 2003/11/18 by smburu@smburu_r400_linux_marlboro

Border color Gamma fixes for RTL and EMU.

Change 132698 on 2003/11/18 by kevino@kevino_r400_release

      Additional agp perf fix.   Fixed typo in .rg file

Change 132675 on 2003/11/18 by danh@danh_xenos_linux_orl

Added the tbtrk_sq_sx_pcaddr tracker.

Change 132667 on 2003/11/18 by danh@danh_xenos_linux_orl

Initial Release.

Change 132649 on 2003/11/18 by vromaker@vromaker_r400_linux_marlboro

- alu_instr_seq timing fixes for constant store read: first the register stage
  on the offset was moved after the sum2 adder; then the init_done_bits signal
  was changed from a combinational ACS state machine output to a registered
  one-bit state machine output to help the path to the new sum2 register
- thread buff status read timing fix - moved the status read back one cycle by
  sending the unregistered, rotated request vector to the arbiter and registering
  the winner out of the arbiter; the output of the status read mux was
  then registered
```

```
Change 132595 on 2003/11/18 by mdesai@mdesai_r400_linux

Fixed random bug (2972) (Hardware used the wrong sign to generate the cc_inv)

Change 132557 on 2003/11/18 by bhankins@bhankins_xenos_linux_orl

Back up to revision #22 to allow non-export-to-memory tests to pass for now.

Change 132516 on 2003/11/18 by rramsey@rramsey_xenos_linux_orl

Add a mova test to the sq regression.
Change no_inc in pix_ctl to use sr version instead of nxt value
out of the ppb.
Fix instr base calc in rbbm_if so rt/nrt determination is correct.
Stop vec_grp tracker from comparing pix auto_count cycles.

Change 132450 on 2003/11/17 by kevino@kevino_r400_release

   Fix for agp that was introduced in earlier agp perf change.

Change 132421 on 2003/11/17 by tien@tien_r500_emu

Fix for MPEG (non-interlaced) failures

Change 132391 on 2003/11/17 by georgev@devel_georgev_r400_lin2_marlboro_tott

Took these memories out of coverage.

Change 132344 on 2003/11/17 by georgev@devel_georgev_r400_lin2_marlboro_tott

Removed from code coverage.

Change 132310 on 2003/11/17 by kevino@kevino_r400_release

     AGP performance fix.   Instead of letting bottom bits of address select which
TC_MH interface the AGP request goes out on, base it on which pipe the request is in.
This should divide requests between the two interfaces more evenly for a variety of
cases.

Change 132283 on 2003/11/17 by smburu@smburu_r400_linux_marlboro

2 Extra stages in tp_addresser for timing reasons.

Change 132281 on 2003/11/17 by smburu@smburu_r400_linux_marlboro

2 Extra pipe stages in tp_addresser for timing reasons.

Change 132259 on 2003/11/17 by mdesai@mdesai_r400_linux
```

```
Fixed most bordersize cases
Fixed texture_to_texel_coordinates to treat exp=96 as normal rather than exp_big case

Change 132246 on 2003/11/17 by dclifton@dclifton_xenos_linux_orl

Swapped X and Y terms on cube compare to match rasterizer.  Fixed inf input on scalar
add.  Fixed a_eq_neg_b for denorm adds.

Change 132236 on 2003/11/17 by bhankins@bhankins_xenos_linux_orl

Increase size of bank_avail_quads_to_free to 8 bits to accomodate a value of 128.

Change 132219 on 2003/11/16 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 132130 on 2003/11/14 by vbhatia@vbhatia_r400_linux_marlboro

       update of stack_map test

Change 132123 on 2003/11/14 by rramsey@rramsey_xenos_linux_orl

Fix a bug in aluconst_mem related to rt constant reads.
Fix const_map_cntl so deallocate_cnt gets updated correctly when alloc and
context_done happen on same clk.
tb_sqsp was missing some primitive boundaries in the pkr for RT prims.

Change 132082 on 2003/11/14 by vbhatia@vbhatia_r400_linux_marlboro

       Added stack_map tests for increased coverage

Change 132067 on 2003/11/14 by rmanapat@rmanapat_r400_release

Modified files for codecoverage

Change 132030 on 2003/11/14 by jayw@jayw_r400_linux_marlboro_syn

Added 96x128 for Dan Harmon, for IKOS.

Change 132011 on 2003/11/14 by vbhatia@vbhatia_r400_linux_marlboro

       Removed tp_track_formatter.v vrom dependencies, no longer needed

Change 131955 on 2003/11/14 by kmeekins@kmeekins_xenos_linux_orl

- Increased the L2 FIFOs from a max depth of 64 to 256.
  - Rewired the patchin and patchout signals to the memories.
```

```
  - Modified the register spec to have a larger programmable
    depth range for the L2 FIFO.
  - Changed the gc and chip builds to use the real memory models.

Change 131910 on 2003/11/13 by vbhatia@vbhatia_r400_linux_marlboro

       Added DumpHeaders option in trackers and level of viewing options in the
       result viewing script

Change 131866 on 2003/11/13 by jayw@jayw_r400_linux_marlboro_syn

New files per Dan Harmon's request for gc level simulation.

Change 131826 on 2003/11/13 by rramsey@rramsey_xenos_linux_orl

get rid of ifndefs so vcs will compile

Change 131814 on 2003/11/13 by dclifton@dclifton_xenos_linux_orl

Added register for undriven signal

Change 131810 on 2003/11/13 by tien@tien_r500_emu

Optimized data_formats that have been previously encoded away

Change 131801 on 2003/11/13 by jayw@jayw_r400_linux_marlboro

Fixes for shader pixel kills and alpha-test pixel kills.

Change 131764 on 2003/11/13 by dclifton@dclifton_xenos_linux_orl

Fixed inf feedback on dot product.

Change 131761 on 2003/11/13 by smburu@smburu_r400_linux_marlboro

Hicolor optimizations for unused logic.

Change 131722 on 2003/11/13 by rramsey@rramsey_xenos_linux_orl

Add capability to dump Cadence shm instead of fsdb. Enabled by defining
DUMP_SHM in tb_sqsp/vcsopts.f file

Change 131689 on 2003/11/12 by vbhatia@vbhatia_r400_linux_marlboro

       Updates towards automatic compares

Change 131670 on 2003/11/12 by dclifton@dclifton_xenos_linux_orl
```

```
Fixed sign on recip_ff(-0) with clamp.
Fixed ma output on cube with x = -y.
Fixed nan interference with mul_prev2 on max with clamp.

Change 131659 on 2003/11/12 by cbrennan@cbrennan_r400_emu

Changed MH perfmon counters to only count tc requests instead of including VC.

Change 131650 on 2003/11/12 by vbhatia@vbhatia_r400_linux_marlboro

       Update to fix texture temporary input file tracking, and added a script
       To simplify life for automatic comparisions.

Change 131613 on 2003/11/12 by cbrennan@cbrennan_r400_emu

Create a tcd source address for fmt 00 and 01 2d tiled.  Fixes bug 2781

Change 131611 on 2003/11/12 by georgev@devel_georgev_r400_lin2_marlboro_coverage

Removed $display from coverage.

Change 131537 on 2003/11/12 by llefebvr@llefebvr_r400_linux_marlboro

1) added register stage to line up pred_override bits with SP phase
2) made the waterfall/predicated override an or instead of an and.

Change 131468 on 2003/11/11 by vbhatia@vbhatia_r400_linux_marlboro

       update of dumping to exactly match emulator for these tp subblock trackers

Change 131465 on 2003/11/11 by donaldl@donaldl_xenos_linux_orl

When in the VS_EVENT state and going to IDLE, update d_sp_sel[3:0] as a default
based on disable_vtx_3,2,1,0 instead of 0.  This is to fix a bug where the correct
o_sp_vsr_valid bit was not being set because the disable simd flags were not being
considered (when going from VS_EVENT to IDLE).

Change 131449 on 2003/11/11 by mearl@mearl_xenos_linux_orl

Bug fixes for 2 primitive interpolation.

Change 131364 on 2003/11/11 by vbhatia@vbhatia_r400_linux_marlboro

updated sub-block trackers

Change 131241 on 2003/11/11 by kmeekins@kmeekins_xenos_linux_orl

Removed event window from VC counters.
```

```
Change 131174 on 2003/11/10 by mearl@mearl_xenos_linux_orl

Fixed 2 bugs with two primitive interpolation.

Change 131148 on 2003/11/10 by jayw@jayw_r400_linux_marlboro3

Fix for when SC_BC has to send a killed tile.

Change 131103 on 2003/11/10 by smburu@smburu_xenos_netlist

Some changes to wireloads.

Change 131096 on 2003/11/10 by smburu@smburu_r400_linux_marlboro

Shaved-off a few bits in some RAMs in tp_rr_fifo, tp_align_fifo
and tp_lod_fifo.

Change 131082 on 2003/11/10 by kmeekins@kmeekins_xenos_linux_orl

tb_vc.v
  ----------
  Fixed instantiation of vc now that delay is removed.

  sq_fetch_arb.v
  --------------
  Changed the bus width of vc_mini_count_q to accomidate the +2 modification.

  vcmi_requestor.v
  ----------------
  Increased the uvcmi_input_fifo FIFO depth to 8.
  Added the FIFO full to the performance monitor.

  tp.blk,
  vc.v,
  vc_perf_config.txt,
  vc_perfmon.v,
  vcmi.v
  ----------------------
  Added the FIFO full for the vcmi_input_fifo to the performance monitor.

Change 131037 on 2003/11/10 by jayw@jayw_r400_linux_marlboro

Improvements for using only SC_BC for quad data and killing SC_RC_detail.

Change 131020 on 2003/11/10 by tien@tien_r400_devel_marlboro

Fixed an IO port leak in TP
```

```
Change 130987 on 2003/11/10 by smburu@smburu_xenos_netlist

Changed some bus sizes to fix port width mismatches.

Change 130983 on 2003/11/10 by dclifton@dclifton_xenos_linux_orl

Disabled Nan detect for comp opcodes.

Change 130908 on 2003/11/08 by jhoule@jhoule_r400_linux_marlboro

RTL changes related to EMU fixes in CL#130898.

fpu_add_expl1.mc:
- Fixed issue where very large exponent difference wouldn't ignored the smallest term
(modification performed by Tien)

tp_addresser.mc:
- Removed needless coordinate override muxes when pix_mask if 0
- Interlaced determination now considers -0 identical as +0
(modifications performed by Manoo, but I removed changed related to GetGradients*
opcodes)

Regenerated tp_addresser.bvrl to reflect those changes.

Change 130892 on 2003/11/07 by vbhatia@vbhatia_r400_linux_marlboro

       Initial checkin of Internal Trackers for TP which are controlled by
tp_track_control.cfg
       Still a work in progress, needs thorough validation and emulator updates to be
automatic

Change 130842 on 2003/11/07 by smburu@smburu_xenos_netlist

Undefined C1.

Change 130840 on 2003/11/07 by smburu@smburu_xenos_netlist

Define CI. This is for synthesis purposes,
I will edit this file again immediately and
undefine C1 so that it does not interfere with SIMS.

Change 130797 on 2003/11/07 by smburu@smburu_r400_linux_marlboro

Not used anymore.

Change 130786 on 2003/11/07 by tien@tien_r500_emu
```

```
Final TPC perf regs

Change 130763 on 2003/11/07 by llefebvr@llefebvr_r400_linux_marlboro

Reverting timing fix that broke r400sq_const_index_04.cpp test.

Change 130693 on 2003/11/07 by kmeekins@kmeekins_xenos_linux_orl

chip_vc.tree,
  vc.v
  ----------------
  Removed the delay logic.

  tbmod_sqvc.v
  -------------
  Changed the L1 counter to use the pipelined elements of the FIFO.

Change 130671 on 2003/11/07 by bhankins@bhankins_xenos_linux_orl

- remove obsolete code in tracker
   - remove obsolete file open/reads in tbmod_fake_rb

Change 130661 on 2003/11/07 by rramsey@rramsey_xenos_linux_orl

Another attempt to keep the pc_out_ppb from overflowing

Change 130635 on 2003/11/06 by vbhatia@vbhatia_r400_linux_marlboro

Tentative checkin of internal interface trackers for TP

Change 130601 on 2003/11/06 by smoss@smoss_crayola_linux_orl_regress

   housekeeping

Change 130581 on 2003/11/06 by smburu@smburu_r400_linux_marlboro

Some changes to memory bit widths.

Change 130572 on 2003/11/06 by jayw@jayw_r400_linux_marlboro_syn

Fixes for pipeline enabled Virage memories detected by IKOS.

Change 130571 on 2003/11/06 by llefebvr@llefebvr_r400_linux_marlboro

This fixes the bad pix/vtx GPR input arbitration performance counter.

Change 130524 on 2003/11/06 by tien@tien_r500_emu
```

```
Added TP perf regs (on to TPC)
Cleaned up some tcf/tpc regs
After cleanup, added TPC_CHICKEN

Change 130521 on 2003/11/06 by cbrennan@cbrennan_r400_emu

Cleaned up TCR and TCM perfmon descriptions.

Change 130421 on 2003/11/06 by bhankins@bhankins_xenos_linux_orl

- sq-sx thread id added to sq output and into and through the sx
   - updated sx-rb trackers to use sq-sx thread id
   - removed obsolete code from sx
   - fixed sx bug where an ea from one export to memory was resetting the valid bits
for the other export to memory

Change 130419 on 2003/11/06 by dclifton@dclifton_xenos_linux_orl

Update to account for module compiler library changes.

Change 130407 on 2003/11/06 by donaldl@donaldl_xenos_linux_orl

Adjusted delays again with new 90nm libraries to meet latencies.

Change 130380 on 2003/11/05 by cbrennan@cbrennan_r400_emu

Added in TCO perfmon counters.

Change 130347 on 2003/11/05 by dclifton@dclifton_xenos_linux_orl

Two fixes for SIN/COS--quadrant selection fixed and inf/nan detection fixed.

Change 130346 on 2003/11/05 by danh@danh_xenos_linux_orl

Removed spi delay_in and delay_out ports.

Change 130345 on 2003/11/05 by dclifton@dclifton_xenos_linux_orl

Update clock delay so sythesis will finish

Change 130216 on 2003/11/04 by mmantor@FL_mmantorLT_r400_win

<changes to enable standalone vector pipe random testbench>

Change 130204 on 2003/11/04 by danh@danh_xenos_linux_orl

Removed the ati_delay_chain and SPI_delay_in and SPI_delay_out ports.
```

```
Change 130164 on 2003/11/04 by chammer@chammer_xenos_linux_orl

Switched SC_RCT(tile) interface to SC_BC(four quad) interface.

Change 130157 on 2003/11/04 by jayw@jayw_r400_linux_marlboro

Increased 2 FIFOs from R400 size to C1 Xenos size.  Fixes SC 1prim/clk.

Change 130127 on 2003/11/04 by vromaker@vromaker_r400_linux_marlboro

- instruction writes to the different SIMD memories now happen
  independently and no longer wait for all SIMD memories to be
  available

Change 130126 on 2003/11/04 by dclifton@dclifton_xenos_linux_orl

Fixed problem with clamp-to-one getting enabled falsely on MUL by 0

Change 130094 on 2003/11/04 by rramsey@rramsey_xenos_linux_orl

Fix scalar tracker so it compares all 128 bits based on write masks
It was only comparing the lower 32 bits based on bit 0 of the write mask

Change 130079 on 2003/11/04 by rramsey@rramsey_xenos_linux_orl

Couple of timing fixes for aiq and cfs
Fix a bug in the rbbm if that was allowing map copies to happen before
memory writes
Fix a problem in the testbench that was causing some incompletes

Change 130072 on 2003/11/04 by rramsey@rramsey_xenos_linux_orl

Update tracker to work with new sp_sx dump file that has all free-done
entries as unique lines between exports

Change 130068 on 2003/11/04 by dclifton@dclifton_xenos_linux_orl

Fixed quandrant assign of SIN/COS, fixed clamp of SQRT with -0 input,
fixed clamp of SIN/COS input for small values

Change 130017 on 2003/11/04 by tien@tien_r400_devel_marlboro

Finish TPC/TP debug regs
Cleaned up clock gating
On the perf connections

Change 130012 on 2003/11/04 by cbrennan@cbrennan_r400_emu
```

```
Revamped TCA and TCB perfmon registers.

Change 129980 on 2003/11/03 by smoss@smoss_crayola_linux_orl_regress

   some housekeeping and removed bad path

Change 129955 on 2003/11/03 by tien@tien_r400_devel_marlboro

Some random LEDA fixes
Most TPC debug reg connections (a couple more left..)

Change 129874 on 2003/11/03 by tien@tien_r400_devel_marlboro

Debug register updates

Change 129739 on 2003/11/02 by smoss@smoss_xenos_linux_orl

   added vgt gate memory file to vgt dir

Change 129723 on 2003/11/01 by vromaker@vromaker_r400_linux_marlboro

- fixed pix ctl output buffer overwrite bug
- backed timing fix out of status reg and pix thread buff

Change 129692 on 2003/10/31 by danh@danh_xenos_linux_orl

This changes spi_interp_ctl back to its original state (Changelist 129259)

Change 129689 on 2003/10/31 by danh@danh_xenos_linux_orl

This version is only for IKOS release 2.1 (r500_ikos_rel2.1_spi)

Change 129640 on 2003/10/31 by vbhatia@vbhatia_r400_linux_marlboro

       Updated to have a whole bunch of aniso tests, various dimensions and filter
combinations

Change 129632 on 2003/10/31 by jayw@jayw_r400_linux_marlboro

Memory export support in RB & DB.

Change 129622 on 2003/10/31 by tien@tien_r400_devel_marlboro

Fixes for GetGradients

Change 129610 on 2003/10/31 by amys@amys_xenos_linux_orl

remove dependency on index_rtr signals for comparison
```

```
Change 129541 on 2003/10/31 by bhankins@bhankins_xenos_linux_orl

clean up signal names for consistency.

Change 129527 on 2003/10/30 by vbhatia@vbhatia_r400_linux_marlboro

Aniso updates for addresser tb and fmt based cycle count update for formatter tb

Change 129451 on 2003/10/30 by tien@tien_r400_devel_marlboro

Fixes for GetTexCompLOD
No longer multicycles for mip/aniso
correct valid pixel detection for this opcode in tsel block

Change 129450 on 2003/10/30 by viviana@viviana_xenos_linux_orl

Configuration file with the 28x99 and 28x100 memories recently added.

Change 129444 on 2003/10/30 by llefebvr@llefebvr_r400_linux_marlboro

Fixing dangling wires in the sq related to performance module.
Fixing shader due to Kill opcode assembler change.
Fixing trakcer problem in the TB_SQSP when autocount vtx is on.

Change 129443 on 2003/10/30 by georgev@devel_georgev_r400_lin2_marlboro_coverage_tc

Copied version from tp directory.

Change 129423 on 2003/10/30 by dclifton@dclifton_xenos_linux_orl

Fixed 0*Nan problem with DST Y result value

Change 129416 on 2003/10/30 by tien@tien_r400_devel_marlboro

Added rule to rebuild mktree-derived .v's (It needs a little more work,
       but works for the TP at least)
Refreshed Makefiles with the new deps.pl

Change 129408 on 2003/10/30 by rramsey@rramsey_xenos_linux_orl

Move some continuous assignments into always blocks to help sim time
Rework cfs_rtr/arb_xfc path to help timing
Fix a problem with detecting serialize for the cf state machine

Change 129348 on 2003/10/30 by mearl@mearl_xenos_linux_orl

Added two primitive interpolation back in.
```

```
Change 129333 on 2003/10/29 by vbhatia@vbhatia_r400_linux_marlboro

       updated tests to only support multisample modes of 1,2 and 4 cases
       for 3,6 and 8 have been optimized from hardware

Change 129259 on 2003/10/29 by danh@danh_xenos_linux_orl

- spi_interp_ctl IJ buffer changed from one 16x200 memory to two 16x100 memories.
       - added additional SQ_SP_interp_qd[0:1]_prim_sela signals to improve spi input
timing.

Change 129232 on 2003/10/29 by smburu@smburu_r400_linux_marlboro

Fix for format 26 xor mask.

Change 129213 on 2003/10/29 by llefebvr@llefebvr_r400_linux_marlboro

Added VC_PERF_ACTUAL_STARVED performance counter in the SQ.

Change 129150 on 2003/10/29 by llefebvr@llefebvr_r400_linux_marlboro

Increasing VC mini count to ll_fifo_size +2.

Change 129145 on 2003/10/29 by mdesai@mdesai_r400_linux

Fixed offset bug 2812
Fixed X's propagaing for y and z coordinates when the exponent causes overflow

Change 129143 on 2003/10/29 by mdesai@mdesai_r400_linux

Fixed offset overflow bug

Change 129135 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl

support adding 2 bits to indicate how quad pixel mask bits are rotated
   for use by the trackers

Change 129128 on 2003/10/29 by dclifton@dclifton_xenos_linux_orl

Fixed PRED_SET result.

Change 129122 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl

fix quad buffer address pointer to support larger depth

Change 129121 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl
```

```
   - increase quad fifo depth to 656 (behavioral only for now).
- fix bug in export to memory logic.

Change 129120 on 2003/10/29 by bhankins@bhankins_xenos_linux_orl

add support for testing memory export data by including a value for the tracker that
   indicates how many bits the pixel quad mask has been shifted.

Change 129066 on 2003/10/28 by vromaker@vromaker_r400_linux_marlboro

- added vtx input optimization for autocount on and continued off
- fixed initialization problem for vtx autocount
- made pix thread buff timing fixes: reduced load on status read
         data bit 19, which is the event bit, and also tried to reduce
         the load on pop_thread (part of the same path) in the status register
- backed out a timing fix in alu_instr_seq that was causing a mova
         test to fail
- fixed the AUTO_COUNT_SIZE definition

Change 129037 on 2003/10/28 by tien@tien_r400_devel_marlboro

Disable multicycle on vol filter for
GetCompTexLOD and GetGradients

Change 129022 on 2003/10/28 by tien@tien_r400_devel_marlboro

14:1 center sample weight fix

Change 128978 on 2003/10/28 by smburu@smburu_r400_linux_marlboro

New logic to decode the data_format signals depending on
whether it is a 8/16/32 bit format.

Change 128816 on 2003/10/27 by llefebvr@llefebvr_r400_linux_marlboro

Adding VC performance counters in the SQ.
Removed the SX->RB warnings on non-initialized GPR channels.

Change 128709 on 2003/10/27 by tien@tien_r400_devel_marlboro

Resolved file, goes with CL 128662

Change 128708 on 2003/10/27 by tien@tien_r400_devel_marlboro

Fix to vtx RF expand for 3 tfetch formats that use it (need channel format_comps)
Removed 3,6,8 sample multisamp tables from deriv
Hooked up encoded format_comp* in tpc where needed
```

```
Change 128705 on 2003/10/27 by vbhatia@vbhatia_r400_linux_marlboro

        added support for format 61 testing, clamps for invalid cases on vertex path
        and other updates to get increased coverage.

Change 128675 on 2003/10/27 by smoss@smoss_xenos_linux_orl

   combined ncverilog and vcs simulators to one build

Change 128670 on 2003/10/27 by smoss@smoss_xenos_linux_orl

   combined ncverilog and vcs into one build, removed a few warnings

Change 128659 on 2003/10/27 by donaldl@donaldl_xenos_linux_orl

Delayed rom_rsp_shift*_* mux shift selects 1 clk to fix synthesis timing.

Change 128657 on 2003/10/27 by donaldl@donaldl_xenos_linux_orl

Added muxes to output of real-time parameter cache mems to select the
correct parameter based on bits [8:7] of the ptr selects.

Change 128656 on 2003/10/27 by donaldl@donaldl_xenos_linux_orl

Changed vc_req's and tex_req's dependencies on vc_pending_q and
tp_pending_q.

Change 128652 on 2003/10/27 by smoss@smoss_crayola_linux_orl_regress

   some housekeeping

Change 128647 on 2003/10/27 by rramsey@rramsey_xenos_linux_orl

Change ais so PS src sel gets priority over PV
Add predicated jumps and calls to cfs
Fix fetch_type connection in sq and tex_instr_seq

Change 128645 on 2003/10/27 by llefebvr@llefebvr_r400_linux_marlboro

Incrementing the number of in flight testure requests from 6 to 7.

Change 128624 on 2003/10/27 by mzini@mzini_crayola_linux_orl

 Added timeout count

Change 128610 on 2003/10/27 by dclifton@dclifton_xenos_linux_orl

Fixed recip/rsq/sqrt of -0, fixed clamp on multiplies
```

```
Change 128601 on 2003/10/27 by mmantor@mmantor_xenos_linux_orl

<Enable SQ use of 128 locations in export memmory instead of 112 locations.  Also added
counters in sq arbiter to give priority to instruction pipe that has the fewest
instructions when both control flow machines are available.  This changlist reguires
both an emulator and hardware rtl code updates>

Change 128592 on 2003/10/26 by danh@danh_xenos_linux_orl

Changed sc_rt_valid to fix the condition when end_of_prim and end_of_vector do not
occur at the same time, the sc_packer will send real time fill quads.

Change 128526 on 2003/10/24 by mearl@mearl_xenos_linux_orl

Took out two prim per clock to get regression to pass.

Change 128464 on 2003/10/24 by kmeekins@kmeekins_xenos_linux_orl

  vc_cc.v,
  vc_cc_tag_compare.v,
  vc_cc_tag_process.v
  ---------------------------
  Added sector miss to the performance counters.

  vcdc.v
  ---------------------------
  Combined two combinational logic always blocks to elliminate a synthesis
  warning about having the same signal set in two different blocks.

  vcmi_receiver.v
  ---------------------------
  Corrected the timestamp delta calculation for the TWO_CHANNEL_VC.

  vcrg.v
  ---------------------------
  Added VC_PERF_send_event and VC_PERF_starved_idle_event to the performance counters.

tp.blk,
  vc.v,
  vc_perf_config.txt,
  vc_perfmon.v
  ---------------------------
  Added more performance counters.

  vcrg.cpp
  ---------------------------
  HACK to get system tests to match with the TP/TC (submitted for Marcos Zini).
```

```
  randomvc
  ---------------------------
  Made the usage message look pretty.

Change 128393 on 2003/10/24 by llefebvr@llefebvr_r400_linux_marlboro

This should fix the instruction count being off. The bad machine (cfs) was used to
determine the thread type and hence some pixel shader instructions were counted as
vertex ones and vice versa.

Change 128374 on 2003/10/24 by vbhatia@vbhatia_r400_linux_marlboro

updates

Change 128373 on 2003/10/24 by cbrennan@cbrennan_r400_release

Fixed cut and paste error in tpc_fifos that was calculating the sec_z_pitch off of
parts of width.

Change 128372 on 2003/10/24 by smoss@smoss_parts_lib_release

   Checking in these files for Mr. Hartog after they passed release_parts_lib

Change 128365 on 2003/10/24 by mearl@mearl_xenos_linux_orl

Added 2 primitive interpolation in SQ and SPI. Fixed a bug in sx_parameter_cache. Fixed
synthesis
       bugs in SC.

Change 128343 on 2003/10/24 by cbrennan@cbrennan_r400_release

Release kevin's tcd coverage changes.

Change 128336 on 2003/10/24 by smoss@smoss_parts_lib_release

   modified for make_stub

Change 128334 on 2003/10/24 by cbrennan@cbrennan_r400_release

Didnt mean to check this one in.

Change 128331 on 2003/10/24 by cbrennan@cbrennan_r400_emu

Allow block levels to use phantom counters by setting PHANTOM_BLOCK

Change 128329 on 2003/10/24 by cbrennan@cbrennan_r400_emu
```

Fix input fifo sizes in perfmon counters.

Change 128319 on 2003/10/24 by bhankins@bhankins_xenos_linux_orl

update the creation of the valid pixel table for export to memory

Change 128240 on 2003/10/23 by jayw@jayw_r400_linux_marlboro

fixed white space.

Change 128238 on 2003/10/23 by jayw@jayw_r400_linux_marlboro

spacing reverted.

Change 128218 on 2003/10/23 by vbhatia@vbhatia_r400_linux_marlboro

Added format based restriction on xyzw_parity to be only values upto cycle multiplier

Change 128209 on 2003/10/23 by vromaker@vromaker_r400_linux_marlboro

- timing fixes for constant store read address

Change 128195 on 2003/10/23 by rramsey@rramsey_xenos_linux_orl

Fix a problem with yield_optimize

Change 128177 on 2003/10/23 by jayw@jayw_r400_linux_marlboro

Fixes for memory exports.

Change 128092 on 2003/10/23 by vbhatia@vbhatia_r400_linux_marlboro

Fixed silly error

Change 128070 on 2003/10/23 by bhankins@bhankins_xenos_linux_orl

fix lint warning. no functional change to logic.

Change 128048 on 2003/10/23 by llefebvr@llefebvr_r400_linux_marlboro

Fixed problem in the active counters when both pixels and vertexes were processing at
the same time.

Change 128046 on 2003/10/23 by bhankins@bhankins_xenos_linux_orl

added missing include statement

Change 128019 on 2003/10/23 by rramsey@rramsey_xenos_linux_orl

```
go back to prev version

Change 127998 on 2003/10/22 by vbhatia@vbhatia_r400_linux_marlboro

More tests

Change 127997 on 2003/10/22 by vbhatia@vbhatia_r400_linux_marlboro

More random tests and increased testlength to 1M.
       Should see increased coverage.

Change 127895 on 2003/10/22 by vromaker@vromaker_r400_linux_marlboro

- timing fixes for gpr alloc

Change 127878 on 2003/10/22 by donaldl@fl_donaldl_p4

Changed oZ_TC from 28 bit to 27 bits to reflect latest sc_ztc_flt2fix.

Change 127872 on 2003/10/22 by rramsey@rramsey_xenos_linux_orl

fixes for MT3 functions

Change 127861 on 2003/10/22 by llefebvr@llefebvr_r400_linux_marlboro

Fixing TP and VC sync stalls for both pixel and vertex threads.

Change 127857 on 2003/10/22 by bhankins@bhankins_xenos_linux_orl

fix bug to correct how position aux buffers are freed

Change 127742 on 2003/10/22 by llefebvr@llefebvr_r400_linux_marlboro

Removed the warnings from the sp->sx trackers and sx->sp.
Now emulator is always executing the scalar instruction even in the case of a 3 operand
vector opcode. This is to match with random shaders.

Change 127734 on 2003/10/22 by dclifton@dclifton_xenos_linux_orl

Fixed recognition of Nans on in3

Change 127730 on 2003/10/22 by rramsey@rramsey_xenos_linux_orl

Fix a bug with start_of_clause

Change 127729 on 2003/10/22 by rramsey@rramsey_xenos_linux_orl
```

```
Add window_valid_busy counts to sc and change sc_starved_by_pa to only count busy
cycles

Change 127701 on 2003/10/21 by vbhatia@vbhatia_r400_linux_marlboro

updates for more tests and interface changes

Change 127610 on 2003/10/21 by tien@tien_r400_devel_marlboro

Some Get/Set fixes for miscompare at sub-block level

Change 127604 on 2003/10/21 by bhankins@bhankins_xenos_linux_orl

- remove debug code
   - put valid quad identifier bit on lsb of quad pixel mask for memory exports

Change 127582 on 2003/10/21 by vbhatia@vbhatia_r400_release

       Fix for timing reasons, in the vertex fetch data path.
       Removed the VC_SP_data_format 57 to 38 substitution which was delaying data
format
       being fed to other parts of the logic, and accordingly added it to the requisite

       data format muxes.

Change 127580 on 2003/10/21 by danh@danh_xenos_linux_orl

Changed any_pred_hi and any_pred_lo generation, now the predicate and valid bits are
now related to the thread that the CFS is working on.

Change 127516 on 2003/10/21 by smburu@smburu_r500_synth

Changed SCLK to the 1.80ns clock rate.

Change 127506 on 2003/10/21 by cbrennan@cbrennan_r400_release

Release syn and coverage changes from tc branch

Change 127504 on 2003/10/21 by kmeekins@kmeekins_r400_win

Released work from my test environment.

Change 127496 on 2003/10/21 by dclifton@dclifton_xenos_linux_orl

Fixed clamp-to-one logic.

Change 127401 on 2003/10/20 by jayw@jayw_r400_linux_marlboro
```

```
Initial memory export support.

Change 127397 on 2003/10/20 by llefebvr@llefebvr_r400_linux_marlboro

Added an event window for pixels. There was a problem in the global event window as if
both pixels and vertexes were turned on at the same time, as soon as one went off it
was turning off the whole window. This fixes pixel counters being 0 for some tests.

Change 127355 on 2003/10/20 by dclifton@dclifton_xenos_linux_orl

Fixed clamp-to-one logic

Change 127348 on 2003/10/20 by bhankins@bhankins_xenos_linux_orl

add register for timing

Change 127325 on 2003/10/20 by vromaker@vromaker_r400_linux_marlboro

- updated VC injector to handle multi-cycle returns (the number of cycles, 1 to 4, is
         read from the vc_rp_sp.dmp file)

Change 127313 on 2003/10/20 by dclifton@dclifton_r400

Updated to testbench changes.

Change 127287 on 2003/10/20 by cbrennan@cbrennan_r400_emu

Fixes "bug" with addresser adder to allow denormalized inputs which happen with cube
mapping.

Change 127269 on 2003/10/19 by rramsey@rramsey_xenos_linux_orl

Change behave mem_model in spi so its read dly matches the real mem
Send interp_valid and ij_line lclk early to account for 2clk read dly
Fix spi_sp tracker so it works with early valid
Change thread_buf and cfs machines so only fetches can modify the
fetch pending bit. The alu machines only read the value out of the buffer.
Get rid of a bunch of extra 'else' clauses

Change 127206 on 2003/10/17 by cbrennan@cbrennan_r400_release

Added coverage pragmas to tca for defaults.  need to do displays too.

Change 127140 on 2003/10/17 by cbrennan@cbrennan_r400_release

Added VCS coverage pragmas around default cases, and also changes some default = 0's to
default = x's.
```

```
Change 127116 on 2003/10/17 by mdesai@mdesai_r400_linux

Fix for getBorderColorFraction

Change 127094 on 2003/10/17 by jayw@jayw_r400_linux_marlboro

Fix for broken TOT.  added missing file to system_db.vcpp

Change 127091 on 2003/10/17 by rramsey@RRAMSEY_P4_r400_win

udpate spreadsheet with 10/17/03 results
modify script so it automatically handles reports with/without runtime

Change 127079 on 2003/10/17 by smoss@smoss_xenos_linux_orl

   initialized memory controller for sc and sx to allow real memories to work in
tb_sqsp

Change 127068 on 2003/10/16 by jayw@jayw_r400_linux_marlboro

some memory export fixes and quad interface ifdef'ed out.

Change 127053 on 2003/10/16 by jhoule@jhoule_r400_linux_marlboro

Fix LSB mismatches in the determinant, which sometimes showed up as LSB differences in
the LOD.

Might increase the multi-sampling correction fails until the emulator fixes that path
as well...

Change 127045 on 2003/10/16 by tien@tien_r400_devel_marlboro

Fix to prevent aligner state machine from hanging on last entry
Uncommented override for get_border_color_fraction on BORDER_COLOR fields

Change 127041 on 2003/10/16 by vbhatia@vbhatia_r400_release

Optimized cmask generation logic to follow tp_fmt_encode,
       hopefully will clean up timing on the formatter.

Change 126983 on 2003/10/16 by vromaker@vromaker_r400_linux_marlboro

fixed code that was causing a latch in synthesis

Change 126908 on 2003/10/16 by rramsey@rramsey_xenos_linux_orl

absolute modifier for constants should apply to all source constants
```

```
Change 126890 on 2003/10/16 by bhankins@bhankins_xenos_linux_orl

Add missing signals to sensitivity lists

Change 126888 on 2003/10/16 by bhankins@bhankins_xenos_linux_orl

Fix perf monitoring signal

Change 126859 on 2003/10/15 by donaldl@donaldl_xenos_linux_orl

Fixed error - need to delay SX_SQ_vtx_data3 an extra clock.

Change 126823 on 2003/10/15 by rramsey@rramsey_xenos_linux_orl

Add sqvc tracker to gc testbench when running with orlando trackers
Rework some of the alu/tex constant logic to get rid of the bug that
was allowing threads to start processing before all of the constants for
their context had been loaded.

Change 126796 on 2003/10/15 by vromaker@vromaker_r400_linux_marlboro

- hooked up the new alu_arb_policy and tx_cache_sel register bits (but
         temporarily tied the tx_cache_sel input to the vtx thread buff low
         since it is being incorrectly set to 1 by Primlib)

Change 126738 on 2003/10/15 by tien@tien_r500_emu

Removed unecessary assign

Change 126705 on 2003/10/15 by cbrennan@cbrennan_r400_release

Revert back to rev #3.  #4 should never have gotten in, and is causing i/o width
mismatches.

Change 126698 on 2003/10/15 by tien@tien_r500_emu

NOT_RTR_FROM_SPSQ counter temporarily attached to TPC_busy.

Change 126692 on 2003/10/15 by cbrennan@cbrennan_r400_release

Fix for an amazingly rare TC hang having to do with a cache thrash situation and great
skews between quad's samples.  Will write better test.

Change 126691 on 2003/10/15 by dclifton@dclifton_xenos_linux_orl

Another timing related change.  Changed twos comp to ones comp on log
post-process (effects log of number less than 1.0).  Aligned inputs
to high precision pipeline to reduce muxing.  Improved carrysave add
```

```
of multiplier results.  Regenerated math tables to reclaim precision
and fix roll-over mismatches.

Change 126689 on 2003/10/15 by dclifton@dclifton_xenos_linux_orl

Fixed cube opcode problem with neg/pos X face_id

Change 126685 on 2003/10/15 by smburu@smburu_r400_linux_marlboro

tp_hicolor logic optimization.

Change 126624 on 2003/10/14 by tien@tien_r400_devel_marlboro

Bug fix for 14:1 aniso +/-0.5 sample

Change 126618 on 2003/10/14 by dclifton@dclifton_xenos_linux_orl

Fixed an lsb precision issue with neg mult result shifted 25 places.

Change 126586 on 2003/10/14 by mdesai@mdesai_r400_linux

checking in again since the last submit didn't take

Change 126574 on 2003/10/14 by mzini@mzini_crayola_linux_orl

 Added ability for random tool to change rsp in mid-test plus TB can now handle this

Change 126568 on 2003/10/14 by mdesai@mdesai_r400_linux

Removed un-necessary logic
Fixed the valid bits for Z

Change 126567 on 2003/10/14 by mdesai@mdesai_r400_linux

       Re-write to use signed int and texel for the vertex and texture fetch offset add

Change 126566 on 2003/10/14 by mearl@mearl_xenos_linux_orl

Fixed bug in multi-pass logic when persistent event increments counter.

Change 126550 on 2003/10/14 by kmeekins@kmeekins_xenos_linux_orl

Preventing an active VC_RSP_valid signal while redundant shader pipe operation is
disabled.

Change 126516 on 2003/10/14 by mzini@mzini_crayola_linux_orl

 VC TB redundancy change
```

```
Change 126491 on 2003/10/14 by kmeekins@kmeekins_xenos_linux_orl

Corrected syntax by defining vc_busy_in.

Change 126490 on 2003/10/14 by danh@danh_xenos_linux_orl

registered SQ_SP_interp_qd[0:1]_prim_sel fanout to improve synthesis timing results.

Change 126487 on 2003/10/14 by bhankins@bhankins_xenos_linux_orl

Change to try and improve on timing.  No functional change.

Change 126483 on 2003/10/13 by mearl@mearl_xenos_linux_orl

Fix One Prim Per Clock bug in sq_ptr_buff. Revert changes in sq_pix_ctl to make
       2 prim interp changes easier. Put known primdata data on all quads across packer
       to iterator interface. Fix dumps for no_inc_pix_cnt signal.

Change 126451 on 2003/10/13 by donaldl@donaldl_xenos_linux_orl

Qualified q_tp_data_valid with q_tp_simd[1:0].

Change 126450 on 2003/10/13 by donaldl@donaldl_xenos_linux_orl

Delayed SQ_SX_sp_simd_id an extra clock to line up for redudancy use.

Change 126435 on 2003/10/13 by cbrennan@cbrennan_r400_release

Didnt need to qualify texture size + 1 by dimension.  Also fixes texture stack tests.

Change 126382 on 2003/10/13 by kmeekins@kmeekins_xenos_linux_orl

tp.blk,
  vc_perf_config.txt,
  vc_perfmon.v
  ------------------------
  Added a new performance monitor field for counting number of valids passed to the SP.

  vc.v,
  vcdc.v
  ------------------
  - Reformatted vc.v using more AUTO commands.
  - Added the new performance monitor field for counting valids passed to SP.
  - Corrected the valid logic to swizzle the data valids similar to the data for
    the redundant shader pipe logic.

  vcmi_receiver.v
```

```
  ----------------
  Corrected the timestamp delta equation.

Change 126362 on 2003/10/13 by rramsey@rramsey_xenos_linux_orl

Change sq_sp_interp dump so it contains all of the pass_count and wrap passes
through the interpolator
Add spi_sp tracker (enabled with ENABLE_SPI_TRACKER define)

Change 126358 on 2003/10/13 by cbrennan@cbrennan_r400_release

Better matches for the TPC interface now that the TPC interface is checked more.
Also bug fixes 1 high/wide/deep maps.

Change 126350 on 2003/10/13 by bhankins@bhankins_xenos_linux_orl

Changes made to improve timing.  No functional change.

Change 126348 on 2003/10/13 by tien@tien_r500_emu

Changed word counts for lod/coord FIFO to 32 to match RAM
Added ati_dff_in to tp4_tc testbench for TP_SQ_dec
Misc. changes to perf test...

Change 126324 on 2003/10/13 by dougd@dougd_r400_linux_marlboro

Added logic to generate read enables for the 4 map rams in sq_aluconst_rams.v
Added SQ_CONTEXT_MISC_YEILD_OPTIMIZE register to sq_rbbm_interface.v

Change 126234 on 2003/10/10 by vromaker@vromaker_r400_linux_marlboro

- added export arbiter module that will limit the number of color buffer export
         threads to one every 4 clocks
- hooked up the export blocker outputs and commented out the previous export
         blocking code
- added export alloc arbiter inputs to exp_alloc_ctl module so that the buf_avail
         counter will be updated by the export allocs
- added logic to support the export arbiter to the vertex and pixel thread buffers
- added logic to support the export arbiter to the thread arbiter
- separated the export alloc request out of the alu request logic in the status
register,
         and added an output for the export alloc request

Change 126226 on 2003/10/10 by cbrennan@cbrennan_r400_emu

Release from my emu branch: texture stacks for TP as well.
Leda rule tweaks
add more .rg files
```

```
Change 126189 on 2003/10/10 by vbhatia@vbhatia_r400_linux_marlboro

       Updated

Change 126168 on 2003/10/10 by dclifton@dclifton_r400

Duplicated internal q_rom_pipe_sel, grouped muxes into new module compiler block to
encourage proper fanout in synthesis.

Change 125951 on 2003/10/09 by danh@danh_xenos_linux_orl

dos2unix conversion for proper Synopsys Module Compiler format.

Change 125870 on 2003/10/09 by tien@tien_r400_devel_marlboro

Size fields are now programmed n-1 as they should have been
from the start :-)
THIS MUST BE ACCOMPANIED BY A CHANGELIST FROM JOCELYN!!!
No pity if you don't catch the preceding line!!!

Change 125835 on 2003/10/09 by jhoule@jhoule_r400_linux_marlboro

Fixed FMT_1* formats

EMU:
Were rf-expanded as 4x8 instead of 1x32

RTL:
Were considered as 4 channels in the formatter; changed to be like FMT_32.
Fixed sp_tp_cmask_gen.mc as well as tpc_cmask.v (equivalent glue logic for tp4_tc
testbench)
Note: All RTL modifications were done by Tien.

Change 125821 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

include unused outputs to eliminate compile-time warnings

Change 125820 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

fix unconnected inputs

Change 125818 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

remove unused input

Change 125815 on 2003/10/09 by smburu@smburu_r400_linux_marlboro
```

More border-color changes and annotation of bvrl for coverage.

Change 125811 on 2003/10/09 by smburu@smburu_r400_linux_marlboro

Change of the WRCK clock names for BIST insertion purposes.

Change 125809 on 2003/10/09 by kevino@kevino_r400_emu

Switch over to kinky degamma in the TC in both the emulator, tcd emulator, and RTL. Both the emu and RTL changes need to used together or degamma tests will fail in the TC.

Change 125806 on 2003/10/09 by cbrennan@cbrennan_r400_release

Temporarily reduce the num SQ_TP vectors in flight back to 6 until fifo overflows can be fixed.

Change 125786 on 2003/10/09 by mearl@mearl_xenos_linux_orl

Fixed the unused port PA_SC_phase[0] when using ONEPPC

Change 125780 on 2003/10/09 by bhankins@bhankins_xenos_linux_orl

update sx test inputs to match the established convention

Change 125703 on 2003/10/08 by vbhatia@vbhatia_r400_linux_marlboro

updated to run coverage on the addresser

Change 125697 on 2003/10/08 by dougd@dougd_r400_linux_marlboro

fixed bug in eqn for *sync_alu_stall

Change 125673 on 2003/10/08 by dclifton@dclifton_xenos_linux_orl

Fixed bug with factor-of-two negative results out of adder

Change 125660 on 2003/10/08 by rramsey@rramsey_xenos_linux_orl

Fix compile warnings for sq (several missing ports)
Fix compile warning in sx_parameter_caches
Fix SQ_SP_fetch_simd_sel so it lines up with the data coming out of the GPRs

Change 125650 on 2003/10/08 by vbhatia@vbhatia_r400_linux_marlboro

Simple script to insert coverage OFF/ON pragmas

Change 125637 on 2003/10/08 by bhankins@bhankins_xenos_linux_orl

```
edits made for timing only.  no functional change.

Change 125622 on 2003/10/08 by cbrennan@cbrennan_r400_emu

Integrate code from branch:
Implemented texture stacks in the TC.
integrated some rg files back from TOTT.
Tweaked leda rules for tca and tcb.
Added texture stacks to nightly tests and randoms.

Change 125598 on 2003/10/08 by dougd@dougd_r400_linux_marlboro

Expanded the read back mux for rbbm diagnostic reads
to include the extra memories for SIMD2 and SIMD3.

Change 125597 on 2003/10/08 by bhankins@bhankins_xenos_linux_orl

move adders outside of comb. process for timing.  no functional change.

Change 125554 on 2003/10/08 by rmanapat@rmanapat_r400_release

Bug fix for fmt00 and fmt01 on the TC

Change 125550 on 2003/10/08 by rramsey@rramsey_xenos_linux_orl

Increase sq_tp_maxcount from 6 to 7
Fix a problem with the simd mux for vtx_alloc_size in export_alloc
Fix a problem with pc_alloc_free_cnt in export_alloc (alloc and dealloc on same clk
was broken)
Make alu ctl_flow and instr trackers work with multiple simd's
Also change these trackers to use common code for pix/vtx by selecting the type with
a parameter

Change 125540 on 2003/10/08 by dclifton@dclifton_r400

Added needed include files.  Strange how these compiled before this.

Change 125509 on 2003/10/07 by dougd@dougd_r400_linux_marlboro

change perfcounters alu(0/1)_fifo_empty_simd* to count
alu(0/1)_stall_simd* instead.

Change 125507 on 2003/10/07 by vbhatia@vbhatia_r400_linux_marlboro

       Interface change and coverage updates

Change 125427 on 2003/10/07 by danh@danh_xenos_linux_orl
```

```
Timing and XY LSB interpolation changes.

Change 125407 on 2003/10/07 by cbrennan@cbrennan_r400_release

Release tcd code coverage pragmas and synth changes just to keep it up to date.

Change 125400 on 2003/10/07 by cbrennan@cbrennan_r400_emu

Fixed cmask for testbench and data format for hi color for FMT_1_1_1_1

Change 125382 on 2003/10/07 by jayw@jayw_r400_linux_marlboro3

MULTIPLE_QUAD_COMMANDS enabled.  new MRT protocol SX->RB&DB.

Change 125370 on 2003/10/07 by mearl@mearl_xenos_linux_orl

Fixed the SQ bug when bad pipe exists before a good pipe. Also, updated
       the RT trackers in the SC testbench.

Change 125368 on 2003/10/07 by cbrennan@cbrennan_r400_emu

Fixed ordering of FMT_1_1_1_1.  two nibbles of byte were swapped, and typo on counting.

Change 125352 on 2003/10/07 by kmeekins@kmeekins_xenos_linux_orl

Added the 128 bit memory hub interface RAM memory controller.

Change 125350 on 2003/10/07 by kmeekins@kmeekins_xenos_linux_orl

buildkdb,
  buildtb
  ----------
  Modified the scripts to NOT use the behavioral RAM models and to use the two channel
  (128 bit) memory interface.

  runvc
  -------
  Modified the script to have the option to run only the verilog simulation which
permits
  the user to generate the dump files from the full chip emulator.

  vc.v
  -----
  Corrected the instantiation of the modules associated with the two channel mode.

  vc_rf_128_awt_gate.v,
  vc_rf_128_fusebox.ctmc,
```

```
  vc_rf_128_fusebox.v,
  vc_rf_128_stp.v,
  vc_rf_128_testreg.v
  ----------------------
  Added the 128 bit memory hub interface version of the RAM memory controller.

  vcmi.v,
  vcmi_receiver.v,
  vcrg.v
  ------------------
  Included header.v to files that used the TWO_CHANNEL_VC directive.

Change 125343 on 2003/10/07 by tien@tien_r400_devel_marlboro

Added FMT_DXT3A_AS_1_1_1_1 and in the process of using the name of
the format as it is in the spec, I think I killed my fingers... Geez.

Change 125314 on 2003/10/07 by chammer@chammer_xenos_linux_orl

Added ifdef to sc_quadmask.mc to remove quadcovered logic which is not used by
 the BC in Xenos.

Change 125305 on 2003/10/07 by cbrennan@cbrennan_r400_emu

Added fmt61 tests (U1111) and DXN tests that should have been there anyway.

Had x%2=0 and x%2=1 cases swapped for DXT3A_AS_1_1_1_1.
Also didnt have test cases defined for fmt49 in mip_cubic and stack tests.

Changed mip stacks to be multiples of 4 instead of powers of two.

Remove cp*e2 tests from other peoples sanity checks since TConst size field change
breaks cp microcode.

Added FMT_DXT3A_AS_1_1_1_1 to emu, test lib, and tx_simple_* tests.

Separated 2d and stack size tconst packing, but left both at the same 13 bit fully
packed.
Changed tconst size packing in HW
Changed testbench to turn on TPC checking more often.  Was ignoring many fields when it
thought they werent used.
Changed tcf_no_tpc in tc testbench to just be called tcf to keep waveform .rc
compatibility with tp4_tc testbench.
Removed tests from emulator regress_e, release_parts_lib and daily_regress that failed
with new size packing, but they are e2 tests which are no longer supported and need to
have a microcode change to pass.

Added texture stacks to tests, primlib, cmn_lib, and emu.
```

```
Change 125285 on 2003/10/07 by smburu@smburu_r400_linux_marlboro

Update of tcf STAR sms files.

Change 125278 on 2003/10/07 by dougd@dougd_r400_linux_marlboro

Added a new state register, vc_fifo_depths_ll_req_fifo_depth to
sq_rbbm_interface.v and wired it up to the compare logic for
vc_mini_count_q in sq_fetch_arb.v.

Corrected a typo in sq_vtx_ctl.v that affected synthesis.

Change 125260 on 2003/10/07 by dclifton@dclifton_r400

Updates for a couple of fifos in sq and new block in sp

Change 125258 on 2003/10/07 by dclifton@dclifton_xenos_linux_orl

Added a 'u' to instance names of const muxes

Change 125257 on 2003/10/07 by dclifton@dclifton_xenos_linux_orl

Fixed latency in pa.  Added mc mux for fanout control on const muxes
for alu constant data in sp.

Change 125059 on 2003/10/06 by rramsey@rramsey_xenos_linux_orl

Fix sq_sx file read in tb_sqsp
Add new tracker for shader writes to gpr
Add myself to failing regression email list

Change 125040 on 2003/10/06 by vbhatia@vbhatia_r400_linux_marlboro

Updates for interface changes and format optimizations

Change 124989 on 2003/10/05 by cbrennan@cbrennan_r400_release

Release FMT_DXT3A_AS_1_1_1_1

Change 124987 on 2003/10/05 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 124967 on 2003/10/04 by smburu@smburu_r400_linux_marlboro

More border-color fixes.
```

```
Change 124864 on 2003/10/03 by rramsey@rramsey_xenos_linux_orl

add some missing wire declarations

Change 124852 on 2003/10/03 by dclifton@dclifton_xenos_linux_orl

Optimizations for timing that changes precision.

Change 124850 on 2003/10/03 by rramsey@rramsey_xenos_linux_orl

move an adder in front of a register and change to a fifo with registered
outputs to help timing

Change 124844 on 2003/10/03 by mzini@mzini_crayola_linux_orl

 Ability for testbench to handle the L1 fifo depth being programmed

Change 124796 on 2003/10/03 by viviana@viviana_xenos_linux_orl

Added rsp_rf_stp.v and rsp_rf_awt_gate.v to the system_sp.vcpp.  Also added the memory
   configuration files for the rsp memories (4 128x128).

Change 124792 on 2003/10/03 by dougd@dougd_r400_linux_marlboro

Removed all references to SIMD1_DISABLE in sq.v and sq_rbbm_interface.v.

Added 32 new performance counters: many are for SIMD2 and SIMD3 but
other existing counters were expanded to differentiate between vertex
and pixel counts. There are now 95 performance counters in the sq.

Change 124776 on 2003/10/03 by donaldl@fl_donaldl_p4

Added new sc_itercmdfifo mems for one-prim-per-clock.

Change 124775 on 2003/10/03 by donaldl@fl_donaldl_p4

Changed bit-width of PA_SC_cntll from 30 bits to 29 bits.  The msb was not being used.

Change 124774 on 2003/10/03 by smoss@smoss_crayola_linux_orl_regress

   re-enabled behavioral memories until real memories are working

Change 124757 on 2003/10/03 by rramsey@rramsey_xenos_linux_orl

move reg declarations out of always blocks for synthesis

Change 124754 on 2003/10/03 by dclifton@dclifton_xenos_linux_orl
```

A few fixes for the mul_prev2 opcode.

Change 124742 on 2003/10/03 by bhankins@bhankins_xenos_linux_orl

fix test pin name

Change 124741 on 2003/10/03 by bhankins@bhankins_xenos_linux_orl

fix name on sx test pin

Change 124738 on 2003/10/03 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 124736 on 2003/10/03 by bhankins@bhankins_xenos_linux_orl

1. Add support for second memory test processor
   2. Add updated behavioral code for mc block in sx

Change 124706 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Changed data width of PA_SC_cntl1 from 30 bits to 29 bits to match
the PA (ie. msb wasn't used).

Change 124705 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Updated MC clock period, input/output delays for new 90nm libraries.

Change 124634 on 2003/10/02 by rramsey@rramsey_xenos_linux_orl

adding cond_pred optimize to control flow seq

Change 124630 on 2003/10/02 by tien@tien_r400_devel_marlboro

New aniso stuff

Change 124608 on 2003/10/02 by mearl@mearl_xenos_linux_orl

Updated to handle up to 4 SIMD engines

Change 124553 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Commented out old delays.

Change 124540 on 2003/10/02 by donaldl@donaldl_xenos_linux_orl

Updated clock, input, & output delays for 90nm technology.

```
Change 124503 on 2003/10/02 by bbuchner@bbuchner_xenos_linux_orl

added more performance counters to VGT to cover starved_busy, starved_idle and static
cases

Change 124472 on 2003/10/01 by jayw@jayw_r400_linux_marlboro

fully validated MRT support, just ifdefed out.

Change 124434 on 2003/10/01 by mmang@mmang_xenos_linux_orl

1.  Turned on 3 simds in emulator (sc_interp.cpp,
    sq_block_model.cpp, and user_block_model.cpp).
2.  Turned on 3 simds in rtl (sc_packer.v,
    tb_sqsp.v, and vgt.v).
3.  Fixed bug in chip_vc.tree to get SQ_VC_simd_id
    and TC_VC_simd hooked up correctly.
4.  Fixed bug in sc_packer.v related to having a 2
    bit simd_id_sel.

Change 124373 on 2003/10/01 by mearl@mearl_xenos_linux_orl

Fixed timing paths through primdata selection logic

Change 124330 on 2003/10/01 by dclifton@dclifton_xenos_linux_orl

Updated timing parameters for 0.09um technology.

Change 124324 on 2003/10/01 by kmeekins@kmeekins_xenos_linux_orl

vc.v
  -----
  - Removed VC_SP_valid. Now the SP is usind all 16 valids.
  - Registered the ROM inputs.
  - Changed the ROM signals to the lower modules to reflect their registered status.

  vcdc.v,
  vcrg.v
  -------
  Changed the ROM signal names to reflect their registered status.

Change 124292 on 2003/10/01 by rramsey@rramsey_xenos_linux_orl

Change sq_vgt_rtr to be driven based on fifo full, rather than by the vsr
load state machine

Change 124224 on 2003/10/01 by bhankins@bhankins_xenos_linux_orl
```

```
Changes made to try to improve on timing.  No functional change

Change 124218 on 2003/10/01 by rmanapat@rmanapat_r400_release

Change of TCA fifo from 18 deep to 12 deep

Change 124203 on 2003/10/01 by dougd@dougd_r400_linux_marlboro

The four existing SYNC_STALL counters were separated into
(8) pix and vtx stall counters.
The two ALU INSTRUCTION ISSUED counters were made to increment
by 1,2,3 or 4.
The two CF INSTRUCTION ISSUED counters were made to increment
by 1,2,3,4,5 or 6.

Added `ifdef's to sq_perfmon_wrapper for SIMD1, SIMD2, SIMD3.

perfmon event window:
An enable for the performance counters is generated by events received
from the VGT and/or SC which create a window of time when the counters
will be active. All of the perf counters are now controlled by this enable.

Change 124193 on 2003/10/01 by bhankins@bhankins_xenos_linux_orl

Undid change made for timing - was not functionally equivalent.

Change 124038 on 2003/09/30 by dclifton@dclifton_r400

Fixed busy and starved performance counters.

Change 124017 on 2003/09/30 by tien@tien_r500_emu

Bug fix for GetCompTexLOD, forcing ws to new 1.0 encoding

Change 123984 on 2003/09/30 by bhankins@bhankins_xenos_linux_orl

change names of sx i/o ROM_MCn_disable signals

Change 123983 on 2003/09/30 by dclifton@dclifton_xenos_linux_orl

Changed output flops to 'dff_out' variety

Change 123979 on 2003/09/30 by dclifton@dclifton_r400

changed instance names for vivian

Change 123975 on 2003/09/30 by dclifton@dclifton_xenos_linux_orl
```

```
Added 'COMMON_OUTPUT_REGISTER' to move output register past scalar fog muxes

Change 123973 on 2003/09/30 by dclifton@dclifton_xenos_linux_orl

Moved output register past scalar fog mux

Change 123966 on 2003/09/30 by smoss@smoss_xenos_linux_orl

   using real memories for sqsp

Change 123960 on 2003/09/30 by rramsey@rramsey_xenos_linux_orl

remove internal tracker enable

Change 123952 on 2003/09/30 by mmantor@mmantor_xenos_linux_orl

<added changes for 2 prim interpolation to the spi and sq and all top level
interconnects, and sq_sx_sp_simd_id for redundancy control, and all changes to test
bench as well as some ncverilog error messages.  Some other misc top level clean up>

Change 123937 on 2003/09/30 by bhankins@bhankins_xenos_linux_orl

Add the thread id debug bits to the detailed quad fifo when we're
   simulating with real memory.  This only affects simulation; the debug
   bits are not included unless 'SIM' is defined.

Change 123923 on 2003/09/29 by mearl@mearl_xenos_linux_orl

Fix to the emulator and corresponding hardware.

Change 123918 on 2003/09/29 by rramsey@rramsey_xenos_linux_orl

Change tp_sqsp dump to use FMT_32_32_32_32_FLOAT
Remove a monitor from tbtrk_sc for now since it is broken for ONEPPC
Need to register the if inputs to aiq since they are put in the fifo
one clk after the transfer
Fix the exec_sm so it is 4 clks even when switching clauses
Remove one clk of latency on tp_dec from fetch_arb
Fix the strap bits in sq.v so the tp and vc cfs and if machines get
two read cycles out of 8 when we have two instruction stores
Change the tp_sq dec input and force the tp_sp format in tb_sqsp
Fix the tif so its state machine is 4 clks between clauses and change
it so 0 count execs can be merged into the instruction ahead of them
Fix the tex_instr_seq for the case where tp_dec happens on the same
clk the fcs state machine kicks off (instr were getting dropped)
Check in Scott's vgt change to clamp vtx_reuse based on good pipes

Change 123893 on 2003/09/29 by kmeekins@kmeekins_xenos_linux_orl
```

```
randomvc,
  regressvc,
  runvc
  -----------------
  Modified scripts to use Brian's changes for the Redundant Shader Pipe testing

  chip_vc.tree
  ------------
  Removed partially driven bits for SQ_VC_simd_id and TC_VC_simd as these are now
  connected in the SQ and TC.

  tb_vc.v,
  tbtrk_vc_out.v
  ---------------
  Modified the testbench and tracker to use Brian's changes for the Redundant
  Shader Pipe logic.

  vc.v,
  vcdc.v,
  vcrg.v
  -------
  Modified the RTL to use Brian's changes for the Redundant Shader Pipe logic.

Change 123848 on 2003/09/29 by mearl@mearl_xenos_linux_orl

Add new memories for iter command FIFO.

Change 123808 on 2003/09/29 by cbrennan@cbrennan_r400_release

Change TP and TC to use ati_skid*fifos instead of ati_fifo*s.

Change 123806 on 2003/09/29 by cbrennan@cbrennan_r400_release

Release 3d enhancement enhancement

Change 123798 on 2003/09/29 by donaldl@donaldl_xenos_linux_orl

Temporary hook-up of SQ_SX_interp_2prim to zero going to SX until
SQ changes for 2 prims is complete.

Change 123795 on 2003/09/29 by donaldl@donaldl_xenos_linux_orl

Allow sx parameter caches to accept 3 more pointers so it can
potentially process 2 primitives at once.

Change 123791 on 2003/09/29 by mdesai@mdesai_r400_linux
```

```
Bug fixes
negative offsets
large exponents

Change 123790 on 2003/09/29 by tien@tien_r500_emu

Fixed connection for vol_min _filter
Optimized timing of TP_SQ_dec

Change 123755 on 2003/09/29 by mearl@mearl_xenos_linux_orl

Fix for timing problems, submitting new memories, using real memories for regressions.

Change 123639 on 2003/09/26 by donaldl@donaldl_xenos_linux_orl

Added redundancy shader pipe and fixed some of the connections
to it.

Change 123613 on 2003/09/26 by vbhatia@vbhatia_r400_linux_marlboro

Large range and randomized tests, with large stimuli,  standalone tp addresser
testbench

Change 123562 on 2003/09/26 by kmeekins@kmeekins_xenos_linux_orl

tp.blk, tp.desc
  ---------------
  - Changed L1 request FIFO depth to reflect max 32 words
  - Corrected debug register fields

  randomvc
  --------
  - Modified to perform infinite number of sequential ramdom tests.
  - Updates pass/fail status after each run.

  vc_cc.v,
  vc_cc_loaded_busy.v,
  vc_cc_pack_align.v,
  vc_cc_tag_process.v
  --------------------
  Created an earlier version of the fetch_pending_en signal for the
  loaded_busy module to correct the cache_lin_in_use logic.

  vc.v,
  vc_rbiu.v,
  vcrp.v
  ------------
  - Changed the width of the RBIU_RP_L1_req_fifo_depth bus to accomidate
```

```
    a max of 32 words.
  - Corrected VC_SP_data_valid logic.

Change 123547 on 2003/09/26 by smoss@smoss_crayola_linux_orl_regress

   added vc_mem

Change 123537 on 2003/09/26 by chammer@chammer_xenos_linux_orl

Fixed random backpressure/input for all interfaces. Removed extra cycle of
 delay in SC_RC_rtr/RC_SC_hier_send path for non-rts version of testbench.

Change 123530 on 2003/09/26 by smburu@smburu_r400_linux_marlboro

REQUIRED by changelist 123519.

Change 123528 on 2003/09/26 by llefebvr@llefebvr_r400_linux_marlboro

The sp->sx, sq->tp and sq->vc trackers now all use the post steered valid bits to know
what is valid. Thus they are now compatible with the redundant pipe. They should track
correctly in any bad pipe configuration. They however don't compare the RSP data for
now (waits for the HW implementation)

Change 123519 on 2003/09/26 by smburu@smburu_r400_linux_marlboro

REQUIRES Emulator changelist #123511. This is the modifications
of WS to 11 bit mantissa.

Change 123515 on 2003/09/26 by bhankins@bhankins_xenos_linux_orl

- add sx_redundancy.v to hierarchy to try and improve on timing
   - add EXP_BUF_112_DEEP switch.  comment out in sx_defines.v to enable
     all 128 locations of the color export buffer to be used
   - add ONE_STAR_PROCESSOR switch.  comment out in sx_defines.v to use
     two star processors.
   - add support for thread id and thread type for debug.
   - misc changes for timing which don't change the logic.

Change 123485 on 2003/09/26 by dougd@dougd_r400_linux_marlboro

I removed these files prematurely.

Change 123462 on 2003/09/26 by dclifton@dclifton_r400

disabled USE_BEHAVE_MEM. Changed 8x104 ram in sq to 8x105.

Change 123458 on 2003/09/26 by jmarsano@jmarsano_r400_UNIX_new
```

```
Adding generated verilog for vgt_rf memories.

Change 123430 on 2003/09/26 by jayw@jayw_r400_linux_marlboro

fix for multiple_render_targets and latest depth stuff..

Change 123378 on 2003/09/25 by vbhatia@vbhatia_r400_release

Added format optimizations (matching tp_fmt_encode) for timing reasons

Change 123343 on 2003/09/25 by dougd@dougd_r400_linux_marlboro

adding the x105 virage memories and deleting the x104 used in the sq_vc_skid_buf

Change 123331 on 2003/09/25 by dougd@dougd_r400_linux_marlboro

usq_alu01_state_mem is used twice as the instance name so I changed
the 2nd one to usq_alu23_state_mem.

Change 123292 on 2003/09/25 by cbrennan@cbrennan_r400_release

Fix bug in DXT1_AS_16 caused by 3d optimization.

Change 123276 on 2003/09/25 by smburu@smburu_r400_linux_marlboro

Testbench improvements.

Change 123275 on 2003/09/25 by smburu@smburu_r400_linux_marlboro

Annotated code with coverage on/off pragmas.

Change 123260 on 2003/09/25 by mmang@mmang_xenos_linux_orl

1.  For Vivian E., added new simd memories and star patch in/out wires.
2.  In vertex thread buffer, fixed bug in simd3 alu state registers.
3.  In pixel thread buffer, fixed bug in simd2/3 cf state read data.
4.  Adjusted simd id bus width for sq to tp tracker.
5.  In sq.v, added vertex shader and pixel shader constant base and
    size connections to simd2/3 alu instruction sequencers.

Change 123223 on 2003/09/25 by dclifton@dclifton_r400

Added PIPE_SEL mux for additional TP_RSP_packed_data, TP_RSP_data_valid, and
SPI_SP_data inputs

Change 123218 on 2003/09/25 by mdesai@mdesai_r400_linux

Fixed tables in tp_offset_adjust
```

```
Removed unused wires

Change 123217 on 2003/09/25 by mdesai@mdesai_r400_linux

Fixed the offset adjust tables
Removed unused logic

Change 123212 on 2003/09/25 by cbrennan@cbrennan_r400_release

Release 3d perf increases.   Revert sctrmx files for synth reasons.

Change 123129 on 2003/09/24 by smburu@smburu_r400_linux_marlboro

Fixes to border-color bugs.

Change 123113 on 2003/09/24 by llefebvr@llefebvr_r400_linux_marlboro

Fixed the autocount pixel timing by removing 5 pipeline registers in the SQ control
path. Also fixed the counter's with back to 17 bits (from 19) int both the vertex and
pixel path such that when it hits the SP it is of the correct 23 bits width (17 bits
count + 2 bits phase + 4 bits index). This fixes r400vgt_multi_pass_pix_shader_01 at
the sqspsx testbench level.

Change 123082 on 2003/09/24 by mearl@mearl_crayola_linux_orl

tb files updated for ONE_PRIM_PER_CLOCK, bug fix in interpolators for
ONE_PRIM_PER_CLOCK

Change 123076 on 2003/09/24 by donaldl@donaldl_xenos_linux_orl

Connected ROM block redundancy signals.
Added sq export address buffer support.

Change 123016 on 2003/09/24 by tien@tien_r400_devel_marlboro

Cleaned up TF_TB border color and xor mask
Modified deps.pl to add LEDA rules to Makefile(s)
Added LEDA rules to Makefile(s)

Change 122991 on 2003/09/24 by dclifton@dclifton_xenos_linux_orl

Moved output register in sp_macc_gpr past phase mux

Change 122989 on 2003/09/24 by dclifton@dclifton_xenos_linux_orl

Moved output register after phase mux in sp_vector

Change 122974 on 2003/09/24 by rmanapat@rmanapat_r400_release
```

Memory/FIFO change for performance

Change 122897 on 2003/09/23 by ctaylor@ctaylor_xenos_linux_orl

Removed 3,6,8 sample MSAA for Xenos. Cleaned up remnants of render state leftover from JSS.

Change 122865 on 2003/09/23 by dougd@dougd_r400_linux_marlboro

fixed typo

Change 122858 on 2003/09/23 by tien@tien_r400_devel_marlboro

1-bpp now pre-RF expanded to 32-bits

Change 122820 on 2003/09/23 by danh@danh_xenos_linux_orl

Added 97 most significant zeros to all auto_count concatenations.

Change 122792 on 2003/09/23 by tien@tien_r400_devel_marlboro

Added coverage override comments around default cases in case statements

Change 122779 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

more changes for cube opcode

Change 122778 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

More changes for cube opcode

Change 122753 on 2003/09/23 by mzini@mzini_crayola_linux_orl

 Added memory swap in VC testbench

Change 122752 on 2003/09/23 by tien@tien_r400_devel_marlboro

Shrunk tpc_tc_fifo
Sync'd generated tp_parameter.mc to .v
A bunch of LEDA fixes/cleanup
SOme cleanup on use of DIM fields (stil using old location for all but tp_lod_deriv)

Change 122720 on 2003/09/23 by smoss@smoss_crayola_linux_orl_regress

   changed SIMD2_PRESENT to VGT_SIMD2_PRESENT until sq hardware catches up

Change 122710 on 2003/09/23 by danh@danh_xenos_linux_orl

```
Registered all ROM_* inputs (Redundant SP control).

Change 122699 on 2003/09/23 by dougd@dougd_r400_linux_marlboro

fix typo (change blocking to non-blocking assignment)

Change 122683 on 2003/09/23 by mearl@mearl_crayola_linux_orl

One primitieve per clock changes in the back of the SC and front of the SQ. Right now,
the ONE_PRIM_PER_CLOCK define in
       header.v and SC_SQ_interface.v are needed for this change. Will update this to
ONEPPC, since this already exists in
       header.v. Also, the sim.cfg file does not have an ifdef, so is hardcoded to one
prim per clock.

Change 122681 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

More cube opcode fixes

Change 122680 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

More cube opcode fixes

Change 122679 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

Many changes for timing, especially using ones comp instead of twos comp in preparation
for exp opcode

Change 122678 on 2003/09/23 by dclifton@dclifton_xenos_linux_orl

Many changes for timing, especially using ones comp instead of twos comp at preparation
for exp opcode

Change 122631 on 2003/09/22 by smoss@smoss_parts_lib_release

   tb_vc changes

   1. changed opened to processed for script
   2. made makefiles more generic

Change 122558 on 2003/09/22 by dougd@dougd_r400_linux_marlboro

1. changed sq_stdrfsdks2p8x104cm1sw0 to sq_stdrfsdks2p8x105cm1sw0 in sq_vc_skid_buf.v
2. added timing fixes to sq_aluconst_mem.v, sq_aluconst_rams.v and
sq_instruction_store.v

Change 122520 on 2003/09/22 by vromaker@vromaker_r400_linux_marlboro
```

```
timing fixes - added registers for vs and ps base and size after the
       context register read mux

Change 122513 on 2003/09/22 by cbrennan@cbrennan_r400_emu

Added in a bit of precision to temporarily match emulator on Z filtering + Mip
filtering.  Will change when both go up one more for mip.
Caught optimization case when wrapping around a NxNx1 texture.

Change 122402 on 2003/09/20 by mmang@mmang_crayola_linux_orl

1.  Added simd2 and simd3 to code.
2.  Added simd2 to synthesized code.
3.  In sq.blk and sq_rbbm_interface, added
    DB_READ_MEMORY, DB_WEN_MEMORY_2, and DB_WEN_MEMORY_3
    to SQ_MISC_DEBUG register.
4.  In header.v, turned on SIMD2_PRESENT.
5.  In sc_packer.v, turned on SIMD2 but don't use it
    with SIMD2_PRESENT_TEMP.
6.  In sq_aluconst_mem.v, sq_aluconst_top.v, sq_cfc.v,
    and sq_instruction_store.v, hooked up DB_WEN_MEMORY_2
    and DB_WEN_MEMORY_3 to appropriate SIMD2/3 memories.
7.  In sq_export_alloc.v, handle position/main export id
    and parameter cache thread base for simd2/3.  Be able
    to handle one type down simd0/1 and a different type
    down simd2/3 on the same clock.
8.  In sq_pix_ctl.v and sq_vtx_ctl.v, multiple simd
    gpr_alloc blocks return different acks, gpr bases,
    and gpr maxes.
9.  In sq_exp_alloc_ctrl.v, handle position/main export
    buffer management.  Be able handle one type down
    simd0/1 and a different type down simd2/3 on the same
    clock.
10. In sq_pix_thread_buff.v and sq_vtx_pix_thread_buff.v,
    added muxing and memories to handle status bits, cfs
    state, and alu state.  Simd2 mirrors simd0, while
    simd3 mirrors simd1.
11. In sq_status_reg.v, added simd2/3 arb requests and
    status bit writing from simd2/3.
12. In tb_sqsp.v, fixed some bugs related to pspv_wr_en,
    pred_override, const_addr, and const_valid hook ups.
13. In tbtrk_spsx.v, SIMD_PRESENT conditional delaying
    and management of thread_id and thread_type for
    tracker.
14. In tbtrk_sq_pix_rs_input.v and tbtrk_sq_vtx_rs_input.v,
    temporary klug to hook up b0b1_predicate instead of
    predicate.
```

15. In tbtrk_sq_sp_vec_gpr.v, added simd2/3 tracking of
    gpr_int_wen interface.
16. In sq_tex_instr_queue.v, get gpr_max from appropriate
    simd data.<enter description here>

Change 122323 on 2003/09/19 by chammer@chammer_xenos_linux_orl

Fixed sc_sx tracker for non-rts case, was not checking properly

Change 122289 on 2003/09/19 by donaldl@donaldl_crayola_linux_orl

Qualified the perf outputs (scis_discard, bb_discard, & supert_discard)
with pipe_rts_elat1 so they become known during reset.

Change 122286 on 2003/09/19 by jayw@jayw_r400_linux_marlboro

Latest depth and support ifdefed out for detail bus removal.

Change 122272 on 2003/09/19 by tien@tien_r500_emu

Hooked up new dim field for tp_lod_deriv
We should be able to start banging away at cubic now...

Change 122201 on 2003/09/19 by mdesai@mdesai_r400_linux

Fixed aniso table entry
Fixed 3D denorm case
Combined Z for cases where z0_texel and z1_texel were the same

Change 122180 on 2003/09/19 by smoss@smoss_crayola_linux_orl_regress

   changed final result message

Change 122072 on 2003/09/18 by donaldl@fl_donaldl_p4

Forced iST_LAST_PIXEL going to sc_pipe to zero to get vectors to work.

Change 122029 on 2003/09/18 by cbrennan@cbrennan_r400_release

Release multiple input port fix.

Change 122020 on 2003/09/18 by vbhatia@vbhatia_r400_linux_marlboro

Initial checkin for a focused random addresser test

Change 122009 on 2003/09/18 by cbrennan@cbrennan_r400_release

Changed parentesis grouping. Was there for timing, but no longer needed. Was

```
potential synth/sim error if sign wasnt extended.

Change 121991 on 2003/09/18 by dclifton@dclifton_r400

First draft of redundant sp block

Change 121972 on 2003/09/18 by smburu@smburu_r400_linux_marlboro

Xenos RSP logic. Also tp_lerp clean-up.

Change 121958 on 2003/09/18 by kmeekins@kmeekins_xenos_linux_orl

Reverse integrated the changes from vc_cc_delay branch spec into the r400 depot.

Change 121905 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Fixes for cube opcode

Change 121904 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Fixes for cube opcode

Change 121902 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Corrected face id definition for cube opcode

Change 121901 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Lots of fixes for cube opcode

Change 121900 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Lots of fixes for cube opcode

Change 121899 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Change in structure to improve timing

Change 121898 on 2003/09/17 by dclifton@dclifton_crayola_linux_orl

Change in structure to improve timing

Change 121784 on 2003/09/17 by bhankins@bhankins_xenos_linux_orl

point to sx files in /proj/xenos

Change 121748 on 2003/09/17 by mmantor@FL_mmantorLT_r400_win
```

<updates to the tb_vector testbench>

Change 121731 on 2003/09/17 by rramsey@RRAMSEY_P4_r400_win

add runtime to report
update spreadsheet with 9/17/2003 results

Change 121684 on 2003/09/16 by tien@tien_r400_devel_marlboro

COnnected up gradient exponent adjusts

Change 121643 on 2003/09/16 by cbrennan@cbrennan_r400_emu

Found bug that was considering a large re-normalize a zero condition too early in the aniso add.

Change 121639 on 2003/09/16 by tien@tien_r400_devel_marlboro

Added tp_pre_rf after tp_border to RF expand border color

Change 121629 on 2003/09/16 by danh@danh_crayola1_linux_orl

Removed XY pipe delay, XY data is now processed by the interpolators

Change 121559 on 2003/09/16 by tien@tien_r500_emu

Reverse order of TP (vfetch and tfetch) const

Change 121537 on 2003/09/16 by smoss@smoss_crayola_linux_orl_regress

   increasing interface idle timeout for randoms

Change 121477 on 2003/09/16 by cbrennan@cbrennan_r400_release

Release all branched C1 tc changes. VC interface removal. Second MC data pair is gone. Kinky degamma.

Change 121380 on 2003/09/15 by jayw@jayw_r400_linux_marlboro

MRT change and latest stuff from John.

Change 121377 on 2003/09/15 by mdesai@mdesai_r400_linux

Added interlaced format bit

Change 121376 on 2003/09/15 by mdesai@mdesai_r400_linux

Fixed the channel add to tfetch ops

```
Change 121348 on 2003/09/15 by dougd@dougd_r400_linux_marlboro

1. corrected the trigger events for VTX_SWAP_IN, VTX_SWAP_OUT,
   PIX_SWAP_IN, PIX_SWAP_OUT, CONSTANTS_USED_SIMD0 and  CONSTANTS_USED_SIMD0.
2. made event counters for these used multibit increment values
3. added  "+incdir+$PARTS_LIB/src/gfx/sp" to vcs_top.ini to pick up
   sp_defines.v included in sq_ais_output.v

Change 121332 on 2003/09/15 by rramsey@rramsey_crayola_linux_orl

Change pix_ctl so deallocs with real pixel vectors don't free param
cache space until interpolation is almost complete
Wire up the vc_sp valid signals correctly
Fix sx_sp_pcdata tracker

Change 121326 on 2003/09/15 by bhankins@bhankins_crayola_linux_orl

Add a pipeline in the generation of the alignment bits for
   memory exports to improve on timing.

Change 121325 on 2003/09/15 by bhankins@bhankins_crayola_linux_orl

Recode redundancy select to try and improve on timing.

Change 121311 on 2003/09/15 by cbrennan@cbrennan_r400_release

Fixes mip 3d..  May have also fixed (or broken) mip aniso, but they havent passed yet
either.

Change 121308 on 2003/09/15 by tien@tien_r400_devel_marlboro

Partial coding of early_is_cube_map
Reverse priority of 1st valid pixel 0..3 for SetGradients*
Fix gradients being used for getset

Change 121295 on 2003/09/15 by mdesai@mdesai_r400_linux

Added interlaced bit

Change 121292 on 2003/09/15 by vromaker@vromaker_r400_linux_marlboro

fixed incorrect loading of loop indices from the thread buffer into
the ctl flow sequencer; this was causing a problem with the test
r400sq_const_index_07

Change 121285 on 2003/09/15 by bhankins@bhankins_crayola_linux_orl
```

```
Add thread id and type

Change 121278 on 2003/09/15 by dclifton@dclifton_r400

Added to SQ include directory list

Change 121219 on 2003/09/14 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 121175 on 2003/09/13 by smoss@smoss_parts_lib_release

   added some missing sensitivity list signals

Change 121157 on 2003/09/13 by smoss@smoss_crayola_linux_orl_regress

   xenos updates

Change 121067 on 2003/09/12 by cbrennan@cbrennan_r400_release

Lengthen the TP_TPC fifo by 1 to allow the aligner to operate on the last entry and not
cause an TP_TPC fifo written when full error.

Change 121065 on 2003/09/12 by donaldl@donaldl_crayola_linux_orl

Registered ROM_EN_RSP and ROM_PIPE_SEL[3:0].

Change 121057 on 2003/09/12 by dclifton@dclifton_crayola_linux_orl

I/O change for VC_SP_data_valid

Change 121038 on 2003/09/12 by tien@tien_r400_devel_marlboro

Aniso fix for when step > max step due to different max step on each TP

Change 120968 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

Updates to simd_id for the sx inteface to use the id sent from the vgt.
   Also, add support for up to four simds.

Change 120910 on 2003/09/12 by donaldl@donaldl_crayola_linux_orl

Removed SPtoSQ kill_type and kill_valid signals and added them internally
in the SQ.  Done to save some gates and also to avoid having to add
redundancy logic to them.

Change 120906 on 2003/09/12 by mdesai@mdesai_r400_linux
```

```
Added Border texels
Added GetCompTexLod and GetGradiants
Added vtx_channel to Vertex Fetches

Change 120895 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

remove some debug logic

Change 120894 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

Fix typo

Change 120887 on 2003/09/12 by bhankins@bhankins_crayola_linux_orl

-  Add sx_mem_export.v module to capture pixel addresses and
       calculate rb id values for use in export to memory.
   -  Add support for redundancy logic.  Inputs are currently
      tied low in tb_sqsp.v and chip_sx.tree.
   -  Add non-synthesizable logic to route thread id and thread
      type from sq through sx and out to rb for test.  Allows
      tracker to identify export to memories, and to distinguish
      between them.  Tied low in chip_sx.tree and tb_sqsp.v
      All associated I/O and logic is qualified on `ifdef SIM.
   -  Remove the register in sx_export_control_common.v that was
      requiring some signals on the sq alloc interface to be present
      one clock before the valid.  Now, all sq_sx_exp_ signals are
      expected to be valid only when sq_sx_exp_valid == 1.
   -  Add a register in the generation of the final pixel address
      value for export to memory, to try and improve on timing.

Change 120857 on 2003/09/11 by jayw@jayw_r400_linux_marlboro

MRT changes `ifdefed, plus a blender and depth MS change update and RC for 2pipe

Change 120802 on 2003/09/11 by tien@tien_r400_devel_marlboro

RF expand 2_10_10_10_AS_16_16_16_16 fix
max aniso cycles fix

Change 120766 on 2003/09/11 by chammer@chammer_crayola_linux_orl

BC_SC_rtr is now tied at the chip level and can be driven in the SC testbench.

Change 120750 on 2003/09/11 by tien@tien_r400_devel_marlboro

FIxed the mult to actually work..

Change 120727 on 2003/09/11 by vbhatia@vbhatia_r400_linux_marlboro
```

```
Fixed gen30

Change 120722 on 2003/09/11 by bhankins@bhankins_crayola_linux_orl

Put known junk values on SQ_SX_exp_ interface signals when SQ_SX_exp_valid==0

Change 120720 on 2003/09/11 by mdesai@mdesai_r400_linux

added clampx, clampy, clampz to vfetch
<enter description here>

Change 120719 on 2003/09/11 by kevino@kevino_r400_win_marlboro

Update to table.pl and table_default.txt to split data case statements into 2 seperate
32 way case statmenments based on tx_fmt[4:0].  The output is then selected based on
Tx_fmt[5].  Note that the "same as" cases are handled differently than the other
generated blocks (and how  this block used to do it.)   Since some texture formats >32
were the same as some <32, this was causing complications with using several cases on
one line (e.g. 6'd07, 6'd33, ...)  since 33 should be in the second case statement.  To
resolve this, there is a first always block that remaps the same as cases to the
texture format they are the same as (so 6'd33 gets replaced by 6'd07).  The Tx_fmt
decode in the two case statements then is based on this remapped tex format (MTx_fmt).

    Note that I visually inspected the resulting code from these updates, but have not
tried to compile this code yet.  Only the script taht generates the verilog is part of
ths check in.  Any fixes to the script and the new generated verilog files will be
checked in under a different changelist.

Change 120717 on 2003/09/11 by tien@tien_r400_devel_marlboro

Refreshed Makefiles
Added fast bvrl option to deps.pl
Cleaned up tpc_walker, esp state_rts
Got rid of x-prop on Set* opcodes in lod_deriv
Loading proper gradients for SetTexLOD

Change 120715 on 2003/09/11 by tien@tien_r500_emu

Half of the lod_grad IO shrink change
Aniso control fix

Change 120672 on 2003/09/11 by vbhatia@vbhatia_r400_linux_marlboro

updated for aniso_walk_enable bits and added a few more randomized tests

Change 120647 on 2003/09/11 by smburu@smburu_r400_linux_marlboro
```

```
Fixes for bug 2674.

Change 120646 on 2003/09/11 by cbrennan@cbrennan_r400_release

Pipe pixmask down the lod logic so that mip, aniso and z walking can be optimized out
if the pixel is invalid.

Change 120645 on 2003/09/11 by rramsey@rramsey_crayola_linux_orl

Remove some unused defines
Add reset condition for primdata pipe stages in qdpr_proc
Fix a bug with tp_count in fetch_arb when running with the VC
Increase loop_cnt for vc inject in tb_sqsp

Change 120631 on 2003/09/11 by chammer@chammer_crayola_linux_orl

Added SC_BC ports to chip_sc.tree as UNCONNECTED, tied BC_SC_RTR to 1

Change 120592 on 2003/09/10 by vromaker@vromaker_r400_linux_marlboro

changed SQ_hs_bclk, TST_SQ_rf_star_wrck, TST_SQ_hs_star_wrck so they
       are defined without the [0:0] range

Change 120521 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Added new scalar opcode definitions

Change 120510 on 2003/09/10 by vromaker@vromaker_r400_linux_marlboro

fix for SQ_VC_simd_id typo

Change 120426 on 2003/09/10 by donaldl@donaldl_crayola_linux_orl

Added redundancy logic.

Change 120423 on 2003/09/10 by donaldl@donaldl_crayola_linux_orl

Added redundancy logic.

Change 120403 on 2003/09/10 by dclifton@dclifton_r400

Conditioned tp_sp_data_valid with gpr_phase for writes to gprs.  Enabled NEGATE signal
to scalar for SC_SUB_CONST_* opcodes

Change 120402 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Fixed neg zero plus neg zero.  Conditioned pred execute with valid ops
```

```
Change 120401 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Fixed neg zero plus neg zero.  Conditioned pred_execute output for active opcode.

Change 120400 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

Eliminated sign modifiers from prev opcodes for previous scalar operand

Change 120399 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

MOVA and MOVA_FLOOR two operand inst. now

Change 120398 on 2003/09/10 by dclifton@dclifton_crayola_linux_orl

MOVA and MOVA_FLOOR now two operand inst.

Change 120397 on 2003/09/10 by rramsey@rramsey_crayola_linux_orl

Add code to keep the vc and tp inject routines from clobbering each other
Fix vc inject routine so it handles formats that require double returns

Change 120333 on 2003/09/09 by tien@tien_r400_devel_marlboro

Fix for state machine part of bugzilla #2659
Fix for 2_10_10_10_AS_16_16_16_16 and 4444 when channels are degamma'd

Change 120331 on 2003/09/09 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 120327 on 2003/09/09 by smburu@smburu_r400_linux_marlboro

Put new Mktree option -#params.

Change 120296 on 2003/09/09 by dougd@dougd_r400_linux_marlboro

added `include "register_addr.v"

Change 120270 on 2003/09/09 by llefebvr@llefebvr_r400_linux_marlboro

Now reading the SIMD_ID from the dump in the tracker. Not doing anything with it
however. It is just read in order to get to the valid data after it.

Change 120256 on 2003/09/09 by smburu@smburu_r400_linux_marlboro

Changed tp_ch_blend to a verilog block, used to be an MC. This
change depends on Jocelyns changelist 120254.
```

```
Change 120190 on 2003/09/09 by dougd@dougd_r400_linux_marlboro

changed SQ_RB_event to SQ_RB_event_pulse and declared as output from sq.v

Change 120187 on 2003/09/09 by rramsey@rramsey_crayola_linux_orl

checking in more of scott's vgt fixes:
       vgt_out_indx.v -- No logical change. Added an "Assert" to check assumption.
vgt_output.v -- Fix to SIMD select logic.

Change 120186 on 2003/09/09 by jayw@jayw_r400_linux_marlboro

Latest pipe disable code and depth updates for MS.

Change 120144 on 2003/09/09 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 120137 on 2003/09/09 by chammer@chammer_crayola_linux_orl

Added control to force invalid quads' data to zero, this is necessary because
 there are no "valids" on the SC to BC interface.

Change 120087 on 2003/09/08 by dougd@dougd_r400_linux_marlboro

Fixed 2 bugs in Real Time address logic in aluconst.
Added correct default value for INST_BASE_VTX in sq_rbbm_interface.v
Fixed bug in Real Time write data buffer in sq_instruction_store.v
Added missing input/output declarations for SIMD2 & SIMD3 signals to sq_aluconst_top.v
Clean up missing SIMD2, SIMD3 wire declarations in sq.v for the aluconst, is and cfc

Change 120051 on 2003/09/08 by rmanapat@rmanapat_r400_release

Fix for 1d formats where tr goes to ee

Change 120047 on 2003/09/08 by dclifton@dclifton_r400

Start of testbench for vector unit

Change 120039 on 2003/09/08 by smburu@smburu_r400_linux_marlboro

Change tp_ch_blend from a MC design to a verilog one.

Change 120029 on 2003/09/08 by tien@tien_r400_devel_marlboro

Fix for port leak that Jay W. sent mail about
Changes to my rt1 test run wrapper :-)  I'm so lazy...
```

```
Change 119992 on 2003/09/08 by rramsey@rramsey_crayola_linux_orl

Add last_pixel logic to SC
Duplicate a bit in the qpp to help fanout

Change 119982 on 2003/09/08 by vromaker@vromaker_r400_linux_marlboro

added defaults to case statements

Change 119944 on 2003/09/08 by rmanapat@rmanapat_r400_release

Added missing formats

Change 119853 on 2003/09/06 by rramsey@rramsey_crayola_linux_orl

Changes to make quad processing resources programmable

Change 119852 on 2003/09/06 by rramsey@rramsey_crayola_linux_orl

Check in Scott's changes for the vgt:

       The current design of the VGT results in the restriction that all
       the simd sets must have the same number of active pipes (with the exception
       of simd pipes that are completely disabled). The emulator does not have
       this restriction (each simd set can have a different number of active
       pipes). If the hardware attempts to run a vector set and the non-zero
       simd pipe sets are different, then the hardware will print an error message
       and assert.

       Connected the SIMD output from VGT.
       Moved the logic for the ROM_BAD_PIPE_DISABLE signals from the vgt_vtx_reuse
block to the vgt_output block.

Change 119747 on 2003/09/05 by danh@danh_crayola1_linux_orl

Removed SQ_SP_interp_mode, SQ_SP_interp_buff_swap, added all SPI Redundant SP
ports/connections.

Change 119746 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed interp_buff_swap

Change 119745 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed sq_spi_interp_mode, sq_spi_buff_swap

Change 119742 on 2003/09/05 by danh@danh_crayola1_linux_orl
```

removed SQ_SP_interp_mode, SQ_SP_interp_buff_swap, added all Redundant SP ports and logic.

Change 119736 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed SQ_SP_interp_mode, SQ_SP_interp_buff_swap, added SQ_SP_interp_simd_id for Redundant SP

Change 119733 on 2003/09/05 by danh@danh_crayola1_linux_orl

removed SQ_SP_interp_mode, added SQ_SP_interp_simd_id for Redundant SP capability.

Change 119720 on 2003/09/05 by vbhatia@vbhatia_r400_linux_marlboro

Updated for is_set_lod and is_set_grad addition, also clamped z'outs for gen's > 24

Change 119694 on 2003/09/05 by cbrennan@cbrennan_r400_release

Had meaning of swapSandT inverted.

Change 119679 on 2003/09/05 by tien@tien_r400_devel_marlboro

Added ANISO_WALK bits to control tp_lod_aniso
Put in mux's to select 1st valid pixel for SetGradients opcodes in tp_lod_deriv

Change 119672 on 2003/09/05 by jayw@jayw_r400_linux_marlboro

Weekly release. need to pull into rb_branch other top level stuff next.

Change 119637 on 2003/09/05 by cbrennan@cbrennan_r400_release

Deleted bit of code that detects of one of the inputs was 0 and muxes the other's mantissa straight through
because it falls out naturally from the subtract and normalize,
and it buys me the normalization of an non-normalized input for free when cube mapping.
Deleted it from the other subtractor because it reduced area.

Change 119636 on 2003/09/05 by cbrennan@cbrennan_r400_release

Add FAST_BVRL make or environment flag for selecting quick mc compile

Change 119539 on 2003/09/04 by vbhatia@vbhatia_r400_linux_marlboro

cube map related update to standalone lod_deriv testbench

Change 119519 on 2003/09/04 by smoss@smoss_crayola_linux_orl_regress

   increased watchdog timeout by x10

Change 119508 on 2003/09/04 by vbhatia@vbhatia_r400_linux_marlboro

cube map related fix

Change 119496 on 2003/09/04 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 119475 on 2003/09/04 by chammer@chammer_crayola_linux_orl

Added four quad per clock interface between SC and BC.

Change 119457 on 2003/09/04 by dclifton@dclifton_r400

added sq_export_blocker to makefile
Fixed TP_SP_data_valid signal

Change 119448 on 2003/09/04 by tien@tien_r400_devel_marlboro

Updated the Makefiles using deps.pl

Change 119440 on 2003/09/04 by cbrennan@cbrennan_r400_release

Fix to walker to allow last cycles of data to flow out after fifo has read out last
control vector.

Change 119439 on 2003/09/04 by cbrennan@cbrennan_r400_release

Add clamp to 1 logic when calculating mipped sizes to allow oblong textures to not wrap
to huge.

Change 119422 on 2003/09/04 by mmang@mmang_crayola_linux_orl

removed vc_sp for now

Change 119421 on 2003/09/04 by cbrennan@cbrennan_r400_release

Woops.. didnt mean to check in the change to timing iterations for mc files.
Backed it out.

Change 119407 on 2003/09/04 by smburu@smburu_r400_linux_marlboro

Changed width of out_rtl.

Change 119393 on 2003/09/04 by smoss@smoss_crayola_linux_orl_regress

   disable grouper tracker always

```
Change 119376 on 2003/09/04 by cbrennan@cbrennan_r400_emu

Added cube map fixes to hardware.
Cube maps now require a range of 1.0 to 2.0 from the shader to work properly.
Coord has 1.0 subtracted from it, then is clamped from 0.0 to 1.0 in the TP.
tp_input.v and tp_addresser still need to move cube_map enable from dim to opcode to
begin testing them.

Change 119369 on 2003/09/04 by rramsey@RRAMSEY_P4_r400_win

fix sensitivity list probs

Change 119359 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Carrysave on final mult to improve timing

Change 119358 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Carrysave on final mult to improve timing

Change 119357 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Fixed w0 bug with clipped lines

Change 119356 on 2003/09/04 by dclifton@dclifton_crayola_linux_orl

Fixed w0 bug with clipped lines

Change 119294 on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro

- instatiation of sq export blocker at sq top level
- thread buffer timing fix related to status read/export count update

Change 119241 on 2003/09/03 by smburu@smburu_r400_linux_marlboro

Optimization of the data format decoding.

Change 119240 on 2003/09/03 by smburu@smburu_r400_linux_marlboro

Modified tp_tt so that there is now only one instance needed and
it is pipelined into 2 adder stages. The first stage is in tp_blend_mux.

Change 119233 on 2003/09/03 by tien@tien_r400_devel_marlboro

Final predicate check-in.
I ran the release_parts_lib.pl scripts TWICE before chekcing this in LOL
```

```
Change 119195 on 2003/09/03 by vromaker@vromaker_r400_linux_marlboro

new file for arbitrating between exporting threads

Change 119162 on 2003/09/03 by viviana@viviana_crayola2_syn

Memories for ONEPPC.

Change 119127 on 2003/09/02 by dougd@dougd_r400_linux_marlboro

Added the extra memories and their support to the instruction and
constant stores to support 4 SIMD's. These memories and their
required wiring and control are instantiated with `ifdef and use
the SIMDn_PRESENT macros defined in header.v
Removed the use of SIMD1 macro.

Change 119123 on 2003/09/02 by jayw@jayw_r400_linux_marlboro

Latest depth changes.

Change 119064 on 2003/09/02 by viviana@viviana_crayola2_syn

Changed the memories to include internal register.

Change 119023 on 2003/09/02 by ctaylor@ctaylor_crayola_linux_orl

Removal of JSS basics

Change 118988 on 2003/09/02 by bhankins@bhankins_crayola_linux_orl

- Pull position export buffer out as a separate memory.  Read-side access of pixel
buffer by the
     rb's no longer competes with pa read access of the position buffer.
   - Increase size of pixel buffer memory to 128.
   - Add hooks to control logic to use all 128 locations once the sq logic is ready.
     For now, only first 112 locations are used.
   - Split memory test into two pieces with two test processors.
   - Add hooks to use second memory test processor.  For now, only one is used, and the
sx i/o is
     unchanged from previous checkins.
   - Add new and remove obsolete memories.

Change 118941 on 2003/08/31 by tien@tien_r400_devel_marlboro

One or two more checkins and predicate should be there

Change 118931 on 2003/08/31 by tien@tien_r400_devel_marlboro
```

```
Fixed assignment of pix_mask.
Together with rebuilding my area from scratch, this should help.

Change 118908 on 2003/08/31 by tien@tien_r400_devel_marlboro

More intermediate changes for predicate

Change 118890 on 2003/08/30 by tien@tien_r500_emu

COrrected defines/params for opcodes
updated opcode logic to use new params

Change 118878 on 2003/08/30 by rramsey@rramsey_crayola_linux_orl

fix a deadlock condition between the input arb and vtx input controller

Change 118760 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Added registered outputs

Change 118759 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Added registered outputs

Change 118757 on 2003/08/29 by tien@tien_r400_devel_marlboro

Fix for 2_10_10_10_AT_16_16_16_16 RF expand of the 2-bit channel

Change 118743 on 2003/08/29 by viviana@viviana_crayola2_syn

Configuration file to build the virage memories with a register in the
   320x32 cfc memory.

Change 118694 on 2003/08/29 by rramsey@rramsey_crayola_linux_orl

changes for random backpressure

Change 118688 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

update for 3 simds

Change 118687 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

update for 3 simds

Change 118686 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

update for 3 simds
```

```
Change 118685 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

update for 3 simds

Change 118684 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Update for 3 simds

Change 118683 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Update for 3 simds

Change 118682 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Connected up upper VC_SP_simd bit

Change 118681 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Latest virage build

Change 118680 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Latest virage build

Change 118679 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Fixed cube opcode

Change 118678 on 2003/08/29 by dclifton@dclifton_crayola_linux_orl

Fixed cube opcode

Change 118677 on 2003/08/29 by smoss@smoss_crayola_linux_orl_regress

   included cp_r, corrected build error check

Change 118645 on 2003/08/28 by smoss@smoss_crayola_linux_orl_regress

   increased size of valid to 4 bits

Change 118622 on 2003/08/28 by llefebvr@llefebvr_r400_emu_montreal

Modified the Orlando trackers to only compare valid channels. This replaces the
0xDEADDEAD values we had previously. Note that any uninitialized channel will generate
a tracker warning still.
 Modified interfaces are:
```

1) SX->SP parameter cache data
2) SP->SX
3) SX->RB

I left alone the SX->PA interface as we did not have problems over it. The qualifiers are there however if anyone wants to do it.

Change 118590 on 2003/08/28 by bbuchner@bbuchner_crayola_linux_orl

fixed two channel mode to allow fully indpendent behavior on the two channels.

Change 118589 on 2003/08/28 by vromaker@vromaker_r400_linux_marlboro

- fix for loop index clamping and constant address generation (both index and offset relative)
- changed the connection of the real time bit such that it now goes directly from the AIQ to the
  AIS output mux (and not thru the AIS)
- sq_tests.simple_reg_indexing tests now pass

Change 118581 on 2003/08/28 by dclifton@dclifton_r400

tied the upper bit of sq_tp_trk_simd_id low.

Change 118490 on 2003/08/28 by dclifton@dclifton_r400

Clean up of unused signals, fix of STAR signals in sp.v

Change 118400 on 2003/08/27 by donaldl@donaldl_crayola_linux_orl

Pipelined vtx_ptr_valid to qualify wrap control signals.

Change 118398 on 2003/08/27 by donaldl@donaldl_crayola_linux_orl

Updated number of skid words for primfifo to 2 to prevent overflow of mem writes.
Placed common bit assignments for PA_SC signals outside ONEPPC ifdef to get around synthesis errors.

Change 118397 on 2003/08/27 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 118326 on 2003/08/27 by tien@tien_r400_devel_marlboro

Final changes for simd expansion to 2 bits

Change 118215 on 2003/08/26 by vromaker@vromaker_r400_linux_marlboro

```
changed define for SQ_VC_MINI_MAXCOUNT from 16 to 32

Change 118200 on 2003/08/26 by rramsey@rramsey_crayola_linux_orl

Increase number of clks the tp_sq inject routine can loop through input data
Fix a problem with the sx_rb color tracker when the sx sends 0 mask quads, or
the rb kills quads

Change 118187 on 2003/08/26 by tien@tien_r400_devel_marlboro

Added pix_mask output, dangling atm.
Cleaned up aligner fifo output.

Change 118178 on 2003/08/26 by rmanapat@rmanapat_r400_release

Changed a debug register bit to use a flopped version of a signal
instead of the non-flopped version

Change 118171 on 2003/08/26 by rramsey@rramsey_crayola_linux_orl

update quad_select compare for q1 so it works with the 4qd/clk changes

Change 118163 on 2003/08/26 by bhankins@bhankins_crayola_linux_orl

   1. Initial checkin of code added to support export-to-memory.  This code is only
partially tested, and not at all optimized yet.
   2. Start to add (dum_mems only) for separate position export memory to split
position and color into two separate memories.
      pos is 16dx128wx16, pix has the full 128dx128wx16, but logic still wraps at 112
for sq compatibility for now.
   3. Split up read-side arbitration to give pa full access to pos buffer, while the
rb's compete only among themselves for the color buffer.

Change 118142 on 2003/08/26 by smburu@smburu_r400_linux_marlboro

Pipelining change for timing reasons.

Change 118139 on 2003/08/26 by tien@tien_r500_emu

MOre pix_mask stuff for predicate handling

Change 118130 on 2003/08/26 by dclifton@dclifton_r400

Added tbtrk_sqvc, fixed vector engine assignments.

Change 118129 on 2003/08/26 by dclifton@dclifton_r400

Fixed bug in adder.
```

```
Change 118128 on 2003/08/26 by dclifton@dclifton_r400

Added definable # of simd's to sp.

Change 118127 on 2003/08/26 by dclifton@dclifton_crayola_linux_orl

Fixed max pos clamp on const addr.  Eliminated some registers in export scalar fog
path.

Change 118107 on 2003/08/25 by jayw@jayw_r400_linux_marlboro

Some surface sync logic added, untested.  Some code clean up in szmask processing in
RBT. Fix for HiZ.

Change 118087 on 2003/08/25 by smburu@smburu_r400_linux_marlboro

Packed format fixes.

Change 118084 on 2003/08/25 by tien@tien_r400_devel_marlboro

More fixes for tp_unsigned32_01 T2D....
The data still mismatches, but it's an EMU issue.
(Hopefully, this is the only bug left)
:
(This test with aniso turned on would be the mother of all TPC tests)

Change 118059 on 2003/08/25 by mdesai@mdesai_r400_linux

Fixed 3D Ws calculations

Change 118058 on 2003/08/25 by mdesai@mdesai_r400_linux

Added the z1 texel and fixed the 3D Ws output along with several other minor fixes

Change 118057 on 2003/08/25 by mdesai@mdesai_r400_linux

Fixed the 3D Ws outputs
<enter description here>

Change 118047 on 2003/08/25 by rmanapat@rmanapat_r400_release

Fix to tp_fetch where not all the ports for tp_pre_rf
were connected...basically added the missing ports (format_comp_*
inputs)

Change 118032 on 2003/08/25 by tien@tien_r500_emu
```

```
More changes for simd and pix_mask, not done yet, this is just the easy stuff

Change 118022 on 2003/08/25 by mzini@mzini_crayola_linux_orl

Bumped instruction fifo depth to 32

Change 118021 on 2003/08/25 by mzini@mzini_crayola_linux_orl

 Added support for 2 or 4 memory return paths.

Change 118013 on 2003/08/25 by tien@tien_r500_emu

Partial checkin 2-bit simd and full pix_mask pipelineing
(Not all the way thru yet) :-)

Change 118011 on 2003/08/25 by tien@tien_r400_devel_marlboro

More fixes for aligner issue.  Bah I don't think it works yet
Added shortcut to cd into emu_ area in projdirs
Used explicite port map to avoid issue that Steve M. found in pre_rf

Change 117993 on 2003/08/25 by bbuchner@bbuchner_crayola_linux_orl

rebuild of memories

Change 117974 on 2003/08/25 by smoss@smoss_crayola_linux_orl_regress

   incorrect define

Change 117957 on 2003/08/25 by dougd@dougd_r400_linux_marlboro

Fixed some wiring errors in the wrapper that prevented some counters from working.

Change 117937 on 2003/08/24 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 117874 on 2003/08/22 by tien@tien_r400_devel_marlboro

More stuff dealing with aligner and odd-sized maps

Change 117861 on 2003/08/22 by mdesai@mdesai_r400_linux

What was CL117848, but forced manaul resolve with Ws stuff Steve submitted
earlier.

Change 117814 on 2003/08/22 by bbuchner@bbuchner_crayola_linux_orl
```

```
added ifdef code that will build a two channel version of the VC

Change 117741 on 2003/08/22 by smburu@smburu_r400_linux_marlboro

Signed RF bug fix.

Change 117737 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<added simd_id between vgtmod injector and the pa for test bench>

Change 117706 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<added new ports and/or expanded to two bits to vgt, sq, and pa for simd_id with
modifications to their test benches and added
    ifdefs with bad pipe signals to input of vgt, replaced SIMD1 macro with
SIMD1_PRESENT macro in the SC files>

Change 117704 on 2003/08/22 by mmantor@mmantor_crayola_linux_orl

<Fixed conflict between vec_3op_no_swap and scalar_const_op to control swizzle
correctly for the scalar engine and deliever the special gpr read  address  created in
the sq_ais_output block>

Change 117645 on 2003/08/21 by bbuchner@bbuchner_crayola_linux_orl

use behavioral mems

Change 117631 on 2003/08/21 by vromaker@vromaker_r400_linux_marlboro

- fix for VC_SQ_data_rdy (this was being asserted too often, but did not
         cause any of the tests to fail...)

Change 117627 on 2003/08/21 by vromaker@vromaker_r400_linux_marlboro

VC tracker added to tb_sqsp

Change 117605 on 2003/08/21 by jayw@jayw_r400_linux_marlboro

Depth fixes and unknown color (MS?) fixes.

Change 117594 on 2003/08/21 by tien@tien_r400_devel_marlboro

Forgot to add this one

Change 117593 on 2003/08/21 by jayw@jayw_r400_linux_marlboro

unused signal.
```

```
Change 117592 on 2003/08/21 by tien@tien_r400_devel_marlboro

Added perfect RF expansion for signed numbers

Change 117515 on 2003/08/21 by smburu@smburu_r400_linux_marlboro

Fixes for 16/32b rf; introduced TT_HI_ch bits.

Change 117514 on 2003/08/21 by omesh@omesh_r400_linux_marlboro_tott

Added the tracker for chip level RB read/write tests.

Change 117504 on 2003/08/21 by mmang@mmang_crayola_linux_orl

1.  Increased simd_id wires to 2 bits throughout SQ.  SQ external
    interfaces are still only 1 bit.
2.  Made SQ simd 1 blocks conditional based on SIMD1_PRESENT in
    header.v.  Realigned some code in anticipation of SIMD2 and SIMD3.

Change 117483 on 2003/08/21 by cbrennan@cbrennan_r400_release

Released C1 ifdef'd out features and first cut at kinky degamma just cuz i was running
a sanity anyway.

Change 117464 on 2003/08/21 by jayw@jayw_r400_linux_marlboro

Latest RB & DB code.

Change 117456 on 2003/08/21 by donaldl@donaldl_crayola_linux_orl

Enabled for one primitive per clock performance.

Change 117446 on 2003/08/21 by dclifton@dclifton_r400

Changes for synthesis--removed unused pins from sp_comp_opcodes and sp_macc32_multiply.
Tweaked input delays on spi_hi_prec_int.

Change 117379 on 2003/08/20 by tien@tien_r400_devel_marlboro

2nd half of aligner-related fix.
Hmm, may need more changes, I just thought of something :-(

Change 117311 on 2003/08/20 by rramsey@rramsey_crayola_linux_orl

Changes to sc for 4 qd/clk picker in KILL_ALL_PIXELS mode
Check in sc memory updates for Vivian
Add some missing connections in sqsp to fix compile warnings
Go to a global define for all trackers to control x vs 0 mismatch/warning
```

(MISMATCH_X_VS_0)

Change 117275 on 2003/08/20 by jayw@jayw_r400_linux_marlboro

removing RB/depth files, all unused, been moved to db/depth. fixed system_dp.vcpp to remove db_depth_slope_to_pixel.v

Change 117233 on 2003/08/20 by tien@tien_r400_devel_marlboro

Fix for early RTS in tpc when tpc_aligner needs to multicycle

Change 117175 on 2003/08/19 by tien@tien_r400_devel_marlboro

1st half proper rts after aligner fix

Change 117140 on 2003/08/19 by donaldl@donaldl_crayola_linux_orl

Updated for one primitive per clock but ifdef'd currently to work
as one primitive every 2 clocks.

Change 117110 on 2003/08/19 by jayw@jayw_r400_linux_marlboro

Latest RB & DB code. Tested agains RELEASE_116888

Change 117103 on 2003/08/19 by donaldl@fl_donaldl_p4

Changed PA_SC_phase bit width back to 2. The msb will be used to determine a clip primitive.

Change 117091 on 2003/08/19 by smoss@smoss_crayola_linux_orl_regress

   more commonality

Change 117064 on 2003/08/19 by smoss@smoss_crayola_linux_orl

   common format for builds

Change 117049 on 2003/08/19 by cbrennan@cbrennan_r400_release

Release: Fix format 51.. synth fixes. tcd testbench with new formats.

Change 117046 on 2003/08/19 by viviana@viviana_crayola2_syn

Memory configuration file.

Change 117042 on 2003/08/19 by tien@tien_r400_devel_marlboro

Gave 16_EXPANDs their own encoded format

```
Disabled tp_hicolor for vtx and packed RF expand cases

Change 117026 on 2003/08/19 by dclifton@dclifton_r400

Fixed -0 + -0 case in vector and scalar.
Fixed flip sign timing issue in sp_macc32.
Delayed negate signal to scalar to sync with input b.

Change 116992 on 2003/08/18 by smburu@smburu_r400_linux_marlboro

Fixes to tp_tt and some new logic for tp_hicolor.

Change 116989 on 2003/08/18 by tien@tien_r400_devel_marlboro

Starting to fix up vtx rf enable... made 3 packed modes pass thru tp_hicolor

Change 116960 on 2003/08/18 by tien@tien_r400_devel_marlboro

Fixed one of the multicycle cases (tl=tr, bl=br was turning into 3 cycles)

Change 116944 on 2003/08/18 by tien@tien_r400_devel_marlboro

Misc border fixes

Change 116908 on 2003/08/18 by mearl@mearl_crayola_linux_orl

This version of sc_packer has the newest bad pipe logic, all of the
       known bug fixes, and is the last version before the one primitive per
       clock changes.

Change 116887 on 2003/08/18 by dougd@dougd_r400_linux_marlboro

restore the `ifdef USE_BEHAVE_MEM that was removed for
testing of virage behavioral models.

Change 116854 on 2003/08/18 by tien@tien_r400_devel_marlboro

FIxed valids to TC

Change 116807 on 2003/08/15 by dclifton@dclifton_r400

Improvement for timing

Change 116795 on 2003/08/15 by vromaker@vromaker_r400_linux_marlboro

adding sq-vc tracker (not debugged yet - just checking in working copy)

Change 116762 on 2003/08/15 by donaldl@donaldl_crayola_unix_orl
```

```
Defines to enable one primitiver per clock and extra edge fractional bits

Change 116761 on 2003/08/15 by donaldl@fl_donaldl_p4

Used ifdef's to run at one primitive per clock.

Change 116751 on 2003/08/15 by smburu@smburu_r400_linux_marlboro

Fix for bug 2522.

Change 116746 on 2003/08/15 by tien@tien_r400_devel_marlboro

Border fixes

Change 116692 on 2003/08/15 by smoss@smoss_crayola_linux_orl_regress

   add pa buildtb

Change 116660 on 2003/08/14 by dclifton@dclifton_r400

Added fix for clipped polymode lines.

Change 116623 on 2003/08/14 by smburu@smburu_r400_linux_marlboro

Fix for bug 2519 and adding channel bits for hicolor.

Change 116619 on 2003/08/14 by cbrennan@cbrennan_r400_emu

Release DXT3A, DXT5A, and CTX1 formats.

Change 116586 on 2003/08/14 by dclifton@dclifton_r400

Added sin/cos to scalar engine
Changed spi_hi_prec_int to improve timing--it now clamps at max float instead of
rolling back to zero.

Change 116474 on 2003/08/14 by bbuchner@fl_bbuchner_r400_win

remove old memories

Change 116462 on 2003/08/14 by tien@tien_r400_devel_marlboro

FIxed connection of tri_juice constant field

Change 116380 on 2003/08/13 by mmang@mmang_crayola_linux_orl

1.  Added separate gpr allocation/deallocation
```

```
    management for multiple simds (sq_gpr_alloc,
    sq_exit_sm, sq_pix_thread_buff, sq_status_reg,
    sq_vtx_thread_buff, sq_pix_ctl, and sq_vtx_ctl)
2.  Made thread_arb poll cfs rtr on a 4 clock
    interval in order to ensure the arbiters
    stayed in phase between simds.
3.  Created new interface signal between
    thread_arb and export_alloc to lock export_id
    and parameter cache base for each simd.  In
    addition, created registers for these values
    for each simd in order to ensure they got
    allocated in order.
4.  In ais_output, used simd to mask pix_ctl gpr
    writes to different simds.
5.  In tb_sqsp, added simd_id and gpr write address
    to texture latency fifo to help trackers and
    read inject return files.
6.  In tex_instr_queue, grab appropriate gpr_max
    based on simd id.

Change 116363 on 2003/08/13 by tien@tien_r400_devel_marlboro

TC FIFO optimizations
Cmask fix for tp4_tc testbench

Change 116337 on 2003/08/13 by bbuchner@bbuchner_crayola_linux_orl

new memory build.  Delelted 16x70 memory.  changed 11h28x47 to 32x112

Change 116333 on 2003/08/13 by bbuchner@bbuchner_crayola_linux_orl

changed coher interfact to CP.  Provide  independent data valids to SP.
   REmove  instruction FIFO from RP.

Change 116318 on 2003/08/13 by dclifton@dclifton_r400

Update for changes in test I/O on pa

Change 116303 on 2003/08/13 by danh@danh_r400_win

Updated failing tests status.

Change 116202 on 2003/08/12 by smburu@smburu_r400_linux_marlboro

Added missing file.

Change 116191 on 2003/08/12 by smburu@smburu_r400_linux_marlboro
```

```
Hicolor and WS changes. Requires new Emulator release from Jocelyn.

Change 116186 on 2003/08/12 by tien@tien_r400_devel_marlboro

More Get/Set changes, overrides for exp_adjust_all

Change 116147 on 2003/08/12 by cbrennan@cbrennan_r400_release

Release rewiring of start/clean from MH to CP.  remove VC clean signal from TC.

Change 116104 on 2003/08/12 by tien@tien_r400_devel_marlboro

Some changes for predicate tfetch (pix_mask) pipelining

Change 116043 on 2003/08/12 by paulv@paulv_r400_release

Update TOTT with rb_branch.

Change 116038 on 2003/08/12 by mearl@mearl_crayola_linux_orl

        added changes for simd id pipe disable logic

Change 116036 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 116034 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 116033 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 116032 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 116031 on 2003/08/12 by mearl@mearl_crayola_linux_orl

added changes for simd id pipe disable logic

Change 115960 on 2003/08/11 by tien@tien_r400_devel_marlboro

WS=1.0 override for GetCompTexLOD and GetGradients

Change 115937 on 2003/08/11 by tien@tien_r400_devel_marlboro
```

```
1st half of data mux's in tp_fetch for Get/Set opcodes

Change 115899 on 2003/08/11 by tien@tien_r400_devel_marlboro

Cmask fix for 3-channel *_AS_16_16_16_16 formats

Change 115863 on 2003/08/11 by rramsey@rramsey_crayola_linux_orl

fix write index into pos export buffer when processing aux vectors

Change 115781 on 2003/08/11 by rramsey@RRAMSEY_P4_r400_win

update sq status
add runtime column to report so it works with the spreadsheet script

Change 115728 on 2003/08/10 by rramsey@rramsey_crayola_linux_orl

Change SQ to hold off popping the RBBM skid fifo while map copies are in
progress. This fixes the problem where gfx_copy writes were being missed
if they were less than 8 clks apart.
Get rid of extra write into RBBM skid fifo for reads, and instead zero out
we and re out of fifo if it's empty. The fifo was overflowing if the filling
entry was a read, since one additional entry was getting pushed.
sx_sp_pcdata tracker now ignores 4f5eaddf (unwritten pc locations)
Fix a problem in the sqsp testbench that was causing rbbm writes to be dropped
if the sq exerted back pressure.

Change 115724 on 2003/08/10 by smoss@smoss_crayola_linux_orl_regress

   added coverage.f option

Change 115723 on 2003/08/10 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 115671 on 2003/08/08 by tien@tien_r400_devel_marlboro

More GetSet stuff
Fixed pre-RF expansion logic

Change 115662 on 2003/08/08 by paulv@paulv_r400_release

Release rb_branch to TOTT.

Change 115620 on 2003/08/08 by dougd@dougd_r400_linux_marlboro

1. change all hs virage memories & files to have subword size in name
2. added diagnostic write enable from rbbm interface register to the modules
```

```
   with extra memories to support multiple SIMDs

Change 115595 on 2003/08/08 by dougd@dougd_r400_linux_marlboro

fixed the path for the real time bit down the alu pipeline
to reach the constant and instruction stores.

Change 115581 on 2003/08/08 by rramsey@RRAMSEY_P4_r400_win

update sq status

Change 115492 on 2003/08/07 by mmang@mmang_crayola_linux_orl

change order of include paths for register_addr.v

Change 115488 on 2003/08/07 by bbuchner@bbuchner_crayola_linux_orl

build script for coverage results

Change 115430 on 2003/08/07 by danh@danh_r400_win

Updated status (lines 271-284).

Change 115426 on 2003/08/07 by dclifton@dclifton_r400

Added another block

Change 115414 on 2003/08/07 by tien@tien_r400_devel_marlboro

Fixed opcode_enc out of tp_lod_fifo in _state vector
Added code to 0 out TC fetches for certain opcodes

Change 115411 on 2003/08/07 by cbrennan@cbrennan_r400_release

Releasing debug register hookup and mip packing fix for tp4_tc.

Change 115386 on 2003/08/07 by grayc@grayc_crayola2_linux_orl

   partial change for pav and test
   update for mh block file change

Change 115381 on 2003/08/07 by dclifton@dclifton_r400

sp_scalar_lut:  mova reverted to act like max, force_mul_prev2_max_float logic changed,
fixed clamp bug in log, clear sign on force zero, single operand inst for zero for b
input, masked pred_set_execute on anything but kill and pred_set ops.  sp_macc:
force_mul_prev2_max_float logic changed.  sp_macc32: masked inf, nan, or unknown unused
operands for DOT3 and DOT2 ops, disabled flip_sign for adds resolving to zero.
```

```
sp_vector:  removed extra register from exported scalar data, fixed mova fixed address
calculation.

Change 115274 on 2003/08/06 by smoss@smoss_crayola_win

monitor strange ncsim errors

Change 115254 on 2003/08/06 by smoss@smoss_crayola_win

fixing deaddead

Change 115241 on 2003/08/06 by dougd@dougd_r400_linux_marlboro

1. corrected the connections to sq_perfmon_wrapper to enable the
ALU active counters.

2. changed a few 1 bit vector declarations ( [0:0] ) to scalar
on SQ outputs because it caused errors in synthesis.

Change 115205 on 2003/08/06 by tien@tien_r400_devel_marlboro

This didn't check in for some reason

Change 115183 on 2003/08/06 by tien@tien_r400_devel_marlboro

Unencoded DIM now driven to tp_addresser and tp_fetch
(for cubic mapping, proper face_id generation)

Change 115159 on 2003/08/06 by rramsey@rramsey_crayola_linux_orl

Change sq_alu_instr_seq so gpr_rd_en is not asserted when reading constants
Changes to thread_arb, ctl_flow_seq, and status_reg to get mem exports flowing

Change 115134 on 2003/08/06 by cbrennan@cbrennan_r400_release

Fixed odd sized 2d wrap cases with EE/EO/OE/OO muxing.

Change 115122 on 2003/08/06 by rramsey@RRAMSEY_P4_r400_win

Update with Aug6 sanity results and add a new worksheet that has failures sorted by
failure type

Change 115115 on 2003/08/06 by smoss@smoss_crayola_linux_orl_regress

   Randy's keeping me honest

Change 115114 on 2003/08/06 by rramsey@rramsey_crayola_linux_orl
```

```
add some missing dummy dump files

Change 115112 on 2003/08/06 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 115075 on 2003/08/05 by askende@askende_r400_linux_marlboro

backing up source code

Change 115068 on 2003/08/05 by askende@askende_r400_linux_marlboro

adding new modules into Perforce

Change 115049 on 2003/08/05 by rramsey@RRAMSEY_P4_r400_win

Put some comments on all of the failing tests so we can try to bin the issues for
debugging

Change 115047 on 2003/08/05 by rramsey@rramsey_crayola_linux_orl

Add register to hold pipe disable bits to tb_sqsp
Hook sx instance up to correct set of RBBM signals in tb_sqsp
Increase depth of sc state avail fifo since some events need
to go through that path
       Change sx pa tracker to always opens its files so it doesn't
       cause hangs when the files are empty
       Add deaddead and a selectable x_vs_0 mismatch disable (reports
       a warning rather than a mismatch) to tbtrk_sx_rb.v

Change 115037 on 2003/08/05 by tien@tien_r400_devel_marlboro

Added some per-pixel LOD support

Change 115032 on 2003/08/05 by grayc@grayc_crayola2_linux_orl

   added back Laurent changes for sx performance counters
   modified sx.v for new performance register names

Change 115025 on 2003/08/05 by cbrennan@cbrennan_r400_release

Fixed weird simulation artifact where VALUE + ~1'b1 was actually doing VALUE +
'b111111111111110 when computing secondary pitches.

Change 115005 on 2003/08/05 by kmeekins@kmeekins_crayola_linux_orl

Added the ability to build and simulate using either NC Verilog or VCS.
  Scripts will detect which environment you have loaded and use the
```

```
  appropriate tools.

Change 114927 on 2003/08/05 by tien@tien_r400_devel_marlboro

More Get/Set Fixes
Fix for TP_SQ_dec (for real)

Change 114915 on 2003/08/05 by mzini@mzini_crayola_linux_orl

 Old fix for VC_RP testbench

Change 114873 on 2003/08/04 by askende@askende_r400_linux_marlboro

releasing changes

Change 114774 on 2003/08/04 by rramsey@RRAMSEY_P4_r400_win

update sqspsx status

Change 114772 on 2003/08/04 by rmanapat@rmanapat_r400_release

Fixes a TC hang caught by tc_random tri8_tex4_fb128x128 0xe38e6531

Change 114719 on 2003/08/04 by bbuchner@bbuchner_crayola_linux_orl

changed two memory sizes

Change 114706 on 2003/08/04 by danh@danh_r400_win

Updated r400sq_* status.

Change 114597 on 2003/08/01 by paulv@paulv_r400_release

RB update to TOTT.

Change 114584 on 2003/08/01 by tien@tien_r400_devel_marlboro

Get/Set cleanup

Change 114561 on 2003/08/01 by smoss@smoss_crayola_linux_orl_regress

   added coverage for vcs
   added coverage for cp
   stop simulation during compile of vgt
   modified fsdb generation for cp

Change 114544 on 2003/08/01 by nkociuk@nkociuk_r400_linux_marl
```

```
misc minor updates to register modules
 tcm perfmon instantiation uncommented

Change 114530 on 2003/08/01 by bbuchner@bbuchner_crayola_linux_orl

provide for from 1-4 simd engines.

Change 114427 on 2003/08/01 by smoss@smoss_crayola_linux_orl_regress

   added rb_sx dump

Change 114404 on 2003/08/01 by amys@amys_r400_regress_linux

changes made to fix running ncsim using Orlando trackers

Change 114319 on 2003/07/31 by kmeekins@kmeekins_crayola_linux_orl

Makefiles used to build new libpli.so for VC PLI memory tasks.

Change 114308 on 2003/07/31 by mdesai@mdesai_r400_linux

bug fixes etc...

Change 114305 on 2003/07/31 by vromaker@vromaker_r400_linux_marlboro

cleaned up the path of ism_state down through the
instruction pipelines and removed the defparams used in the
multiple instantiations of several modules.

Change 114302 on 2003/07/31 by mdesai@mdesai_r400_linux

enhanced tests

Change 114265 on 2003/07/31 by paulv@paulv_r400_release

Release of RB/DB code to TOTT.

Change 114239 on 2003/07/31 by cbrennan@cbrennan_r400_release

Releasing VC_TC_info width change.

Change 114235 on 2003/07/31 by tien@tien_r400_devel_marlboro

Completed fix for TP_SP_simd

Change 114229 on 2003/07/31 by donaldl@fl_donaldl_p4

Updated for latest versions of sc_pipe, sc_coarse_walker, and sc_quadmask.
```

```
Change 114192 on 2003/07/31 by tien@tien_r400_devel_marlboro

Bug fixes and change in tpc_out_fifo width

Change 114167 on 2003/07/31 by danh@danh_r400_win

Updated the r400sq_* status.

Change 114159 on 2003/07/31 by rramsey@RRAMSEY_P4_r400_win

update status. remove some CP tests that don't anything at sqsp.

Change 114156 on 2003/07/31 by kmeekins@kmeekins_crayola_linux_orl

Removed the bit field from the scalar VC_SP_data_valid to stop ncverilog errors.

Change 113990 on 2003/07/30 by rramsey@rramsey_crayola_linux_orl

Changes to support real time prims.
Tests that draw rt only now drive sc inputs
RBBM stream is held off while each rt prim processes so
rt code/const/params are not clobbered

Change 113958 on 2003/07/30 by cbrennan@cbrennan_r400_release

Fixes Z coordinate and pulls border bit from right phase of constant register info.

Change 113953 on 2003/07/30 by danh@danh_r400_win

Updated r400sq_* status.

Change 113881 on 2003/07/29 by cbrennan@cbrennan_r400_release

Delete tc branch files, which are all very old.

Change 113873 on 2003/07/29 by paulv@paulv_r400_release

RB and MH updates to TOTT.

Change 113794 on 2003/07/29 by nkociuk@nkociuk_r400_linux_marl

fix tri-juice cases where fraction overflows or underflows
 fix aniso_clamp_sel for negative lg2major cases

 get/set opcodes now mismatch in standalone tb after cl#113623, but without
corresponding emu changes, that's to be expected...
```

```
Change 113723 on 2003/07/29 by bhankins@bhankins_crayola_linux_orl

modify to use rb_sx.dmp file to generate indices and index_op bit

Change 113623 on 2003/07/28 by tien@tien_r400_devel_marlboro

Man it's been a long time coming :-)
formatter fix for TP to output to 1 simd only
drive simd signal from TPC to VC (will prolly need to skew it a bit, but that will fall
out from debug)
Clean up get/set logic

Change 113577 on 2003/07/28 by jayw@jayw_r400_linux_marlboro

removed unused reg pixel_res0

Change 113553 on 2003/07/28 by bbuchner@bbuchner_crayola_linux_orl

added new performance capabilities

Change 113550 on 2003/07/28 by dougd@dougd_r400_linux_marlboro

added define+virage_ignore_read_addx to support virage behavoral models

Change 113548 on 2003/07/28 by dougd@dougd_r400_linux_marlboro

Added missing register stage in memory address path that caused
memory  failures only with the virage behavoral model.

Change 113533 on 2003/07/28 by paulv@paulv_r400_release

Releasing small amount of RB fixes.

Change 113527 on 2003/07/28 by kmeekins@kmeekins_crayola_linux_orl

Modified code and added comments to remove/supress LEDA warnings/errors
  on code sections known to be error free.

Change 113503 on 2003/07/28 by rramsey@RRAMSEY_P4_r400_win

update sq stats

Change 113413 on 2003/07/27 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 113385 on 2003/07/26 by gregs@gregs_r400_linux_marlboro
```

```
<removed iTEST_EN ports>

Change 113302 on 2003/07/25 by danh@danh_r400_win

Updated r400sq_* status.

Change 113293 on 2003/07/25 by rramsey@RRAMSEY_P4_r400_win

update sq status

Change 113291 on 2003/07/25 by johnchen@johnchen_r400_linux_marlboro

timing fix

Change 113286 on 2003/07/25 by vromaker@vromaker_r400_linux_marlboro

- a few more fixes for SQ_VC/TP interfaces; the sq mini-regress now passes
  with the VC turned on

Change 113242 on 2003/07/25 by johnchen@johnchen_r400_linux_marlboro

more random tb fixes

Change 113236 on 2003/07/25 by kmeekins@kmeekins_crayola_linux_orl

Changed increment/decrement logic to relieve timing. Treating cc_freeze_b
  signal as late arriving.

Change 113223 on 2003/07/25 by rramsey@rramsey_crayola_linux_orl

uncomment driver for SQ_SP_interp_xyline

Change 113217 on 2003/07/25 by kmeekins@kmeekins_crayola_linux_orl

Removed signals/ports that are no longer needed.
  Changed muxing logic in vc_cc_way_mem.v to help timing.

Change 113216 on 2003/07/25 by paulv@paulv_r400_linux_marlboro

Fixed a typo.

Change 113215 on 2003/07/25 by paulv@paulv_r400_linux_marlboro

Ugh!  More timing fixes.

Change 113214 on 2003/07/25 by askende@askende_r400_linux_marlboro

fix related to PRED instructions
```

Change 113209 on 2003/07/25 by mzini@mzini_crayola_linux_orl

Made info field 25 bits to make room for the latency counters

Change 113207 on 2003/07/25 by danh@danh_r400_win

Updated the r400sq_* status.

Change 113167 on 2003/07/25 by nkociuk@nkociuk_r400_linux_marl

updates to kill invalid inputs in randomly-generated patterns

Change 113146 on 2003/07/25 by wlawless@wlawless_r400_linux_marlboro

paralled up the addresses into the CAM's for timing... I think this will
help because the buffering was a killer

Change 113138 on 2003/07/25 by cbrennan@cbrennan_r400_linux_marlboro

Some minor debug bus changes.

Change 113091 on 2003/07/24 by johnchen@johnchen_r400_linux_marlboro

more random fixes

Change 113082 on 2003/07/24 by johnchen@johnchen_r400_linux_marlboro

write depth_clear plane to the cache even if zpass_mask is zero

Change 113039 on 2003/07/24 by danh@danh_crayola1_linux_orl

Changed src_c_const_addr_rel generation so it matches the emulator code.

Change 113017 on 2003/07/24 by paulv@paulv_r400_linux_marlboro

Fixed my horrid timing "fixes" from yesterday.

Change 113007 on 2003/07/24 by rramsey@RRAMSEY_P4_r400_win

add +define+MEM_CHECK_OFF unless compiling for gate sims

Change 112998 on 2003/07/24 by johnchen@johnchen_r400_linux_marlboro

random tb fix

Change 112962 on 2003/07/24 by mzini@mzini_crayola_linux_orl

Added delete option

Change 112903 on 2003/07/24 by jcarroll@jcarroll_crayola_linux_orl

Added default values for the 'load_coher' signals.

Change 112899 on 2003/07/24 by danh@danh_crayola1_linux_orl

Changed src_c_const_addr_rel generation.

Change 112882 on 2003/07/24 by rramsey@RRAMSEY_P4_r400_win

update sqspsx status

Change 112833 on 2003/07/23 by paulv@paulv_r400_linux_marlboro

Commented out all dummy memory models and the tile block is now using the macro verilog models. Also, added logic between the tile cache and quad cache to invalidate a quad cache cacheline when a tile cache cacheline gets flushed out to make room for new data.

Change 112796 on 2003/07/23 by kevino@kevino_r400_linux_marlboro

Replaced memory model with _rtl.v version to get it working in VCS again

Change 112773 on 2003/07/23 by nkociuk@nkociuk_r400_linux_marl

drop all but 6 most-significant fraction bits on generated log[whd] so that values read by emulator match hw precision

this is one of those things that i initially thought was a non-issue, since the emulator does its own precision dropping, but the heavy hand i was using in the emulator code caused other precision problems on some test cases. revisited this after Vishal pointed it out.

Change 112745 on 2003/07/23 by wlawless@wlawless_r400_linux_marlboro

fixed pitch0 to use flopped version when more quads and some timing in frag op

Change 112716 on 2003/07/23 by johnchen@johnchen_r400_linux_marlboro

update smask for expaned when smask is enabled

Change 112689 on 2003/07/23 by johnchen@johnchen_r400_linux_marlboro

randon tb test fix

Change 112660 on 2003/07/23 by paulv@paulv_r400_linux_marlboro

```
Timing fix.

Change 112626 on 2003/07/23 by kmeekins@kmeekins_crayola_linux_orl

Added more performance monitiors for checking the stall conditions.

Change 112610 on 2003/07/23 by paulv@paulv_r400_linux_marlboro

Few minor signal reassignments to be more consistent with rest of tile.

Change 112600 on 2003/07/23 by rramsey@rramsey_crayola_linux_orl

Change sx-rb trackers so they always open their files at time 0,
that way they don't cause hangs for tests that don't hit any quads
Hook up the real pixel mask in the sx_rb color tracker

Change 112546 on 2003/07/22 by tien@tien_r400_devel_marlboro

Clean up for get/set

Change 112486 on 2003/07/22 by kevino@kevino_r400_linux_marlboro

 cleaned up fetch gen debug info

Change 112469 on 2003/07/22 by nkociuk@nkociuk_r400_linux_marl

fix bug in mip loops logic

Change 112453 on 2003/07/22 by kevino@kevino_r400_linux_marlboro

       Cleaned up TCD debug bus.  Still need to concat signals into 32 bit words
instead of having then as NO_CONNECT

Change 112450 on 2003/07/22 by johnchen@johnchen_r400_linux_marlboro

timing fixes around probe logic

Change 112438 on 2003/07/22 by bbuchner@bbuchner_crayola_linux_orl

make start signal to CC be a pulse

Change 112428 on 2003/07/22 by bbuchner@bbuchner_crayola_linux_orl

<fixed to match tc invalidate behavior

Change 112425 on 2003/07/22 by wlawless@wlawless_r400_linux_marlboro
```

```
gated if_dec2 with num_equal instead of stop_pipe... didn't need all those
conditions

Change 112422 on 2003/07/22 by johnchen@johnchen_r400_linux_marlboro

r400rb_tb test fix

Change 112408 on 2003/07/22 by nkociuk@nkociuk_r400_linux_marl

change assignment to x (don't care) to assignment to 0.  the don't care condition
should never happen, ensured by external logic, and this way, formality
 checks against the rtl shouldn't have miscompares...

Change 112383 on 2003/07/22 by kevino@kevino_r400_linux_marlboro

updated tco debug regs

Change 112375 on 2003/07/22 by vromaker@vromaker_r400_linux_marlboro

- fixed VC interface counter

Change 112347 on 2003/07/22 by wlawless@wlawless_r400_linux_marlboro

moved linear128 per ping pong for timing

Change 112344 on 2003/07/22 by nkociuk@nkociuk_r400_linux_marl

improved aniso_2 approximation logic

Change 112343 on 2003/07/22 by kevino@kevino_r400_linux_marlboro

tcd debug info

Change 112341 on 2003/07/22 by paulv@paulv_r400_linux_marlboro

Shrunk total delay by 600ps (from 6000ps to 5400ps total).

Change 112340 on 2003/07/22 by nkociuk@nkociuk_r400_linux_marl

update testbench to match IO changes from cl#112333

Change 112335 on 2003/07/22 by danh@danh_r400_win

Updated the r400sq* status.

Change 112333 on 2003/07/22 by tien@tien_r400_devel_marlboro

Cleaned up Get/Set stuff in upper part of pipe
```

```
Change 112331 on 2003/07/22 by paulv@paulv_r400_linux_marlboro

Fixed tile_fifo_probe_read when surface not enabled.

Change 112313 on 2003/07/22 by amys@amys_crayola2_linux_orl

fixed bug so tracker can compile

Change 112312 on 2003/07/22 by jayw@jayw_r400_linux_marlboro

Hooking up register read logic.  removed dummy memory from rb_rbt_fragment_fifo.v

Change 112292 on 2003/07/22 by johnchen@johnchen_r400_linux_marlboro

more stencil expand stuff

Change 112289 on 2003/07/22 by dclifton@dclifton_r400

Updated staging registers in sp_macc.
Revised sp_scalar_lut.
Test signals connected.

Change 112280 on 2003/07/21 by johnchen@johnchen_r400_linux_marlboro

tb test with smask on fix

Change 112259 on 2003/07/21 by johnchen@johnchen_r400_linux_marlboro

expand with stencil initial

Change 112244 on 2003/07/21 by tien@tien_r400_devel_marlboro

Fixed drop writes to lod/coord fifos
Removed 2 ports that were leaking to top-level of tp

Change 112216 on 2003/07/21 by kmeekins@kmeekins_crayola_linux_orl

Added logic to invalidate the cache on an address range.
  Added the new CC module vc_cc_cache_invalidate.

Change 112191 on 2003/07/21 by cbrennan@cbrennan_r400_linux_marlboro

Removed TCA_TCB stall from tca's rtr to TPC.  should increase performance as it was not
needed.

Change 112189 on 2003/07/21 by bbuchner@bbuchner_crayola_linux_orl
```

new invalidation scheme, added more debug

Change 112182 on 2003/07/21 by wlawless@wlawless_r400_linux_marlboro

broke up the read muxes for cam outputs for timing

Change 112163 on 2003/07/21 by paulv@paulv_r400_linux_marlboro

Fixed clk domains for a few signals.

Change 112149 on 2003/07/21 by jbrady@jbrady_crayola_linux_orl

Gate build.

Change 112147 on 2003/07/21 by jbrady@jbrady_crayola_linux_orl

Change VC_gpr_phase_q sense to match what is expected in gc.

Change 112143 on 2003/07/21 by mzini@mzini_crayola_linux_orl

 Delayed gpr_phase by 2 cycles to match the hardware

Change 112130 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

removed dummy memory.

Change 112129 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

double skid depth of input quad fifo to accomodate decreasing it to 1-quad wide

Change 112109 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

switching to using real rams, some LEDA fixes

Change 112108 on 2003/07/21 by rramsey@RRAMSEY_P4_r400_win

update with 07/21 status and some comments on the failing tests

Change 112098 on 2003/07/21 by johnchen@johnchen_r400_linux_marlboro

timing fix

Change 112097 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

removed duplicate declaration.

Change 112094 on 2003/07/21 by jayw@jayw_r400_linux_marlboro

```
Fix for mc disable signals, needed to be registered.

Change 112093 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

fix to keep a proper tally of position vectors exported when auxillary vectors are
included

Change 112084 on 2003/07/21 by rramsey@rramsey_crayola_linux_orl

mask fifo was not quite deep enough

Change 112073 on 2003/07/21 by vromaker@vromaker_r400_linux_marlboro

- fix for SQ_VC interface
- TP_SQ_dec was hooked up to the interface counter
- timing fix in vtx thread buffer
- simd_num connected thru ptr buff and pix ctl to pix thread buff
- performance fix in pix ctl

Change 112064 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

add missing port

Change 112062 on 2003/07/21 by bhankins@bhankins_crayola_linux_orl

add commented line, to be uncommented to enable mrt support

Change 112034 on 2003/07/19 by rramsey@rramsey_crayola_linux_orl

Change vcs build script so cover is off by default
Get rid of some compile warnings in tb_sqsp
Change sx_rb color tracker so it doesn't use the sx_rb_quad dump
to get pixel masks

Change 111995 on 2003/07/18 by johnchen@johnchen_r400_linux_marlboro

random fixes

Change 111986 on 2003/07/18 by dougd@dougd_r400_linux_marlboro

Added dummy mems for all virage memorie that didn't already have them.
Moved memory data output register in sq_cfc.v into the memory and dummy memory.
Replaced all virage memories, etc. to get the memory needed for sq_cfc.v

Change 111959 on 2003/07/18 by mzini@mzini_crayola_linux_orl

 Delete testcase if it passes
```

```
Change 111945 on 2003/07/18 by jcarroll@jcarroll_crayola_linux_orl

            Recoded the L2 Request Control Logic.
            No functional changes.  Restructured for future timing fixes between CC and
RP.

Change 111928 on 2003/07/18 by bhankins@bhankins_crayola_linux_orl

misc fixes.  also add support for multiple render targets.  Not fully tested, and
currently disabled by default.

Change 111923 on 2003/07/18 by kevino@kevino_r400_linux_marlboro

   Added some tcd debug.  Need to add dxtc still.

Change 111921 on 2003/07/18 by nkociuk@nkociuk_r400_linux_marl

misc cleanup

Change 111918 on 2003/07/18 by kmeekins@kmeekins_crayola_linux_orl

Added the request size to the cache tag.

Change 111905 on 2003/07/18 by ygiang@ygiang_r400_pv2_marlboro

added: new perf counters for sq hardware

Change 111894 on 2003/07/18 by cbrennan@cbrennan_r400_linux_marlboro

Remove sec_endian signals from ferret and tpc.
Was leaking out.

Change 111892 on 2003/07/18 by johnchen@johnchen_r400_linux_marlboro

more stencil comp support

Change 111884 on 2003/07/18 by johnchen@johnchen_r400_linux_marlboro

timing fixes

Change 111882 on 2003/07/18 by nkociuk@nkociuk_r400_linux_marl

get rid of unused signals

Change 111880 on 2003/07/18 by paulv@paulv_r400_linux_marlboro

Various HiZ related fixes, including the updating of smask and zrange when specific
enable bits (e.g., stencil_enable, etc.) are set.
```

```
Change 111877 on 2003/07/18 by nkociuk@nkociuk_r400_linux_marl

signal cleanup...

 also adding tcm_perfmon.v but not instantiating until tp.blk file enumerates the
required registers

Change 111807 on 2003/07/18 by mmantor@mmantor_crayola_linux_orl

<added new dummy file for test cases that needed it>

Change 111806 on 2003/07/18 by mmantor@mmantor_crayola_linux_orl

<extended rb_sx_index to 8 bits for Orlando trackers with bigger export buffers>

Change 111776 on 2003/07/17 by jayw@jayw_r400_linux_marlboro

Fixing use of non-registered inputs from DB.

Change 111737 on 2003/07/17 by kmeekins@kmeekins_crayola_linux_orl

Registered RP->CC bank read address and read enables to fix a timing path.
  Propagated the newly registered signals to the vc_cc_loaded_busy module.

Change 111736 on 2003/07/17 by mmang@mmang_crayola_linux_orl

Added sp->sx export arbitration between multiple simd engines.
Added register after instr_start OR of multiple simd engines by
taking unregistered signal out of sq_ais_output.

Change 111732 on 2003/07/17 by rramsey@RRAMSEY_P4_r400_win

Update with regression results, plus a couple of my own

Change 111728 on 2003/07/17 by kevino@kevino_r400_linux_marlboro

  scaled back debug info to mostly rtr's, busy, etc.

Change 111726 on 2003/07/17 by smoss@smoss_crayola_linux_orl_regress

   modified $value$plusargs to keep cadence happy

Change 111725 on 2003/07/17 by kevino@kevino_r400_linux_marlboro

   scaled back fetch gen debug info, added seperate debug_info_stalls

Change 111722 on 2003/07/17 by amys@amys_crayola2_linux_orl
```

fixed a type in PA_PATH for the chip

Change 111719 on 2003/07/17 by johnchen@johnchen_r400_linux_marlboro

yet another timing fix to the expand logic

Change 111715 on 2003/07/17 by rramsey@RRAMSEY_P4_r400_win

some old fixes for an SC modelsim script

Change 111699 on 2003/07/17 by wlawless@wlawless_r400_linux_marlboro

inc_amount went neg need to be sign extended

Change 111693 on 2003/07/17 by rmanapat@rmanapat_r400_sun_marlboro

Delete obsolete memories and also added full signals for debug regs

Change 111692 on 2003/07/17 by danh@danh_r400_win

Updated the r400sq* status.

Change 111682 on 2003/07/17 by jgibney@jgibney_r400_linux_marlboro

Fix for multiple render targets bug. Connected registered version of blend_rd_color_sel to buffer_sol0 into urb_c_cache_state, to align properly with pixel_res.

Change 111650 on 2003/07/17 by rramsey@rramsey_crayola_linux_orl

Add pasx done to testbench timeout logic

Change 111628 on 2003/07/17 by smoss@smoss_crayola_linux_orl_regress

   changed tbmod_fake_pa for ncsim because all requests weren't occurring this was also true for vcs but sim was passing. changed buildt for nc to not run a sim after a compile

Change 111626 on 2003/07/17 by wlawless@wlawless_r400_linux_marlboro

broke up the big always block

Change 111625 on 2003/07/17 by rmanapat@rmanapat_r400_sun_marlboro

Increased the size of a tca fifo by 1 bit

Change 111621 on 2003/07/17 by jbrady@jbrady_crayola_linux_orl

```
In next_RG_RP_L2a_clamp, qualify clamp_min and clamp_max with the fact that
  the vert is valid. Otherwise our mux will output vert 0 index and clamp
  with vert 1 banks and tags.

Change 111612 on 2003/07/17 by moev@moev2_r400_linux_marlboro

Clean up files no longer used by the verification flow

Change 111603 on 2003/07/17 by moev@moev2_r400_linux_marlboro

SQ changes to test Virage's HS memories.

Change 111600 on 2003/07/17 by kevino@kevino_r400_linux_marlboro

     Added some fetch gen debug registers

Change 111555 on 2003/07/16 by tien@tien_r400_devel_marlboro

Fixed log calculation of sec pitches

Change 111541 on 2003/07/16 by kmeekins@kmeekins_crayola_linux_orl

Backed out the removal of the cache miss condition in the cache_line_in_use signal.
  The cache miss is needed to prevent stalls on a cache hit sector miss condition.

Change 111520 on 2003/07/16 by grayc@grayc_crayola2_linux_orl

   fix for new tile

Change 111515 on 2003/07/16 by grayc@grayc_crayola2_linux_orl

   fix for new tile path

Change 111491 on 2003/07/16 by johnchen@johnchen_r400_linux_marlboro

funtional and timing fixes

Change 111486 on 2003/07/16 by rmanapat@rmanapat_r400_sun_marlboro

More changes for debug registers for tca/tcb

Change 111480 on 2003/07/16 by wlawless@wlawless_r400_linux_marlboro

needed to set max probe so it doesn't wrap...

Change 111427 on 2003/07/16 by rmanapat@rmanapat_r400_sun_marlboro
```

```
1st pass at identifying and wiring signals to be routed to DEBUG REGS
for the tcb...used same metod I used in tca

Change 111425 on 2003/07/16 by mzini@mzini_crayola_linux_orl

 Increased timeout counters

Change 111422 on 2003/07/16 by grayc@grayc_crayola2_linux_orl

   delete KS tile ... add PAV and CP_R tile

Change 111419 on 2003/07/16 by rramsey@rramsey_crayola_linux_orl

Connect TST_awt_enable to vc_skid_buf and wire it up to the top level

Change 111407 on 2003/07/16 by smburu@smburu_r400_linux_marlboro

tp_ch_blend testbench files.

Change 111406 on 2003/07/16 by kevino@kevino_r400_linux_marlboro

   Updated debug info for TCO to include requested and written sector masks as well as
setlines

Change 111403 on 2003/07/16 by paulv@paulv_r400_linux_marlboro

Needed to use the flopped read data when determining the *queue_vector vector.

Change 111381 on 2003/07/16 by rramsey@rramsey_crayola_linux_orl

Fix compile result check in buildtb
Tie off sx related done signals when the sx is not there
and spit them out if it is there and the tb hangs
Don't source sx_sp_pcdata stimulus when using live sx
Remove extra ifdef

Change 111372 on 2003/07/16 by rramsey@rramsey_crayola_linux_orl

add filename to mismatch message

Change 111370 on 2003/07/16 by mzini@mzini_crayola_linux_orl

 Added option to generate incremental data

Change 111366 on 2003/07/16 by wlawless@wlawless_r400_linux_marlboro

Fixed 128x128 blend 2 samp
```

```
Change 111353 on 2003/07/16 by bhankins@bhankins_crayola_linux_orl

when the sx is present, include the sx trackers in on the decision to stop the
simulation

Change 111350 on 2003/07/16 by rmanapat@rmanapat_r400_sun_marlboro

1st pass at selecting which signals in the tca  will be routed to DEBUG REGs
Currently I'm wiring up signals and then commenting them out
until they have a destination for them to connect to.

Change 111347 on 2003/07/16 by viviana@viviana_crayola2_syn

SPI memories with registers inside and new version of the compiler.

Change 111345 on 2003/07/16 by rramsey@RRAMSEY_P4_r400_win

Fix the update script to handle 'run time' being reported
Redo the last status update to the spreadsheet since 'run time'
caused all the fields to get shifted

Change 111342 on 2003/07/16 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 111317 on 2003/07/15 by mmang@mmang_crayola_linux_orl

Blocking/non-blocking fix found by synthesis.

Change 111305 on 2003/07/15 by smoss@smoss_crayola_win

update

Change 111303 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

allow pa/sx requests before the rbbm file is empty

Change 111283 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

Corrected a problem that was permitting new allocations to proceed when
  there was still data in-flight. Now looking for fetch contitions as
  opposed to cache miss conditions.

Change 111280 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

need to wait for vc_done if serialize and vc_pending

Change 111275 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl
```

```
add SX_BLOCK_SIM so the sx trackers know where they are running

Change 111267 on 2003/07/15 by jcarroll@jcarroll_crayola_linux_orl

Added a data ready for the L2 coast reg.

Change 111266 on 2003/07/15 by johnchen@johnchen_r400_linux_marlboro

more timing fixes

Change 111239 on 2003/07/15 by nkociuk@nkociuk_r400_linux_marl

if user-specified min miplevel is greater than max miplevel, clamp lod to max.

Change 111221 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

Fixed typo that resulted in wrong sector mask value.

Change 111213 on 2003/07/15 by johnchen@johnchen_r400_linux_marlboro

add sync_start to toplevel signals

Change 111211 on 2003/07/15 by paulv@paulv_r400_linux_marlboro

Forgot to wire up RB_DB_mem_sync_start from the RBM to here.  Fixed.

Change 111186 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

  vc_cc.v
vc_cc_loaded_busy.v
  vc_cc_tag_process.v
  --------------------
  Added more signals to the debug bus.
  Created a third debug bus.

  vc.v
  vc_debug.v
  ----------
  Created CC_DEBUG_DATA_2 bus.

Change 111181 on 2003/07/15 by johnchen@johnchen_r400_linux_marlboro

functional clean and busy signals

Change 111173 on 2003/07/15 by tien@tien_r400_devel_marlboro

Zero'd out LSB of mantissa output on multiplier if 2.0 bit is set
```

```
Change 111134 on 2003/07/15 by tien@tien_r400_devel_marlboro

sub sign fixes

Change 111133 on 2003/07/15 by kmeekins@kmeekins_crayola_linux_orl

vc_cc.v
  vc_cc_tag_process.v
  -------------------
  Created signals for performance monitor and debug bus.

  vc_cc_pack_align.v
  vc_cc_loaded_busy.v
  -------------------
  Corrected timing loop.
  Removed unused signals.

Change 111132 on 2003/07/15 by smoss@smoss_crayola_linux_orl

   just copying randy

Change 111123 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

had a typo in the vc_pending logic

Change 111107 on 2003/07/15 by smoss@smoss_crayola_linux_orl

   updated

Change 111100 on 2003/07/15 by rramsey@rramsey_crayola_linux_orl

Change sc build scripts for TB_SC to tb_sc change
Add cmd line option for fsdb dumping (+SC_DEBUSSY=level)
Add verdi compile to build scripts
Change default build to use real mems

Change 111093 on 2003/07/15 by smoss@smoss_crayola_linux_orl

   decapitating tb_sc

Change 111091 on 2003/07/15 by bhankins@bhankins_crayola_linux_orl

fix sensitivity list

Change 111089 on 2003/07/15 by grayc@grayc_crayola2_linux_orl

   causes a problem with Windows regressions ... removing
```

```
Change 111085 on 2003/07/15 by smoss@smoss_crayola_linux_orl_regress

   attempt to remove again

Change 111084 on 2003/07/15 by smoss@smoss_crayola_linux_orl_regress

   attempt to remove the capital of tb_sc

Change 111070 on 2003/07/14 by grayc@grayc_crayola2_linux_orl

   add a link  tb_sc->TB_SC

Change 111068 on 2003/07/14 by johnchen@johnchen_r400_linux_marlboro

fix a problem for the previous fix

Change 111062 on 2003/07/14 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 111038 on 2003/07/14 by vbhatia@vbhatia_r400_linux_marlboro

Added -coverage option for line,tgl,fsm and conditional coverage to the scripts
and accordingly updated testbenches for enhanced coverage

Change 111011 on 2003/07/14 by johnchen@johnchen_r400_linux_marlboro

timing fix for expansion detection

Change 111008 on 2003/07/14 by dougd@dougd_r400_linux_marlboro

added logic to support programmable memory size for texconst and
aluconst stores.

Change 110982 on 2003/07/14 by jayw@jayw_r400_linux_marlboro

fix attempt for RB performance. (fill test)

Change 110959 on 2003/07/14 by wlawless@wlawless_r400_linux_marlboro

A timing fix broke the randoms so fixed it, hope the timing is still good..

Change 110957 on 2003/07/14 by hmonsef@hmonsef

Replace 8x113 with 8x117 and 12x111 with 12x117. Requested by Paul V.

Change 110939 on 2003/07/14 by johnchen@johnchen_r400_linux_marlboro
```

```
a stencil cache write fix

Change 110904 on 2003/07/14 by johnchen@johnchen_r400_linux_marlboro

type_tag==0 access fix for stencil

Change 110903 on 2003/07/14 by paulv@paulv_r400_linux_marlboro

Removed some commented out code.

Change 110902 on 2003/07/14 by paulv@paulv_r400_linux_marlboro

Increased both the DB_RB_quaddata_mask and the hiz_qc_quaddata_mask to 8 bits.  There
are now 2 bits/quad, with the bits denoting when to update zrange and smask.

Change 110899 on 2003/07/14 by rramsey@rramsey_crayola_linux_orl

change tp/vc pending bits so they look at tgt_instr_str_vc_q bits to
determine what type of fetch is being issued

Change 110888 on 2003/07/14 by johnchen@johnchen_r400_linux_marlboro

write to smask only when smask and stencil is enabled

Change 110886 on 2003/07/14 by rramsey@rramsey_crayola_linux_orl

mask off serial bit for first instruction of a clause.
this change fixes e2blit_src_8888 and probably some other hanging
e2/cp tests

Change 110884 on 2003/07/14 by rramsey@RRAMSEY_P4_r400_win

update with latest regression results

Change 110880 on 2003/07/14 by rramsey@rramsey_crayola_linux_orl

Add back in a signal declaration to fix the no SX build
Move some signals to the other half of a REMOVE_SX ifdef

Change 110877 on 2003/07/14 by dclifton@dclifton_r400

changed rom disable address

Change 110874 on 2003/07/14 by rmanapat@rmanapat_r400_sun_marlboro

Fixed a bug found by random test tc_simple_mip_3d testcase
random_level3 randomseed 0xaf545e96
```

```
Change 110857 on 2003/07/14 by kevino@kevino_r400_linux_marlboro

        Count all 16 sector masks in sector mask walker then mux out counts based on
set and quad selected
        as a timing fix.

Change 110852 on 2003/07/14 by nkociuk@nkociuk_r400_linux_marl

prevent flagging 0-difference results as overflows...

Change 110836 on 2003/07/14 by dclifton@dclifton_r400

Removed DOS carriage returns

Change 110831 on 2003/07/14 by johnchen@johnchen_r400_linux_marlboro

interface update

Change 110827 on 2003/07/14 by mzini@mzini_crayola_linux_orl

 Added option to run the TB with the memory model generating incremental data for tests
other than random

Change 110818 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

remove obsolete memory

Change 110817 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

add new memory files

Change 110811 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

remove obsolete memory

Change 110809 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

update memories

Change 110796 on 2003/07/14 by smburu@smburu_r400_linux_marlboro

More changes for 16/32b RF Expand.

Change 110793 on 2003/07/14 by bhankins@bhankins_crayola_linux_orl

disable run fast sq for now
```

```
Change 110748 on 2003/07/13 by mmantor@mmantor_crayola_linux_orl

<I forgot to add this file>

Change 110669 on 2003/07/12 by smoss@smoss_crayola_linux_orl_regress

   removed errant else

Change 110640 on 2003/07/12 by mmantor@mmantor_crayola_linux_orl

<1. Enlarge export memories for performance fill rate  (emulator, sq, sx, rb, ferret
gc, tb_sqsp, tb_sx)
    2. Fix Sx diff engine (interpolators) for shift bug with added guard bit
    3. Fix compile/src code problem with s-blocks memories
    4. Added the sx to tb_sqsp by default, can still disable by macro
    5. Added mode to tb_sqsp and tb_sx to run interfaces at max rate
    6. Initialized state in vc to allow cp surface synchronizer micro code to
invalidate tc/vc
    7. Added test signals to sc.v, sc_b.v, sq, sp, spi, sx and testbenches
    THIS CHANGES REQUIRES THE RELEASE OF SC, SC_B, SQ, SPI, SP, SX, RB,
src/chip/chip_**.tree files,
    parts_lib/sim/test/gc/vcs_top.ini, gc/tb_sqsp/tb_sx updates  and the emulator
togeather
    >

Change 110616 on 2003/07/11 by tien@tien_r400_devel_marlboro

CHanges to mult and sub functions
No longer clamping output region on mult

Change 110610 on 2003/07/11 by johnchen@johnchen_r400_linux_marlboro

fix inflight once more

Change 110601 on 2003/07/11 by jayw@jayw_r400_linux_marlboro

LEDA and some changes/fixes for 7->8 bits SX index.

Change 110561 on 2003/07/11 by johnchen@johnchen_r400_linux_marlboro

inflight dec fix and zmask==0 stencil support

Change 110552 on 2003/07/11 by cbrennan@cbrennan_r400_linux_marlboro

Makes the invalidate or surface sync function a bit more robust by hopefully not
hanging in user error cases.

Change 110533 on 2003/07/11 by rmanapat@rmanapat_r400_sun_marlboro
```

```
Fix for rounding bug found using tc_simple_cubic random_level test...

Change 110527 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed the Virage compiler version.

Change 110525 on 2003/07/11 by viviana@viviana_crayola2_syn

Removed the STAR_cmdscout connection from the memories instantiated in spi_vsr_ctl.v.

Change 110520 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed the virage compiler for rf memories.

Change 110519 on 2003/07/11 by paulv@paulv_r400_linux_marlboro

Moved logic around in the RBM to fix (hopefully) timing.

Change 110512 on 2003/07/11 by mmang@mmang_crayola_linux_orl

Fix for Vivian for synthesis in loop i07 and i15.

Change 110508 on 2003/07/11 by nkociuk@nkociuk_r400_linux_marl

//depot/r400/devel/parts_lib/src/gfx/tp/inc_mc/fp_fast_mult_dno.mc was updated in
changelist #110505, so checking in updated .bvrl

Change 110505 on 2003/07/11 by tien@tien_r400_devel_marlboro

tp_lod_deriv fix (denorms -> 0 in fp_fast_mult_dno)
formatter fix (1.0 detection for 32- and 16- bit channels)

Change 110503 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed versions of the compiler for the rf memories.

Change 110494 on 2003/07/11 by smoss@smoss_crayola_linux_orl

   turned internal trackers off

Change 110492 on 2003/07/11 by kmeekins@kmeekins_crayola_linux_orl

- Removed the CF_CC_stall signal
  - Added the debug and performance monitor signals to the vc_cc.v I/O.
    Temporarily driving these values to zero.

Change 110473 on 2003/07/11 by kmeekins@kmeekins_crayola_linux_orl
```

```
- Cleaned up signal names.
  - Corrected sector_loaded control logic for multi-cycle fetch operations.
  - Cleaned up sector mask logic for non-256 bit fetch requests.

Change 110467 on 2003/07/11 by llefebvr@llefebvr_r400_emu_montreal

Disabling the COND_EXEC_PRED optimization. a COND_EXEC_PRED in the SQ is now threated
like a regular EXEC. We can re-enable this optimization in the future by putting the
thread back to the RS BEFORE making the predicate compare because now we are comapring
a dirty predicate bit set and it causes corruptions. This fixes mova_test.cpp
TEST_CASE=pMova_const.

Change 110451 on 2003/07/11 by dclifton@dclifton_r400

Fixed typo for spi ram compile

Change 110443 on 2003/07/11 by bbuchner@bbuchner_crayola_linux_orl

    added CC debug path in to debug module

Change 110421 on 2003/07/11 by llefebvr@llefebvr_r400_linux_marlboro

This is the bvrl file I forgot to submit along with the .mc file.

Change 110419 on 2003/07/11 by llefebvr@llefebvr_r400_emu_montreal

Added MOVA to the list of compare opcodes. The SP instead of doing a simple compare of
the GPRs for mova (as it should do) was doing an Add. This was causing corruptions
whenever MOVA was used to move data from GPR to GPR. This change fixed test
mova_tests.cpp TEST_CASE=mova_reg.

Change 110414 on 2003/07/11 by jayw@jayw_r400_linux_marlboro

Fix clean signals.

Change 110410 on 2003/07/11 by nkociuk@nkociuk_r400_linux_marl

a few small bug fixes

Change 110406 on 2003/07/11 by cbrennan@cbrennan_r400_linux_marlboro

X out sector format for unknown formats.

Change 110401 on 2003/07/11 by viviana@viviana_crayola2_syn

Changed the sq/vc 103 memory to 104.
```

```
Change 110399 on 2003/07/11 by cbrennan@cbrennan_r400_linux_marlboro

Changed TPC data pipeline to ignore channel only state changes for efficiency and to
get around emu high color issues.
Also checks for TPC data collisions better than it used to.

Change 110384 on 2003/07/11 by smburu@smburu_r400_linux_marlboro

New function used by tp_hicolor.mc

Change 110348 on 2003/07/10 by vbhatia@vbhatia_r400_linux_marlboro

Added test and emu support for fmt_32_32_32 float (fmt number 57)

Change 110340 on 2003/07/10 by paulv@paulv_r400_linux_marlboro

Fixed typo.

Change 110338 on 2003/07/10 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 110332 on 2003/07/10 by johnchen@johnchen_r400_linux_marlboro

expand logic moved to probe side

Change 110328 on 2003/07/10 by donaldl@donaldl_crayola_linux_orl

Bug fix - delayed read address in real-time parameter caches & added missing clocks
when instantiating sx_rt_param_cache.

Change 110310 on 2003/07/10 by viviana@viviana_crayola2_syn

Changed the vc memory to 104 bits wide, deleted the 103 memory and rebuilt all
   memories with latest version of virage.

Change 110302 on 2003/07/10 by smburu@smburu_r400_linux_marlboro

.

Change 110300 on 2003/07/10 by viviana@viviana_crayola2_syn

STAR_cmdscout should be an output of this module and not an input.

Change 110281 on 2003/07/10 by smburu@smburu_r400_linux_marlboro

A whole bunch of new logic to take care of sign-mag convertion,
and RF EXPAND.
```

```
Change 110266 on 2003/07/10 by tien@tien_r400_devel_marlboro

Cleaned up TP_SQ_dec
More formatter fixes.

Change 110250 on 2003/07/10 by jbrady@jbrady_crayola_linux_orl

Select request bus based on bit 6 again, not bit 7. This is the proper interleave.

Change 110248 on 2003/07/10 by mzini@mzini_crayola_linux_orl

 Bit 6 of the address selects controller pair and bit 7 selects the controller

Change 110240 on 2003/07/10 by cbrennan@cbrennan_r400_emu

Moved data around a flop to help mip packing timing.

Change 110200 on 2003/07/10 by tien@tien_r400_devel_marlboro

formatter clamping fix
driving TP_SQ_dec as it should be

Change 110177 on 2003/07/10 by rramsey@rramsey_crayola_linux_orl

Changes to get simd_id piped down the vertex side and into the thread
buffer. Also only write the active simd's gprs and mux pipe_disable bits.
The memory in sq_vc_skid_buf increased by 1 bit, so this will require
a new memory to be checked in before running without USE_BEHAVE_MEM.

Change 110165 on 2003/07/10 by kevino@kevino_r400_linux_marlboro

 Got rid of parens from 16 bit add-  not sure if it will help, but this code has met
timing before and this was the only change.

Change 110110 on 2003/07/09 by mzini@mzini_crayola_linux_orl

 Show usage

Change 110107 on 2003/07/09 by paulv@paulv_r400_linux_marlboro

Leda fixes.

Change 110105 on 2003/07/09 by msprague@msprague_r400_synth

Fixed width mismatch between data ports and ram size.

Change 110083 on 2003/07/09 by dougd@dougd_r400_linux_marlboro
```

```
added data output mux to select between the two memories (SIMD1, SIMD0)
for RBBM diagnostic reads. The mux is controlled by a rbbm register bit
in the SQ_DEBUG_MISC register.

Change 110066 on 2003/07/09 by vromaker@vromaker_r400_linux_marlboro

- fixed a bug in tex instr seq related to back-to-back constant reads

Change 110052 on 2003/07/09 by paulv@paulv_r400_linux_marlboro

Timing fix.

Change 110041 on 2003/07/09 by tien@tien_r400_devel_marlboro

More formatter fixes
Fixed sec pitch calcs

Change 110035 on 2003/07/09 by moev@moev2_r400_linux_marlboro

Changed the HS Star Processor connections to match the clients. In particular BiraFail
& Err_pip_or

Change 110023 on 2003/07/09 by kevino@kevino_r400_linux_marlboro

  re-added end of file

Change 110019 on 2003/07/09 by donaldl@fl_donaldl_p4

Testbench (vsim) for sx_param_sub block.

Change 110018 on 2003/07/09 by kevino@kevino_r400_linux_marlboro

   last revision was empty-  not sure why

Change 110014 on 2003/07/09 by kevino@kevino_r400_linux_marlboro

      Added code for agp512 to be done in tcb_mh_arb.
      tcb_core adds other halves of 512 bit requests (if not already in the sector
mask) Needed for the tag and cacheline to know which sectors fetched.
      tcb_fetch_fifo removes them
      tcb_mh_arb multicycles to request the original and missing halves.
      tcb_agp_type figures out which sector bit determines which half of a 512 bit
request the sector is based on format, tiled, and opcode.

Change 110004 on 2003/07/09 by cbrennan@cbrennan_r400_emu

fix mip packing disable for 1d textures.
```

```
Change 109998 on 2003/07/09 by wlawless@wlawless_r400_linux_marlboro

Reorganized how to manage probe more then one tile to avoid locking up
the ops.... hard to explain

Change 109978 on 2003/07/09 by vbhatia@vbhatia_r400_linux_marlboro

updated gen15 and gen31 to not generate invalid dst_sel

Change 109960 on 2003/07/09 by bbuchner@bbuchner_crayola_linux_orl

     added register readback, modified cache invalidate, removied dc busy

Change 109951 on 2003/07/09 by llefebvr@llefebvr_r400_emu_montreal

Fixing yet another mova problem when the mova is not back to back with it's use and
there is only one waterfall pass, PVPS detection wasn't re-enabled correctly. Fixes
mova_tests.cpp TEST_CASE=mova512_nop_check

Change 109932 on 2003/07/09 by mzini@mzini_crayola_linux_orl

 Changed the serialization of the constant and remapped the gpr_phase to match the SQ
hardware

Change 109930 on 2003/07/09 by jbrady@jbrady_crayola_linux_orl

Reverse constant serialization.
 Receive sq send on cycles 2301, not 0123.

Change 109922 on 2003/07/09 by cbrennan@cbrennan_r400_linux_marlboro

Put parens back to when packing met timing.
Disable packing when doing a 1d fetch.

Change 109897 on 2003/07/09 by mzini@mzini_crayola_linux_orl

 Fixed typo

Change 109819 on 2003/07/08 by tien@tien_r400_devel_marlboro

Final port SQ_TP_simd_id

Change 109814 on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro

- contains RT bit connection from pix input ctl to pix thread buff
- added SQ_TP_simd_id output to top level
```

```
Change 109791 on 2003/07/08 by rmanapat@rmanapat_r400_sun_marlboro

Fix for random test fail...regarding fmt 51 and agp512

Change 109785 on 2003/07/08 by tien@tien_r400_devel_marlboro

VC mode fixes for formatter

Change 109777 on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro


Change 109760 on 2003/07/08 by mzini@mzini_crayola_linux_orl

 Added more error checking

Change 109759 on 2003/07/08 by mzini@mzini_crayola_linux_orl

 Added comment

Change 109758 on 2003/07/08 by mzini@mzini_crayola_linux_orl

 Enabled random fifo depths

Change 109744 on 2003/07/08 by paulv@paulv_r400_linux_marlboro

Hardwired the rb_rc_sync_clean* signals to 1 for Orlando (until color and depth
implement their surface sync logic).

Change 109741 on 2003/07/08 by smburu@smburu_r400_linux_marlboro

Virage proc. creation for TCM due to change in TCO mems.

Change 109735 on 2003/07/08 by rmanapat@rmanapat_r400_sun_marlboro

this fixes the DXT formats for the volume tests

Change 109719 on 2003/07/08 by kmeekins@kmeekins_crayola_linux_orl

Moved the error checking to its own process. Now testing only the cache address
  that is getting written.

Change 109701 on 2003/07/08 by kmeekins@kmeekins_crayola_linux_orl

Initial release.

Change 109679 on 2003/07/08 by llefebvr@llefebvr_r400_emu_montreal

Fixed r400sp_mova_tests.cpp TEST_CASE=mova512.
```

```
The PVPS detection was rightly disabled during the waterfall but wasn't re-enabled for
the following instructions of the clause. I used the waterfall_done signal to re-enable
the PVPS detection after the waterfalling.

Change 109671 on 2003/07/08 by vromaker@vromaker_r400_linux_marlboro

- updated tex instr seq to sync to the texconst phase
- changed fetch arb to output both the mega grant and the mini
         grant to the tex instr seq

Change 109666 on 2003/07/08 by rmanapat@rmanapat_r400_sun_marlboro

Fix for fmt 19, 20 , 49 3d tiled...still working on other dxt fmts...

Change 109661 on 2003/07/08 by viviana@viviana_crayola2_syn

Changed to the latest version of the Virage compilers.

Change 109660 on 2003/07/08 by kevino@kevino_r400_win_marlboro

removed parens from add of 16 single bits-  hope that synopsys will pick adder better
now.

Change 109658 on 2003/07/08 by kmeekins@kmeekins_crayola_linux_orl

vc_cc.v
  -------
  - Created new register name request_size_dl_q.
  - Created new signal to indicate a request size greater than 256 bit mode
    and attached it to required module I/O.

  vc_cc_pack_align.v
  vc_cc_tag_process.v
  -------------------
  New signal I/O

  vc_cc_loaded_busy.v
  -------------------
  - Created a new storage bit for request size in each cache line.
  - Added new logic to prevent allocation if all requested sectors are not loaded.

Change 109631 on 2003/07/07 by mzini@mzini_crayola_linux_orl

 Delete the results directory if the random tests passes

Change 109617 on 2003/07/07 by vbhatia@vbhatia_r400_linux_marlboro
```

```
Added few more tests for ease of debug

Change 109590 on 2003/07/07 by viviana@viviana_crayola2_syn

Corrected another non-blocking assignment to blocking in a combinational logic block.

Change 109568 on 2003/07/07 by johnchen@johnchen_r400_linux_marlboro

add rb_include.v

Change 109565 on 2003/07/07 by viviana@viviana_crayola2_syn

Corrected non-blocking assignments to blocking in combinational block.

Change 109561 on 2003/07/07 by smburu@smburu_r400_sun_marlboro

Changed the width of one instance of ati_dff_inout to overcome
synthesis problems.

Change 109555 on 2003/07/07 by kmeekins@kmeekins_crayola_linux_orl

vc_cc.v
  -------
  Added request size to the pack_align interface.

  vc_cc_pack_align.v
  ------------------
  Using the request size to modify the sector mask for requests. The 512 bit
  mode will force a fetch of both sectors but only if at least one of the sectors
  has been requested. This improves the efficiency between 256 and 512 bit modes.

  vc_cc_tag_compare.v
  -------------------
  Created a way write enable for tag 0 and tag 1 to better control how a way is
  written when the same way is effected by two different tags.

Change 109535 on 2003/07/07 by cbrennan@cbrennan_r400_linux_marlboro

Oops.. inserted bug by mistake.  ste-upid parentheses.

Change 109526 on 2003/07/07 by cbrennan@cbrennan_r400_linux_marlboro

Leda errors.

Change 109467 on 2003/07/07 by vbhatia@vbhatia_r400_linux_marlboro

few formatter emu fixes and testbench updates
```

```
Change 109466 on 2003/07/07 by dougd@dougd_r400_linux_marlboro

fixed error in bit width of ais_real_time

Change 109464 on 2003/07/07 by viviana@viviana_crayola2_syn

Added the register in the 128x128 memory, rebuilt the Virage system with latest
compilers.

Change 109463 on 2003/07/07 by cbrennan@cbrennan_r400_linux_marlboro

Leda errors.

Change 109454 on 2003/07/07 by hmonsef@hmonsef

Replaced 64x49 with 64x50

Change 109443 on 2003/07/07 by cbrennan@cbrennan_r400_linux_marlboro

Small timing fix for mip packing chain.

Change 109202 on 2003/07/03 by tien@tien_r400_devel_marlboro

Removed cmask
Reduced data_valid to 1 bits

Change 109183 on 2003/07/03 by cbrennan@cbrennan_r400_linux_marlboro

fixing compile errors from vcs in tcm_registers stub.

Change 109167 on 2003/07/03 by mzini@mzini_crayola_linux_orl

 Script to submit multiple random tests

Change 109151 on 2003/07/03 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 109138 on 2003/07/03 by cbrennan@cbrennan_r400_emu

Mip packing fix for strongly rectangular and 1D textures.

Change 109132 on 2003/07/03 by smburu@smburu_r400_linux_marlboro

Moved to tp_hicolor_tb directory.

Change 109128 on 2003/07/03 by mzini@mzini_crayola_linux_orl
```

```
 Added error checking in RP

Change 109126 on 2003/07/03 by dougd@dougd_r400_linux_marlboro

pipelined the Real Time bit from the pix thread buffer down through
both arbiters, the vc, tex and alu instruction pipelines to the alu,
tex and cfc constant stores to enable reading the real time constants.

Change 109105 on 2003/07/03 by cbrennan@cbrennan_r400_emu

Enable mip packing in ferret.
       Enable mip packing in directed tests.
       Mip packing bug fixes in HW.

Change 109091 on 2003/07/03 by paulv@paulv_r400_linux_marlboro

Yet more timing fixes.

Change 109058 on 2003/07/03 by dclifton@dclifton_r400

Got rid of warning about bit size mismatch.

Change 109043 on 2003/07/03 by vromaker@vromaker_r400_linux_marlboro

made all loop counter variables unique for sythesis

Change 109020 on 2003/07/03 by mzini@mzini_crayola_linux_orl

 Bumped timeout counters

Change 108994 on 2003/07/02 by jayw@jayw_r400_linux_marlboro

couple of missing sx index size fixes and move rb_include.

Change 108960 on 2003/07/02 by paulv@paulv_r400_linux_marlboro

Timing fixes for RBM and RBT.  With both subblocks, I removed the cam_lookup modules
and just moved the logic into their respective blocks.

Change 108947 on 2003/07/02 by dclifton@dclifton_r400

Updated makefile for latest changes.  Fixed testbench test signals into SP and SPI.

Change 108942 on 2003/07/02 by dclifton@dclifton_r400

double buffered resets

Change 108937 on 2003/07/02 by kmeekins@kmeekins_crayola_linux_orl
```

```
Seperated the set valids for each tag to permit cache hit status to each
  way that is dependent on the tags. This prevents a tag 0 hit from altering
  the way replacement policy for tag 1 and vice versa.

Change 108920 on 2003/07/02 by nkociuk@nkociuk_r400_linux_marl

adding missing files...

Change 108901 on 2003/07/02 by kevino@kevino_r400_linux_marlboro

  replaced these with mems 51 wide

Change 108887 on 2003/07/02 by jcarroll@jcarroll_crayola_linux_orl

VCRP: added debug, performance and prog depth FIFOs

Change 108880 on 2003/07/02 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 108879 on 2003/07/02 by nkociuk@nkociuk_r400_linux_marl

add rbbm interface to tcm and wire up tcr to readback daisy chain

 move tco perfmon signals from tcr perfmon block to new perfmon block in tcm,
add/remove relevent top-level wires

Change 108876 on 2003/07/02 by rmanapat@rmanapat_r400_sun_marlboro

Moved some logic related to agp512 from the tcb_sectormask_generator module
to it's own module tcb_agp_type which is at the same hierarchy level as
the sectormask_generator module...This prevent the logic from being repeated
4x since the sectormask_generator module is a per quad module but the values
being generated by the tcb_agp_type.v module is spread across all quads

Change 108869 on 2003/07/02 by jayw@jayw_r400_linux_marlboro

Moving file to common directory from gfx/rb, no other change.

Change 108858 on 2003/07/02 by mzini@mzini_crayola_linux_orl

 Bumped timout counters

Change 108857 on 2003/07/02 by jcarroll@jcarroll_crayola_linux_orl

Updated signal name: VC_SP_xyzw_cycle
```

Change 108842 on 2003/07/02 by kevino@kevino_r400_linux_marlboro

  Group together add of 16 1 bit values into clumps of three to try to optimize for synthesis.

Change 108840 on 2003/07/02 by mzini@mzini_crayola_linux_orl

 Added usage message

Change 108829 on 2003/07/02 by smburu@smburu_r400_linux_marlboro

Corrected error in format table for formats 2-0.

Change 108828 on 2003/07/02 by kevino@kevino_r400_linux_marlboro

      Some changes to send the 512bit request signal down to the TCO so it can expand the mask of sectors it is waiting to be written to include the other halves of each 256 bit request to avoid a condition where the cacheline is cleared before the other (unneeded) half is written.

Change 108818 on 2003/07/02 by bbuchner@bbuchner_crayola_linux_orl

updated I/O

Change 108808 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Testbench enhancements

Change 108786 on 2003/07/01 by paulv@paulv_r400_linux_marlboro

Fixed the probe logic so tiles with no surfaces enabled get probed with out a cycle delay between them (necessary due to the 2-cycle address calculation, which is needed to determine cam hits/misses). This problem was causing a non-surface-enabled test to hang.

Change 108781 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Bumped timeout counters

Change 108778 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Added a slow sq mode where simd grants are issued less often

Change 108774 on 2003/07/01 by tien@tien_r400_devel_marlboro

Bug fix in tpc_fifos for pm4ply test
Misc formatter fixes

```
Change 108765 on 2003/07/01 by nkociuk@nkociuk_r400_linux_marl

checkin...

Change 108764 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Fixed fail checking

Change 108763 on 2003/07/01 by llefebvr@llefebvr_r400_emu_montreal

Updates for r400sq_const_index_0x.cpp

Change 108760 on 2003/07/01 by llefebvr@llefebvr_r400_linux_marlboro

Fixed r400sq_const_index_03.cpp. Now works on the SQSP testbench. Still has issues on
the GC because of bad ferret/cp ring buffer synchronization.

Fixed:

1) Bad clamping of the address register in the SP
2) Bad error handling of an out of range address in the SQ.

Change 108751 on 2003/07/01 by paulv@paulv_r400_linux_marlboro

More minor timing fixes.

Change 108750 on 2003/07/01 by wlawless@wlawless_r400_linux_marlboro

fixed a pesky little bug

Change 108744 on 2003/07/01 by vromaker@vromaker_r400_linux_marlboro

- registered winner_ack out of thread arb for timing
- connected correct instruction store read output based on SIMD1
  for VC ctl flow instruction reads; now SQ_VC interface appears to
  be driven correctly
- minor change to tb_sqsp (commented out random stall for TP_SQ_fetch
  stall, which no longer exists)

Change 108733 on 2003/07/01 by rmanapat@rmanapat_r400_sun_marlboro

fix for agp512

Change 108728 on 2003/07/01 by kmeekins@kmeekins_crayola_linux_orl

Changed the sector valid logic to correctly use the tag set id in determining
  the write enable.
```

```
Change 108726 on 2003/07/01 by rmanapat@rmanapat_r400_sun_marlboro

Submission of new file

Change 108723 on 2003/07/01 by mzini@mzini_crayola_linux_orl

 Cleanup

Change 108718 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Added ability to run VC testbench without dumping signals

Change 108703 on 2003/07/01 by kevino@kevino_r400_linux_marlboro

  Get rid of soi/newstate being piped down to fetch fifo.  Not used.

Change 108701 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Testbench was timing out early in random tests

Change 108700 on 2003/07/01 by nkociuk@nkociuk_r400_linux_marl

add log2 lookup tables

 hw updates to match emulator, changelist #108505

Change 108698 on 2003/07/01 by kevino@kevino_r400_linux_marlboro

  Timing fix for fetch gen walker-  count smasks to be sent to generate RTR.
  Fetch generator file also added in a ifdef sim for the number of requests going out
to the mh arbs at each cycle

Change 108691 on 2003/07/01 by jcarroll@jcarroll_crayola_linux_orl

Added more support for 3 float data format.

Change 108685 on 2003/07/01 by mzini@mzini_crayola_linux_orl

Rewrote the RP testbench to handle random tests

Change 108683 on 2003/07/01 by bhankins@bhankins_crayola_linux_orl

edit for timing.  no functional difference

Change 108681 on 2003/07/01 by kmeekins@kmeekins_crayola_linux_orl

Corrected logic for multicycle control.
```

```
Change 108676 on 2003/07/01 by dougd@dougd_r400_linux_marlboro

generated trigger signals for SIMD0,SIMD1 perfmon counters

Change 108642 on 2003/06/30 by donaldl@donaldl_crayola_linux_orl

Added rbiu controls for real-time updates to parameter cache mems (real-time mems)

Change 108632 on 2003/06/30 by nkociuk@nkociuk_r400_linux_marl

change probe filter busy.  replaced tca_stall with out_stall_q.  original change was to
keep sclk_tca running long enough to always capture the last high-to-low
 transition of TCA_TCB_stall (without the change, sometimes the clock shut off before
the transition reached the capture flop in the tca.  only effect of this
 that i'm aware of is that the perf logic would end up counting several hundred invalid
probe filter stalls).  this modification achieves the same basic result,
  but is less likely to hurt timing.

Change 108627 on 2003/06/30 by tien@tien_r400_devel_marlboro

More formatter fixes

Change 108616 on 2003/06/30 by jcarroll@jcarroll_crayola_linux_orl

Added support for 3 float data format.

Change 108595 on 2003/06/30 by jayw@jayw_r400_linux_marlboro

missed module name.

Change 108593 on 2003/06/30 by jayw@jayw_r400_linux_marlboro

Adding 16 bit pixel mask through DB. NOTE: db_stdrfsdks2p8x136cm1sw0 is now
db_stdrfsdks2p8x152cm1sw0

Change 108585 on 2003/06/30 by rramsey@rramsey_crayola_linux_orl

hook up the sx_rb_quad_mask signals to the fake_rb's
not sure how this was working at all with the live SX

Change 108572 on 2003/06/30 by jcarroll@jcarroll_crayola_linux_orl

VCRP: Added logic to handle an L2 request with 4 invalid banks.

Change 108556 on 2003/06/30 by jbrady@jbrady_crayola_linux_orl

Add new 3 float format to count override mux.
```

```
Change 108552 on 2003/06/30 by paulv@paulv_r400_linux_marlboro

Some minor timing fixes.

Change 108551 on 2003/06/30 by hmonsef@hmonsef

replaced by 8x152

Change 108550 on 2003/06/30 by hmonsef@hmonsef

Replaces 8x132

Change 108549 on 2003/06/30 by hmonsef@hmonsef

Replaced 8x132 with 8x152

Change 108543 on 2003/06/30 by tien@tien_r400_devel_marlboro

Vector width mismatch fixes

Change 108536 on 2003/06/30 by smoss@smoss_crayola_linux_orl_regress

   removed rand function warning

Change 108533 on 2003/06/30 by smburu@smburu_r400_sun_marlboro

Missing sensitivity list variable.

Change 108524 on 2003/06/30 by dougd@dougd_r400_linux_marlboro

generate read enable for sq_hs_sms_sq_shsd1_320x96cm4 in sq_texconst_mem
and read enable for sq_stdrfsdks2p64x32cm4sw0 in sq_texconst_rams

Change 108523 on 2003/06/30 by jbrady@jbrady_crayola_linux_orl

Send written signals to MH on 256 bit boundaries, not 128 bit.
 Fix hook-up of written in testbench - were driven to 1. Not sure how we were passing..

Change 108521 on 2003/06/30 by wlawless@wlawless_r400_linux_marlboro

Gated mask_q with load_src_addr

Change 108519 on 2003/06/30 by mzini@mzini_crayola_linux_orl

Fixed data in return data path

Change 108512 on 2003/06/30 by mzini@mzini_crayola_linux_orl
```

```
The MI now send a written on every 256 bits of data instead of 128

Change 108511 on 2003/06/30 by rramsey@rramsey_crayola_linux_orl

changes for new sp top level

Change 108507 on 2003/06/30 by paulv@paulv_r400_linux_marlboro

Fixed LEDA error.

Change 108494 on 2003/06/30 by tien@tien_r400_devel_marlboro

Finalized VC_SP IO on the sp side

Change 108491 on 2003/06/30 by johnchen@johnchen_r400_linux_marlboro

small fix for flush

Change 108444 on 2003/06/27 by vbhatia@vbhatia_r400_linux_marlboro

Added extra test vector clamp for vertex rf expand enabled, signed no-zero case

Change 108420 on 2003/06/27 by vbhatia@vbhatia_r400_linux_marlboro

updated vc formatter testbench and added a few tests

Change 108417 on 2003/06/27 by paulv@paulv_r400_linux_marlboro

Converted rb_rba_alpha_blend_cntl.v to rb_rba_alpha_blend_cntl_alpha and _color
versions.  This was done to reduce area (instantiating rb_rba_alpha_blend_cntl.v for 8
channels wasted gates) and to fix some minor timing problems.

Change 108403 on 2003/06/27 by mzini@mzini_crayola_linux_orl

 Don't always send data when receiver is ready

Change 108400 on 2003/06/27 by rmanapat@rmanapat_r400_sun_marlboro

Fix for a tc_simple_mip_random testcase

Change 108392 on 2003/06/27 by paulv@paulv_r400_linux_marlboro

Timing fixes and logic fix (smask decode of GEQUAL and NOTEQUAL was backwards).

Change 108358 on 2003/06/27 by mzini@mzini_crayola_linux_orl

 Randomize the rdy to the MI
```

```
Change 108354 on 2003/06/27 by moev@moev2_r400_linux_marlboro

Added module for needed for Virage AWT mode

Change 108353 on 2003/06/27 by jbrady@jbrady_crayola_linux_orl

Fix internal_pipe_freeze. Only freeze if stage 1 rts, otherwise I'm looking
  at old data.

Change 108336 on 2003/06/27 by kmeekins@kmeekins_crayola_linux_orl

Corrected more sector, bank bit field mismatches.
  Conditioned the sector loading bits with the fetch size so that a fetch
  size greater that 256 will always fetch both sectors.

Change 108332 on 2003/06/27 by rmanapat@rmanapat_r400_sun_marlboro

Additional fix for nonZero Framebuffer...previous fix only worked
for 1d formats

Change 108319 on 2003/06/27 by rmanapat@rmanapat_r400_sun_marlboro

Fixes a bug where if the mip level gets too high in cubic_mip
the face_offset goes to 0 due to the height not being clamped
correctly...this should fix all the fails from last night
directed tests on tc_simple_mip_cubic that aren't EMU fails

Change 108316 on 2003/06/27 by johnchen@johnchen_r400_linux_marlboro

fix so the expanded flushes works correctly when rtr goes away at anytime

Change 108315 on 2003/06/27 by mmang@mmang_crayola_linux_orl

Qualify constant address register write using constant waterfalling mask

Change 108304 on 2003/06/27 by moev@moev2_r400_linux_marlboro

Made changes to fix Virage test signals, added awt_gate.

Change 108303 on 2003/06/27 by moev@moev2_r400_linux_marlboro

recreated control file to correct invalid number of fuses in the fusebox.

Change 108296 on 2003/06/27 by nkociuk@nkociuk_r400_linux_marl

remove tc-testbench sclk_tca hack
 include tca_stall in busy bit for dynamic clocking
```

```
Change 108276 on 2003/06/27 by tien@tien_r400_devel_marlboro

Fixed runme script yet again :-)
More formatter fixes

Change 108266 on 2003/06/27 by rmanapat@rmanapat_r400_sun_marlboro

Fix for simple_mip_1d tests that use a secondary_pitch_x larger
than the clamp value...This got all the tc_simple_mip_1d random tests
that failed last night to pass

Change 108263 on 2003/06/27 by paulv@paulv_r400_linux_marlboro

Forgot to assign the fog and const color flopped values to their respective outputs.
Fixed.

Change 108254 on 2003/06/27 by moev@moev2_r400_linux_marlboro

Changes for virage test connections.

Change 108253 on 2003/06/27 by wlawless@wlawless_r400_linux_marlboro

stuff

Change 108251 on 2003/06/27 by johnchen@johnchen_r400_linux_marlboro

convert a 28fixed value to 16bits and 24bits depth values

Change 108250 on 2003/06/27 by rramsey@rramsey_crayola_linux_orl

left some signals out of a sensitivity list

Change 108249 on 2003/06/27 by jcarroll@jcarroll_crayola_linux_orl

Increased timeout count.

Change 108227 on 2003/06/27 by bhankins@bhankins_crayola_linux_orl

add some debug signals

Change 108222 on 2003/06/27 by smoss@smoss_crayola_linux_orl_regress

   I have too many i's

Change 108208 on 2003/06/26 by dclifton@dclifton_r400

Changes to get the tb_sqsp to work in modelsim
```

```
Change 108196 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

More agp request fixes and fixed the addresses after determining if a request is using
the external queue.

Change 108195 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 108188 on 2003/06/26 by mmang@mmang_crayola_linux_orl

For pixel quads, enable all pixels of a quad when any pixel is hit
for gpr write enables and constant address waterfalling sequencing.
Another update will fix constant address register writing.

Change 108184 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 108181 on 2003/06/26 by tien@tien_r400_devel_marlboro

Formatter fixes

Change 108175 on 2003/06/26 by mmang@mmang_crayola_linux_orl

Re-put in sx SQ_SX_free_id fix that was lost in merge.

Change 108169 on 2003/06/26 by wlawless@wlawless_r400_linux_marlboro

fixed a cache cohearicncy bug in ms

Change 108147 on 2003/06/26 by mzini@mzini_crayola_linux_orl

Added trackinh of the data that gets piped along the VC to the SP

Change 108140 on 2003/06/26 by rramsey@rramsey_crayola_linux_orl

Split src_swizzle out of SQ_SP_instr bus so fetch swizzle can be
driven during unused phase
Add interp_xyline from SQ to SPI to drive read address for xy buffer
Clean up some compile warnings in sc_iter
Change the existing macc to handle the swizzle being driven for all
4 phases and add the fetch address swizzling
Fix param_gen and gen_index pipeline length around the interpolators
Replace src_c_swizzle.z with src_c_swizzle.x for all instructions
other then MULADD and CNDx
Fix the generation of init_cycle_cnt_q in sq_pix_ctl for interpolation
involving param_gen and gen_index params
```

```
Add compares for SQ_SX_export_mask_we and SQ_SX_kill_mask to tbtrk_spsx
Fix the fetch_addr swizzle generation for vertex fetches (need to use
[31:30] instead of [27:26])
Fix a bug in sq_vtx_ctl related to gpr allocation (size requested was
off by a clock)

Change 108132 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Add wait for license to simv command line.

Change 108121 on 2003/06/26 by smoss@smoss_crayola_linux_orl_regress

   $value$plusargs doesn't currently work properly for cadence changed logic to turn
off grouper by default

Change 108117 on 2003/06/26 by vbhatia@vbhatia_r400_linux_marlboro

Added +CLAMPOFF option, regularly on with clamping data to only values supported by
hardware and can be turned off by this option to test behavior for other values

Change 108112 on 2003/06/26 by jcarroll@jcarroll_crayola_linux_orl

When clamping, vert0_offset is used for both even and odd requests.

Change 108099 on 2003/06/26 by jayw@jayw_r400_linux_marlboro

Missing definition of HIGH.

Change 108097 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Remove nusiance error check code.

Change 108096 on 2003/06/26 by kmeekins@kmeekins_crayola_linux_orl

Added a register on the input FIFO read data to help with critical path timing.
  Changed the fifo valid register delay being used by the pack and align logic.

Change 108094 on 2003/06/26 by kevino@kevino_r400_linux_marlboro

    removed [0:0] from 1 bit signals so that ncverilog could compile it as well

Change 108093 on 2003/06/26 by kevino@kevino_r400_linux_marlboro

  chchchchchchchchchanged VC_TC_info to be 8 bits instead of 18

Change 108092 on 2003/06/26 by kevino@kevino_r400_linux_marlboro

  revamped timiing fix to hopefully be better
```

```
Change 108088 on 2003/06/26 by rmanapat@rmanapat_r400_sun_marlboro

Added support for 3d tiled formats that do not use cacheline format 9
til_fmt11 and til_fmt12 will now pass tc_simple_3d

Change 108083 on 2003/06/26 by nkociuk@nkociuk_r400_linux_marl

update .bvrl files to match changes in changelist 108078

Change 108080 on 2003/06/26 by tien@tien_r400_devel_marlboro

Fixed mini-regress script for release_* area usage
Fixed large unnuomed coord handling (for a cp_e2* test) .. for real this time I think )
Misc sp_tp_formatter fixes

Change 108079 on 2003/06/26 by nkociuk@nkociuk_r400_linux_marl

mini-testbench updates

Change 108078 on 2003/06/26 by nkociuk@nkociuk_r400_linux_marl

change log2 logic to lookup table, drop unused lsb...

update lod_aniso_test as appropriate

Change 108077 on 2003/06/26 by wlawless@wlawless_r400_linux_marlboro

Added toggle_q to dec2

Change 108073 on 2003/06/26 by jayw@jayw_r400_linux_marlboro

Preparing for making SX index 8 bits instead of 7 bits.

Change 108065 on 2003/06/26 by wlawless@wlawless_r400_linux_marlboro

Got the first blend multisample to work,,, changed a few things

Change 108063 on 2003/06/26 by viviana@viviana_crayola2_syn

Regenerated the high speed memories to add two instances of the 1280x128 and two
instances of the
   4096x96.

Change 108059 on 2003/06/26 by jayw@jayw_r400_linux_marlboro

Preparing for Extending SX index from 7 to 8 bits.
```

```
Change 108058 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Fix nstate for state 0a. Fix for both requests valid and not conflicting, where
  request 1 has sector mask of 0x3 and request size is 256.

Change 108050 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Fixes for external queue logic.

Change 108049 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

Fixes for quad cache stall logic.

Change 108045 on 2003/06/26 by donaldl@donaldl_crayola_linux_orl

No functional change -- regenerated to remove compare warnings during synthesis

Change 108024 on 2003/06/26 by mmantor@FL_mmantorLT_r400_win

remove template file having problems in ncverilog

Change 108023 on 2003/06/26 by jbrady@jbrady_crayola_linux_orl

Use bit 7 off address to determine which interface to place request on, not bit 6.
  Bit 7 makes the interleave 1024 bits between interfaces, 512 on each mc.
 Fix bug in 256 bit request mode state machine. nstate was wrong for only
  request 1 valid in state 0a.

Change 108020 on 2003/06/26 by paulv@paulv_r400_linux_marlboro

LEDA fix.

Change 108015 on 2003/06/26 by moev@moev2_r400_linux_marlboro

Fixed STAR connections in particualr the cmdscin signals.
cm1 gets STAR_testbus_rf[6], cm2 gets STAR_testbus_rf[7] and cm4 gets
STAR_testbus_rf[8]

Change 108014 on 2003/06/26 by rmanapat@rmanapat_r400_sun_marlboro

Just a readbility change getting ready for implementing 3d tiled
cases that are assigned like 2d tiled

Change 108012 on 2003/06/26 by bhankins@bhankins_crayola_linux_orl

fix some signals used for debug

Change 108011 on 2003/06/26 by bhankins@bhankins_crayola_linux_orl
```

```
minor fix

Change 108009 on 2003/06/26 by bhankins@bhankins_crayola_linux_orl

fix logic errors in alpha test

Change 107997 on 2003/06/26 by mmantor@mmantor_crayola_linux_orl

<remove extra delay stage on scalar_data for scalar_input_red when scalar_opcode_prev
and the creation of force_mul_prev2_max_float to compensate for the stage added back
into the scalar engine>

Change 107977 on 2003/06/25 by viviana@viviana_crayola2_syn

Recompiled the sx memories to remove second instantiation of the sx_rf_awt_gate module.

Change 107914 on 2003/06/25 by jcarroll@jcarroll_crayola_linux_orl

Removed the coast regs for the L2 read address.
       Added coast regs for the L2 read data.

Change 107913 on 2003/06/25 by mzini@mzini_crayola_linux_orl

 Fixed bug in data return path. Plus added other 2 return paths

Change 107911 on 2003/06/25 by mdesai@mdesai_r400_linux

Generated a new bvrl file with several bug fixes

Change 107909 on 2003/06/25 by mdesai@mdesai_r400_linux

Added the full c_texel value to tp_clamp.mc

Change 107908 on 2003/06/25 by mdesai@mdesai_r400_linux

Fixed several bugs:
incorrect coordinate (needed to decrement the x0 and y0 texels)
incorrect inc values for x and y
incorrect valid
incorrect fraction

Change 107907 on 2003/06/25 by kmeekins@kmeekins_crayola_linux_orl

Corrected sector valid write enable logic.

Change 107906 on 2003/06/25 by mdesai@mdesai_r400_linux
```

```
Fixed Mirror Once to Border case by changing the texel_sel bit

Change 107898 on 2003/06/25 by paulv@paulv_r400_linux_marlboro

Timing fixes and fixed a typo in the quad cache.

Change 107879 on 2003/06/25 by paulv@paulv_r400_linux_marlboro

Put the probe_address mux back in (it must have been deleted by accident when I was
doing a timing fix).

Change 107872 on 2003/06/25 by cbrennan@cbrennan_r400_linux_marlboro

Removed Local_Base_Addr from top level.  Was accidentally leaked out.

Change 107871 on 2003/06/25 by cbrennan@cbrennan_r400_linux_marlboro

Tied in VC#_TC_send and VC_TC_clean# signals over top level.  TC requires chip_vc.tree

Change 107865 on 2003/06/25 by johnchen@johnchen_r400_linux_marlboro

16fixed overflow correction

Change 107850 on 2003/06/25 by rmanapat@rmanapat_r400_sun_marlboro

I broke fmt_52 and fmt_53 linear when I fixed the tiled case
now this fix lets fmt52 and fmt53 linear and tiled pass

Change 107849 on 2003/06/25 by kevino@kevino_r400_linux_marlboro

 Updated for new CLF3/SA2 format

Change 107845 on 2003/06/25 by jbrady@jbrady_crayola_linux_orl

Monitor on negedge, not posedge. Don't set done if !rtr.

Change 107841 on 2003/06/25 by bhankins@bhankins_crayola_linux_orl

remove enable from memory output register

Change 107822 on 2003/06/25 by rramsey@RRAMSEY_P4_r400_win

and another syntax error

Change 107820 on 2003/06/25 by rramsey@RRAMSEY_P4_r400_win

fix decimal vs hex problem
```

```
Change 107817 on 2003/06/25 by fhsien@fhsien_r400_LT

correct syntax error

Change 107814 on 2003/06/25 by moev@moev2_r400_linux_marlboro

Updated connectivity to reflect new memory clock

Change 107812 on 2003/06/25 by moev@moev2_r400_linux_marlboro

Updated instance to reflect two Virage SMS groups

Change 107811 on 2003/06/25 by moev@moev2_r400_linux_marlboro

Updated Makefile that supports nc and new Virage features

Change 107806 on 2003/06/25 by moev@moev2_r400_linux_marlboro

Update file to reflect split between sp and spi

Change 107804 on 2003/06/25 by moev@moev2_r400_linux_marlboro

done with temp file

Change 107802 on 2003/06/25 by moev@moev2_r400_linux_marlboro

Updates to the make file to verify virage RFs.

Change 107801 on 2003/06/25 by grayc@grayc_crayola2_linux_orl

   fix syntax

Change 107799 on 2003/06/25 by rmanapat@rmanapat_r400_sun_marlboro

Fix for til_fmt52 and til_fmt53 tc_simple_2d again...
I had fixed it on the 16th but then screwed it up almost
a week later when I was looking at the spec which needed to be updated
to reflect the correct changes I had put in on the 16th..DOH

Change 107792 on 2003/06/25 by viviana@viviana_crayola2_syn

Connected the STAR test patch signals to L1 cache, L2 cache, L2a, L2b fifos.
   Rebuilt the memories deleting the pipeline register inside.

Change 107789 on 2003/06/25 by mzini@mzini_crayola_linux_orl

Fixed interface comparison in MI testbench
```

```
Change 107788 on 2003/06/25 by jayw@jayw_r400_linux_marlboro

updated to yesterday

Change 107781 on 2003/06/25 by bhankins@bhankins_crayola_linux_orl

add register to output of alpha sample mask memory

Change 107757 on 2003/06/25 by mmantor@mmantor_crayola_linux_orl

< 1. sq_alu_instr_seq.v  - Use the Queue pop signal to qualify last_in_clause
        and last_in_shader out of the queue.
     2. sq_target_instr_fetch.v  - Fixed a buf in the the target_instruct_fetch
        write to the queue to prevent dropping last_in_shader and last_in_clause
        if the queue is full when first trying to send instruction.  >

Change 107743 on 2003/06/24 by paulv@paulv_r400_linux_marlboro

Fixed some skid values of some fifos (and in turn had to resize some RBM fifos).

Change 107735 on 2003/06/24 by vbhatia@vbhatia_r400_linux_marlboro

Updated test bench to clamp out values that are not possible as input to formatter in
rf_expand_enable mode.

Change 107717 on 2003/06/24 by mmantor@mmantor_crayola_linux_orl

<added new regression test for cyl_wrap and changed vcs for texconst mem and fixed wrap
bug in controller during interpolation and added a dum mem config for the texconst
memory  >

Change 107711 on 2003/06/24 by nkociuk@nkociuk_r400_linux_marl

interim checkin

Change 107708 on 2003/06/24 by mzini@mzini_crayola_linux_orl

Module to kill the sim if rtr's go low for too long

Change 107667 on 2003/06/24 by johnchen@johnchen_r400_linux_marlboro

correct 24float overflow detection

Change 107665 on 2003/06/24 by tien@tien_r400_devel_marlboro

Added >1.0 mag clamp in formatter
A few bug fixes with normalizer mux
Added some features to tp_formatter regression script
```

```
Updated tp4_tc  mini regression script

Change 107649 on 2003/06/24 by mzini@mzini_crayola_linux_orl

Fixed buildtb script to only include rtr_checker if running the full VCTB

Change 107645 on 2003/06/24 by tien@tien_r400_devel_marlboro

Possible fix for unnormed coords cp_e2* test found

Change 107639 on 2003/06/24 by mzini@mzini_crayola_linux_orl

Added a module to track how long rtr's stay low and kill the sim

Change 107628 on 2003/06/24 by kevino@kevino_r400_linux_marlboro

  hopefully a timing fix.  Counting sectors in mask may break timing, though, so may be
just first cut.  Also, fg0 and fg1 are a bit different (want to see if one breaks and
the othe doesn't)

Change 107618 on 2003/06/24 by cbrennan@cbrennan_r400_linux_marlboro

Removing verilog 2000 code.

Change 107613 on 2003/06/24 by smburu@smburu_r400_linux_marlboro

Hicolor testbench.

Change 107609 on 2003/06/24 by rmanapat@rmanapat_r400_sun_marlboro

Fixed a problem found using randomseed 0xc9eb0178 and tc_simple_mip_cubic
(before the multiple of 2 changes to the texture size) Due to the mip level
height was being shifted to 0x0 and not being clamped to 0x20 as it should.
this fix clamps it to 0x20 if it is shifted to 0x0 or is less that 0x20.

Change 107606 on 2003/06/24 by paulv@paulv_r400_linux_marlboro

Fixed some LEDA warnings.

Change 107603 on 2003/06/24 by wlawless@wlawless_r400_linux_marlboro

move dest_inflight_q to be free flowing flop... wasn't getting updated

Change 107599 on 2003/06/24 by rmanapat@rmanapat_r400_sun_marlboro

Change to cacheline format 3

Change 107595 on 2003/06/24 by kmeekins@kmeekins_crayola_linux_orl
```

```
Separated cache flush from reset logic. Cache flush now only effects
  the sector valids registers.
  Changed I/O names for the clock, reset, and cache flush signals to match
  top level.

Change 107593 on 2003/06/24 by vbhatia@vbhatia_r400_linux_marlboro

Added new tests and fix for same format_comp_x,y,z,w for rf_expand_enabled mode

Change 107579 on 2003/06/24 by dougd@dougd_r400_linux_marlboro

ncverilog will error with
output [0:0] SQ_SP_instruct_start
wire  SQ_SP_instruct_start
because it considers the 1st declaration a vector and
the 2nd one a scalar.

Change 107561 on 2003/06/23 by mzini@mzini_crayola_linux_orl

Changed script to take tests.run as default

Change 107545 on 2003/06/23 by paulv@paulv_r400_linux_marlboro

Timing fixes and LEDA fixes.  Also removed a file (moved rb_rba_alpha_blend_preswap
logic into rb_rba_blend_bypass).

Change 107529 on 2003/06/23 by viviana@viviana_crayola2_syn

Changed the 64x21 to a 64x19 memory in the rg.

Change 107527 on 2003/06/23 by viviana@viviana_crayola2_syn

Rebuilt the memories to delete 64x21 and add 64x19 in the rp.

Change 107526 on 2003/06/23 by johnchen@johnchen_r400_linux_marlboro

stencil flushing with planes

Change 107525 on 2003/06/23 by jcarroll@jcarroll_crayola_linux_orl

Added test pin connections to RAMs.

Change 107504 on 2003/06/23 by cbrennan@cbrennan_r400_linux_marlboro

Add a stall after the probe filters to make sure they are never 4 or more
end of samples out of sync from eachother.  This fixes the deadlock conditions
found in 3d_mip's and possibly others.
```

```
Change 107502 on 2003/06/23 by vbhatia@vbhatia_r400_linux_marlboro

Enable rf_expand_enable bypass path in emu and testbench

Change 107493 on 2003/06/23 by rmanapat@rmanapat_r400_sun_marlboro

Fix for bug related to when the agp512 bit is set comming in from the
TP to the TC and the generation of the appropriate sector masks

Change 107488 on 2003/06/23 by wlawless@wlawless_r400_linux_marlboro

sig missing from sensitivity list

Change 107487 on 2003/06/23 by jbrady@jbrady_crayola_linux_orl

Change request_size to a 2 bit field from 1 bit.

Change 107477 on 2003/06/23 by vbhatia@vbhatia_r400_linux_marlboro

Added more auto generated directed and randomized tp formatter tests

Change 107471 on 2003/06/23 by nkociuk@nkociuk_r400_linux_marl

pointless checkin...

Change 107447 on 2003/06/23 by kmeekins@kmeekins_crayola_linux_orl

Qualified the II request valids with the fetch sector to ensure only those
  addresses in need of fetching are valid.

Change 107442 on 2003/06/23 by bhankins@bhankins_crayola_linux_orl

fix memory test wiring error

Change 107439 on 2003/06/23 by paulv@paulv_r400_linux_marlboro

Connected MC_RB_read_source (need for external queue data read returns and, in the
future, TC hw-resolve data) and RB_MH_queuecount (which tells the MH that the RB has
received external queue data).  NOTE:  at this time, RB_MH_queuecount means the RB has
received any external queue data, even though clients who made read requests to the
external queue already allocate space for the data (therefore, they have no queues).
There may be a MH fix forthcoming to negate the use of this signal except for TC hw
resolve data to RBC.

Change 107438 on 2003/06/23 by bhankins@bhankins_crayola_linux_orl

improve on counting param cache exports
```

```
Change 107430 on 2003/06/23 by wlawless@wlawless_r400_linux_marlboro

The toggle into ATI-FIFO_CAM was changed for pipelining the data
in... Anyway the toggle inside for testing pixels 01 or 23 need
to be changed also.... oooppps

Change 107424 on 2003/06/23 by jayw@jayw_r400_linux_marlboro

pre move

Change 107418 on 2003/06/23 by rmanapat@rmanapat_r400_sun_marlboro

Removed a comment that was obsolete in the unpack file
and added a fix to the tcb_2dxycoord file which allows for
proper operation for lin_fmt52 and lin_fmt53 for tc_simple_2d tests

Change 107389 on 2003/06/22 by mmang@mmang_crayola_linux_orl

1.  made change sp_vector.v to grab pred/kill results
    a clock sooner since Vic a register delay to
    sp_scalar_lut.bvrl.  May have to change back later.
2.  Took away register delay in sq_ais_output to account
    for extra register needed for muxing and registering
    both simd engines for SQ_SX_sp signals.
3.  In sq_alu_instr_seq.v, backed out Laurent's previous
    fix for constant waterfalling and made different change
    where ism registers are loaded based on ais_start
    instead of ais_rtr.  With waterfalling, the ais_rtr
    does not happen early enough for ism registers to be
    available for AIS state machine.
4.  In sq_export_alloc.v, added connections for second simd
    engine to handle sx export allocation and deallocation.
5.  In sq.v, added muxing between simd0 and simd1
    sq_ais_output for SQ_SX signals.
6.  In sq_exp_alloc_ctrl.v, added simd1 connections for
    sx export control logic.
7.  In sq_pix_thread_buff.v and sq_vtx_thread_buff.v, added
        A)  Simd1 logic for ALU memory write (register delayed
            simd1 information to avoid overlap with simd0)
        B)  Appropriate read mux for simd0/simd1 for control
            flow memory (based on status simd num).
        C)  Added simd1 status register write data connections.
8.  In sq_status_reg.v, added connections and muxing for second
    simd engine status bits write.
9.  Added a variety of connections for simd1 to tb_sqsp.v.
10. Added delay pipe for thread_id and thread_type for simd1
    in order to correctly track sp to sx interface. (tbtrk_spsx.v)
```

```
11. Fixed bug in sx related to using correct export id during
    free done process of pixel to rb buffers
    (sx_export_control_common.v)

Change 107352 on 2003/06/21 by johnchen@johnchen_r400_linux_marlboro

correct cache read for stencil with zplanes

Change 107290 on 2003/06/20 by vbhatia@vbhatia_r400_linux_marlboro

Tp and Vc formatter standalone testbenches around the unified sp_tp_formatter
along with scripts to regress against emulator

Change 107268 on 2003/06/20 by johnchen@johnchen_r400_linux_marlboro

update smask to tile cache and depth cache

Change 107266 on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro

reverted a change that was made for VC testing (and that did not work correctly)

Change 107257 on 2003/06/20 by tien@tien_r400_devel_marlboro

Complewted first pass and vc part of formatter
Made regression script more thorough

Change 107255 on 2003/06/20 by moev@moev2_r400_linux_marlboro

Makefile that uses ncverilog (it also uses modeltech),

Change 107249 on 2003/06/20 by moev@moev2_r400_linux_marlboro

deleted un-needed ports

Change 107246 on 2003/06/20 by smburu@smburu_r400_linux_marlboro

Redo of TP virage work to get latest compilers.

Change 107209 on 2003/06/20 by mzini@mzini_crayola_linux_orl

Created VC regression script

Change 107193 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

fix scforce warning

Change 107182 on 2003/06/20 by viviana@viviana_crayola2_syn
```

```
Memories for the sx built 6/20/03.

Change 107181 on 2003/06/20 by viviana@viviana_crayola2_syn

The memories that were not bit maskable had the rtl bit maskable.
   All memories were built from scratch to correct this.

Change 107178 on 2003/06/20 by jbrady@jbrady_crayola_linux_orl

Fix tests for full/partial tests - the boundary conditions were not right.
 Change clamp_count for partial max - must consider 8 dwords, not just valid dwords.

Change 107176 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

remove obsolete files

Change 107175 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

delete memory models from this directory (they don't belong here)

Change 107174 on 2003/06/20 by vromaker@vromaker_r400_linux_marlboro

- swapped PS and ID gpr write phases

Change 107173 on 2003/06/20 by wlawless@wlawless_r400_linux_marlboro

Some timing fixes, and added rb_id frops

Change 107170 on 2003/06/20 by johnchen@johnchen_r400_linux_marlboro

fix the case of boths and z are on and not expanded

Change 107167 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

updates

Change 107160 on 2003/06/20 by smburu@smburu_r400_linux_marlboro

Update for border color.

Change 107157 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

skip the checking of quads that have no mask bits set

Change 107156 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

fix generation of index_op bit
```

```
Change 107155 on 2003/06/20 by smburu@smburu_r400_linux_marlboro

Redo of TCF virage hook-up.

Change 107151 on 2003/06/20 by bhankins@bhankins_crayola_linux_orl

remove dos carriage returns

Change 107148 on 2003/06/20 by mdesai@mdesai_r400_linux

Modifed to include directed test capability

Change 107140 on 2003/06/20 by smburu@smburu_r400_linux_marlboro

Bit number 7 instead of 8 needs to connect to CSCIN.

Change 107094 on 2003/06/19 by jbrady@jbrady_crayola_linux_orl

Set clamped count to 7 for fully clamped verts. It was necessary for min clamping.
 Set vert_offset to dw_addr[3:0] always -- it doesn't matter in fully clamped cases
now.

Change 107089 on 2003/06/19 by johnchen@johnchen_r400_linux_marlboro

correct quaddata_snd functionality

Change 107077 on 2003/06/19 by smburu@smburu_r400_linux_marlboro

Fix to Virage hook-up.

Change 107072 on 2003/06/19 by jbrady@jbrady_crayola_linux_orl

Rename clamped_count to unclamped_count. It's a better name.
 Change unclamped_count to be count_lo - clamp_count - 1. It now reflects
  the number of clamped words in the vert, not per 8 dwords.
 For partial min, set vert_offset to dw_addr, not base_addr. This is necessary
  for the vcrp to know how many dw's to clamp at the beginning of the vert. Otherwise
  it's ambiguous which dw's are clamped, and which are unclamped.

Change 107070 on 2003/06/19 by jcarroll@jcarroll_crayola_linux_orl

Added logic to VCRP to handle clamp_x = 1

Change 107069 on 2003/06/19 by askende@askende_r400_linux_marlboro

checking in changes related to area/timing optimization

Change 107068 on 2003/06/19 by cbrennan@cbrennan_r400_linux_marlboro
```

```
Now only shows TPC new state error when state actually is changing when dropped.

Change 107066 on 2003/06/19 by askende@askende_r400_linux_marlboro

area/timing optimization

Change 107059 on 2003/06/19 by johnchen@johnchen_r400_linux_marlboro

more hier stencil

Change 107053 on 2003/06/19 by bhankins@bhankins_crayola_linux_orl

wiring error on memory test logic

Change 107026 on 2003/06/19 by llefebvr@llefebvr_r400_linux_marlboro

1) Added a guard bit to the parameter sub engine of the SX in both the emulator and HW
this was causing a failure on a WQL test.
2) Fixed zero detection problem in parameter_sub engine of the HW were an explicit 1
was added all the time even when the number was 0.0. This was causing
r400sx_wrapper_01.cpp to fail (this is a test that I wrote to duplicate the WQL test
that was failing in order to run it on HW).

Change 107017 on 2003/06/19 by bhankins@bhankins_crayola_linux_orl

delete obsolete memory file

Change 107015 on 2003/06/19 by viviana@viviana_crayola2_syn

Re-ran cover on the high speed memories to add fuse_box318 files previously deleted.
   Also deleted fuse_box29 files no longer used.

Change 107014 on 2003/06/19 by hmonsef@hmonsef

Replaced by 12x111

Change 107010 on 2003/06/19 by rmanapat@rmanapat_r400_sun_marlboro

Fix which pulls the filter function and context id from the
correct spots in the tag for a fetch multisample

Change 107009 on 2003/06/19 by smoss@smoss_crayola_linux_orl_regress

   update

Change 107000 on 2003/06/19 by jbrady@jbrady_crayola_linux_orl
```

```
Move tag merge to after conflict detection. only merge if there are no conflicts.
 fixes merge_conflict test and is necessary for clamping.

Change 106990 on 2003/06/19 by tien@tien_r400_devel_marlboro

Forgot leading one, expanded channels out one more bits

Change 106966 on 2003/06/19 by cbrennan@cbrennan_r400_linux_marlboro

Tied in TPC_TC_mip_packed.  Also marked up some TODO spots.

Change 106960 on 2003/06/19 by rmanapat@rmanapat_r400_sun_marlboro

Fix for bug found with tc_simple_cubic random_level1 0x4030f957
Needed to clamp onefaceoffset to 4k boundary and add 4k if there were
any bits set below the 4k boundary and also clamp the height to the
next value of 32 if it was inbetween multiples of 32

Change 106949 on 2003/06/19 by smoss@smoss_crayola_linux_orl_regress

   removed sq_tp_stall signal in anticipation of new sq_tp interface

Change 106938 on 2003/06/19 by viviana@viviana_crayola2_syn

Removed unused Virage files from the src directory.

Change 106897 on 2003/06/18 by tien@tien_r400_devel_marlboro

Added mip_packed output on tpc
More fixed to formatter

Change 106891 on 2003/06/18 by bbuchner@bbuchner_crayola_linux_orl

add additional debug busses

Change 106842 on 2003/06/18 by jcarroll@jcarroll_crayola_linux_orl

Added all of the clamping logic.

Change 106827 on 2003/06/18 by cbrennan@cbrennan_r400_linux_marlboro

Timing tweek on tag load path..  hopefully wont create a new one.

Change 106825 on 2003/06/18 by llefebvr@llefebvr_r400_linux_marlboro

Changing the cylindrical wrap test from > to >= in order to match MS ref rast and R300
algorithm.
```

```
Change 106822 on 2003/06/18 by moev@moev2_r400_linux_marlboro

fixed patchbox to reflect proper connectivity of the star system

Change 106821 on 2003/06/18 by moev@moev2_r400_linux_marlboro

part of new compiler

Change 106819 on 2003/06/18 by moev@moev2_r400_linux_marlboro

updated compilers

Change 106817 on 2003/06/18 by moev@moev2_r400_linux_marlboro

fix port definition of STAR_cmdscout from input to output

Change 106810 on 2003/06/18 by askende@askende_r400_linux_marlboro

checking in a fix to force q2_param_array0_tmp signal to load on  WRAP 1 when
       cylindrical wrap is enabled

Change 106804 on 2003/06/18 by moev@moev2_r400_linux_marlboro

fixed syntax errors in some of the entries

Change 106795 on 2003/06/18 by jbrady@jbrady_crayola_linux_orl

Wire rbiu decoded fifo depth to vcmi_receiver fifos instead of hardcoding to 16.

Change 106786 on 2003/06/18 by nkociuk@nkociuk_r400_linux_marl

remove NO_CONNECT and change signal names to match each other

Change 106784 on 2003/06/18 by paulv@paulv_r400_linux_marlboro

Reverted most of the timing fixes from yesterday since Mark S. told me that the problem
most likely was a tool problem with optimize_registers.

Change 106783 on 2003/06/18 by bbuchner@bbuchner_crayola_linux_orl

added control and fifo size regs

Change 106770 on 2003/06/18 by rmanapat@rmanapat_r400_sun_marlboro

Fixed height so that for 3d fetches it clamps to the next multiple of
32...this version should also fix the latch issue that was going on
with the previous version of code
```

```
Change 106767 on 2003/06/18 by nkociuk@nkociuk_r400_linux_marl

use proper reset...

Change 106751 on 2003/06/18 by danh@danh_r400_win

Updated r400sq_* status.

Change 106744 on 2003/06/18 by wlawless@wlawless_r400_linux_marlboro

removed some levels of delay in the ping pong for rtr_local...

Change 106727 on 2003/06/18 by mzini@mzini_crayola_linux_orl

Only capture data when both rdy and rtr are high

Change 106721 on 2003/06/18 by llefebvr@llefebvr_r400_emu_montreal

Changed the names of he channels in the tracker so that they are placed correctly
(order was ARGB correct order is ABGR)

Change 106713 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

undo prev change

Change 106710 on 2003/06/18 by moev@moev2_r400_linux_marlboro

Updated files that reflect the SP/SPI split.

Change 106697 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

correct fifo width

Change 106695 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

modify tbmod_fake_rb.v to generate op bit only if mask is nonzero

Change 106688 on 2003/06/18 by wlawless@wlawless_r400_linux_marlboro

Flopped the output of the Color Cache RAM's to ati_fifo_cam...
This is through the endian logic

Change 106681 on 2003/06/18 by bhankins@bhankins_crayola_linux_orl

fix bug in quad mask generation

Change 106627 on 2003/06/17 by paulv@paulv_r400_linux_marlboro
```

```
Timing fixes.

Change 106621 on 2003/06/17 by mzini@mzini_crayola_linux_orl

 Only compare valid verts when data gets moved from L2->l1

Change 106618 on 2003/06/17 by jbrady@jbrady_crayola_linux_orl

>    //  Even banks only conflict if even tags aren't equal. Therefore, we
 >    //   can compare vcrg4_gen_even_tag0_bank_mask instead of vcrg4_even_tag1_valid
 >    //   because there will not have been a merge. Same goes for valids.
 >    //   This helps timing. Same goes for odd bank conflict.

Change 106611 on 2003/06/17 by danh@danh_crayola1_linux_orl

 Changed the cfs_return_addrs_q[51:0] generation so the correct cfs_return_addr[3:0]_q
order
 will be written into the thread buffer CFS mem when a thread is returned to the thread
buffer.

Change 106609 on 2003/06/17 by johnchen@johnchen_r400_linux_marlboro

new way to do n_free_cachelines

Change 106598 on 2003/06/17 by rmanapat@rmanapat_r400_sun_marlboro

Height now clamps to the next multiple of 32 for Volume Map (fetch3d) tests
Bug was found using a random seed

Change 106597 on 2003/06/17 by rramsey@RRAMSEY_P4_r400_win

more status

Change 106591 on 2003/06/17 by mzini@mzini_crayola_linux_orl

Randomize TC_VC_simd_id

Change 106582 on 2003/06/17 by johnchen@johnchen_r400_linux_marlboro

fixed functionally: adds and round

Change 106581 on 2003/06/17 by jbrady@jbrady_crayola_linux_orl

Keep L1_rdy, L2a_rdy, and CC_rdy high even if rtr=0.
 Remove programmability from instruction fifo depth.

Change 106572 on 2003/06/17 by tien@tien_r400_devel_marlboro
```

```
More sp_tp_formatter changes and a port fix on tpc notied by Steve Mburu

Change 106570 on 2003/06/17 by mzini@mzini_crayola_linux_orl

Made memory return data out of order by default

Change 106566 on 2003/06/17 by bhankins@bhankins_crayola_linux_orl

bug fix when free done happens outside of an export

Change 106565 on 2003/06/17 by mzini@mzini_crayola_linux_orl

 Added option to return data from memory out of order

Change 106562 on 2003/06/17 by jbrady@jbrady_crayola_linux_orl

only write to input_fifo when rtr is high. cc leaves rdy high even when
  rtr is low.

Change 106553 on 2003/06/17 by mzini@mzini_crayola_linux_orl

 Make sure the RTR's are high before sampling data

Change 106539 on 2003/06/17 by mzini@mzini_crayola_linux_orl

Added VC->SQ interface tracking

Change 106528 on 2003/06/17 by rramsey@rramsey_crayola_linux_orl

hook up iterator_SP_cntx0 so realtime works correctly

Change 106512 on 2003/06/17 by jcarroll@jcarroll_crayola_linux_orl

Changed end_of_group logic to only strobe on last transfer.

Change 106502 on 2003/06/17 by nkociuk@nkociuk_r400_linux_marl

update tcd busy generation to include logic stages after ipbuf fifos

Change 106483 on 2003/06/17 by mzini@mzini_crayola_linux_orl

Added more time at the end of the sim once the input files have been read

Change 106434 on 2003/06/16 by johnchen@johnchen_r400_linux_marlboro

lastest fixes.  functional incorrect

Change 106427 on 2003/06/16 by johnchen@johnchen_r400_linux_marlboro
```

```
timing fix for flush cacheline address

Change 106422 on 2003/06/16 by cbrennan@cbrennan_r400_linux_marlboro

Fix LEDA issue on missing default from a case.

Change 106420 on 2003/06/16 by cbrennan@cbrennan_r400_linux_marlboro

Changed tag load signal path.  Should fix timing for it.

Change 106414 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Fixed the data return path from the MI for RP testbench

Change 106408 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Fixed vc_rg_rp2.tr file so that null_request field shows properly

Change 106390 on 2003/06/16 by jbrady@jbrady_crayola_linux_orl

Fix width of constant - it changed when we removed border color.

Change 106387 on 2003/06/16 by jcarroll@jcarroll_crayola_linux_orl

L2a interface change for clamping.

Change 106386 on 2003/06/16 by jbrady@jbrady_crayola_linux_orl

Remove border_color from vc.
 Move L2 null request into the L2 data field for non-clamped entries.

Change 106384 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Removed null_request and border_color from RG->RP1 interface

Change 106375 on 2003/06/16 by danh@danh_r400_win

Updated the r400sq* status.

Change 106373 on 2003/06/16 by jcarroll@jcarroll_crayola_linux_orl

Removed internal register for gpr_phase so that output data
       will sync to external gpr_phase.

Change 106372 on 2003/06/16 by cbrennan@cbrennan_r400_linux_marlboro

Timing fix to probe filter that mirrors how the setfilter timing fix was done.
```

```
Change 106368 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Made tbmod_sqvc drive gpr_phase instead of tb_vc for the rp testbench

Change 106364 on 2003/06/16 by rmanapat@rmanapat_r400_sun_marlboro

Fix for til_fmt52_l and til_fmt53_l for tc_simple_2d

Change 106357 on 2003/06/16 by rramsey@rramsey_crayola_linux_orl

fix latency of tp/sp signals in tb_sqsp after tp_formatter change
clean up the fetch swizzle warning msg in tb_sqsp
add new memory to sq/tb.f
fix fech_swizzle signal width in tex_instr_seq

Change 106346 on 2003/06/16 by nkociuk@nkociuk_r400_linux_marl

fix wire name mismatch

Change 106344 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Drive simd_id ready's in VC environment

Change 106341 on 2003/06/16 by bhankins@bhankins_crayola_linux_orl

fix the generation of nan_kill_flag bits from being reset buy subsequent non-NaN
numbers.

Change 106320 on 2003/06/16 by jcarroll@jcarroll_crayola_linux_orl

Fixed a bug.  One piece of L2 read data was being lost when both
       L1 buffers were full and the entire L2 pipe was frozen.  Fixed by
       adding a coast reg that stores the L2 read address when the entire
       L2 pipeline is held.

Change 106311 on 2003/06/16 by mzini@mzini_crayola_linux_orl

Set gpr_phase even when there's no valid data to the VC

Change 106308 on 2003/06/16 by wlawless@wlawless_r400_linux_marlboro

Added rb_regs.v to rb_c_cache.v for Mark S... include.v didn't work ???

Change 106298 on 2003/06/16 by paulv@paulv_r400_linux_marlboro

Just a minor code optimization.
```

Change 106293 on 2003/06/16 by vromaker@vromaker_r400_linux_marlboro

code fix to prevent latches

Change 106287 on 2003/06/16 by paulv@paulv_r400_linux_marlboro

Removed the GL_ redefines in rb_include.v (since the emulator has been released with the new names).

Change 106283 on 2003/06/16 by wlawless@wlawless_r400_linux_marlboro

Nothing... removed [0] from a single wire... oops

Change 106277 on 2003/06/16 by viviana@viviana_crayola2_syn

Extra bit added to pixel state data.

Change 106274 on 2003/06/16 by rramsey@FL_RAMSEY_r400_win

add new rf block to vsim makefile

Change 106273 on 2003/06/16 by danh@danh_crayola1_linux_orl

Changed TB_TP_REQ_FIFO_DEPTH (128 to 256) & TB_TP_REQ_FIFO_ADDR_WIDTH (7 to 8) to resolve fifo overflow.

Change 106242 on 2003/06/15 by tien@tien_r400_devel_marlboro

Added cmask gen code

Change 106193 on 2003/06/14 by bhankins@bhankins_crayola_linux_orl

enable alpha logic

Change 106191 on 2003/06/14 by viviana@viviana_crayola2_syn

48x154 memory changed to 48x155.

Change 106190 on 2003/06/14 by viviana@viviana_crayola2_syn

Changed the width of the state memory to 155 bits.

Change 106181 on 2003/06/14 by mzini@mzini_crayola_linux_orl

Removed print statements

Change 106179 on 2003/06/14 by mzini@mzini_crayola_linux_orl

Make sure number of transfers on each tracked interface exactly matches betwee the HW and emu

Change 106176 on 2003/06/14 by mzini@mzini_crayola_linux_orl

Renamed element to set

Change 106126 on 2003/06/13 by paulv@paulv_r400_linux_marlboro

Fix for the generation of external queue (MH) addresses.

Change 106117 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

sp_stdrfsdks2p128x128cm2sw1.v for SP.

Change 106112 on 2003/06/13 by jbrady@jbrady_crayola_linux_orl

add 128x128 memory.

Change 106110 on 2003/06/13 by moev@moev2_r400_linux_marlboro

MAV's version of cnt file

Change 106109 on 2003/06/13 by moev@moev2_r400_linux_marlboro

fixes to eliminate temp area left in by accident.

Change 106108 on 2003/06/13 by smburu@smburu_r400_sun_marlboro

packed_z_q missing from sens. list.

Change 106095 on 2003/06/13 by johnchen@johnchen_r400_linux_marlboro

more hier stencil stuff

Change 106092 on 2003/06/13 by tien@tien_r400_devel_marlboro

Many updates.

Change 106085 on 2003/06/13 by smburu@smburu_r400_sun_marlboro

Typo, FW0_new_state instead of FR0_new_state.

Change 106078 on 2003/06/13 by rramsey@RRAMSEY_P4_r400_win

more status updates

Change 106069 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

```
vc_cc.v
  -------
  Added a registered version of the input fifo read enable to detect a non-valid
  fifo entry for the CC->RP interface.

  vc_cc_pack_align.v
  ------------------
  - Fixed the CC_RP_L2b_rdy to permit a non-valid entry into the L2b FIFO.
  - Swizzled the bank mask bits to agree with the RG on the bank representation.

Change 106056 on 2003/06/13 by cbrennan@cbrennan_r400_linux_marlboro

Piping valids inside coord sort so that its busy doesnt go unknown with unknown data.

Change 106055 on 2003/06/13 by cbrennan@cbrennan_r400_linux_marlboro

Really removed the TCA_TCB ping pong buffer this time,

Change 106050 on 2003/06/13 by mzini@mzini_crayola_linux_orl

 Added gpr_phase in vc_rp_sp.dmp

Change 106044 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

bug fix to allow free done to be generated after the 4 phases of data

Change 106040 on 2003/06/13 by kevino@kevino_r400_linux_marlboro

 Hack to extend tcd timout from end of busy to when clock gets shut off.  Need to do
this right later.

Change 106031 on 2003/06/13 by mzini@mzini_crayola_linux_orl

Fixed vc output tracker

Change 106030 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_rf_fusebox.ctmc for SPI.

Change 106029 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_rf_fusebox.v for SPI.

Change 106028 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

 spi_stdrfsdks2p8x96cm1sw0.v for SPI.
```

Change 106027 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_stdrfsdks2p16x200cmlsw0.v file for SPI

Change 106026 on 2003/06/13 by asutkows@asutkows_r400_sun_marlboro

spi_rf.cnt file for SPI.

Change 106023 on 2003/06/13 by bbuchner@bbuchner_crayola_linux_orl

removed skew from DC signals; added thread type, cycle

Change 106018 on 2003/06/13 by paulv@paulv_r400_linux_marlboro

Fixes for AGP requests.

Change 106016 on 2003/06/13 by wlawless@wlawless_r400_linux_marlboro

timing

Change 106015 on 2003/06/13 by paulv@paulv_r400_linux_marlboro

Renamed all false rts signals to snd signals (e.g., DB_RB_quaddata_rts ->
DB_RB_quaddata_snd) in order to maintain consistency and avoid confusion. Also fixed a
problem writing the db quaddata fifo in the quad cache.

Change 106012 on 2003/06/13 by jbrady@jbrady_crayola_linux_orl

Instantiate ati_dff_out's for all outputs instead of inferring regular flops.

Change 106009 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

Corrected multicycle determination logic.

Change 106008 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

Corrected syntax for user supplied compile options file.

Change 106007 on 2003/06/13 by kmeekins@kmeekins_crayola_linux_orl

Changed element_id to way_id to match spec and CC->MI port names.

Change 105995 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

disable alpha test for now

Change 105988 on 2003/06/13 by smburu@smburu_r400_sun_marlboro

```
Corrected width of tcf_sclk_perf_disable flops.

Change 105986 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

delete obsolete files

Change 105985 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

delete obsolete files

Change 105982 on 2003/06/13 by bhankins@bhankins_crayola_linux_orl

advance sq-sx control signals by one clock to solve sx timing issues
   add support for updated sx hierarchy

Change 105978 on 2003/06/13 by cbrennan@cbrennan_r400_linux_marlboro

Leda errors.

Change 105969 on 2003/06/13 by cbrennan@cbrennan_r400_linux_marlboro

Rework of lru update path.  Should be major improvement in timing. Added
tcb_sort_drop.v.

Change 105962 on 2003/06/12 by johnchen@johnchen_r400_linux_marlboro

revert the muxing back to the slope_to_pix mc file

Change 105943 on 2003/06/12 by dougd@dougd_r400_linux_marlboro

Added a 2nd write buffer to aluconst, texconst and instruction store to handle
real time writes from cp mixed with non real time writes. This code passes the
mini-regress on tb_sqsp and cp_lcc_tex, cp_lcc_alu, cp_im_load_basic on the gc
testbench but fails cp_lcc_tex_rt and cp_lcc_alu_rt. It appears work for non-realtime.

Added real time prim bit from pix_ctl to ISM in pix_thread_buff when loading a
pixel thread. This bit will allow reading real time constants from the constant stores.

Added VC_wake_up logic.

Change 105940 on 2003/06/12 by jcarroll@jcarroll_crayola_linux_orl

Added RP_DC_thread_type to I/O
       First revision of VCRP with all functionality (except clamping).

Change 105927 on 2003/06/12 by mzini@mzini_crayola_linux_orl

 Added thread type
```

```
Change 105925 on 2003/06/12 by johnchen@johnchen_r400_linux_marlboro

some hi-stencil work

Change 105924 on 2003/06/12 by vromaker@vromaker_r400_linux_marlboro

timing fixes

Change 105916 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Fix replication syntax error.

Change 105914 on 2003/06/12 by danh@danh_r400_win

Updated r400cl* status.

Change 105908 on 2003/06/12 by bbuchner@bbuchner_crayola_linux_orl

use behavioral memories

Change 105903 on 2003/06/12 by bbuchner@bbuchner_crayola_linux_orl

remove dup. tracker

Change 105900 on 2003/06/12 by kmeekins@kmeekins_crayola_linux_orl

Added tbmods for CC standalone testbench.
  Assigned values to MH_TC_start0, 1, and 2 to get stall and flush signals known.

Change 105891 on 2003/06/12 by rramsey@RRAMSEY_P4_r400_win

more status updates

Change 105890 on 2003/06/12 by paulv@paulv_r400_linux_marlboro

Timing fixes and some functional fixes in the quad_cache (specifically, both the HiZ
data and DB quaddata fifos are memory macro fifos and one must be careful about when
data is actually available at the top).

Change 105889 on 2003/06/12 by danh@danh_crayola1_linux_orl

Changed the "pix: check for buf avail and export count < 16" section of the alu_req
generation,
       added parentheses around the alloc_size_q & sx_buf_avail logic.

Change 105888 on 2003/06/12 by mzini@mzini_crayola_linux_orl
```

```
 Fixed typo

Change 105869 on 2003/06/12 by mzini@mzini_crayola_linux_orl

 Fixed vc_out tracker

Change 105853 on 2003/06/12 by moev@moev2_r400_linux_marlboro

Files for testing the Virage system

Change 105852 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Added gpr phase to Rp testbench

Change 105851 on 2003/06/12 by bhankins@bhankins_crayola_linux_orl

add new files for updated sx hierarchy

Change 105847 on 2003/06/12 by smburu@smburu_r400_sun_marlboro

Put a flop in the path of tcf_sclk_perf_disable.

Change 105844 on 2003/06/12 by kevino@kevino_r400_linux_marlboro

  Hopefully some changes to improve timing

Change 105843 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Only compare valid dwords

Change 105831 on 2003/06/12 by wlawless@wlawless_r400_linux_marlboro

moved expand state from going into the state decode... timing

Change 105829 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Add vcmi debug monitor ports.
 Propagate x's through some muxes.

Change 105823 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Do not trigger a compare if it's a null request

Change 105816 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Last and clamp were swaped

Change 105811 on 2003/06/12 by rramsey@rramsey_crayola_linux_orl
```

```
update spsx tracker so msg signal names match the rtl signal names
fix a typo in a pix_rs_input msg

Change 105809 on 2003/06/12 by rramsey@rramsey_crayola_linux_orl

some of the compares had not been updated with the new
vc field in the dump file

Change 105788 on 2003/06/12 by moev@moev2_r400_linux_marlboro

Made changes to support the Virage memory systems. These include the rewiring of the
patchbox, changes to the width of the SCFORCE bus, addition of the AWT gate the change
of port STAR_cmdscout from input to output.

Change 105784 on 2003/06/12 by rramsey@rramsey_crayola_linux_orl

fix width of num_params_q

Change 105780 on 2003/06/12 by wlawless@wlawless_r400_linux_marlboro

used doing_frag_zero for the mux control in probe_mask

Change 105770 on 2003/06/12 by rramsey@RRAMSEY_P4_r400_win

picking more tests, adding comments to tests with known issues

Change 105767 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Add vcrg debug monitor.

Change 105766 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Add debug monitor signals.
 Propagate x's in vcrg0_data_format_min_count case statement.

Change 105765 on 2003/06/12 by jbrady@jbrady_crayola_linux_orl

Remove possible index out of range error for 12 & 8 dword verts on next_done.
 Remove leda error on size mismatch for done reset value.

Change 105756 on 2003/06/12 by mzini@mzini_crayola_linux_orl

Reordered vc_L2_L1.tr

Change 105750 on 2003/06/12 by smoss@smoss_crayola_linux_orl_regress

   removed sq_sp_simd1_instruct_start to coincide with @105565
```

```
Change 105740 on 2003/06/12 by kmeekins@kmeekins_crayola_linux_orl

Added the macro for VC_PATH definition.

Change 105739 on 2003/06/12 by cbrennan@cbrennan_r400_linux_marlboro

Removed TCB core ping pong buffer because miss_stall is now out of a flop.  Area
savings, and should help sectormask timing.

Change 105693 on 2003/06/11 by askende@askende_r400_linux_marlboro

releasing a change in the interpolators to compensate for the bug introduced by SX
(hardware and emulator)
       when dealing with NaNs and Infs

Change 105692 on 2003/06/11 by askende@askende_r400_linux_marlboro

releasing a change in the interpolators to compensate for the bug introduced by SX
(hardware and emulator)
       when dealing with NaNs and Infs

Change 105688 on 2003/06/11 by danh@danh_crayola1_linux_orl

Added sq_ef_pb_avail_la, changed nxt_sent_sq_cntl_cnt and itercmdfifo_re generation to
       resolve a sq.u_sq_ptr_buff.sq_event_fifo overflow error.

Change 105687 on 2003/06/11 by jcarroll@jcarroll_crayola_linux_orl

Updates to the VCRP ports
       Added yet more functionality!!!!!

Change 105680 on 2003/06/11 by tien@tien_r400_devel_marlboro

Recoded sp_tp_formatter in Module Compiler

Change 105679 on 2003/06/11 by jcarroll@jcarroll_crayola_linux_orl

Fixed model

Change 105675 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Once bank valids are set keep them set

Change 105671 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Setting only the valid bank readys on the CC->RP snoop bus
```

```
Change 105668 on 2003/06/11 by mzini@mzini_crayola_linux_orl

 Fixed copy-paste error

Change 105667 on 2003/06/11 by cbrennan@cbrennan_r400_linux_marlboro

Added a stage to the TPC data path bringing it up to 2 stages.
Also added a sanity check to report a failure if that weren't enough.
Unfortunately had to comment it out because the emu is driving TPC_TC_state_rts
incorrectly.

Change 105666 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Added RP->SP file

Change 105652 on 2003/06/11 by wlawless@wlawless_r400_linux_marlboro

floped inputs to frag probe state machine

Change 105642 on 2003/06/11 by hmonsef@hmonsef

Previous Rev the code was instatiated twice by Virage.

Change 105634 on 2003/06/11 by johnchen@johnchen_r400_linux_marlboro

more timing fixes

Change 105629 on 2003/06/11 by jayw@jayw_r400_linux_marlboro

removed extra name declaration.

Change 105626 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Changed some assignments to non-blocking

Change 105610 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Fixed L2->L1 dump

Change 105607 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Added USE_BEHAVE_MEM define to the RP testbench

Change 105601 on 2003/06/11 by rmanapat@rmanapat_r400_sun_marlboro

Fix for tc_simple_mip_3d testcases lin_fmt2 8 and 9 _l

Change 105592 on 2003/06/11 by llefebvr@llefebvr_r400_linux_marlboro
```

Added storage element in the SQ to store the valid addresses of the mova so that they can de restored at any instruction that uses the address register. The way it was currently would only work if the use of the address was directly following the MOVA instruction. This fixes r400sq_const_index_02.cpp.

Change 105587 on 2003/06/11 by wlawless@wlawless_r400_linux_marlboro

timing

Change 105580 on 2003/06/11 by johnchen@johnchen_r400_linux_marlboro

new way of round

Change 105573 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Correctly read mi_rp file

Change 105566 on 2003/06/11 by mzini@mzini_crayola_linux_orl

CC->RP signals changed names

Change 105565 on 2003/06/11 by askende@askende_r400_linux_marlboro

top level clean-up

Change 105556 on 2003/06/11 by kmeekins@kmeekins_crayola_linux_orl

Changed the cache_flush logic to use cache_stall_q.

Change 105547 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Fixed build script

Change 105545 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Fixed build script

Change 105542 on 2003/06/11 by mzini@mzini_crayola_linux_orl

Added RP tesbench modules

Change 105538 on 2003/06/11 by johnchen@johnchen_r400_linux_marlboro

rounding, trunking
 logic

Change 105537 on 2003/06/11 by vromaker@vromaker_r400_linux_marlboro

```
- added sq_fetch_arb to and removed sq_thread_buff_cntl from system_sq.vcpp
- made a timing fix to gpr alloc

Change 105528 on 2003/06/11 by smburu@smburu_r400_linux_marlboro

Corrected harmless bit truncation.

Change 105527 on 2003/06/11 by smburu@smburu_r400_linux_marlboro

Corrected harmless bit truncation.

Change 105525 on 2003/06/11 by rramsey@RRAMSEY_P4_r400_win

picking more tests

Change 105520 on 2003/06/11 by jbrady@jbrady_crayola_linux_orl

Use partial products to save area in addr_calc.

Change 105519 on 2003/06/11 by paulv@paulv_r400_linux_marlboro

Forgot to add the new signal MC_RB_rank_ba3_location to port list (its declared,
though).  Fixed.

Change 105483 on 2003/06/10 by johnchen@johnchen_r400_linux_marlboro

move the selects outside of mc file

Change 105477 on 2003/06/10 by cbrennan@cbrennan_r400_linux_marlboro

A good(?) attempt at fixing setfilter timing.. if it works for setfilter, i'll do it
for probefilter.
tca_sel_siref is gone again.

Change 105465 on 2003/06/10 by vromaker@vromaker_r400_linux_marlboro

- timing fix in pix_thread_buff
- VC interface is connected to vc instruction seq
- TP_SQ_fetch stall replaced by TP_SQ_dec (but not tested at GC level)
- SQ_TP_gpr_wr_addr and SQ_TP_clause removed from top level (and tb updated)
- fetch arbitration for VC and TP updated
- recoded a few lines in gpr alloc to see if it will help timing

Change 105457 on 2003/06/10 by danh@danh_r400_win

Made changes in regards to my simulation results.
```

```
Change 105437 on 2003/06/10 by rramsey@RRAMSEY_P4_r400_win

picking some tests to debug

Change 105429 on 2003/06/10 by cbrennan@cbrennan_r400_linux_marlboro

Deleted unneeded files that got instantiated in chip toplevel.

Change 105417 on 2003/06/10 by rramsey@RRAMSEY_P4_r400_win

update status for jun 9 regression

Change 105399 on 2003/06/10 by wlawless@wlawless_r400_linux_marlboro

fixed linear 32_32_32_32 test... made load_new_pipe

Change 105396 on 2003/06/10 by rmanapat@rmanapat_r400_sun_marlboro

This fix allows FB_START to be non-zero

Change 105395 on 2003/06/10 by hmonsef@hmonsef

Changed the IO_RC_scan to 1 bit from 14

Change 105389 on 2003/06/10 by kmeekins@kmeekins_crayola_linux_orl

Added tbmod_rg_cc.v.

Change 105386 on 2003/06/10 by mzini@mzini_crayola_linux_orl

Additions for the CC testbench

Change 105385 on 2003/06/10 by kevino@kevino_r400_linux_marlboro

  Fixed typo where packed_z_q qas incorrect.

Change 105384 on 2003/06/10 by kmeekins@kmeekins_crayola_linux_orl

Changed the LRU logic to use the set cache hit result. This correctected the
   problem of incrementing all but the hit way.

Change 105383 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add the following performance monitors:
 >               RG_PERF_megafetch_event,
 >               RG_PERF_end_of_group_event,
 >               RG_PERF_conflict_event,
 >               MI_PERF_requests_event
```

```
Change 105382 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add the following performance monitors:
 >               RG_PERF_megafetch_event,
 >               RG_PERF_end_of_group_event,
 >               RG_PERF_conflict_event,

Change 105375 on 2003/06/10 by asutkows@asutkows_r400_sun_marlboro

spi.cnt file for the SPI block.

Change 105371 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add performance monitor signal MI_PERF_requests_event.

Change 105370 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add performance monitor signal MI_PERF_requests_event.
 Enumerate state machine states with "parameter" to make leda happy.
 Declare next_vcmi1_request_0_mem_addr_msbs and next_vcmi1_request_1_mem_addr_msbs
  as intermediate steps in constructing next_vcmi1_request_0_mem_addr and
  next_vcmi1_request_1_mem_addr to make leda happy.

Change 105368 on 2003/06/10 by rmanapat@rmanapat_r400_sun_marlboro

Fixes tc_video til_fmt40 and 48 _l

Change 105366 on 2003/06/10 by mzini@mzini_crayola_linux_orl

Resubmitting stupid fix

Change 105362 on 2003/06/10 by mzini@mzini_crayola_linux_orl

Drive mc_send2 and mc_send3 to 0 for now

Change 105353 on 2003/06/10 by bbuchner@bbuchner_crayola_linux_orl

added additional performance monitoring to RG

Change 105352 on 2003/06/10 by wlawless@wlawless_r400_linux_marlboro

slight change in read cam valids for timing

Change 105322 on 2003/06/10 by kevino@kevino_r400_linux_marlboro

        added pipe stage to baddr gen, correspding stage to fetch_var_decode.
```

```
Change 105320 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

added performance monitor outputs RG_PERF_vertices_event, RG_PERF_clamped_event,
  RG_PERF_L2_request_event, RG_PERF_L1_request_event.
 moved dw_end_address calculation from vcrg_tag_gen to vcrg_addr_calc for timing.
 added count feature for backward compatibility. if count_lo is too small for
  data_format, we bump it up to the proper # of dwords for the data_format.

Change 105319 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

added the dw_end_addr calculation here. it's better for timing - mc can still make it.

Change 105317 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

dw_end_addr is calculated a cycle earlier for timing. it's now an input to the block,
  not calculated here.

Change 105316 on 2003/06/10 by jbrady@jbrady_crayola_linux_orl

Add 4 RG performance monitor outputs.

Change 105294 on 2003/06/10 by kevino@kevino_r400_linux_marlboro

 Added flop stage for timing fix.

Change 105292 on 2003/06/10 by rmanapat@rmanapat_r400_sun_marlboro

Fix for tc_video testcase til_fmt39_l

Change 105285 on 2003/06/10 by bbuchner@bbuchner_crayola_linux_orl

typo

Change 105283 on 2003/06/10 by llefebvr@llefebvr_r400_linux_marlboro

I have added the write enables to qualify the data sent to the SX. This is needed when
doing predicated exports or constant waterfalling on exports. This fixed
r400sq_const_index_01.cpp test.

Change 105277 on 2003/06/10 by dougd@dougd_r400_linux_marlboro

added output VC_clk_en to sq_rbbm_interface.v and wired it to
SQ_VC_wake_up in sq.v

Change 105269 on 2003/06/10 by cbrennan@cbrennan_r400_linux_marlboro

Delete testbenches.
```

```
Change 105266 on 2003/06/10 by cbrennan@cbrennan_r400_linux_marlboro

Delete out of date test benches.

Change 105265 on 2003/06/10 by cbrennan@cbrennan_r400_linux_marlboro

Change "'bx"'s to width specified 'bx's so that synopsys wont reset or fill in case
value for bits above 31. (ARGH!)

Change 105217 on 2003/06/10 by tien@tien_r400_devel_marlboro

Fixed and issue with the read strobe

Change 105079 on 2003/06/09 by grayc@grayc_crayola2_linux_orl

   adding VC to chip build

Change 105052 on 2003/06/09 by smoss@smoss_crayola_linux_orl_regress

   a few cadence related changes
   1) moved rbbm_event_type to occur after the read of rbbm_re
   2) temporarily disabled randomization on the clock for the tb_sqsp dump file

Change 105049 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Forgot to declare q_mc_rb_rank_ba3_location.

Change 105047 on 2003/06/09 by bbuchner@bbuchner_crayola_linux_orl

       fixed merge problem

Change 105045 on 2003/06/09 by bbuchner@bbuchner_crayola_linux_orl

add debug module

Change 105043 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Fixed a few typos.

Change 105041 on 2003/06/09 by jbrady@jbrady_crayola_linux_orl

Remove leda error by declaring intermediate end signal. Leda wants a carry bit.
  The carry bit is not flopped. Doesn't affect function or synthesis.

Change 105040 on 2003/06/09 by rmanapat@rmanapat_r400_sun_marlboro

fix for tc_video lin_fmt 43, 44, 48 _l
```

Change 105036 on 2003/06/09 by cbrennan@cbrennan_r400_linux_marlboro

making match whats in candidate.. i think.. just a change in the comment.

Change 105030 on 2003/06/09 by tien@tien_r400_devel_marlboro

CHanged TP_SQ_fetch_stall to TP_SQ_dec

Change 105024 on 2003/06/09 by smburu@smburu_r400_sun_marlboro

Fixes for test IOs.

Change 105016 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Removed some unused tst_ signals from the top-level db and added TM1 and TM2 signals to
both RB and DB top-level.

Change 105004 on 2003/06/09 by wlawless@wlawless_r400_linux_marlboro

mistake in the 'define size for the linear mul stuff added

Change 105003 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Fixed the TST_bist_reuse_seed signal name (reuse was being spelled as resue).

Change 104976 on 2003/06/09 by paulv@paulv_r400_linux_marlboro

Fixed some top-level I/O size mismatches, renamed the MC_RB_queuecount signals and
added MC_RB_rank_ba3_location.

Change 104967 on 2003/06/09 by bbuchner@bbuchner_crayola_linux_orl

    added performance monitoring block

Change 104958 on 2003/06/09 by jbrady@jbrady_crayola_linux_orl

Implement rotating priority for selecting which mc to send to a particular bank.

Change 104917 on 2003/06/09 by smburu@smburu_r400_sun_marlboro

Corrected hook-up of TCM_IO_scan and IO_TCM_scan.

Change 104895 on 2003/06/09 by rramsey@rramsey_crayola_linux_orl

Fix a bug with sticky bit used for dot_product nan detection

Change 104880 on 2003/06/09 by smburu@smburu_r400_sun_marlboro

```
Some synthesis fixes.

Change 104848 on 2003/06/08 by grayc@grayc_crayola2_linux_orl

   fix simd1_valid -> simd1_const_valid

Change 104832 on 2003/06/08 by smoss@smoss_crayola_linux_orl_regress

   add rom disable bits

Change 104797 on 2003/06/07 by grayc@grayc_crayola2_linux_orl

   add VC ports
   modify SP-SQ port names

Change 104775 on 2003/06/07 by johnchen@johnchen_r400_linux_marlboro

more functional corrections

Change 104771 on 2003/06/07 by johnchen@johnchen_r400_linux_marlboro

correction

Change 104757 on 2003/06/06 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 104748 on 2003/06/06 by cbrennan@cbrennan_r400_linux_marlboro

timing tweak to set filter

Change 104747 on 2003/06/06 by cbrennan@cbrennan_r400_linux_marlboro

Added make leda rule to tcf.

Change 104716 on 2003/06/06 by johnchen@johnchen_r400_linux_marlboro

precision update (38 frac instead of 42) and other timing changes

Change 104715 on 2003/06/06 by danh@danh_r400_win

Updated per simulation results.

Change 104713 on 2003/06/06 by smburu@smburu_r400_sun_marlboro

Tied iTEST_EN to the iTEST_EN pin for all ati_master_clock_gater instances as requested
by Jim Bosco.
```

```
Change 104708 on 2003/06/06 by tien@tien_r400_devel_marlboro

Reduced coords from 36 to 32 bits

Change 104695 on 2003/06/06 by cbrennan@cbrennan_r400_linux_marlboro

Miscellaneous leda and gc testbench build warnings.

Change 104673 on 2003/06/06 by nkociuk@nkociuk_r400_linux_marl

minor cleanup...

Change 104671 on 2003/06/06 by rmanapat@rmanapat_r400_sun_marlboro

Fix for testcases til_fmt18 19 and 20 for tc_simple_cubic

Change 104667 on 2003/06/06 by paulv@paulv_r400_linux_marlboro

Fixed an oversized memory (to remove Synopsys Lint warnings) and did another LEDA
cleanup.

Change 104662 on 2003/06/06 by grayc@grayc_crayola2_linux_orl

   added VC interfaces

Change 104661 on 2003/06/06 by dougd@dougd_r400_linux_marlboro

fixed typo

Change 104651 on 2003/06/06 by smburu@smburu_r400_linux_marlboro

New rams in TCF.

Change 104638 on 2003/06/06 by cbrennan@cbrennan_r400_linux_marlboro

Shrunk external top_left_coord busses to 32 bits from 36.
Replaced virage memories of TP, TPC, and fetch_fifo due to shrink of coord and addition
of tpc_packed bit.

Change 104634 on 2003/06/06 by smburu@smburu_r400_linux_marlboro

Redo of TCR ram work due to change in ram.

Change 104625 on 2003/06/06 by smburu@smburu_r400_sun_marlboro

Changes due to clock gen work.

Change 104619 on 2003/06/06 by kevino@kevino_r400_linux_marlboro
```

A bit of cleanup of signal names. Plus, move logic after flops in rfconv back before flops. Should be plently of time in this stage now, so give next stage a little extra.

Change 104618 on 2003/06/06 by wlawless@wlawless_r400_linux_marlboro

made mux_ctl the state flops for timing...

Change 104616 on 2003/06/06 by llefebvr@llefebvr_r400_linux_marlboro

HW was clamping to 0 on a GPR addressing error. It should clamp to GPR_base of the shader.

Change 104609 on 2003/06/06 by kevino@kevino_r400_linux_marlboro

  Add a stage to fvfconv. The dgmmen and bpc is now stored centrally in the ctrl block.
   still need to do some cleanup, but checking in now since it works.

Change 104600 on 2003/06/06 by dougd@dougd_r400_linux_marlboro

added missing case value that was causing synopsys to infer latches

Change 104597 on 2003/06/06 by wlawless@wlawless_r400_linux_marlboro

Removed ports on scan and bist... per Mark S.

Change 104585 on 2003/06/06 by hmonsef@hmonsef

16x228 was replaced by 16x225

Change 104580 on 2003/06/06 by wlawless@wlawless_r400_linux_marlboro

changed how the linear offset was done because of timing

Change 104578 on 2003/06/06 by hmonsef@hmonsef

Replaces 16x225

Change 104577 on 2003/06/06 by hmonsef@hmonsef

Replaces 16x228

Change 104566 on 2003/06/06 by kmeekins@kmeekins_crayola_linux_orl

Inserted AUTO_CONSTANT construct to remove constants from sensitivity lists.

Change 104555 on 2003/06/06 by danh@danh_r400_win

```
Made changes per simulation results.

Change 104554 on 2003/06/06 by dougd@dougd_r400_linux_marlboro

fixed typo -
d_rd0_addr was assigned in two process blocks
and d_rd1_addr was not being assigned at all.

Change 104543 on 2003/06/06 by kmeekins@kmeekins_crayola_linux_orl

Corrected templates to fix snooped write enable name changes.

Change 104458 on 2003/06/05 by askende@askende_r400_linux_marlboro

added indelay in the sp_hi_prec_int.mc module

Change 104450 on 2003/06/05 by nkociuk@nkociuk_r400_linux_marl

misc cleanup...

Change 104444 on 2003/06/05 by tien@tien_r400_devel_marlboro

Fixed 2 cases in float 2 fixed conversion of reg lods

Change 104439 on 2003/06/05 by viviana@viviana_crayola2_syn

vc_rf_awt_gate.v had two instantiations of the module.  This occurs whenever
   the directory where the virage files get generated is not removed before
   remaking any changes to any of the memories.

Change 104367 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

update cc bank write snoop interface.

Change 104364 on 2003/06/05 by rmanapat@rmanapat_r400_sun_marlboro

Fix that gets linear and tiled cases for tc_simple_mip_cubic to pass

Change 104363 on 2003/06/05 by subad@subad_r400_linux_marlboro

added random unique cacheline,sector generation

Change 104361 on 2003/06/05 by jcarroll@jcarroll_crayola_linux_orl

Changed names of CC snooping signals.

Change 104358 on 2003/06/05 by paulv@paulv_r400_linux_marlboro
```

```
Timing fixes.

Change 104357 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro

timing

Change 104354 on 2003/06/05 by smburu@smburu_r400_linux_marlboro

Redo to fix error in num. of cto rams.

Change 104349 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to relect they are no longer driven by registers.
  Changed bank write names to match change in snooped MI signals.

Change 104346 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to reflect that they are no longer driven by registers.
  Created delayed versions of the cache miss signals for tag 0 and 1 and
  connected them to vc_cc_loaded_busy for use with the cache line in use logic.

Change 104344 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to relect that they are no loger driven by registers.
  Added cache miss for tag 0 and tag 1 to input ports to use with the
  cache line in use logic.

Change 104341 on 2003/06/05 by kmeekins@kmeekins_crayola_linux_orl

Changed signal names to reflect no longer driven by registers.

Change 104337 on 2003/06/05 by cbrennan@cbrennan_r400_linux_marlboro

Couple gates squeezed out from probe filter.

Change 104335 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

some regs had to be wires.

Change 104333 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

add RG_RP_L2a_vert_0_offset to vcrp instantiation.

Change 104321 on 2003/06/05 by mzini@mzini_crayola_linux_orl

Some signals in RP had name changes
```

```
Change 104318 on 2003/06/05 by jcarroll@jcarroll_crayola_linux_orl

I/O changes to L2a input data.

Change 104314 on 2003/06/05 by johnchen@johnchen_r400_linux_marlboro

flop register value out of the fifo.  Timing fix

Change 104302 on 2003/06/05 by ashishs@fl_ashishs_r400_win

upadted the script since it was just fetching data till 4000 rows. Now it will fetch
data till 10000 rows (break after it finds null rows) and then sort them
accordingly....

Change 104296 on 2003/06/05 by johnchen@johnchen_r400_linux_marlboro

cache access takes one more clk to proccess cause pmask and number_of_total_access_q
can't be calculated in one cycle...timing fix

Change 104291 on 2003/06/05 by jcarroll@jcarroll_crayola_linux_orl

Change RAM sizes of L1 fifo and L2a fifo.
       Continued adding required functionality.
       Tons of internal name changes.

Change 104286 on 2003/06/05 by smburu@smburu_r400_linux_marlboro

tp_hicolor standalone testbench.

Change 104280 on 2003/06/05 by bbuchner@bbuchner_crayola_linux_orl

fixed leda errors.  Reduced SP return data width from 68 to 32 bits per index

Change 104277 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro

timing

Change 104272 on 2003/06/05 by tien@tien_r400_devel_marlboro

New file

Change 104271 on 2003/06/05 by tien@tien_r400_devel_marlboro

Aniso fixes
Aniso step order change

Change 104262 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro
```

```
timing

Change 104261 on 2003/06/05 by rramsey@rramsey_crayola_linux_orl

Fix some wiring issues in tb_sqsp
Add warning msg to tb_sqsp to tell when a test is trying to swizzle
fetch addresses since this is not supported yet in the SP
(didn't make it a failure since some tests are passing with swizzle
-- they must have the same value in all channels)
Fix predicate compare in pix_rs_input tracker
fetch_swizzle bit of instr needed to be muxed based on thread_type
in sqtp tracker

Change 104227 on 2003/06/05 by donaldl@donaldl_crayola_linux_orl

Created separate integers for each process using a for loop.

Change 104226 on 2003/06/05 by smoss@smoss_crayola_linux_orl

   quick check-in for vc release (code works in release)

Change 104223 on 2003/06/05 by bhankins@bhankins_crayola_linux_orl

fix STAR_cmdscout bus.  Partial hack until sx with new hierarchy is checked in

Change 104218 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

Add thread_type to testbench.
 Fix dst_gpr in tbmod_sqvc.

Change 104215 on 2003/06/05 by smoss@smoss_crayola_linux_orl

   pa.v back to new broken state

Change 104211 on 2003/06/05 by rramsey@RRAMSEY_P4_r400_win

status from 6_4_2003

Change 104210 on 2003/06/05 by smoss@smoss_crayola_linux_orl

   removed sp disable and simd references to get back to stability

Change 104201 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

change 16x69 memory to 16x70 to add thread_type.

Change 104200 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl
```

```
Remove SQ_VC_send from RG_busy for synthesis reasons, and because we
  are covered by SQ_VC_wake_up for that cycle.
 Make vcrg4_request_size 2 bit vector to match the rest of the pipe.

Change 104199 on 2003/06/05 by jbrady@jbrady_crayola_linux_orl

Changed some memory files: 16x69 to 16x70
                           64x17 to 64x21
                           128x45 to 128x47

Change 104197 on 2003/06/05 by wlawless@wlawless_r400_linux_marlboro

changed the clear if_notzero_q to somthing much easier

Change 104193 on 2003/06/05 by bhankins@FL_BHANKINS_P4

fix wiring error in bad pipe

Change 104178 on 2003/06/04 by johnchen@johnchen_r400_linux_marlboro

correct functionally

Change 104162 on 2003/06/04 by viviana@viviana_crayola2_syn

Changed 16x69 memory to 16x70, 64x17 to 64x21, 128x45 to 128x47 and
   added 2 more instances of 128x16.

Change 104159 on 2003/06/04 by danh@danh_crayola1_linux_orl

Changed count_match[3:0] generation, when param_gen_cycle is high all count_match[3:0]
bits will now go high.

Change 104158 on 2003/06/04 by kmeekins@kmeekins_crayola_linux_orl

Connected CF_CC_stall and CF_CC_cache_flush.

Change 104151 on 2003/06/04 by cbrennan@cbrennan_r400_linux_marlboro

Timing tweak to LRU path..  Changed if tree to case.

Change 104148 on 2003/06/04 by kmeekins@kmeekins_crayola_linux_orl

Simplified the sector fetch logic.
  Optimized the cache hit and cache miss logic.
  Corrected the fetch way generation for cache misses.

Change 104142 on 2003/06/04 by bbuchner@bbuchner_crayola_linux_orl
```

```
        connecte up cf unit

Change 104139 on 2003/06/04 by rramsey@rramsey_crayola_linux_orl

turn off debug print for this one too

Change 104134 on 2003/06/04 by rmanapat@rmanapat_r400_sun_marlboro

Fix for determining 3d basemap texbase address
Fix for LRU algo bug

Change 104125 on 2003/06/04 by johnchen@johnchen_r400_linux_marlboro

flop carry-save (need functional correction)

Change 104124 on 2003/06/04 by smoss@smoss_crayola_linux_orl

   changed back to #161

Change 104122 on 2003/06/04 by cbrennan@cbrennan_r400_linux_marlboro

Reverted part of earlier timing fix to set filter.
Added new timing changes for set and probe filter.
Widened mux vector on probe filter ping pong buffer for fanout timing.

Change 104121 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

use non-block assignments in clock process.

Change 104120 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

connect memory return bus up to vc.
 extend reset a little longer.

Change 104117 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Add some new test signals for vcmi fifos 2 and 3.

Change 104116 on 2003/06/04 by smoss@smoss_crayola_linux_orl

   old version with pa_sc_phase fix

Change 104114 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Added memory macro test I/O.

Change 104113 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl
```

```
 Added arbiter and data path from input fifos to RP.
  Arbiter always gives priority to mc0 return data. This will change to
  a revolving priority in a later check-in.
 Added test I/O for memory macros.

Change 104112 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Add test I/O.

Change 104106 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Fixed typo

Change 104103 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Use non-blocking assignments where necessary

Change 104102 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Added dump files coming out of memory and the MI

Change 104101 on 2003/06/04 by bbuchner@bbuchner_crayola_linux_orl

      fixing I/O, added cache flush moduel(not yet hooked up) and data converter unit

Change 104078 on 2003/06/04 by nkociuk@nkociuk_r400_linux_marl

tcd dynamic clocking reimplementation...

 new implementation relies on the existance of any outstanding requests to the MH as a
wakeup/busy condition to turn/keep the tcd clock on.  this change
 requires two new top level wires from the TCB to the TCR (identical to the
TC[0|1]_MH_send signals.  i created new signals to avoid confusion), but no change
 to chip.tree (or its numerous progeny...)

  also fix the TC_RBBM_busy signals from tcm and tcr to have ati_dff_out flops

Change 104077 on 2003/06/04 by wlawless@wlawless_r400_linux_marlboro

timing in read_dest_miss

Change 104076 on 2003/06/04 by dougd@dougd_r400_linux_marlboro

fixed bug in the loading of the write data buffer.

Change 104075 on 2003/06/04 by dclifton@dclifton_r400

added test controller
```

```
Change 104069 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Look for X's in the data readys

Change 104064 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

change to non-blocking assignments in clock process.

Change 104062 on 2003/06/04 by nkociuk@nkociuk_r400_linux_marl

clean up comments...

Change 104056 on 2003/06/04 by smburu@smburu_r400_linux_marlboro

New TCM virage run to fix the 128x128 ram area issue.

Change 104054 on 2003/06/04 by mzini@mzini_crayola_linux_orl

 Use Or'ed reset

Change 104053 on 2003/06/04 by paulv@paulv_r400_linux_marlboro

Temporarirly created new defines in rb_include.v for all GL_*
blendcontrol cases until they are added to
cmn_lib/include/rb_reg.v (all the GL_* defines needed to be
renamed due to a conflict with FireGL).

Change 104046 on 2003/06/04 by smoss@smoss_crayola_linux_orl_regress

   removed print statements

Change 104040 on 2003/06/04 by mzini@mzini_crayola_linux_orl

 Look at thedelay reset

Change 104035 on 2003/06/04 by wlawless@wlawless_r400_linux_marlboro

changed the inflight count logic, should get some better timing

Change 104032 on 2003/06/04 by mzini@mzini_crayola_linux_orl

 Check for X's on the data ready

Change 104031 on 2003/06/04 by rramsey@rramsey_crayola_linux_orl

Fix trackers so they actually compare, and compare the correct data
```

Change 104029 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Check for X's on the data ready's

Change 104026 on 2003/06/04 by rramsey@RRAMSEY_P4_r400_win

update makefile with spi block, memory changes, etc

Change 104012 on 2003/06/04 by paulv@paulv_r400_linux_marlboro

Another fix to the skid of the color write request fifo.

Change 104011 on 2003/06/04 by wlawless@wlawless_r400_linux_marlboro

added reg on data out to rbm

Change 103991 on 2003/06/04 by moev@moev2_r400_linux_marlboro

Makefile for the PA tile which uses soft variables such a ROOT & BRANCH. It also uses NCVerilog

Change 103989 on 2003/06/04 by viviana@viviana_crayola2_syn

Changed the processor to exclude the two memories for the ONEPPC define.

Change 103988 on 2003/06/04 by donaldl@donaldl_crayola_linux_orl

Initial

Change 103987 on 2003/06/04 by paulv@paulv_r400_linux_marlboro

Resized color read request fifo and fixed both the color r/w skids.

Change 103984 on 2003/06/04 by mzini@mzini_crayola_linux_orl

Added VC->SP tracker

Change 103971 on 2003/06/04 by bhankins@fl_bhankins_r400_win

fixes to support bad pipe for 2 simds

Change 103970 on 2003/06/04 by jbrady@jbrady_crayola_linux_orl

Renamed usc_ati_master_clock_gater_sclk_vc to uvc_ati_master_clock_gater_sclk_vc.

Change 103958 on 2003/06/04 by bhankins@fl_bhankins_r400_win

minor fix

```
Change 103932 on 2003/06/03 by mmantor@mmantor_crayola_linux_orl

   update for new pipe disable routing

Change 103931 on 2003/06/03 by danh@danh_r400_win

Updated per simulation results.

Change 103912 on 2003/06/03 by mzini@mzini_crayola_linux_orl

Added L2->L1 interface tracking

Change 103894 on 2003/06/03 by johnchen@johnchen_r400_linux_marlboro

makes functions.  use different shift_right and change csa 24fixed round

Change 103888 on 2003/06/03 by mzini@mzini_crayola_linux_orl

Added thread_type to VC
 Added TB_RP modules

Change 103887 on 2003/06/03 by nkociuk@nkociuk_r400_linux_marl

prevent sclk_tcd from shutting off prematurely...

 fix is to force clock on while i come up with a better way of handling the shutoff
(using memclk_active isn't going to cut it...)

Change 103882 on 2003/06/03 by johnchen@johnchen_r400_linux_marlboro

register state values instead of muxing

Change 103872 on 2003/06/03 by wlawless@wlawless_r400_linux_marlboro

timing

Change 103849 on 2003/06/03 by rramsey@rramsey_crayola_linux_orl

Fix a bug in sq_input_arb that was allowing the state machine to go
to IDLE even though a pixel thread was active. This could allow a vtx
and pix thread to try and write into the GPRs at the same time.
Turn tex ctlflow trackers back on in tb_sqsp
Fix TP_SP_data_valid connections in tb_sqsp
Modify alu ctlflow trackers so they can skip over expected instr
with serialize bits set if the rtl does not serialize them

Change 103835 on 2003/06/03 by paulv@paulv_r400_linux_marlboro
```

```
Replaced all parameters for memory macro fifos with defines.

Change 103828 on 2003/06/03 by dclifton@dclifton_r400

Fixed PA_SC_phase so it works with stub file generator.

Change 103821 on 2003/06/03 by kevino@kevino_r400_linux_marlboro

      Hopefully a timing improvement on the sctrmx RTR paths

Change 103804 on 2003/06/03 by nkociuk@nkociuk_r400_linux_marl

temp fix for tc testbench, force TPC_TCA_wakeup high, to turn on tca clock...

 also small cleanup

Change 103802 on 2003/06/03 by cbrennan@cbrennan_r400_linux_marlboro

Leda issues.  Still had some shrinking to do.

Change 103800 on 2003/06/03 by cbrennan@cbrennan_r400_linux_marlboro

Add VC_TC_clear bits for surface sync from VC.

Change 103789 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Remove 8x256 RAM macro from compile. It's not used anymore and was generating
  a warning.

Change 103784 on 2003/06/03 by paulv@paulv_r400_linux_marlboro

Fixed skid and depth of RBC color read and write fifos due to timing fix in color.

Change 103780 on 2003/06/03 by nkociuk@nkociuk_r400_linux_marl

tco and tcm dynamic clocking changes...

Change 103777 on 2003/06/03 by viviana@viviana_crayola2_syn

Deleted two 8x256 memories.

Change 103776 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Change sclk to sclk_vc.
 Change reset to RS_MI_reset.
 Add I/O to RP (not driven yet).
```

```
Change 103775 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_MI_reset.

Change 103774 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_MI_reset.
 Add RP I/O to vcmi_receiver instantiation.

Change 103773 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_RG_reset.

Change 103772 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename sclk to sclk_vc.
 Rename reset to RS_RG_reset.
 Change some combinational assignments from non-blocking to blocking for leda.

Change 103771 on 2003/06/03 by jbrady@jbrady_crayola_linux_orl

Rename usc_ati_master_clock_gater_vc_clk to usc_ati_master_clock_gater_sclk_vc.
 Rename resets on vcmi and vcrg to match vc names.
 Rename sclk on vcmi and vcrg to sclk_vc.

Change 103769 on 2003/06/03 by rmanapat@rmanapat_r400_sun_marlboro

Added new memories for Chris and reflected them on the virage.cnt file

Change 103763 on 2003/06/03 by wlawless@wlawless_r400_linux_marlboro

timing

Change 103761 on 2003/06/03 by bhankins@fl_bhankins_r400_win

updates to support bad pipe for two simds

Change 103760 on 2003/06/03 by kevino@kevino_r400_linux_marlboro

  Move some of the clamp logic back to previous stage.  Hopefully half and half with
give better results.  If not, may need to add flops.

Change 103736 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Real fix for determining the state_wr_addr and removed an
```

unused clock in rb_rbt_hiz_quad_checker.v.

Change 103731 on 2003/06/02 by nkociuk@nkociuk_r400_linux_marl

fix TCA_TCB_tca_capture_busy generation to include tca_rts (TPC_TC_rts)

Change 103717 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Timing fixes, lint fixes and finished resizing the 8x111
memory in the quad cache to 12x111.

Change 103714 on 2003/06/02 by johnchen@johnchen_r400_linux_marlboro

mult, add length fix

Change 103704 on 2003/06/02 by hmonsef@hmonsef

8x111 replaced by l2x111

Change 103702 on 2003/06/02 by hmonsef@hmonsef

Replaces 8x111

Change 103701 on 2003/06/02 by hmonsef@hmonsef

Replaces 8x111

Change 103689 on 2003/06/02 by kmeekins@kmeekins_crayola_linux_orl

Included header.v.

Change 103687 on 2003/06/02 by wlawless@wlawless_r400_linux_marlboro

move state look up for timing

Change 103681 on 2003/06/02 by mzini@mzini_crayola_linux_orl

SQ model now reads simd_id from the test file

Change 103668 on 2003/06/02 by johnchen@johnchen_r400_linux_marlboro

connect db dangling nets

Change 103659 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Resized the 11x111 ram inside the quad cache as 12x111 (depth has to be an even
number), fixed the register decode in rb_tile_fifo for the cmask_enable. Also removed
some unnecessary I/O at the top of RB and connected some DB_RB_mem signals.

```
Change 103655 on 2003/06/02 by jbrady@jbrady_crayola_linux_orl

Fix set bits in info field. Should include even/odd bit (mem_addr[6]).

Change 103649 on 2003/06/02 by jbrady@jbrady_crayola_linux_orl

Fixed a typo that caused one index to be repeated and one dropped.
 Fixed conflict_serialization. It wasn't holding it's value for external_freeze. Fix
  was to only let it change values with a vcrg5_load.

Change 103648 on 2003/06/02 by jbrady@jbrady_crayola_linux_orl

Change VC_TCx_info field to 8 bits wide, and drive it from vcmi_requestor.
 Enable VC_TCx_info tracker.

Change 103647 on 2003/06/02 by moev@moev2_r400_linux_marlboro

Made changes to the Virage patchbox to mimic the Virage order (as described in the Data
Sheet).

Change 103646 on 2003/06/02 by wlawless@wlawless_r400_linux_marlboro

tied some scan and bist this because they where not connected and
causes lint errors, as per Mark S. request

Change 103639 on 2003/06/02 by smburu@smburu_r400_linux_marlboro

n0_stall missing from sensitivity list.

Change 103625 on 2003/06/02 by wlawless@wlawless_r400_linux_marlboro

timing, added 1 more to ati_fifo_cam skid

Change 103618 on 2003/06/02 by nkociuk@nkociuk_r400_linux_marl

create TCB_TCO_wakeup signal, and fix problem with TC_RBBM_busy generation (two of the
tca busy signals can get stuck high, depending on data recieved from tp
 blocks, so just commenting those out of the busy generation for now...)

Change 103611 on 2003/06/02 by bhankins@fl_bhankins_r400_win

fix syntax error

Change 103610 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate bad pipes for 2 simd engines.  New I/O is commented out for now
for compatibility.
```

Change 103607 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

I accidentally removed a signal that shouldn't have been removed (a test I ran still passed, though). Strange. Anyway, all is better.

Change 103605 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate bad pipe signals for 2 simds

Change 103604 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate bad pipes for 2 simds

Change 103603 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate 2 simd bad pipe signals

Change 103602 on 2003/06/02 by bhankins@fl_bhankins_r400_win

changes to accomodate 2 simd bad pipe signals

Change 103579 on 2003/06/02 by paulv@paulv_r400_linux_marlboro

Some lint (synthesis and simulation) fixes, resized the HiZ data fifo in the quad cache from 8 to 11 deep and fixed a bug with the reading of the DB data fifo in the quad cache.

Change 103563 on 2003/06/02 by dclifton@dclifton_r400

typo in STAR signals

Change 103561 on 2003/06/02 by mzini@mzini_crayola_linux_orl

Force pre_rdy low once file has ended

Change 103557 on 2003/06/02 by nkociuk@nkociuk_r400_linux_marl

tcb is now dynamically clocked, so is tcd

changed clock on some perfmon-related flops

Change 103527 on 2003/06/02 by mzini@mzini_crayola_linux_orl

Exclude vc_mem.v from rg testbencvh

Change 103525 on 2003/06/02 by mzini@mzini_crayola_linux_orl

```
Let the memory model drive MH->VC RTR's

Change 103500 on 2003/06/01 by mzini@mzini_crayola_linux_orl

Submodule testbench infrastructure in place

Change 103446 on 2003/05/30 by mzini@mzini_crayola_linux_orl

 Modified scripts and vc.v to handle module testbenches

Change 103385 on 2003/05/30 by moev@moev2_r400_linux_marlboro

added termination to TST_awt_enable

Change 103382 on 2003/05/30 by bbuchner@bbuchner_crayola_linux_orl

       vc now builds with rest of chip

Change 103379 on 2003/05/30 by danh@danh_r400_win

updated per simulation results.

Change 103378 on 2003/05/30 by jbrady@jbrady_crayola_linux_orl

Remove ram macro index fifo and replace with flop based fifo. saves about
  0.078mm2 right now. may reduce it further...

Change 103373 on 2003/05/30 by viviana@viviana_crayola2_syn

Added another 12x104 memory for xyz for the ONEPPC ifdef to the pa and reconnected
   the patchin/patchout signals.

Change 103369 on 2003/05/30 by vromaker@vromaker_r400_linux_marlboro

- fix for width mismatch on thread_id input of vtx TB status regs
- initial pass of VC/TP fetch arbiter (not instantiated in sq.v yet)

Change 103366 on 2003/05/30 by cbrennan@cbrennan_r400_linux_marlboro

Another timing tweek to the LRU chain.  Precompute the used lrus for each quad.

Change 103365 on 2003/05/30 by dougd@dougd_r400_linux_marlboro

Added missing wire declaration for param_wrap_0_set

Change 103364 on 2003/05/30 by johnchen@johnchen_r400_linux_marlboro

slope_to_pixel normalize 24bits float fix
```

```
Change 103340 on 2003/05/30 by johnchen@johnchen_r400_linux_marlboro

more flopped IOs

Change 103336 on 2003/05/30 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 103324 on 2003/05/30 by nkociuk@nkociuk_r400_linux_marl

replace tc_cg block in tcf with tcf_cg (needed because ultimately the local clock
blocks in tcf/tcm/tcr will be quite different) and added tcf_cg to
 system_tc.vcpp

 also adding initial revs of tcm_cg.v and tcr_cg.v, though these modules are currently
unused

 changed clock going to some perfmon flops in tcf

 tca is now on the dynamic clock sclk_tca

Change 103320 on 2003/05/30 by kevino@kevino_r400_linux_marlboro

   in tcd_mc_test.v,  changed genm6 mc2 to use format0 2d tiled instead of linear,
since 2d linear is not a supported mode.

Change 103315 on 2003/05/30 by kevino@kevino_r400_linux_marlboro

     Fixes to load sctrarb data at right time and to not send extra valids for dxtc
requests (when some RTR's are low and some are high)

Change 103308 on 2003/05/30 by mzini@mzini_crayola_linux_orl

 Fixed build script

Change 103286 on 2003/05/30 by jbrady@jbrady_crayola_linux_orl

changed clamping conflict logic:
    // ---------------------------------------------------------------
    //  Detect conflicts due to clamping
    //   Conflict when both verts are valid and vert 0 is clamped.
    //   Conflict when vert 1 is valid and clamped.
    //   Don't conflict when vert 0 is valid and clamped but vert 1 is not valid.
    //   If only vert 1 is valid, and it is clamped, we'll conflict and send
    //    an invalid vert 0, but this should be OK. It shouldn't happen in
    //    the real world anyway, because verts should be packed toward the
    //    lower relative offsets.
```

```
    // ---------------------------------------------------------------

Change 103281 on 2003/05/30 by kevino@kevino_r400_linux_marlboro

     Moved sctrarb/dxtc arbitration from tcd_dgmmpd_dgmm_mux to
tcd_dgmmpd_sctrarb_ctrl.  This should help timing as well as giving a central point to
arbitrate between the 4 sctrmx inputs and the dxtc for the 4 dgmm units.    It also
(inadvertantly) fixed the multichannel cases genm4 and genm7.

Change 103277 on 2003/05/30 by tien@tien_r400_devel_marlboro

Mipmapping fixes

Change 103270 on 2003/05/30 by mzini@mzini_crayola_linux_orl

Define _VCAPI

Change 103261 on 2003/05/30 by jbrady@jbrady_crayola_linux_orl

flop TC_VC0_rtr and TC_VC1_rtr before using them.

Change 103256 on 2003/05/30 by dougd@dougd_r400_linux_marlboro

fixed bug in wrapping logic for rtn_ptr, read_ptr and stop_ptr for addressing the
mapping table address freelist

Change 103226 on 2003/05/29 by johnchen@johnchen_r400_linux_marlboro

flop more IOs

Change 103204 on 2003/05/29 by dougd@dougd_r400_linux_marlboro

initial submit of a submodule to count and bin pixels for perfmon

Change 103187 on 2003/05/29 by subad@subad_r400_linux_marlboro

did some clean up

Change 103168 on 2003/05/29 by johnchen@johnchen_r400_linux_marlboro

flop input rtr of memory interface

Change 103166 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

fix for l2a_vert_0_offset. was being set to vert_1_offset on 2nd cycle when only
  vert 0 was clamped. vert 1 was not clamped, so l2a_vert_0_offset should have
  vert 0's offset.
```

```
Change 103154 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

clamp count was not biased by 1, so change constant in subtract from 7 to 6.

Change 103149 on 2003/05/29 by smburu@smburu_r400_linux_marlboro

border color logic changes.

Change 103141 on 2003/05/29 by vromaker@vromaker_r400_linux_marlboro

- added simd_num input to the thread buffers (tied low in sq.v) and connected
         it down to the status regs
- added simd_num to the staging registers in the CFS
- connected simd_num thru the target_instr_fetch and tex_instr_queue
  modules (so it is an output of the tex_instr_queue)

Change 103106 on 2003/05/29 by cbrennan@cbrennan_r400_linux_marlboro

Added a stage to the register balanced portion of the baddr_gen for timing.

Change 103092 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

change default parameter to match size of memory macro. this prevents synthesis
  from complaining during an analyze.

Change 103089 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

change default parameters to match actual size of fifo. this way synthesis
  doesn't complain about mismatching ports and always re-analyze this module.

Change 103085 on 2003/05/29 by kmeekins@kmeekins_crayola_linux_orl

Added the definitions for cc_rp_stall and cc_mi_stall.

Change 103084 on 2003/05/29 by kmeekins@kmeekins_crayola_linux_orl

Included transfer_cycle_q in the definition of CC_RP_L2b_rdy to prevent multiple
  L2b FIFO writes of the same request.

Change 103082 on 2003/05/29 by smburu@smburu_r400_linux_marlboro

Hook up of border logic to tp_blend.

Change 103077 on 2003/05/29 by mzini@mzini_crayola_linux_orl

Fixed build script to include behavioranl memories for the RP block for simulation

Change 103074 on 2003/05/29 by viviana@viviana_crayola2_syn
```

```
Added a `include of sq_reg.v for synthesis purposes.

Change 103071 on 2003/05/29 by viviana@viviana_crayola2_syn

Corrected the patchin and patchout signals.

Change 103069 on 2003/05/29 by johnchen@johnchen_r400_linux_marlboro

make carry save adders

Change 103056 on 2003/05/29 by jbrady@jbrady_crayola_linux_orl

Wired STAR_scforce_16 into vcrg. This goes along with the change from an 8 deep
  to 16 deep instruction fifo.

Change 103055 on 2003/05/29 by jcarroll@jcarroll_crayola_linux_orl

I/O changes (CC_RP readys)
       Adding more functionality

Change 103050 on 2003/05/29 by bbuchner@bbuchner_crayola_linux_orl

 fixed mismatching signal names

Change 103032 on 2003/05/29 by cbrennan@cbrennan_r400_linux_marlboro

Deleted unused files.

Change 103031 on 2003/05/29 by cbrennan@cbrennan_r400_linux_marlboro

Added tca_pack_tag.v

Change 103017 on 2003/05/29 by viviana@viviana_crayola2_syn

Added 16 instances of 80x128 and 16 of 64x8.

Change 103015 on 2003/05/29 by bbuchner@bbuchner_crayola_linux_orl

   fix signal name from L2B to L2b

Change 103013 on 2003/05/29 by viviana@viviana_crayola2_syn

Changed 80x8 memory to 64x8, changed 80x128 memory to be bit writable.

Change 102987 on 2003/05/28 by subad@subad_r400_linux_marlboro

this is the fixed tcd_mc testbench. Should work.
```

```
Change 102979 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

Implement clamping feature
 change vert_0_offset to 4 bits from 5
 change to 16 deep instruction fifo
 add stage to pipe - new stage 4. output is now stage 5.

Change 102978 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

add RG_RP_L2a_clamp to RG instantiation
 change RG_RP_L2a_vert_1_offset to  RG_RP_L2a_data
 change RG_RP_L2a_vert_0_offset to 4 bits from 5 bits

Change 102977 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Added `include "vc_cc_define.v"

Change 102975 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

add clamping feature before tag generation
 change vert_offset to 4 bit field from 5 bits.

Change 102974 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

instantiate 16 deep memory macro from 8 deep. this goes with the change
  from a 4 dword to 8 dword machine.
 make default width 69 to match memory

Change 102973 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

add a missing 'end' statement

Change 102972 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

Increase counter limits to 16 for instruction fifo depth.

Change 102971 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

change 8 deep instruction fifo to 16 deep

Change 102970 on 2003/05/28 by bbuchner@bbuchner_crayola_linux_orl

  instantiate RP, modifiy signal names to match SP/SQ

Change 102968 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Changed input_fifo_rdata to use "wire" type.
```

```
Change 102961 on 2003/05/28 by mzini@mzini_crayola_linux_orl

Interface chnages for clamping

Change 102959 on 2003/05/28 by tien@tien_r400_devel_marlboro

Routed channel id to tp_fetch
Fixed loading of tp_tt

Change 102956 on 2003/05/28 by cbrennan@cbrennan_r400_linux_marlboro

Change sizes of 1d coords to 30 bits..
       Change size of 3d to 11 11 10 bits.
Change size of probe/tag/etc to 2 bits less: 29 bits from 31 in general.
Still need to do actual fifo size reduction in virage mems.

Change 102947 on 2003/05/28 by viviana@viviana_crayola2_syn

Corrected the STAR_rf_testbus[7] wired to 64x128cm2 memory instead of
STAR_rf_testbus[6].

Change 102945 on 2003/05/28 by viviana@viviana_crayola2_syn

Corrected STAR_rf_testbus[7] wired to the 64x8cm2 memory instead of STAR_rf_testbus[8].

Change 102943 on 2003/05/28 by wlawless@wlawless_r400_linux_marlboro

timing

Change 102936 on 2003/05/28 by jcarroll@jcarroll_crayola_linux_orl

            Fixed syntax error on outreg_en.

Change 102930 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Initial release.

Change 102929 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Added input FIFO data fields.

Change 102928 on 2003/05/28 by kmeekins@kmeekins_crayola_linux_orl

Removed include directive.

Change 102924 on 2003/05/28 by viviana@viviana_crayola2_syn
```

```
Added an additional 48x170 and 16x170 and rebuilt the memories.

Change 102906 on 2003/05/28 by jcarroll@jcarroll_crayola_linux_orl

Added more of the functionality.

Change 102903 on 2003/05/28 by jcarroll@jcarroll_crayola_linux_orl

Added an output register enable (outreg_en)

Change 102901 on 2003/05/28 by viviana@viviana_crayola2_syn

Changed the 69x8 to 69x16, deleted 32x32 and replaced with 32x64.

Change 102892 on 2003/05/28 by mzini@mzini_crayola_linux_orl

runvc script now handles random tests

Change 102860 on 2003/05/28 by paulv@paulv_r400_linux_marlboro

Timing fixes.

Change 102853 on 2003/05/28 by bbuchner@bbuchner_crayola_linux_orl

added vc_reset.v

Change 102840 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

fix i/o list finishing with ,
 instantiate fifos 3 and 4 for synthesis

Change 102837 on 2003/05/28 by jbrady@jbrady_crayola_linux_orl

Start of clamping logic.
 Fix for tag generation. Was adding 1 to tag_b bit 5 instead of bit 4.

Change 102812 on 2003/05/28 by mzini@mzini_crayola_linux_orl

 Added VC testbench HOWTO

Change 102802 on 2003/05/27 by nkociuk@nkociuk_r400_linux_marl

fix latency calc stuff to deal with data returned for agp requests on tf1

Change 102763 on 2003/05/27 by kevino@kevino_r400_linux_marlboro

      Added round robin arbitration to sctrarb_ctrl.
      Revamp priority in dxtc_arb so if one of the dxtx's gets the access, it gets put
```

on bottom of list.

Change 102762 on 2003/05/27 by kevino@kevino_r400_linux_marlboro

  Undo timing "fic" (that actuyally made timing worse) in fvfconv. Put mpeg clampoing after flop in rfconv to see if that meets timing.

Change 102758 on 2003/05/27 by nkociuk@nkociuk_r400_linux_marl

additional tcd dynamic clocking changes

 dynamic clocking still not enabled...

Change 102755 on 2003/05/27 by tien@tien_r400_devel_marlboro

Cleaned up some bad IO from tp_border until it is connected

Change 102745 on 2003/05/27 by tien@tien_r400_devel_marlboro

Expanded reg lod inputs to aniso to 16-bit floats

Change 102740 on 2003/05/27 by smburu@smburu_r400_linux_marlboro

Fixed an error in a bus width.

Change 102737 on 2003/05/27 by kevino@kevino_r400_linux_marlboro

  Got rid of latch inferreence

Change 102732 on 2003/05/27 by wlawless@wlawless_r400_linux_marlboro

Timing fix, removed cam_read_hit from the allocate_case

Change 102728 on 2003/05/27 by bbuchner@fl_bbuchner_r400_win

vc reset logic

Change 102723 on 2003/05/27 by ygiang@ygiang_r400_linux_marlboro

added:ppvella's block perf counters

Change 102671 on 2003/05/26 by johnchen@johnchen_r400_linux_marlboro

fix for when both q_rbt_rbd_tile_killed and q_rbt_rbd_pendingsx are high

Change 102536 on 2003/05/25 by mzini@mzini_crayola_linux_orl

Properly initialize memory model

```
Change 102486 on 2003/05/24 by mzini@mzini_crayola_linux_orl

Script for running VC testbench tests

Change 102456 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

put lines of code inside begin/end for case. it was a cut/paste to the wrong
 lines.

Change 102455 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

don't send request on state 1 in 256 bit mode if both sector bits aren't set.

Change 102431 on 2003/05/23 by nkociuk@nkociuk_r400_linux_marl

preliminary tcd dynamic clocking changes...

Change 102427 on 2003/05/23 by tien@tien_r400_devel_marlboro

Misc fixes

Change 102423 on 2003/05/23 by paulv@paulv_r400_linux_marlboro

Removed the db_data_fifo counter and just used the full signal
from the fifo logic.

Change 102411 on 2003/05/23 by dougd@dougd_r400_linux_marlboro

Simulation only protocol checking logic was moved to a clock process block
to prevent a difference in order of evaluation between vcs and ncverilog
from causing a false error assertion due to a race condition in simulation.

Change 102404 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

Fix lsb of address in states 00 and 10.

Change 102394 on 2003/05/23 by kevino@kevino_r400_linux_marlboro

       Round robin arbitrate between dxtc and dgmm instead of always giving dxtc
preference.
        If dxtc transfer is not last sent, don't accept any more dgmm transfers until
dxtc is done.  (Check if this is necessary)

Change 102389 on 2003/05/23 by paulv@paulv_r400_linux_marlboro

Requalified z_surface_enable signal to only include smask and
zrange enable (since it is only used by the quad_cache and the
```

```
HiZ blocks, which don't deal with zmask).

Change 102384 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Not ready for integration.

Change 102383 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Removed cache miss and sector miss signals from the I/O.
  Only used internally now.

Change 102381 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Maded major changes to use fetch and hit addresses to increment "busy" counter.

Change 102380 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Added definitions for RG_CC input FIFO parameters.

Change 102375 on 2003/05/23 by jbrady@jbrady_crayola_linux_orl

Issue two requests when in 256 bit mode and sector mask is '11'

Change 102370 on 2003/05/23 by wlawless@wlawless_r400_linux_marlboro

Added the ATI fifo's to sx index interface... and some timing fixes

Change 102367 on 2003/05/23 by kmeekins@kmeekins_crayola_linux_orl

Changed reset to use cache_flush.

Change 102365 on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro

moved wire declaration of sx_exp_buff_full_0 (and others) before the
instantiation of the status registers to fix ncverilog warning

Change 102360 on 2003/05/23 by johnchen@johnchen_r400_linux_marlboro

quad cache update fix

Change 102353 on 2003/05/23 by smburu@smburu_r400_linux_marlboro

Had to recreate SMS due to Virage bug.

Change 102349 on 2003/05/23 by johnchen@johnchen_r400_linux_marlboro

IO flops for color interface
```

Change 102342 on 2003/05/23 by kevino@kevino_r400_linux_marlboro

       use round-robin approach to give different inputs priority instead of always giving the priority of n0 n1 n2 n3

Change 102341 on 2003/05/23 by paulv@paulv_r400_linux_marlboro

Many fixes, including increasing the fifo depth of DB->RBM writes, STAR memory fixes and some logic issues.

Change 102317 on 2003/05/23 by hmonsef@hmonsef

16x45 and 16x242 moved from RB to Db

Change 102310 on 2003/05/23 by nkociuk@nkociuk_r400_linux_marl

send TC_MH_memreq ahead of TC[01]_MH_send signals (only one cycle early right now, but previously it wasn't sent at all...) to turn on mclk

Change 102307 on 2003/05/23 by nkociuk@nkociuk_r400_linux_marl

adding miss_stall perfmon bit

 also increased counter width of mem latency counter to 16 bits, to allow more room for agp latencies
   no real reason not to make them even bigger, since this is sim-only logic, but my suspicion is
   that the latency is unlikely to actually be 2^15 sclk cycles...

Change 102304 on 2003/05/23 by kevino@kevino_r400_linux_marlboro

      Got rid of tcd_opmux. (Was no longer a mux- just flops.)   For PD, we wanted to move these flops into the dgmm block. New module is tcd_dgmmpd_dgmm_opbuf.v which takes input from opfsm and flops it for output with ati_dff's.

Change 102301 on 2003/05/23 by hmonsef@hmonsef

2 RAMs moved from RB To DB due to DB break up from RB

Change 102300 on 2003/05/23 by hmonsef@hmonsef

Due to DB break up

Change 102298 on 2003/05/23 by hmonsef@hmonsef

New RAM due to DB break up

Change 102297 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102296 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102295 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102294 on 2003/05/23 by hmonsef@hmonsef

Moved to DB

Change 102286 on 2003/05/23 by kevino@kevino_r400_linux_marlboro

Since info went from 27 to 25 bits, reduce tcd_ipbuf fifo mem to 141 bits from 142 (info enters across 2 cycles)

Change 102276 on 2003/05/23 by johnchen@johnchen_r400_linux_marlboro

fix port mismatch

Change 102264 on 2003/05/23 by vromaker@vromaker_r400_linux_marlboro

- updated pix thread buffer for simd1 (and removed ctl sub module and redundant logic)
- renamed state_read_phase to arb_phase
- fixed CFSM serialize detection (had to add case of fetch initiated by current clause)
- removed reference to sq_thread_buff_cntl in tracker

Change 102252 on 2003/05/23 by kevino@kevino_r400_linux_marlboro

This file got replaced with tcd_dgmm_pd_sctrarb_ctrl.v and _data.v with an arb fix.

Change 102249 on 2003/05/23 by kevino@kevino_r400_linux_marlboro

Fixed sector arb. Now, no sctrmx can go until all of its sctrarbs can accept. It is still priority encoded, so must update to round robin.
Fixed ipbuf. When switching between RB (fms) and MH inputs, could get 128 bits from MH and then 128 from RB. Added state machine to only accept the second half of the request that was stared.

Change 102246 on 2003/05/23 by mearl@mearl_crayola_linux_orl

Added mask bits to behavioral parameter cache memories

```
Change 102242 on 2003/05/23 by grayc@grayc_crayola2_linux_orl

   change memory name from sc to sx

Change 102230 on 2003/05/23 by tien@tien_r400_devel_marlboro

Number of aniso fixes

Change 102202 on 2003/05/22 by mzini@mzini_crayola_linux_orl

 Made rg->cc file wasier to read

Change 102196 on 2003/05/22 by paulv@paulv_r400_linux_marlboro

Resized skid.

Change 102193 on 2003/05/22 by danh@danh_r400_win

updated per simulation results.

Change 102188 on 2003/05/22 by paulv@paulv_r400_linux_marlboro

Fixes for the DB-RB interfaces (only to/from RBT and RBM).

Change 102187 on 2003/05/22 by paulv@paulv_r400_linux_marlboro

Fixes for the DB-RB interfaces (only to/from RBT and RBM).

Change 102186 on 2003/05/22 by nkociuk@nkociuk_r400_linux_marl

leda cleanup

Change 102177 on 2003/05/22 by rmanapat@rmanapat_r400_sun_marlboro

FIxed a bug that was introduced when I was debugging simple_cubic tests
for 3d tests the min height is always 4'h20 while in simple_cubic it can
be less

Change 102158 on 2003/05/22 by rmanapat@rmanapat_r400_sun_marlboro

Fix for til_fmt19_l and til_fmt20_l for tc_simple_2d

Change 102154 on 2003/05/22 by rramsey@RRAMSEY_P4_r400_win

Update with 5/17/03 status

Change 102148 on 2003/05/22 by nkociuk@nkociuk_r400_linux_marl
```

```
remove extra port instantiation...

Change 102139 on 2003/05/22 by johnchen@johnchen_r400_linux_marlboro

ATI IO flop

Change 102138 on 2003/05/22 by nkociuk@nkociuk_r400_linux_marl

initial dynamic clocking changes (dynamic clocking functionality not currently enabled)

 also a handful of register cleanup changes in tcf (removing unused sub-block ports)

Change 102132 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Added freeze logic.

Change 102125 on 2003/05/22 by jcarroll@jcarroll_crayola_linux_orl

Initial revision

Change 102116 on 2003/05/22 by jbrady@jbrady_crayola_linux_orl

fix typo. had /, should have been '

Change 102114 on 2003/05/22 by jbrady@jbrady_crayola_linux_orl

remove extra -v

Change 102112 on 2003/05/22 by jcarroll@jcarroll_crayola_linux_orl

Initial Revisision

Change 102111 on 2003/05/22 by vbhatia@vbhatia_r400_linux_marlboro

Added gen22 test for Jocelyn to test fractional mip stuff

Change 102105 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Included logic for determining fetch and cache hit addresses for
  tag 0 and tag 1.

Change 102095 on 2003/05/22 by dougd@dougd_r400_linux_marlboro

Added the following new fields to control registers in the rbbm interface:
 SQ_CONTEXT_MISC_PERFCOUNTER_REF
 SQ_CONTEXT_MISC_YEILD_OPTIMIZE
 SQ_FLOW_CONTROL_VC_ARBITRATION_POLICY
```

```
 SQ_FLOW_CONTROL_SIMD1_DISABLE
 SQ_DEBUG_MISC_DB_READ_MEMORY

Change 102093 on 2003/05/22 by wlawless@wlawless_r400_linux_marlboro

added this pingpong fifo to color cam for timing

Change 102092 on 2003/05/22 by wlawless@wlawless_r400_linux_marlboro

Added a pingpong fifo in the probe path for timing

Change 102091 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Added freeze logic.

Change 102089 on 2003/05/22 by kmeekins@kmeekins_crayola_linux_orl

Added freeze logic.

Change 102075 on 2003/05/22 by jbrady@jbrady_crayola_linux_orl

Make change to tag gen logic to handle 8 dword verts now, not just four.
 Cache width stayed 512 bits, though, so I couldn't just change FOUR_DWORD_VERT
  in vc_common, because that assumed the cache doubled to 1024 bits with 256 bit
  banks. Now a vert can span 3 128 bit banks.

Change 102052 on 2003/05/22 by danh@danh_crayola1_linux_orl

instr_ptr and instr_ptr_q are now only compared when event_vld_q is low.

Change 102042 on 2003/05/22 by danh@danh_r400_win

updated per simulation results.

Change 102041 on 2003/05/22 by smburu@smburu_r400_sun_marlboro

Killport on sclk_tc which was floating.

Change 102039 on 2003/05/22 by dougd@dougd_r400_linux_marlboro

restored the missing line ".pb_event_state(pb_event_state)," to the instantiation of
sq_export_alloc in sq.v that somehow was removed when a merge was done in the last
submit

Change 102013 on 2003/05/21 by danh@danh_r400_win

Made changes per the simulations I ran today.
```

```
Change 102008 on 2003/05/21 by nkociuk@nkociuk_r400_linux_marl

branch test

Change 102000 on 2003/05/21 by tien@tien_r400_devel_marlboro

Cleaned up clamping logic

Change 101991 on 2003/05/21 by jcarroll@jcarroll_crayola_linux_orl

Initial checkin

Change 101985 on 2003/05/21 by johnchen@johnchen_r400_linux_marlboro

some hier stencil depth support

Change 101978 on 2003/05/21 by wlawless@wlawless_r400_linux_marlboro

TIMING FIXES

Change 101966 on 2003/05/21 by nkociuk@nkociuk_r400_linux_marl

missed one mc block with previous change...

Change 101963 on 2003/05/21 by nkociuk@nkociuk_r400_linux_marl

change module compiler instantionations into verilog to make synthesis easier

Change 101948 on 2003/05/21 by rmanapat@rmanapat_r400_sun_marlboro

Added the proper support for cube map fetches...haven't tested
the cube mip map support but if faces changes and mip = 0 testcases
works
so this fix gets tests to pass for tc_simple_cubic but not yet
for tc_simple_mip_cubic

Change 101946 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Remove another timing loop in external_pipe_freeze.

Change 101942 on 2003/05/21 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Not ready for integration.

Change 101929 on 2003/05/21 by paulv@paulv_r400_linux_marlboro

Timing experiment/fix.
```

```
Change 101922 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Add memory macros.

Change 101921 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Fix prog_depth width warnings.

Change 101920 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Module compiler source code for vcrg_addr_calc

Change 101919 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

Use ati_dff_out for VC_SQ outputs.
 Fix timing loop in pipe_freeze/RG_RP_L1_rdy.

Change 101918 on 2003/05/21 by jbrady@jbrady_crayola_linux_orl

add vcmi memories to vcs invocation

Change 101908 on 2003/05/21 by mmang@mmang_crayola_linux_orl

Fixed bug in waterfalling by grabbing register input of done_bits
instead of registered value when performing init_done_bits operation.

Change 101906 on 2003/05/21 by dougd@dougd_r400_linux_marlboro

added a 2nd read port for VC to texconst and redesigned sq_texconst_wrt_buff to perform
opportunistic writes because the write access slot was given up for VC reads

Change 101902 on 2003/05/21 by smburu@smburu_r400_sun_marlboro

Fixes related to moving TCO into TCM tile.

Change 101885 on 2003/05/21 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Not ready for integration.

Change 101883 on 2003/05/21 by rramsey@rramsey_crayola_linux_orl

fix pc write addr generation in ais_output
fix cf state machine so unexecuted conditionals don't cause a thread
to end
turn off cf trackers for now
fix a problem in the test bench related to draw pkts with no draw inits
```

```
(some cp tests do this)

Change 101881 on 2003/05/21 by danh@danh_crayola1_linux_orl

Changed PB_READ_3 state, it now uses pi_interp_cnt_q instead of interp_cnt_q.

Change 101849 on 2003/05/20 by subad@subad_r400_linux_marlboro

added all the testcases. Changed testnames to genm*

Change 101842 on 2003/05/20 by askende@askende_r400_linux_marlboro

releasing the top level change related to adding one set of flops at the interface
       between SPI and SP.

Change 101841 on 2003/05/20 by askende@askende_r400_linux_marlboro

checking in the interpolator control latency changes in SQ and SP.

Change 101839 on 2003/05/20 by smburu@smburu_r400_linux_marlboro

Changes to accomodate into. of TCO into TCM.

Change 101824 on 2003/05/20 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Not ready for integration.

Change 101811 on 2003/05/20 by smburu@smburu_r400_linux_marlboro

Change in SMS hook-up due to TCO being removed from TCR.

Change 101796 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

fix typo on memory interface

Change 101794 on 2003/05/20 by ygiang@ygiang_r400_linux_marlboro

fixed: performace signal bus from db to rb block

Change 101785 on 2003/05/20 by kevino@kevino_r400_linux_marlboro

       set last_send high on first cycle for non-dxt1 formats.

Change 101778 on 2003/05/20 by smburu@smburu_r400_sun_marlboro

Typo.
```

Change 101776 on 2003/05/20 by smburu@smburu_r400_sun_marlboro

Changed order of some dependencies.

Change 101774 on 2003/05/20 by smoss@smoss_crayola_linux_orl

   test

Change 101771 on 2003/05/20 by dclifton@dclifton_r400

Fixed some typos in STAR signal connections.
Added readback for cl_status.

Change 101764 on 2003/05/20 by nkociuk@nkociuk_r400_linux_marl

comment out unused code. leaving in as a reminder of additional required changes, and will remove later.

Change 101762 on 2003/05/20 by nkociuk@nkociuk_r400_linux_marl

fix port name mis-match

Change 101756 on 2003/05/20 by paulv@paulv_r400_linux_marlboro

Added more performance counter signals.

Change 101754 on 2003/05/20 by smburu@smburu_r400_sun_marlboro

Some NO_CONNECTS for TCO patch wires.

Change 101751 on 2003/05/20 by nkociuk@nkociuk_r400_linux_marl

change tco perfmon signals to have ati_dff input/output flops

Change 101745 on 2003/05/20 by kevino@kevino_r400_linux_marlboro

      Put in early mant2's compliment for neg sign that only has to add 1 to 11 bits insteaqd of all 31. Hopefully this will fix timing.

Change 101742 on 2003/05/20 by viviana@viviana_crayola2_syn

Added the new module for the virage memories new revision.

Change 101741 on 2003/05/20 by viviana@viviana_crayola2_syn

Added sx_rf_awt_gate module and connected it.

Change 101733 on 2003/05/20 by hmonsef@hmonsef

LOG2_NUM_PIPES was defined as a register and a wire. Needs to be a register.

Change 101732 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add test I/O.

Change 101730 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add in MH ports that were clobbered.

Change 101729 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Instantiate RAM and test I/O.

Change 101728 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Instantiate RAMs and test I/O.

Change 101727 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add test I/O.

Change 101726 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Instantiate test and scan logic and I/O.

Change 101725 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Add test interface to vc instantiation - tie to zero and drive test clock.

Change 101724 on 2003/05/20 by jbrady@jbrady_crayola_linux_orl

Put memory -v's in front of library -y's so we get the _rtl versions without
 timing.

Change 101696 on 2003/05/19 by viviana@viviana_crayola2_syn

Added an additional 10x96 memory to be used if ONEPPC is defined.

Change 101690 on 2003/05/19 by subad@subad_r400_linux_marlboro

fixed the random generation code. Still needs work..

Change 101687 on 2003/05/19 by tien@tien_r400_devel_marlboro

Fix for Mark Earl. cp tests. It's a good thing someone is testing
unnormalized texture coordinates

```
Change 101682 on 2003/05/19 by viviana@viviana_crayola2_syn

Added the virage modules and memories.

Change 101678 on 2003/05/19 by nkociuk@nkociuk_r400_linux_marl

move tco from tcr into tcm
 tree files, makefiles, and DEPS updated.

 minor perfmon update also included.

 IO flops (ati_dff) might still need to be updated in some sub-blocks, and STAR memory
connections will undoubtedly need to be updated too

Change 101651 on 2003/05/19 by moev@moev2_r400_linux_marlboro

added '0' constant to TST_awt_enable.

Change 101642 on 2003/05/19 by vromaker@vromaker_r400_linux_marlboro

- made top level SQ signal changes/additions for SP simd0 and simd1
- added an alu thread arbiter, pairs of alu ctl flow seq, instr
  fetch, instr que, and instr seq modules, and ais_output for simd1
- thread buff cntl sub module removed from vtx thread buffer, and its
  logic moved up to the thread buff level (this still needs to be done
  for the pix thread buffer)
- only one status reg read mux and arb request shifter is needed in the
  thread buffer to support 4 arbiters (since the state mem can only be
  read by one arbiter per cycle), so the duplicates were removed

Change 101640 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

fix prog_depth port width.

Change 101637 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

First check in. Just instantiates input fifos.

Change 101636 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

Add data and info ports to vcmi.

Change 101635 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

Instantiate vcmi_receiver.

Change 101633 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl
```

```
Fix sensitivity list.

Change 101626 on 2003/05/19 by mzini@mzini_crayola_linux_orl

Fixed data return

Change 101603 on 2003/05/19 by kevino@kevino_r400_linux_marlboro

       Fixed busy in fetch_gen_sector_walker.

Change 101590 on 2003/05/19 by jbrady@jbrady_crayola_linux_orl

Move stride and index_round from instruction fifo to constant fifo - they are
 only used for megafetches, and this saves area.

Change 101589 on 2003/05/19 by cbrennan@cbrennan_r400_linux_marlboro

Add a simv target for compile checking.

Change 101587 on 2003/05/19 by cbrennan@cbrennan_r400_linux_marlboro

Fix more leda errors.
Sensitivity list errors and missing ports.

Change 101583 on 2003/05/19 by rmanapat@rmanapat_r400_sun_marlboro

removed tca_sel_siref.v from the system_tc.vcpp file
changed assign statments for d_pitch and d_height to be more readable

Change 101580 on 2003/05/19 by kevino@kevino_r400_linux_marlboro

       Fix for cacheline format 6.   Select is based on channel_in[0],  not Z.

Change 101575 on 2003/05/19 by smoss@smoss_crayola_linux_orl_regress

   changed delay on tp_sp signals

Change 101572 on 2003/05/19 by kevino@kevino_r400_linux_marlboro

  Fix formats 43 and 44.  Attempt to fix formats 45-47 but still fail

Change 101568 on 2003/05/19 by cbrennan@cbrennan_r400_linux_marlboro

Fix new leda error.

Change 101567 on 2003/05/19 by cbrennan@cbrennan_r400_linux_marlboro
```

```
Update file list.

Change 101499 on 2003/05/18 by mzini@mzini_crayola_linux_orl

 Added MH->VC files

Change 101497 on 2003/05/18 by mzini@mzini_crayola_linux_orl

 Fixed random delays

Change 101494 on 2003/05/18 by tien@tien_r400_devel_marlboro

sp_tp_formatter fix

Change 101423 on 2003/05/16 by mzini@mzini_crayola_linux_orl

Coded data return path in the memory model

Change 101419 on 2003/05/16 by tien@tien_r400_devel_marlboro

Moved input flops out of sp_tp_formatter

Change 101411 on 2003/05/16 by subad@subad_r400_linux_marlboro

middle of duplicating random number changes to the other channels

Change 101388 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

add RG_busy output.
 set instruction fifo depth to 8.
 store index valids in index fifo now, not instruction fifo. they go in the sign
 position of the float index. the exponent msb's get cleared for negative numbers
 now, so negative numbers still clamp to zero because their exponent is < 64. this
 allows us to save 64 bits in instruction fifo, selected_valids muxing, and valid
 reconstruction flops.

Change 101387 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

valids don't come out of instruction fifo anymore. we get 16 valids with their
 indices out of the index fifo (valids in msb of index). the selected_valids
 mux goes away.

Change 101385 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

hardwire sign bit to 0 (positive). negative indices have their exponent
 clamped to <=63 now, so they are clamped to zero by the exponent compare.

Change 101384 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl
```

```
add RG_busy port to vcrg

Change 101382 on 2003/05/16 by mzini@mzini_crayola_linux_orl

Instr FIFO depth changed from 16 to 8

Change 101378 on 2003/05/16 by smoss@smoss_crayola_linux_orl_regress

   added field for TP_SP_rf_expand_enable

Change 101367 on 2003/05/16 by dclifton@dclifton_r400

Added one-prim-per-clock mode for setup engine.  Define ONEPPC to get compiler to build
for this mode.

Change 101364 on 2003/05/16 by jbrady@jbrady_crayola_linux_orl

qualify next_vc_tcx_send with vcmi1_rts, else we propogate x's

Change 101360 on 2003/05/16 by dclifton@dclifton_r400

Added ONEPPC define for one-prim-per-clock build mode of setup engine.

Change 101358 on 2003/05/16 by cbrennan@cbrennan_r400_linux_marlboro

Fixed typo..   Adds missing sensitivity list entry.

Change 101357 on 2003/05/16 by nkociuk@nkociuk_r400_linux_marl

final (mostly anyway...) perfmon cleanup

Change 101344 on 2003/05/16 by vbhatia@vbhatia_r400_linux_marlboro

clean up some code and updated regressions to remove stimulus files after compare

Change 101334 on 2003/05/16 by kevino@kevino_r400_linux_marlboro

      Replaced TCD_TCO input flops with ati_dff's for when TCO is moved out of the TCR
block to the TCM block (so that TCD and TCO are now in seperate blocks)

Change 101332 on 2003/05/16 by kevino@kevino_r400_linux_marlboro

        Updated SA3 to SA5 based on TC spec 0.51 for the interlaced formats
        It turns out this doesn't change any code since the addresses, data, and write
masks ar ethe same, but table.pl was updated to be correct

Change 101321 on 2003/05/16 by cbrennan@cbrennan_r400_linux_marlboro
```

Another timing tweek.. This time on the lru drop chain.

Change 101314 on 2003/05/16 by moev@moev_r400_linux_marlboro

updates

Change 101283 on 2003/05/16 by smburu@smburu_r400_linux_marlboro

tp_ch_blend testbench.

Change 101262 on 2003/05/15 by cbrennan@cbrennan_r400_linux_marlboro

Timing tweak on set filter.

Change 101243 on 2003/05/15 by tien@tien_r400_devel_marlboro

Update makefiles and dependecies
Added border code

Change 101230 on 2003/05/15 by johnchen@johnchen_r400_linux_marlboro

send memory export like event

Change 101224 on 2003/05/15 by subad@subad_r400_linux_marlboro

Need to split into four individual loops

Change 101221 on 2003/05/15 by nkociuk@nkociuk_r400_linux_marl

connect internal tcf rbbm readback daisy chain

Change 101211 on 2003/05/15 by paulv@paulv_r400_linux_marlboro

Memory export fix.

Change 101206 on 2003/05/15 by rmanapat@rmanapat_r400_sun_marlboro

change to tc_tca_unpack_coord makes this module correspond more directly to ver .51 of the spec in terms of cacheline format
Change to tca_smask_control_gen fixes fmt 28, 29, 32, 34, 35, 37, 50, 54, 55, 56 for 3d tiled accesses
Commented out some unecessary logic in tcb_ldso_offset
Change to tcb_sector_gen fixes fmt 28, 29, 32, 34, 35, 37, 50, 54, 55, 56 for 3d tiled accesses
Change to tcb_tex_baddr_gen should fix cp_e2paint_565 which started to fail for Orlando recently

```
Change 101200 on 2003/05/15 by wlawless@wlawless_r400_linux_marlboro

timing fixes

Change 101198 on 2003/05/15 by johnchen@johnchen_r400_linux_marlboro

fix for memory export

Change 101195 on 2003/05/15 by paulv@paulv_r400_linux_marlboro

Added some performance counter signals.

Change 101168 on 2003/05/15 by rramsey@rramsey_crayola_linux_orl

fix a problem with my param cache allocate fix and fill the hole
in our spsx tracker that let the problem slip through my regressions
(pc write addr was not being checked)

Change 101139 on 2003/05/15 by paulv@paulv_r400_linux_marlboro

Memory Export fixes (not done yet, though...).

Change 101103 on 2003/05/14 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 101067 on 2003/05/14 by mzini@mzini_crayola_linux_orl

 Fixed rdy behacior

Change 101064 on 2003/05/14 by danh@danh_r400_win

Updated fields in regards to my simulation results.

Change 101062 on 2003/05/14 by cbrennan@cbrennan_r400_linux_marlboro

Timing rework that makes miss_stall come out of a flop.

Change 101059 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

fix serialization of constant 1 base address.

Change 101049 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

fix type 2'b1 to 2'b01

Change 101041 on 2003/05/14 by tien@tien_r400_devel_marlboro
```

```
Change 101035 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

add another condition to MI_CC_rtr (|| input_fifo_re) to prevent unnecessary
 lowering of rtr.

Change 101019 on 2003/05/14 by jbrady@jbrady_crayola_linux_orl

Don't send last_index_of_vv during both cycles of a conflict serialization. Only
 send it on the last cycle of the serialization.

Change 101009 on 2003/05/14 by rramsey@rramsey_crayola_linux_orl

Changes for parameter cache deallocation. Need to multiply dealloc
count by (vs_export_count +1) so the correct number of lines are
freed.

Change 100992 on 2003/05/14 by cbrennan@cbrennan_r400_linux_marlboro

Fixes signal name collision on two stages of z_pitch_sec.
Caused two successive fetches of different maps with different z pitches to mismatch.
Fixes tp_mipmap_smallprim_01 MipMinMag_LinearLinearLinear_16x16_on_2x2.

Change 100990 on 2003/05/14 by rmanapat@rmanapat_r400_sun_marlboro

I changed the way I did the offsets when a mip fell below the min value
and this fix reflects that change for 1D fetches

Change 100983 on 2003/05/14 by wlawless@wlawless_r400_linux_marlboro

Yet another small fix for 2 sample, now all basic pass......

Change 100977 on 2003/05/14 by cbrennan@cbrennan_r400_linux_marlboro

forgot this file.

Change 100973 on 2003/05/14 by nkociuk@nkociuk_r400_linux_marl

last small valid_probe fix...

Change 100969 on 2003/05/14 by cbrennan@cbrennan_r400_linux_marlboro

implemented mip packing into coord sorter.    Still need to fix timing on coord sort.

Change 100962 on 2003/05/14 by rmanapat@rmanapat_r400_sun_marlboro

Fixed a bug related to generating the correct texture_base_address
once the calculated address had offsets that dipped below the min
```

```
value for the given format

Change 100961 on 2003/05/14 by tien@tien_r400_devel_marlboro

Fixed TP_SP_rf_expand_enable.

Change 100952 on 2003/05/14 by jayw@jayw_r400_linux_marlboro

Fixes for 2-sample

Change 100943 on 2003/05/14 by nkociuk@nkociuk_r400_linux_marl

fix valid_probes signal width...

Change 100940 on 2003/05/14 by nkociuk@nkociuk_r400_linux_marl

increased bus width and changed bit definitions of TCB_PM_valid_probes (simple
concatenation now, rather than sum)

Change 100938 on 2003/05/14 by tien@tien_r400_devel_marlboro

Fixed width of TP_SP_simd

Change 100934 on 2003/05/14 by mzini@mzini_crayola_linux_orl

 Added CC->MI interface tracker

Change 100885 on 2003/05/14 by rramsey@RRAMSEY_P4_r400_win

update validation report

Change 100881 on 2003/05/14 by danh@danh_r400_win

Changed the lines of the simulations that I have run.

Change 100877 on 2003/05/14 by rramsey@rramsey_crayola_linux_orl

Fix 3 issues related to parameter cache allocation/deallocation
  1) Move allocate subtract for pc_free_cnt so it happens when
     an allocating vtx thread wins arbitration instead of when
     the thread is sent to the CFS. This puts the arbitration/
     allocate path at four clks (from six) so we can correctly
     allocate every four clocks.
  2) Deallocs were being dropped in sq_ptr_buff on back to back
     row transfers if the first of the pair was the last row
     (end of buffer) and the second of the pair had dealloc.
  3) Deallocs need to be accumulated in sq_ptr_buff since multiple
     row transfers of a pixel vector can be marked with dealloc
```

```
     and the deallocs are put in the event fifo at end_of_buffer.

Clean up some duplicate code in tb_sqsp and set the default dump
level back to 1 (instead of 3).

Change 100872 on 2003/05/14 by mzini@mzini_crayola_linux_orl

Added MI->MH interface tracker

Change 100871 on 2003/05/14 by mzini@mzini_crayola_linux_orl

Stop sending ddata once the file is empty

Change 100855 on 2003/05/13 by smoss@smoss_crayola_linux_orl_regress

<Orlando Hardware Regression Results >

Change 100833 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Fix stage 2 control.
 Fix typo where vc0_tc_request_type was assigned twice, and vc1 wasn't there at all.

Change 100822 on 2003/05/13 by nkociuk@nkociuk_r400_linux_marl

perf logic updates

Change 100821 on 2003/05/13 by nkociuk@nkociuk_r400_linux_marl

get the correct read/write signals for perf logic...

Change 100809 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Force unused rtrs to 1

Change 100806 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Fix cut/paste errors in output mux. Only change stage 2 control when vcmi2_load
 is true. Fix cut/paste error in vc0_tc_send flop.

Change 100801 on 2003/05/13 by dougd@dougd_r400_linux_marlboro

corrected port width mismatches in sq_aluconst_top; removed unused input and output
from sq_const_map_cntl and in it's instantiations in sq_aluconst_top and
sq_texconst_top

Change 100795 on 2003/05/13 by dougd@dougd_r400_linux_marlboro

corrected signal names to b1 ports of sq_cfc
```

```
Change 100794 on 2003/05/13 by tien@tien_r400_devel_marlboro

Top level May 15th changes for TPC/TP

Change 100793 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Added CC trackers and drivers

Change 100791 on 2003/05/13 by jayw@jayw_r400_linux_marlboro

Flip128L now does full swap.  for memory exports.

Change 100790 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

De-muxed piping of request_type.

Change 100785 on 2003/05/13 by smburu@smburu_r400_linux_marlboro

Ram daisy chain connections.

Change 100780 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Only check one request for local memory aperature. Since both requests are to
 the same surface, they will both be local or agp. This saves some big comparitors.

Change 100774 on 2003/05/13 by smburu@smburu_r400_linux_marlboro

Corrected hook-up of scforce.

Change 100771 on 2003/05/13 by rmanapat@rmanapat_r400_sun_marlboro

changed a comment in the 3d file
fixed a cut and paste error in the baddr_gen file

Change 100770 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Initial check-in of memory interface module. Only has requestor, not data return
 path at this time.

Change 100768 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Add memory request ports to vc instantiation.

Change 100766 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Instantiate memory interface module (vcmi).
```

```
Change 100765 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Instead of sending fb_size, compute fb_start+fb_size and send it out as
 fb_end.

Change 100755 on 2003/05/13 by smburu@smburu_r400_linux_marlboro

Corrected an error in the exponent in the case of denorms.

Change 100754 on 2003/05/13 by wlawless@wlawless_r400_linux_marlboro

LEDA fixes only

Change 100748 on 2003/05/13 by danh@danh_crayola1_linux_orl

instr_ptr and instr_ptr_q are now only compared when event_vld_q is low.

Change 100711 on 2003/05/13 by smburu@smburu_r400_sun_marlboro

Put in range statement for iTEST_EN to make mktree happy.

Change 100707 on 2003/05/13 by smburu@smburu_r400_sun_marlboro

Put in the iTEST_EN pin.

Change 100706 on 2003/05/13 by jayw@jayw_r400_linux_marlboro

DB leda

Change 100705 on 2003/05/13 by jayw@jayw_r400_linux_marlboro

updated for DB split

Change 100699 on 2003/05/13 by mzini@mzini_crayola_linux_orl

Only enable SQ->VC interface after reset

Change 100694 on 2003/05/13 by wlawless@wlawless_r400_linux_marlboro

Added all the 2 sample stuff..........

Change 100677 on 2003/05/13 by paulv@paulv_r400_linux_marlboro

HiZ/HiS fixes and a fix for back-to-back quad cache
uninitialized tiles.

Change 100673 on 2003/05/13 by askende@askende_r400_linux_marlboro
```

```
fix a typo related to out-of-range indexing

Change 100671 on 2003/05/13 by jbrady@jbrady_crayola_linux_orl

Only save megafetch_offset on megafetches. It was getting updated for minis also.

Change 100638 on 2003/05/13 by smburu@smburu_r400_linux_marlboro

Optimizations plus rounding-off of ws multiply.

Change 100637 on 2003/05/13 by smburu@smburu_r400_linux_marlboro

Optimizations for area plus rounding-off of ws multiply.

Change 100631 on 2003/05/13 by dougd@dougd_r400_linux_marlboro

Added `define SIMD1 to header.v and corrected connections for SIMD1 in sq.v

Change 100629 on 2003/05/13 by rramsey@rramsey_crayola_linux_orl

Update tb_sqsp for latest SP top level changes
Zero out rbbm fifo data when writing for re_dly
Add a couple of missing wire declarations to sq

Change 100601 on 2003/05/12 by tien@tien_r400_devel_marlboro

MOved unused bits in FIFOs to MSBs for future removal

Change 100574 on 2003/05/12 by mzini@mzini_crayola_linux_orl

Fixed odd set conflict check

Change 100546 on 2003/05/12 by subad@subad_r400_linux_marlboro

testbench works fine. Need to add tests.

Change 100537 on 2003/05/12 by rmanapat@rmanapat_r400_sun_marlboro

Problems found when determining 3d texture base addresses these
should fix them

Change 100518 on 2003/05/12 by paulv@paulv_r400_linux_marlboro

Added signal to denote that the HiZ quad checker will not
update the quad cache (for example, when only z enabled and z
write enabled is false).

Change 100508 on 2003/05/12 by wlawless@wlawless_r400_linux_marlboro
```

```
got 2 test passing....

Change 100501 on 2003/05/12 by smoss@smoss_crayola_linux_orl_regress

   ncverilog for vgt pa

Change 100480 on 2003/05/12 by mzini@mzini_crayola_linux_orl

Fixed FIFO counts

Change 100468 on 2003/05/12 by dougd@dougd_r400_linux_marlboro

removed incorrect bit width assignments to eo_rt_aluconst and eo_rt_texconst to prevent
compile errors with ncverilog

Change 100456 on 2003/05/12 by kevino@kevino_r400_linux_marlboro

    Fixed state_info size mismatch : drop AGP512

Change 100453 on 2003/05/12 by rramsey@rramsey_crayola_linux_orl

Update for top level sp changes

Change 100431 on 2003/05/12 by tien@tien_r400_devel_marlboro

Cleanup

Change 100417 on 2003/05/12 by paulv@paulv_r400_linux_marlboro

Some name changes and HiZ/HiS fixes.

Change 100416 on 2003/05/12 by paulv@paulv_r400_linux_marlboro

LEDA fixes.

Change 100400 on 2003/05/12 by nkociuk@nkociuk_r400_linux_marl

perfmon fixes
 some cleanup of tcf_registers unintended IO ports...

Change 100393 on 2003/05/12 by bhankins@bhankins_crayola_win_orl

finish making change of mem_we to mem_wen

Change 100383 on 2003/05/12 by smburu@smburu_r400_linux_marlboro

Redo of TCM virage work.
```

```
Change 100382 on 2003/05/12 by bhankins@bhankins_crayola_win_orl

rename mem_we to mem_wen

Change 100381 on 2003/05/12 by bhankins@bhankins_crayola_win_orl

fix input data rotate mux

Change 100310 on 2003/05/10 by smoss@smoss_crayola_linux_orl_regress

   ncsim for sqsp and sx

Change 100254 on 2003/05/09 by mzini@mzini_crayola_linux_orl

Changed VCCC output monitors

Change 100243 on 2003/05/09 by dclifton@dclifton_r400

added pa_rf_awt_gate dependency for pa

Change 100242 on 2003/05/09 by danh@danh_crayola_linux_orl

Changed p<3:0>_blue_norm and p<3:0>_screen_y_final MSB generation per C code.

Change 100226 on 2003/05/09 by nkociuk@nkociuk_r400_linux_marl

interim checkin

Change 100223 on 2003/05/09 by subad@subad_r400_linux_marlboro

still need to fix tcd_test.v for gen0.

Change 100221 on 2003/05/09 by wlawless@wlawless_r400_linux_marlboro

Added some counter so that op would not get ahead of probes inc and dec on tiles

Change 100217 on 2003/05/09 by kevino@kevino_r400_linux_marlboro

 Fix for fmt 3,4,5,15 linear degamma

Change 100212 on 2003/05/09 by jayw@jayw_r400_linux_marlboro

Added db_read_or.v, replacing an instance of rb_read_or.v

Change 100206 on 2003/05/09 by nkociuk@nkociuk_r400_linux_marl

remove unused block...
```

```
Change 100199 on 2003/05/09 by bhankins@bhankins_crayola_win_orl

try to get rid of wierd carriage returns

Change 100190 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

change sector_mask to bank_mask

Change 100187 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

generate 4 bit bank mask rather than 2 bit sector mask. made it parametizable for
 4 or 8 dword indices.

Change 100186 on 2003/05/09 by nkociuk@nkociuk_r400_linux_marl

fix fifo_busy connection

Change 100185 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

Remove unused loop1 integer

Change 100182 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

change sector_mask to bank_mask. also change conflict detection logic to detect
 conflict between even0 and odd1, or between odd0 and even1

Change 100181 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

Add DWORD_SIZE and FOUR_DWORD_INDICES

Change 100180 on 2003/05/09 by jbrady@jbrady_crayola_linux_orl

Change RG_CC_sector_mask to RG_CC_bank_mask

Change 100175 on 2003/05/09 by askende@askende_r400_linux_marlboro

releasing R500 related IO top level changes for SP/SPI system

Change 100167 on 2003/05/09 by rramsey@RRAMSEY_P4_r400_win

Updating status

Change 100164 on 2003/05/09 by dougd@dougd_r400_linux_marlboro

ifdef'd connections in sq.v to sq_aluconst_top.v for the extra SIMD1 memory

Change 100154 on 2003/05/09 by rramsey@rramsey_crayola_linux_orl
```

```
Changes for instruction store addressing (wrapping and absolute)
  Add absolute addressing for cf and exec addresses to cfs
  Add wrapping for jumps and calls to cfs
  Add wrapping for execute addresses to cfs
  Fix wrapping in instr_fetch (vtx wrap at pix_base-1)

These changes fix cp_event_timestamp_instruction_loading_stall at tb_sqsp

Change 100141 on 2003/05/09 by viviana@viviana_crayola2_syn

Corrected a wire name for new vgt_rf_awt_gate module addition.

Change 100118 on 2003/05/09 by dougd@dougd_r400_linux_marlboro

added 2nd memory to sq_cfc to support SIMD1 and ifdef'd the connections in sq_cfc and
sq.v

Change 100113 on 2003/05/09 by bhankins@bhankins_crayola_linux_orl

1. bug fix with quad_gen_cnt and quad_pair_base_offset.
   2. replace pa_pos_req_buff (skid_buff_top) with ati_fifo to remove unnecessary
warnings.

Change 100111 on 2003/05/09 by bhankins@bhankins_crayola_linux_orl

misc updates

Change 100093 on 2003/05/08 by jayw@jayw_r400_linux_marlboro

removed unused depth files and one color file.  removed from system_db.vcpp too.

Change 100080 on 2003/05/08 by johnchen@johnchen_r400_linux_marlboro

fix for 24bits float rounding

Change 100077 on 2003/05/08 by tien@tien_r400_devel_marlboro

Updated IO

Change 100076 on 2003/05/08 by tien@tien_r400_devel_marlboro

LEDA fixes
Aniso fixes

Change 100024 on 2003/05/08 by subad@subad_r400_linux_marlboro

still needs work. But just added the forked print. May not be
```

```
       compilable.

Change 100016 on 2003/05/08 by mmantor@mmantor_crayola_linux_orl

<changed index to 7 bits to get compilation>

Change 100015 on 2003/05/08 by mmantor@mmantor_crayola_linux_orl

<sq_ais_output - re-ordered kill_mask going to the sx so bits flow in order msb->lsg
sp2(v3-v0)sp0(v3-v0)) to match exp_mask
                  - removed improper final update of kill mask with predication mask
                  - enable export_mask for all exports
    SX_PA_interfaces.v - fixed checker for back to back transfers
    SX_RB_interfaces.v - hooked up to 7 bit sx_rb_index and rb_sx_index instead of
incorrect 8 bits
    sx.v - changed interfaces for sx_rb and rb_sx interfaces to become 7 bits instead
of 8 bits
    tb_sx.v - changed sx inputs to be 7 bits instead of 8 bits on the above index
interfaces
    tbmod_fake_sp.v - reordered the kill mask and enabled channel mask for exports
    sx_export_buffers.v - moved register after export mems and only load when memory
read, mimized client read muxes added input rotate muxes for export to memory
operations and indivual write address for each memory and set up predication,
kill_mask, alpha kill,and channel mask in the determination of writing data into the
export buffers
    sx_export_control.v - removed dead clock on rb and pa data fetch interface and
client and made arbiter behave as round robin and removed unecessary second input
register, added support for z render targets and multiple render targets and clean up
items
    ex_export_alloc_dealloc.v - enabled channel mask, kill mask, export_mask, and apha
test conditioning of valid bitsa doubled the free rate>

Change 99998 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl

tb_vc - hook up rbbm interface
 vc_rbui - use registered version of rbbm inputs, not the inputs themselves

Change 99991 on 2003/05/08 by danh@danh_crayola_linux_orl

Made minor Param*blue, Param*alpha sensitivity list changes.

Change 99978 on 2003/05/08 by kevino@kevino_r400_linux_marlboro

     Changed TC_MH_info to be 25 bits from 27.   Changed VC_TC_info to 18 bits since
the VC guys say that's all they'll use.  Pad the top 7 bits with 0's.

Change 99977 on 2003/05/08 by kevino@kevino_r400_linux_marlboro
```

```
        change agp_access to be before or after framerbuffer (was just after)

Change 99967 on 2003/05/08 by jayw@jayw_r400_linux_marlboro

Added clock enable pin from rb to db.

Change 99965 on 2003/05/08 by mzini@mzini_crayola_linux_orl

Fixed RBBM interface

Change 99956 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl

First check-in of RBBM interface and render state decode module for vc.

Change 99955 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl

Added rbbm interface and vc_rbiu.v

Change 99947 on 2003/05/08 by mzini@mzini_crayola_linux_orl

RBBM interface

Change 99946 on 2003/05/08 by mzini@mzini_crayola_linux_orl

Added RBBM interface

Change 99920 on 2003/05/08 by kevino@kevino_r400_linux_marlboro

   Removed some files from te old fetch gen

Change 99919 on 2003/05/08 by vbhatia@vbhatia_r400_linux_marlboro

Added clamp for logw, h and d to valid values and created gen100 for testing out of
range non hang condition

Change 99918 on 2003/05/08 by dougd@dougd_r400_linux_marlboro

fixed typo

Change 99912 on 2003/05/08 by dougd@dougd_r400_linux_marlboro

doubled the instruction store memory, changed the access allocation to accomdate SIMD1
and VC, and `ifdef'd the connections for SIMD1 in sq.v

Change 99911 on 2003/05/08 by kevino@kevino_r400_linux_marlboro

   Updated fetch generator for performance.  Now two pipes walk list of all sectors
from opposite ends.  Two stages for timing.
```

Change 99902 on 2003/05/08 by jbrady@jbrady_crayola_linux_orl

Fix typo for syntax

Change 99893 on 2003/05/08 by wlawless@wlawless_r400_linux_marlboro

Block probes back to the same tile if there is more then 2 tiles... things were
getting plugged up,

Change 99890 on 2003/05/08 by kevino@kevino_r400_linux_marlboro

    Got rid of fetch gen registers. Replaced for now with constants. Next checkin,
shouldbe able to remove them completely.

Change 99868 on 2003/05/08 by mzini@mzini_crayola_linux_orl

Added VC behavioral memory

Change 99863 on 2003/05/08 by smburu@smburu_r400_sun_marlboro

Corrected an indexing into a non-array variable error.

Change 99818 on 2003/05/07 by cbrennan@cbrennan_r400_linux_marlboro

Added ping pong buffer back in front of probe filter to break up stall fanout.

Change 99808 on 2003/05/07 by paulv@paulv_r400_linux_marlboro

Fixed toplevel *rfsms_stp instantiations.

Change 99799 on 2003/05/07 by viviana@viviana_crayola2_syn

Updated the virage memories built to include the atpg_gate and sync_reset.

Change 99786 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99784 on 2003/05/07 by danh@danh_crayola_linux_orl

Changed all Param*blue and Param*alpha generation so it matches the C code.

Change 99783 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99778 on 2003/05/07 by hmonsef@hmonsef

new DB

Change 99774 on 2003/05/07 by hmonsef@hmonsef

New Db

Change 99772 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99771 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99770 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99769 on 2003/05/07 by hmonsef@hmonsef

new DB

Change 99768 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99767 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99766 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99765 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99764 on 2003/05/07 by hmonsef@hmonsef

new DB

Change 99762 on 2003/05/07 by hmonsef@hmonsef

New DB

Change 99736 on 2003/05/07 by viviana@viviana_crayola2_syn

Rebuilt the memories with virage/3300 at 444 Mhz from scratch.

Change 99733 on 2003/05/07 by hmonsef@hmonsef

Dpeth removed from Rb

Change 99729 on 2003/05/07 by hmonsef@hmonsef

New version is checked in from a different directory

Change 99722 on 2003/05/07 by hmonsef@hmonsef

removed<enter description here>

Change 99721 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99719 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99718 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99717 on 2003/05/07 by hmonsef@hmonsef

removed <enter description here>

Change 99716 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99714 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99713 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99712 on 2003/05/07 by hmonsef@hmonsef

Removed

Change 99711 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99710 on 2003/05/07 by hmonsef@hmonsef

removed

Change 99709 on 2003/05/07 by hmonsef@hmonsef

Change 99707 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99706 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99701 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99697 on 2003/05/07 by hmonsef@hmonsef

comp new rev

Change 99695 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99694 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99693 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99692 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99691 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99690 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99689 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99688 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99687 on 2003/05/07 by hmonsef@hmonsef

comp with new rev

Change 99686 on 2003/05/07 by hmonsef@hmonsef

comp new rev

Change 99684 on 2003/05/07 by hmonsef@hmonsef

new com rev

Change 99682 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99681 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99680 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99679 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99678 on 2003/05/07 by hmonsef@hmonsef

New comp rev

Change 99677 on 2003/05/07 by hmonsef@hmonsef

new comp rev

Change 99676 on 2003/05/07 by hmonsef@hmonsef

New comp rev

Change 99675 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99674 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99673 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99672 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99670 on 2003/05/07 by hmonsef@hmonsef

New comp rev

Change 99668 on 2003/05/07 by hmonsef@hmonsef

New compiler Rev

Change 99667 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99666 on 2003/05/07 by hmonsef@hmonsef

New compiler rev

Change 99662 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

updates to approach running at full speed

Change 99659 on 2003/05/07 by hmonsef@hmonsef

DB removed from RB

Change 99657 on 2003/05/07 by hmonsef@hmonsef

DB removed form RB

Change 99656 on 2003/05/07 by hmonsef@hmonsef

```
DB removed from RB

Change 99655 on 2003/05/07 by hmonsef@hmonsef

DB is removed from RB

Change 99654 on 2003/05/07 by hmonsef@hmonsef

 DB is removed from RB

Change 99650 on 2003/05/07 by hmonsef@hmonsef

Checking in the file form virage directory

Change 99649 on 2003/05/07 by hmonsef@hmonsef

Checking in the file from virage directory

Change 99620 on 2003/05/07 by hmonsef@hmonsef

Remove Depth from RB

Change 99618 on 2003/05/07 by hmonsef@hmonsef

Remove Depth from RB

Change 99615 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB

Change 99614 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB

Change 99612 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB

Change 99611 on 2003/05/07 by hmonsef@hmonsef

Removing Depth from RB

Change 99602 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

speed up resets to pixel scoreboard

Change 99599 on 2003/05/07 by paulv@paulv_r400_linux_marlboro
```

```
DB split changes, LEDA fixes, other fixes, yadda, yadda, yadda.

Change 99567 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

fix to properly stall on quad rtr == 0 from sx

Change 99562 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

More missing files! doooh 2!

Change 99546 on 2003/05/07 by mzini@mzini_crayola_linux_orl

 Added vccc signals to testbench

Change 99545 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

Signal renaming.  Paul Mitchell's fix.

Change 99543 on 2003/05/07 by rmanapat@rmanapat_r400_sun_marlboro

Fixed a sector mask generation problem for formats 55 and 56

Change 99542 on 2003/05/07 by kevino@kevino_r400_linux_marlboro

  New sector walker files.  Don't meet timing so need to break into 2 stages

Change 99531 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

New DB block Part I.  Still renaming a couple of signals.

Change 99528 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Parameterize # of SP's on instantiation of vc.v.

Change 99527 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Parameterize # of SP's (# of valids and indices)

Change 99524 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Leda clean up.
 Parameterize # of SP's.

Change 99522 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl

Add defines for parameterization of # of SP's.

Change 99521 on 2003/05/07 by jbrady@jbrady_crayola_linux_orl
```

```
Add ifdef's around SP2 and SP3 input ports for 8 and 12 pipe versions.

Change 99520 on 2003/05/07 by mmang@mmang_crayola_linux_orl

Bug occurred where first_in_clause was getting lost when instr_queue
was full.  Previously, internal first_in_clause register was cleared
with tif_rts.  Had to delay clearing to tif_rts & tiq_rtr.

Change 99519 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

Fixed names in dependencies

Change 99517 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

Old unused file.  renamed 96_128

Change 99516 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

Old unused file.

Change 99515 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

New files, but some signals need to be updated.

Change 99506 on 2003/05/07 by jayw@jayw_r400_linux_marlboro

New Depth Files Part I

Change 99505 on 2003/05/07 by smburu@smburu_r400_sun_marlboro

Put in the dependencies for tpc.

Change 99499 on 2003/05/07 by bhankins@bhankins_crayola_linux_orl

update to support running fast via RUN_MAX_SPEED parameter

Change 99428 on 2003/05/06 by tien@tien_r400_devel_marlboro

More aniso fixes and a fix for 2D 1555 mode

Change 99405 on 2003/05/06 by rmanapat@rmanapat_r400_sun_marlboro

More fixes to the pitch determination for linear requests...

Change 99403 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.
```

Change 99402 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99400 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99399 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99398 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99397 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

Put 'u' before instance name.

Change 99396 on 2003/05/06 by jayw@jayw_r400_linux_marlboro

put 'u' before instance names.

Change 99378 on 2003/05/06 by ygiang@ygiang_r400_linux_marlboro

added: perf signals

Change 99377 on 2003/05/06 by ygiang@ygiang_r400_linux_marlboro

added: rb perfcounters for depth flushes/fills and color reads/writes

Change 99374 on 2003/05/06 by bhankins@bhankins_crayola_linux_orl

Include support to send indices to sx one per clock. Enabled via parameter.

Change 99373 on 2003/05/06 by smburu@smburu_r400_sun_marlboro

Some changes to test module names.

Change 99370 on 2003/05/06 by bhankins@bhankins_crayola_linux_orl

add check for data send signals going unknown

Change 99353 on 2003/05/06 by tien@tien_r400_devel_marlboro

Misc aniso fixes

```
Change 99347 on 2003/05/06 by paulv@paulv_r400_linux_marlboro

Added RBM performance signals.

Change 99346 on 2003/05/06 by mmang@mmang_crayola_linux_orl

Fixed bug (I created) related to initializing the constant address
register valids at the beginning of a clause.  I used ais_init_pred
which in some cases was too late.  Created new ais_init_const_addr
that is 3 clocks sooner.

Change 99343 on 2003/05/06 by smburu@smburu_r400_linux_marlboro

Changes to tpc_fifo ram.

Change 99315 on 2003/05/06 by vromaker@vromaker_r400_linux_marlboro

fixed typos that were causing cp_e2polyscanlines_simple to fail

Change 99311 on 2003/05/06 by paulv@paulv_r400_linux_marlboro

Timing fix.  Address calc modules are now 3 cycles long.

Change 99309 on 2003/05/06 by smburu@smburu_r400_linux_marlboro

New test hook-up and Virage hook-up.

Change 99307 on 2003/05/06 by smburu@smburu_r400_linux_marlboro

Changed ram to a cm4 type.

Change 99306 on 2003/05/06 by smburu@smburu_r400_linux_marlboro

Changed ram from 24X86cm1 to 32x87cm1.

Change 99293 on 2003/05/06 by subad@subad_r400_linux_marlboro

first try for ftfconv-rfconv-dgmm timing fix

Change 99253 on 2003/05/05 by cbrennan@cbrennan_r400_linux_marlboro

Probe filter and TPC data area reduction and cleanup.

Change 99252 on 2003/05/05 by cbrennan@cbrennan_r400_linux_marlboro

Added leda make targets.  outputs to leda_results.txt
```

```
Change 99236 on 2003/05/05 by vbhatia@vbhatia_r400_linux_marlboro

Added a lot of new gen tests towards comprehensive test coverage.
Also updated test bench for interface changes

Change 99221 on 2003/05/05 by grayc@grayc_crayola2_linux_orl

   changes for ncsim compile

Change 99205 on 2003/05/05 by nkociuk@nkociuk_r400_linux_marl

add wires for future perfmon use...

Change 99198 on 2003/05/05 by paulv@paulv_r400_linux_marlboro

LEDA fix.

Change 99192 on 2003/05/05 by subad@subad_r400_linux_marlboro

removed dxtc interpolation when degamma is enabled.
       Fixed mutlicycle data

Change 99183 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl

First check-in of common file with vc defines and parameters.

Change 99182 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl

Add set conflict detection and serialization.
 Fix RG_RP_L2a_null_request pipeline typo.

Change 99180 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl

Set next_vertex_pair_mask to 0 in the case where no indices in the group of 16
 were valid. This indicates a null request gets sent down the L2 fifo.

Change 99179 on 2003/05/05 by jbrady@jbrady_crayola_linux_orl

Prevent x's from propagating through dw_addr or spans_banks into the tag valids by
 or'ing with vertex valid at the output of the module.

Change 99176 on 2003/05/05 by rmanapat@rmanapat_r400_sun_marlboro

Fix for format 26 and 37 2d linear formats
fix for 2d linear texture base address calcs as well

Change 99175 on 2003/05/05 by wlawless@wlawless_r400_linux_marlboro
```

```
Blocked ld_p2 from comming on if a freeze_on_ms_allocate, 2 cache line loaded with the
same
address..........

Change 99173 on 2003/05/05 by smburu@smburu_r400_linux_marlboro

TCM new test hook-up and virage hook-up.

Change 99169 on 2003/05/05 by paulv@paulv_r400_linux_marlboro

HiZ/HiS fixes.

Change 99166 on 2003/05/05 by nkociuk@nkociuk_r400_linux_marl

change to account for skid words when counting fifo "full" condition

Change 99149 on 2003/05/05 by smburu@smburu_r400_linux_marlboro

Error in awt connection.

Change 99145 on 2003/05/05 by johnchen@johnchen_r400_linux_marlboro

fix for a quaddata synchronization problem when surface is enabled and z and s are
enabled

Change 99134 on 2003/05/05 by viviana@viviana_crayola2_syn

Rebuilt the memories with 444 Mhz and Virage/3300 compiler.  Also, added
   sc_rf_awt_gate.v to sc.v for test purposes.

Change 99129 on 2003/05/05 by viviana@viviana_crayola2_syn

Rebuilt the memories using Virage/3300 compiler and 444 Mhz.  Added pa_rf_awt_gate.v
   instantiated at the pa.v level and used for test purposes.

Change 99123 on 2003/05/05 by rramsey@rramsey_crayola_linux_orl

Add some control to hold off inputs at vs/ps done events
Increase utb_tp_req_fifo depth
Change writes into vtx/pix done fifos so they only happen on the first
draw_init for a context

Change 99118 on 2003/05/05 by rmanapat@rmanapat_r400_sun_marlboro

Fixed a sensetivity list issue when I changed a case statment

Change 99116 on 2003/05/05 by wlawless@wlawless_r400_linux_marlboro
```

Change to the fragment cache flush, needed to jump back if nothing to flush

Change 99106 on 2003/05/05 by smburu@smburu_r400_linux_marlboro

New dependency tcf_rf_awt_gate.v

Change 99105 on 2003/05/05 by smburu@smburu_r400_linux_marlboro

TCF new test hook-up plus virage hook-up.

Change 99104 on 2003/05/05 by kevino@kevino_r400_linux_marlboro

Simplified fetch_gen_out. mh_arb can acept requests from both fg pipes at ocne, so no need to arbitrate in fetch_gen_out. Make it a per-pipe block and put it inside fetch_gen_pipe. Also, change fg->mh_arb interface to be a normal rts/rtr so the skid buffer is not needed.

Change 99089 on 2003/05/05 by bhankins@bhankins_crayola_linux_orl

update

Change 99088 on 2003/05/05 by bhankins@bhankins_crayola_linux_orl

updates

Change 99085 on 2003/05/05 by jayw@jayw_r400_linux_marlboro

Creating DB directory.

Change 99081 on 2003/05/05 by rmanapat@rmanapat_r400_sun_marlboro

Missing some signals on the sensativity list for the create_valid module
added the use of x_clamp and y_clamp and linear mip pitches

Change 99067 on 2003/05/05 by paulv@paulv_r400_linux_marlboro

AB moved back into the RB.

Change 99058 on 2003/05/05 by viviana@viviana_crayola2_syn

New module added to vgt.v for test purposes.

Change 99057 on 2003/05/05 by viviana@viviana_crayola2_syn

New version of the virage compiler was received and memories were rebuilt.
Also, a new module was added at the top level called vgt_rf_awt_gate.v for
test purposes.

```
Change 99056 on 2003/05/05 by smburu@smburu_r400_linux_marlboro

New test hook-up scheme, plus virage hook-up.

Change 99043 on 2003/05/05 by vromaker@vromaker_r400_linux_marlboro

- added VC ctl flow seq, instr fetch, instr que and instr seq, and top level IOs
- made some leda fixes
- added non time multiplexed gpr write address output to VC and TP (gpr_dst_addr[6:0])

Change 99041 on 2003/05/05 by rramsey@RRAMSEY_P4_r400_win

Regression results from 5/4/03
3451 tests: 66% Pass, 12% Fail, 23% incomplete

Change 98997 on 2003/05/04 by smoss@smoss_crayola_linux_orl_regress

   dos2unix

Change 98995 on 2003/05/04 by johnchen@johnchen_r400_linux_marlboro

perf counter stuff

Change 98990 on 2003/05/04 by rramsey@rramsey_crayola_unix_orl

Fix for stipple when a real-time prim breaks in as one prim
is finishing, and a stippled line is sitting in the front
stage of the walker

Change 98936 on 2003/05/02 by mzini@mzini_crayola_linux_orl

Fixed tag gen

Change 98935 on 2003/05/02 by mzini@mzini_crayola_linux_orl

Only check valid transfers on trackers

Change 98920 on 2003/05/02 by vbhatia@vbhatia_r400_linux_marlboro

updated gen104 behaviour and a whole bunch of changes towards multi channel support

Change 98910 on 2003/05/02 by johnchen@johnchen_r400_linux_marlboro

fix for quaddata update

Change 98906 on 2003/05/02 by tien@tien_r400_devel_marlboro

aniso fixes
```

```
Change 98898 on 2003/05/02 by mzini@mzini_crayola_linux_orl

Added trackers for all the VC_RG outputs

Change 98893 on 2003/05/02 by jbrady@jbrady_crayola_linux_orl

qualify conflict_serialization assignment with vcrg3_ready

Change 98892 on 2003/05/02 by jbrady@jbrady_crayola_linux_orl

First check in of vcrg.

Change 98891 on 2003/05/02 by jbrady@jbrady_crayola_linux_orl

First check in of address generator.

Change 98867 on 2003/05/02 by johnchen@johnchen_r400_linux_marlboro

fix for subnormal 24 float numbers

Change 98861 on 2003/05/02 by smoss@smoss_crayola_linux_orl_regress

   more sq stuff

Change 98836 on 2003/05/02 by subad@subad_r400_linux_marlboro

fix for fmt 54. gen20 passes!

Change 98835 on 2003/05/02 by rmanapat@rmanapat_r400_sun_marlboro

Changed how ld tl tr mapping is done now the tr request also depends
on the coord_incr_x wether it is a oo,oe,eo or a ee type

Change 98834 on 2003/05/02 by smburu@smburu_r400_linux_marlboro

New ports on tc_cg.v

Change 98818 on 2003/05/02 by smoss@smoss_crayola_linux_orl_regress

   added missing dump

Change 98813 on 2003/05/02 by tien@tien_r400_devel_marlboro

Aniso fix to comp_lod

Change 98793 on 2003/05/02 by rramsey@rramsey_crayola_linux_orl
```

```
Check in Dan's fixes for the control flow trackers
Turn internal trackers back on in tb_sqsp

Change 98792 on 2003/05/02 by smburu@smburu_r400_sun_marlboro

Changes to support 2 STAR procs. in TCM.

Change 98781 on 2003/05/02 by subad@subad_r400_linux_marlboro

fix for fmt55. gen19 passes!

Change 98775 on 2003/05/02 by paulv@paulv_r400_linux_marlboro

Fixed decode of hier_stencil_enable.

Change 98774 on 2003/05/02 by kevino@kevino_r400_linux_marlboro

       changed mt_tc_info to 27 bits from 33.

Change 98773 on 2003/05/02 by mmang@mmang_crayola_linux_orl

1.  Added constant address register valids to validate the
    address register data.  The valid is set when address register
    is written.  If valid is not set, sequencer will not waterfall
    those vertices or pixels.  This disables waterfalling for
    predicated off writes and improperly initialized contant
    address registers.
2.  Fixed bug in sqs_alu_instr_seq for phase 3 snooping of
    constant address registers bus.  Previously, this snooping
    did not account for predication of those registers.
3.  Fixed bug where ais_load_done_bits was not hooked up.  This
    signal disables previous vector/scalar management which needs
    to be turned off during constant waterfalling.  With bug,
    pvps logic went unknown which caused unknowns to eventually
    propagate in and out of the gprs.
4.  Fixed bug where non-optimized offset was not being determined
    properly.  non_opt_offset is determined by a priority encoder
    of p0_done, p1_done, p2_done, and p3_done.
5.  With advent of constant address register valids, created
    waterfall_active_q to properly init and avoid re-initing of
    different pixel and vertex done bits.

Change 98768 on 2003/05/02 by paulv@paulv_r400_linux_marlboro

Code optimization.

Change 98765 on 2003/05/02 by subad@subad_r400_linux_marlboro
```

```
fix for dxn. Changed rf replicate to fill with 0's. gen18 passes!

Change 98757 on 2003/05/02 by mzini@mzini_crayola_linux_orl

 Added vc and tb_vc structures to parts_lib

Change 98750 on 2003/05/02 by viviana@viviana_crayola2_syn

Memory increased from 48x155 to 48x170.

Change 98690 on 2003/05/01 by tien@tien_r400_devel_marlboro

cleaned up IO

Change 98686 on 2003/05/01 by subad@subad_r400_linux_marlboro

fix for last signal

Change 98680 on 2003/05/01 by rmanapat@rmanapat_r400_sun_marlboro

Added debug comment that prints out a error if there is a bad req from the TP to the TC

Change 98675 on 2003/05/01 by vbhatia@vbhatia_r400_linux_marlboro

updated multicycling for gen101

Change 98671 on 2003/05/01 by paulv@paulv_r400_linux_marlboro

Fixed valids.

Change 98668 on 2003/05/01 by rmanapat@rmanapat_r400_sun_marlboro

Added some debug stuff to detect when a bad TP to TC request has occured

Change 98654 on 2003/05/01 by johnchen@johnchen_r400_linux_marlboro

update inflight correctly

Change 98652 on 2003/05/01 by vbhatia@vbhatia_r400_linux_marlboro

Update cycle multiplier handling for the tcd emu according to recent spec change

Change 98606 on 2003/05/01 by cbrennan@cbrennan_r400_linux_marlboro

Deleted tc_tca_create_coord.v as it is unused.

Change 98577 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress
```

```
   reverting changes due to over-engineered process

Change 98576 on 2003/05/01 by nkociuk@nkociuk_r400_linux_marl

perfmon updates..

Change 98572 on 2003/05/01 by jayw@jayw_r400_linux_marlboro

Timing fix for Hamid.

Change 98571 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress

   sometime it helps when you save the file first

Change 98569 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress

   added FSDB_DUMP option for VCS

Change 98552 on 2003/05/01 by nkociuk@nkociuk_r400_linux_marl

perfmon updates...

Change 98543 on 2003/05/01 by bhankins@fl_bhankins_r400_win

increase depth of vgt_to_ccgen fifo to 24

Change 98538 on 2003/05/01 by subad@subad_r400_linux_marlboro

fix for format 26. gen21 passes!

Change 98528 on 2003/05/01 by subad@subad_r400_linux_marlboro

fix for hicolor formats and vertical half

Change 98509 on 2003/05/01 by smoss@smoss_crayola_linux_orl_regress

   removed tb_sqsp

Change 98495 on 2003/05/01 by wlawless@wlawless_r400_linux_marlboro

Slight change to how the ms_lock probes are calculated...

Change 98470 on 2003/05/01 by johnchen@johnchen_r400_linux_marlboro

some bug fixes

Change 98462 on 2003/05/01 by vromaker@vromaker_r400_linux_marlboro
```

```
- added bits and re-arranged the order of bits in the status register
- added VC support in thread buffers (vc request from status register,
  read muxes, connections to other modules, etc.)
- removed is_subphase and made is_phase 3 bits
- removed cfc_phase
- expanded state_read_phase to 2 bits
- changed the strapping and phase relationships on the ctl flow seqs
- SQ_SP_fetch_swizzle and SQ_SP_fetch_resource outputs added
- disabled internal SQ trackers and changed to DEBUG_PRINT ifdef in tb_sqsp.v

Change 98461 on 2003/05/01 by rramsey@RRAMSEY_P4_r400_win

fixes for some of the non-context based sc perfcounters

Change 98443 on 2003/05/01 by markf@markf_r400_linux_marlboro

Doubled write ports for request queues in the TC memory request interface

Change 98418 on 2003/04/30 by nkociuk@nkociuk_r400_linux_marl

fixed typo...

Change 98398 on 2003/04/30 by smoss@smoss_crayola_linux_orl_regress

   new sq stuff

Change 98397 on 2003/04/30 by grayc@grayc_crayola2_linux_orl

   new tb

Change 98396 on 2003/04/30 by grayc@grayc_crayola2_linux_orl

   new testbench

Change 98395 on 2003/04/30 by grayc@grayc_crayola2_linux_orl

   new testbench

Change 98392 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

Module compiler area reductions and some minor fixes.

Change 98387 on 2003/04/30 by jayw@jayw_r400_linux_marlboro

moved rb_rbd_quad_address_calc from depth into color for DB split.renamed bus for sx
index reads

Change 98369 on 2003/04/30 by subad@subad_r400_linux_marlboro
```

fix for dxt4. gen18 passes!

Change 98367 on 2003/04/30 by rramsey@rramsey_crayola_linux_orl

these trackers were looking at the wrong register stage to determine
thread_id and thread_type

Change 98361 on 2003/04/30 by subad@subad_r400_linux_marlboro

fix for dxt2

Change 98356 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Chnaged the way number_of_total_access_q was calculated. It replaces 4 cascading adders

Change 98343 on 2003/04/30 by ashishs@fl_ashishs_r400_win

Correcting an error from script since it wasn't updating the user's comments and locked
by user correctly. Also adding an empty XLS file which is used by the script to add and
merge data

Change 98340 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

For data going to tile block, since multisample read data has the same tag, the send
back to tile is not active when multisample data is being returned from the MC.

Change 98326 on 2003/04/30 by jayw@jayw_r400_linux_marlboro

fixed makefile

Change 98307 on 2003/04/30 by ashishs@fl_ashishs_r400_win

fixed a small error in the script because of which it wasnt getting the comments from
the report. Also updated some comments.

Change 98304 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

LEDA fix.

Change 98302 on 2003/04/30 by subad@subad_r400_linux_marlboro

fix for fmt 48. gen17 passes!

Change 98297 on 2003/04/30 by paulv@paulv_r400_linux_marlboro

Fixed probe flush logic.

```
Change 98289 on 2003/04/30 by subad@subad_r400_linux_marlboro

fix for fmt 45. gen15 passes.

Change 98287 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Replaced 128x96 RAM with 96x128

Change 98283 on 2003/04/30 by viviana@viviana_crayola2_syn

Files no longer used in the SQ.

Change 98279 on 2003/04/30 by rmanapat@rmanapat_r400_sun_marlboro

Moved a debug counter from the TCF to the TCR

Change 98274 on 2003/04/30 by rramsey@rramsey_crayola_linux_orl

change if(`DEBUG_PRINT) to `ifdef DEBUG_PRINT so trackers
work at gc level

Change 98267 on 2003/04/30 by smburu@smburu_r400_sun_marlboro

NO_CONNECT on a new tc_cg port.

Change 98266 on 2003/04/30 by smburu@smburu_r400_sun_marlboro

NO_CONNECT on a new tc_cg port.

Change 98262 on 2003/04/30 by smburu@smburu_r400_sun_marlboro

New port to support TCM.

Change 98261 on 2003/04/30 by ashishs@fl_ashishs_r400_win

added the script for updating the XLS hadware regression data. Can have more
enhancements depending on requirements

Change 98260 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Replaced 128x96 (incoorect naming) with 96x128

Change 98256 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Replaces the 128x96 RAM with 96x128 used in  rb_rbd_cache_ram.v

Change 98254 on 2003/04/30 by hmonsef@hmonsef_r400_linux_marlboro_rbrc
```

```
The RAM in access_fifo was changed from 8x131 to 8x136. Spare RAM bits are provided for
future use

Change 98186 on 2003/04/29 by tien@tien_r400_devel_marlboro

Fixes

Change 98172 on 2003/04/29 by kevino@kevino_r400_linux_marlboro

      Replace per-TP tc_tp_send with a single TCO_TPC_send

Change 98171 on 2003/04/29 by subad@subad_r400_linux_marlboro

fix for sa3 formats. sa3 is like two layer formats and has sector dependency.
       Since there are outputs with both sector and srcaddr dependency, added srcaddr
       dependency for all cases

Change 98147 on 2003/04/29 by cbrennan@cbrennan_r400_linux_marlboro

Replicated stall flop to a vector to help with the timing of the fanout.

Change 98146 on 2003/04/29 by cbrennan@cbrennan_r400_linux_marlboro

Moved hit/miss bit to previous stage for timing.

Change 98145 on 2003/04/29 by johnchen@johnchen_r400_linux_marlboro

fix for backfacing

Change 98144 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

Add internal trackers to tb_sqsp, clean up memory files listed in tb.f
Remove DEBUG_PRINT from tb.f, it should be specified in vcsopts.f

Change 98142 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

timing fix for rbi_addr

Change 98140 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

fix a typo in a signal path

Change 98132 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

update trackers for new fields in dump files and make them
work for events

Change 98122 on 2003/04/29 by rmanapat@rmanapat_r400_sun_marlboro
```

```
Fixes for various formats for 3d tiled tc_simple_3d tests

Change 98115 on 2003/04/29 by nkociuk@nkociuk_r400_linux_marl

bring tcr rbbm signals to top level, left unconnected to readback daisy chain for now

Change 98095 on 2003/04/29 by kevino@kevino_r400_linux_marlboro

      was taking 9 dwords from data/write enable, instead of 8

Change 98091 on 2003/04/29 by bhankins@bhankins_crayola_linux_orl

add mechanism to throttle tbmod_fake_int from initiating reads to parameter cache lines
that have
   not yet been written to.

Change 98079 on 2003/04/29 by rramsey@rramsey_crayola_linux_orl

Fix a bug with alu1's trigger
Add define control for comment printing

Change 98067 on 2003/04/29 by danh@danh_crayola_linux_orl

Made type_serialize_1 and vc_request_1 changes.

Change 98066 on 2003/04/29 by paulv@paulv_r400_linux_marlboro

LEDA fixes, timing fixes and logic fixes (oh my).

Change 98047 on 2003/04/29 by vbhatia@vbhatia_r400_linux_marlboro

few updates for pipeline changes in hardware and added a bunch of tests

Change 98046 on 2003/04/29 by danh@danh_crayola_linux_orl

Initial release.

Change 98041 on 2003/04/29 by bhankins@bhankins_crayola_linux_orl

init file done signal

Change 98034 on 2003/04/29 by bhankins@bhankins_crayola_linux_orl

remove reset of 'done' signal.  the signal should be initialized only
   by the InitVec call.

Change 98018 on 2003/04/28 by jayw@jayw_r400_linux_marlboro
```

```
LEDA fixes and removed 96x96

Change 98017 on 2003/04/28 by vbhatia@vbhatia_r400_linux_marlboro

Few updates to handle grad_exp_adjust_h and _v added to hardware

Change 98008 on 2003/04/28 by vbhatia@vbhatia_r400_linux_marlboro

updated to test all cases of sector address

Change 98001 on 2003/04/28 by tien@tien_r400_devel_marlboro

Fixed MAX clamp on fast_sun_dni
Added exp adjust ports to deriv and tp_input

Change 97997 on 2003/04/28 by cbrennan@cbrennan_r400_linux_marlboro

LEDA Error cleanup

Change 97992 on 2003/04/28 by dougd@dougd_r400_linux_marlboro

fixed some Leda reported problems

Change 97991 on 2003/04/28 by dougd@dougd_r400_linux_marlboro

added R500 dual read ports and extra memories.

Change 97989 on 2003/04/28 by johnchen@johnchen_r400_linux_marlboro

add reg_state signal

Change 97962 on 2003/04/28 by danh@danh_crayola_linux_orl

Made signal changes in regards to .dmp file changes.

Change 97961 on 2003/04/28 by danh@danh_crayola_linux_orl

Made signal name changes in regards to .dmp file changes.

Change 97958 on 2003/04/28 by danh@danh_crayola_linux_orl

Made signal changes in regards to the .dmp file changes.

Change 97956 on 2003/04/28 by danh@danh_crayola_linux_orl

Added jump_call_addr registers.
```

```
Change 97944 on 2003/04/28 by rmanapat@rmanapat_r400_sun_marlboro

Fixed a error that was affecting 2d linear tests
Fixed a sector gen problem for format 0x02 3d tiled
fixed a slice problem for cacheline 8 involvind 32 bpp 3d

Change 97943 on 2003/04/28 by subad@subad_r400_linux_marlboro

fix for fmt 39 and 40. gen11 now passes!

Change 97942 on 2003/04/28 by johnchen@johnchen_r400_linux_marlboro

fix memory return validation problem

Change 97901 on 2003/04/28 by kevino@kevino_r400_linux_marlboro

  LEDA fix : some ports defined multiple times in port list

Change 97897 on 2003/04/28 by subad@subad_r400_linux_marlboro

added two files and changed one file name

Change 97892 on 2003/04/28 by danh@danh_crayola_linux_orl

       no changes made.

Change 97882 on 2003/04/28 by kevino@kevino_r400_linux_marlboro

   Script to run leda on the TCB

Change 97880 on 2003/04/28 by kevino@kevino_r400_linux_marlboro

    Added log2_sec_pitch parameter

Change 97879 on 2003/04/28 by kevino@kevino_r400_linux_marlboro

     TCO stall condition logic incorrect, so wasn't stalling when it was supposed to.

Change 97861 on 2003/04/28 by bhankins@bhankins_crayola_win_orl

update after junk submit

Change 97860 on 2003/04/28 by bhankins@bhankins_crayola_win_orl

junk submit to get perforce gui in sync after samba put back on line.

Change 97758 on 2003/04/25 by tien@tien_r400_devel_marlboro
```

LEDA changes

Change 97732 on 2003/04/25 by danh@danh_crayola_linux_orl

Changed signal names per sq_pix_control_flow_alu.dmp

Change 97717 on 2003/04/25 by johnchen@johnchen_r400_linux_marlboro_rbrc

no fixes...just make it look better

Change 97708 on 2003/04/25 by rramsey@rramsey_crayola_linux_orl

Move inc for event thread count to front of event fifo
They were still happening on the same clk as real threads

Change 97702 on 2003/04/25 by subad@subad_r400_linux_marlboro

fix for yuv formats 11 and 12. gen10 now passes

Change 97685 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

Going back to version 38.

Change 97681 on 2003/04/25 by wlawless@wlawless_r400_linux_marlboro

read pending in frag cache, and 2k crossing..

Change 97670 on 2003/04/25 by rramsey@rramsey_crayola_linux_orl

Change buildtb and buildkdb to use tb.f for libraries and compile options
to keep from having to add files in two places
Couple of bug fixes/enhancements for tb_sqsp
Fix path define for sp_macc tracker when running tb_sqsp

Change 97664 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

Comments. Removed unnecessary sx fifo count.

Change 97654 on 2003/04/25 by tien@tien_r400_devel_marlboro

Added some parms, so refreshed .bvrls
Removed some obsolete code from tp_addresser
Started to fix tp_lod_aniso, but realized I still have questions about it

Change 97653 on 2003/04/25 by rmanapat@rmanapat_r400_sun_marlboro

Getting rid of a file that will be generated by the tb

Change 97645 on 2003/04/25 by bhankins@bhankins_crayola_linux_orl

misc fixes

Change 97643 on 2003/04/25 by subad@subad_r400_linux_marlboro

fix for DXT1 test gn100

Change 97635 on 2003/04/25 by vbhatia@vbhatia_r400_linux_marlboro

expanded gen* test cases to gen0 to gen23, gen100 to gen105 to separate some tests for ease of debug. Also added seeded random, and enhanced help menu.

Change 97634 on 2003/04/25 by subad@subad_r400_linux_marlboro

fixed fmt00 and 01 and the "valid staying high" issue in
tcd_ipbuf.v

Change 97620 on 2003/04/25 by johnchen@johnchen_r400_linux_marlboro_rbrc

wait for the cacheline to be filled up even when detail_mask is zero

Change 97601 on 2003/04/25 by johnchen@johnchen_r400_linux_marlboro_rbrc

stencil fixes for random

Change 97594 on 2003/04/25 by smburu@smburu_r400_sun_marlboro

Virage Hook-up.

Change 97580 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

LEDA fixes.

Change 97575 on 2003/04/25 by wlawless@wlawless_r400_linux_marlboro

a more "BETTER" way to check for 2k boundary crossing to skip over AB or CD banks.... nice english!!!

Change 97567 on 2003/04/25 by smburu@smburu_r400_sun_marlboro

New TCF virage files.

Change 97562 on 2003/04/25 by jayw@jayw_r400_linux_marlboro

More LEDA fixes.

Change 97548 on 2003/04/25 by askende@askende_r400_linux_marlboro

```
modified the PRED instructions to match the new definition. Src.W channel is now used
instead of Src.X

Change 97540 on 2003/04/24 by vbhatia@vbhatia_r400_linux_marlboro

update for degamma change to tcd hw

Change 97538 on 2003/04/24 by ygiang@ygiang_r400_pv2_marlboro

added: more sq perf counters

Change 97521 on 2003/04/24 by subad@subad_r400_linux_marlboro

fixes for fmt 00 and 01
       fixed data in opfsm

Change 97512 on 2003/04/24 by paulv@paulv_r400_linux_marlboro

The valid, last_quarter_tile and associated cacheline signals
going into the calc_new_tile module were off by a cycle.  Fixed.

Change 97503 on 2003/04/24 by sallen@sallen_r400_lin_marlboro

   ferret: ferret now reads either a single or multi fill file (based on environment
variable)
           TP_TC comparitor bits for sec_pitch corrected
           a few nsim fixes
           comparitor cleanups
           auto build of tc files needed
           error cnt check removed from ferret.cpp

Change 97498 on 2003/04/24 by kevino@kevino_r400_linux_marlboro

   MH_TC0_rtr was going where TC1 was supposed to go

Change 97487 on 2003/04/24 by rmanapat@rmanapat_r400_sun_marlboro

fixed 00 wher it should have been OO fixed my 3d linear eqs
and clamp height to 32 when it is 32 or lower

Change 97458 on 2003/04/24 by johnchen@johnchen_r400_linux_marlboro_rbrc

stall event flush to color block until depth block finishes flushing

Change 97432 on 2003/04/24 by nkociuk@nkociuk_r400_linux_marl

removing unused clk pin to get rid of leda warnings
```

```
Change 97402 on 2003/04/24 by kmeekins@kmeekins_crayola_linux_orl

Initial release.
  Tracker used to test the inputs and outputs of all MACC units within the shader
pipes.

Change 97401 on 2003/04/24 by johnchen@johnchen_r400_linux_marlboro_rbrc

LEDA fixes

Change 97399 on 2003/04/24 by tien@tien_r400_devel_marlboro

Updated pipeline lengths

Change 97395 on 2003/04/24 by wlawless@wlawless_r400_linux_marlboro

Set valid on both 1/2's of the cache line when in multisample...

Change 97394 on 2003/04/24 by subad@subad_r400_linux_marlboro

removed the tco_info related signals from tcd instantiation

Change 97392 on 2003/04/24 by kevino@kevino_r400_linux_marlboro

       Made changes for TC_MH rtr updates

Change 97378 on 2003/04/24 by vbhatia@vbhatia_r400_linux_marlboro

Few updates

Change 97370 on 2003/04/24 by subad@subad_r400_linux_marlboro

done coding the degamma multicycling fixes, compiles and ran leda

Change 97368 on 2003/04/24 by jayw@jayw_r400_linux_marlboro

LEDA fixes

Change 97366 on 2003/04/24 by nkociuk@nkociuk_r400_linux_marl

interim checkin...

Change 97365 on 2003/04/24 by nkociuk@nkociuk_r400_linux_marl

bring out fetch_gen perfmon signals

Change 97346 on 2003/04/24 by kevino@kevino_r400_linux_marlboro
```

```
    Some PM changes required the regen of these files

Change 97323 on 2003/04/24 by tien@tien_r400_devel_marlboro

Fixes for 32_32_32_32_float

Change 97285 on 2003/04/23 by subad@subad_r400_linux_marlboro

continuing fixes for dxtc

Change 97281 on 2003/04/23 by johnchen@johnchen_r400_linux_marlboro_rbrc

stall the tile side if the probe side is not quite ready

Change 97256 on 2003/04/23 by nkociuk@nkociuk_r400_linux_marl

get rid of unneeded include

Change 97253 on 2003/04/23 by nkociuk@nkociuk_r400_linux_marl

updates...

Change 97244 on 2003/04/23 by wlawless@wlawless_r400_linux_marlboro

Fixed 1713 with a block quad in fifo if it a event

Change 97218 on 2003/04/23 by jayw@jayw_r400_linux_marlboro

fix include missing, and removed ab

Change 97205 on 2003/04/23 by askende@askende_r400_linux_marlboro

1. fix to allow src (argument a)  to be written back to the GPRs when doing a MOVA
       2. modified the 4 LSBs of the autocount bus to use the SPI block id as supposed
to SP block id + vector unit id

Change 97201 on 2003/04/23 by paulv@paulv_r400_linux_marlboro

Fixed interpretation of x to mean the quad (little endian), not the pixel (big endian).

Change 97186 on 2003/04/23 by kevino@kevino_r400_linux_marlboro

    Removed port sizes from port list.  They were in there inadvertantly from a cut and
paste-  and were causing some cadence tool problems

Change 97182 on 2003/04/23 by nkociuk@nkociuk_r400_linux_marl
```

```
checkpoint check-in...

Change 97173 on 2003/04/23 by kevino@kevino_r400_linux_marlboro

   More leda fixes

Change 97170 on 2003/04/23 by johnchen@johnchen_r400_linux_marlboro_rbrc

some random fixes, timing fixes

Change 97162 on 2003/04/23 by nkociuk@nkociuk_r400_linux_marl

l2 cache-related perfmon updates

Change 97152 on 2003/04/23 by dougd@dougd_r400_linux_marlboro

added logic to control vtx perf counters to sq_vtx_ctl.v and sq.v; fixed bug in write
logic in sq_aluconst_wrt_buf.v

Change 97150 on 2003/04/23 by bhankins@bhankins_crayola_linux_orl

Update SX trackers to do a better job of helping to check for incomplete tests.
   File streams are now opened only if they are needed in a particular test.  Each
   file stream that is opened must be fully consumed.  Each tracker also outputs a
   "tracker_done" signal indicating that all opened streams have been consumed.

Change 97144 on 2003/04/23 by wlawless@wlawless_r400_linux_marlboro

small fix for 3 and 6 sample in the cover/overlap logic

Change 97139 on 2003/04/23 by jayw@jayw_r400_linux_marlboro

updates

Change 97113 on 2003/04/23 by jayw@jayw_r400_linux_marlboro

AB removal and LEDA fixes, fix for 3 and 6 sample MSAA.

Change 97095 on 2003/04/23 by kevino@kevino_r400_linux_marlboro

   More leda fixes

Change 97078 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97075 on 2003/04/23 by hmonsef@hmonsef
```

```
Replaced 128x96 with 96x128

Change 97074 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97073 on 2003/04/23 by smburu@smburu_r400_sun_marlboro

      Re-adding the fusebox that must have been deleted by mistake.

Change 97071 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in Depth

Change 97070 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97069 on 2003/04/23 by hmonsef@hmonsef

Replaced 128x96 with 96x128 in depth

Change 97068 on 2003/04/23 by hmonsef@hmonsef

Replaces 128x96 in depth

Change 97067 on 2003/04/23 by hmonsef@hmonsef

Replaces 128x96 in depth

Change 97062 on 2003/04/23 by hmonsef@hmonsef

Replaced 3 RAMs for the tile.

Change 97060 on 2003/04/23 by bhankins@bhankins_crayola_linux_orl

fix to more properly handle the counting of position and pixel buffer free signals
       from the SX.

Change 97030 on 2003/04/22 by subad@subad_r400_linux_marlboro

partially added the multicycling support for 8B degamma

Change 97010 on 2003/04/22 by paulv@paulv_r400_linux_marlboro

Fixed x_sel and y_sel signals.

Change 97008 on 2003/04/22 by paulv@paulv_r400_linux_marlboro
```

```
The AB (alpha blender) has been moved back into the RB as a subblock (RBA).

Change 96996 on 2003/04/22 by rmanapat@rmanapat_r400_sun_marlboro

fix for formats 55 and 56 with regards to MH addr calculation
also added 3d linear address calc to MH addr calculation

Change 96990 on 2003/04/22 by viviana@viviana_crayola2_syn

Ran cover on the sq_rf.cnt to add the new 16x170 and 48x170 memories.

Change 96981 on 2003/04/22 by viviana@viviana_crayola2_syn

Added TST_awt_enable to the interfaces with ss/sq_pix_thread_buff.v and
   ss/sq_vtx_thread_buff.v.
   Replaced the 16x155 and 48x155 memories with 16x170 and 48x170 respectively.
   Replaced the memory to be compiled in buildtb from the 155 to the 170.

Change 96974 on 2003/04/22 by smburu@smburu_r400_sun_marlboro

Makefile for tcb.

Change 96973 on 2003/04/22 by kevino@kevino_r400_linux_marlboro

   accidently had sclk_tc instead of posedge sclk_tc in a clock block.

Change 96971 on 2003/04/22 by kevino@kevino_r400_linux_marlboro

      Fixed some LEDA violations.  Renamed fetch gen to mh arb interface tf instead of
fg (fg is used internally and doesn't necessarily map directly to the output interface)

Change 96959 on 2003/04/22 by johnchen@johnchen_r400_linux_marlboro_rbrc

handful od random fixes

Change 96949 on 2003/04/22 by jayw@jayw_r400_linux_marlboro

LEDA fixes.

Change 96948 on 2003/04/22 by viviana@viviana_crayola2_syn

Changed the name of the FIFO.

Change 96947 on 2003/04/22 by viviana@viviana_crayola2_syn

Removed width from paramenter definitions.
```

```
Change 96946 on 2003/04/22 by viviana@viviana_crayola2_syn

Added done_vector to sensitivity list at line 902.
   Removed `SQ_SRCB_PHASE from sensitivity list at line 1018.
   Added isr_thread_type_q to sensitivity list at line 1233.

Change 96939 on 2003/04/22 by wlawless@wlawless_r400_linux_marlboro

fixed some LEDA things, and got basic_multisample 128x128_4samp working
This was an addressing bug in reading the fragment bit back from the MC

Change 96901 on 2003/04/22 by jayw@jayw_r400_linux_marlboro

LEDA fixes for RC to run clean.

Change 96877 on 2003/04/22 by kevino@kevino_r400_linux_marlboro

 fixed inadvertant "7" at start of file

Change 96876 on 2003/04/22 by rramsey@rramsey_crayola_linux_orl

only compare if one of the vector unit bits is valid

Change 96874 on 2003/04/22 by rramsey@rramsey_crayola_linux_orl

fix for pv/ps swizzling

Change 96868 on 2003/04/22 by kevino@kevino_r400_linux_marlboro

       Some changes to get rid of LEDA warnings

Change 96816 on 2003/04/21 by subad@subad_r400_linux_marlboro

added sector dependency for data and
       generated dgmmen.v from table.txt and table_default.txt

Change 96795 on 2003/04/21 by tien@tien_r400_devel_marlboro

Added ch_dly1 port for TPC to TPs

Change 96794 on 2003/04/21 by tien@tien_r400_devel_marlboro

Port width mismatch fix

Change 96778 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x230
```

```
Change 96776 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x225

Change 96774 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x225

Change 96773 on 2003/04/21 by hmonsef@hmonsef

Repalced 16x225

Change 96772 on 2003/04/21 by hmonsef@hmonsef

Replaced 16x241

Change 96771 on 2003/04/21 by hmonsef@hmonsef

Replaced 32x230

Change 96766 on 2003/04/21 by hmonsef@hmonsef

Changed 3 tiles RAM width

Change 96764 on 2003/04/21 by hmonsef@hmonsef

Changed 3 tiles RAM width

Change 96763 on 2003/04/21 by hmonsef@hmonsef

Chaged 3 Tile RAMs width

Change 96761 on 2003/04/21 by hmonsef@hmonsef

Change 3 Tile RAMs width

Change 96758 on 2003/04/21 by hmonsef@hmonsef

Changed Tile 3 RAMs width

Change 96738 on 2003/04/21 by mmang@mmang_crayola_linux_orl

Fixed bug in sq_ais_output.v related to address register write and
predication.  Fixed a variety of tests to not use uninitialized gpr
or address registers.  2 tests still fail because of previous vector
scalar swizzle bug, 1 test still fails because of MOVA hardware bug, and
1 test still fails because of predicated address register write causes
XXXXXX which causes waterfalling to hang.
```

Change 96719 on 2003/04/21 by smburu@smburu_r400_sun_marlboro

valid_q3 defined twice.

Change 96694 on 2003/04/21 by moev@moev_r400_linux_marlboro

updated files to allow serial test to work.

Change 96688 on 2003/04/21 by tien@tien_r400_devel_marlboro

Refresh tpc MC code

Change 96681 on 2003/04/21 by rmanapat@rmanapat_r400_sun_marlboro

Fixes for TPC data pipe problem

Change 96654 on 2003/04/21 by tien@tien_r400_devel_marlboro

Moved determinant to tp_lod_aniso from tp_ldo_deriv

Change 96646 on 2003/04/21 by kevino@kevino_r400_linux_marlboro

     Fix for SA10, SA11 sectors 6,7 (was a typo) and for SA4, SA5 (was using sect[1] instead of sect[2])

Change 96639 on 2003/04/21 by viviana@viviana_crayola2_syn

Corrected the clock to the Virage memory.

Change 96638 on 2003/04/21 by kevino@kevino_r400_linux_marlboro

      got rid of quad0 in tcm's call inside quad block
      update of tcf_no_tpc.v (not sure what changed- it updated when I ran make tctb)

Change 96635 on 2003/04/21 by smburu@smburu_r400_sun_marlboro

More NO_CONNECTs to tcr_perfmon_wrapper.

Change 96633 on 2003/04/21 by bhankins@bhankins_crayola_linux_orl

remove unused include

Change 96623 on 2003/04/21 by bhankins@bhankins_crayola_linux_orl

add support for including SX units into tb_sqsp.v

Change 96548 on 2003/04/19 by markf@markf_r400_linux_marlboro

Added TC/VC request arbiter (tcb_mh_arb.v)

Change 96534 on 2003/04/18 by johnchen@johnchen_r400_linux_marlboro_rbrc

make sure hiz kills don't get to color

Change 96532 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Fixed the read signal for the detail_fifo.

Change 96529 on 2003/04/18 by vbhatia@vbhatia_r400_linux_marlboro

Added a bunch of directed tests to help debug. Also added lot of randomized tests for added coverage

Change 96526 on 2003/04/18 by johnchen@johnchen_r400_linux_marlboro_rbrc

hiz kill signal added

Change 96523 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Few bug fixes with the tile_killed signaling.

Change 96503 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Now passing a tile_killed signal on the RBT_RBD_* interface.

Change 96497 on 2003/04/18 by hmonsef@hmonsef

Replaced 4 instance of 96x96 with 3 instance of 128x96

Change 96495 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96494 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96492 on 2003/04/18 by hmonsef@hmonsef

Replaces 96x96 RAM

Change 96491 on 2003/04/18 by hmonsef@hmonsef

Replaces 96x96 RAM

```
Change 96490 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96488 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96487 on 2003/04/18 by hmonsef@hmonsef

Replaced 96x96 with 128x96

Change 96484 on 2003/04/18 by wlawless@wlawless_r400_linux_marlboro

Multisample stuff, got 128x128 to pass....

Change 96471 on 2003/04/18 by nkociuk@nkociuk_r400_linux_marl

perfmon updates...

Change 96455 on 2003/04/18 by bhankins@bhankins_crayola_linux_orl

initial checkin to optionally include (not included by default) two SX units
       with associated support logic and trackers.

Change 96448 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Added a signal between RBT and RBD to denote killed tiles.

Change 96445 on 2003/04/18 by rramsey@rramsey_crayola_linux_orl

Move compares into a task, add a flag
to enable marking x vs 0 compares as warnings

Change 96439 on 2003/04/18 by tien@tien_r400_devel_marlboro

New auto-gen'd LUTs

Change 96436 on 2003/04/18 by nkociuk@nkociuk_r400_linux_marl

perfmon updates

Change 96411 on 2003/04/18 by tien@tien_r400_devel_marlboro

LOD fixes

Change 96409 on 2003/04/18 by smburu@smburu_r400_sun_marlboro
```

Some perfmon NO_CONNECTs.

Change 96394 on 2003/04/18 by paulv@paulv_r400_linux_marlboro

Renamed the HiZ tilechecker tile killed signal (from hiz_flightcount_tiledone to hiz_tilecheck_tile_killed) and added hiz_quadcheck_tile_killed (from HiZ quad checker).

Change 96389 on 2003/04/18 by mzini@mzini_crayola_linux_orl

Temporarily removed the checking of control bits until the hardware catches up

Change 96388 on 2003/04/18 by grayc@grayc_crayola2_linux_orl

add new include path

Change 96381 on 2003/04/18 by bhankins@bhankins_crayola_linux_orl

resubmitting changes

Change 96380 on 2003/04/18 by bhankins@bhankins_crayola_linux_orl

changes

Change 96339 on 2003/04/17 by paulv@paulv_r400_linux_marlboro

Fix for the RBT write fifo.

Change 96318 on 2003/04/17 by rramsey@rramsey_crayola_linux_orl

change Openning to Opening

Change 96303 on 2003/04/17 by kevino@kevino_r400_linux_marlboro

Re-submit after automatically making these (with bmake tctb in the tc testbench sim area)

Change 96299 on 2003/04/17 by kevino@kevino_r400_linux_marlboro

Hand edit to add TCA_TCB_sector_format to .v file (tree doesn't wanna build)

Change 96295 on 2003/04/17 by johnchen@johnchen_r400_linux_marlboro_rbrc

major changes: using 3 128x96 rams instead of 4 96x96 rams

Change 96283 on 2003/04/17 by subad@subad_r400_linux_marlboro

added the new changes in degmma and added the flipping

Change 96282 on 2003/04/17 by smburu@smburu_r400_sun_marlboro

tpc Makefile.

Change 96278 on 2003/04/17 by scamlin@scamlin_crayola_unix_orl

.

Change 96254 on 2003/04/17 by bhankins@bhankins_crayola_linux_orl

fix syntax error affecting synthesis

Change 96253 on 2003/04/17 by rmanapat@rmanapat_r400_sun_marlboro

Fixes a error frank found

Change 96252 on 2003/04/17 by rramsey@rramsey_crayola_linux_orl

Add new signal between sq_vtx_ctl and sq_input_arb to mark gpr_ld_busy
which fixes a deadlock condition where gpr_ld state machine is waiting
on an ack from the arb, which is waiting on vsr_ld machine not busy, which
is waiting on the gpr_ld machine to finish.
Add a reset for sp_sel in sq_vtx_ctl when the vsr_ld machine goes from ld
to idle. This is needed if there is valid data sitting in the vgt fifo since
a vsr load will happen on the following clock.
Connect pred_kill_valid bits in tb_sqsp.
Fix typo in visr_wr tracker.

Change 96248 on 2003/04/17 by paulv@paulv_r400_linux_marlboro

Timing fix.

Change 96215 on 2003/04/17 by cbrennan@cbrennan_r400_linux_marlboro

moved sector format calculation back one stage into TCA for timing.

Change 96210 on 2003/04/17 by smburu@smburu_r400_sun_marlboro

Make file for tca.

Change 96193 on 2003/04/17 by bhankins@bhankins_crayola_linux_orl

edits to support the replacement of sx_rb_detailed_quad_data_fifo

Change 96189 on 2003/04/17 by viviana@viviana_crayola_unix_orl

A new memory was added to the sx and all the simulation verilog models were
checked into the test directory.

Change 96187 on 2003/04/17 by bhankins@bhankins_crayola_linux_orl

initial checkin to replace register based fifo with ram based; clone of ati_fifo_top.v

Change 96186 on 2003/04/17 by viviana@viviana_crayola_unix_orl

A new memory was added to the sx (128x104).

Change 96184 on 2003/04/17 by rmanapat@rmanapat_r400_sun_marlboro

Changed some format decodes for formats 0,1,11,12,39,40,44,45

Change 96181 on 2003/04/17 by smburu@smburu_r400_sun_marlboro

Some NO_CONNECT work.

Change 96167 on 2003/04/17 by nkociuk@nkociuk_r400_linux_marl

bring out perfmon signals for read latency fifos

Change 96137 on 2003/04/17 by kevino@kevino_r400_linux_marlboro

  Timing fix for sector gen in tco. Add a register stage between sector gen and cache read.

Change 96104 on 2003/04/16 by cbrennan@cbrennan_r400_linux_marlboro

Timing fix for LRU path.   Does LRU update from both ends of drop list instead of in 4 steps.

Change 96103 on 2003/04/16 by cbrennan@cbrennan_r400_linux_marlboro

Add ping pong buffer between TCA and TCB for timing.

Change 96098 on 2003/04/16 by vbhatia@vbhatia_r400_linux_marlboro

Added more testcases

Change 95985 on 2003/04/16 by nkociuk@nkociuk_r400_linux_marl

misc updates

Change 95961 on 2003/04/16 by jayw@jayw_r400_linux_marlboro

LEDA fixes.

Change 95892 on 2003/04/16 by tien@tien_r400_devel_marlboro

```
More LOD fixes

Change 95884 on 2003/04/16 by smburu@smburu_r400_sun_marlboro

More NO_CONNECT fixes.

Change 95880 on 2003/04/16 by smburu@smburu_r400_sun_marlboro

Took care of some needed NO_CONNECTs.

Change 95859 on 2003/04/16 by rramsey@rramsey_crayola_linux_orl

fix width

Change 95847 on 2003/04/16 by rramsey@rramsey_crayola_linux_orl

script to build the verdi kdb for tb_sqsp

Change 95839 on 2003/04/16 by rramsey@rramsey_crayola_linux_orl

Multiple changes throughout the SQ to get tb_sqsp working, and to fix bugs
uncovered by the new testbench
  sq_gpr_alloc - wrap was broken for vertex side if ptr wrapped exactly at max
  sq_rbbm_interface - context/new_ld sent to constant mems was being pulled from wrong
                      side of skid buffer
  sq_pix_thread_buff - change to send context_done event back to CP on the pixel side
  buildtb, tb_sqsp, tbtrk_* - changes for new sp/spi configuration and new dump file
                              fields

Change 95833 on 2003/04/16 by paulv@paulv_r400_linux_marlboro

Major HiZ rework (equations fixed, some misunderstandings corrected, etc.).  Tests
passing again.

Change 95810 on 2003/04/16 by dougd@dougd_r400_linux_marlboro

fixed bug in the pix_cntx counter increment signal where both event and pix were trying
to increment during the same cycle

Change 95783 on 2003/04/15 by vbhatia@vbhatia_r400_linux_marlboro

Lod aniso standalone testbench

Change 95781 on 2003/04/15 by vbhatia@vbhatia_r400_linux_marlboro

Aniso standalone testbench and few testcases
```

```
Change 95728 on 2003/04/15 by kevino@kevino_r400_linux_marlboro

           Fix for formats 22, and 23.  Updated to new format conversion table (SA0 and
1 in 32BPP instead of sa4 abd 5 in 64BPP)

Change 95727 on 2003/04/15 by kevino@kevino_r400_linux_marlboro

   Fix for formats 22, and 23.  Updated to new format conversion table (SA0 and 1 in
32BPP instead of sa4 abd 5 in 64BPP)

Change 95676 on 2003/04/15 by kevino@kevino_r400_linux_marlboro

  files no longer used

Change 95658 on 2003/04/15 by vbhatia@vbhatia_r400_linux_marlboro

Update help menu and support for multicycle tests

Change 95640 on 2003/04/15 by rmanapat@rmanapat_r400_sun_marlboro

Fixes in pipelining TPC data...

Change 95635 on 2003/04/15 by smburu@smburu_r400_sun_marlboro

NO_CONNECT on some TCO_PM* wires.

Change 95623 on 2003/04/15 by mzini@mzini_crayola_linux_orl

New SQ trackers

Change 95621 on 2003/04/15 by mzini@mzini_crayola_linux_orl

Using an unregistered data-ready signal now to trigger compare

Change 95611 on 2003/04/15 by kevino@kevino_r400_linux_marlboro

    removed unused fuse_box files

Change 95604 on 2003/04/15 by kevino@kevino_r400_linux_marlboro

       Move fuse boxes to top level subdir's

Change 95598 on 2003/04/15 by kevino@kevino_r400_linux_marlboro

  Move tcd_perfmon_flops to tcd subdirectory

Change 95535 on 2003/04/14 by sallen@sallen_r400_lin_marlboro
```

TC: testbench issues - change DEPS to *not* try to build tcf_no_tpc.v (this is a manual step)
	regenerate v files and check them in.

Change 95534 on 2003/04/14 by paulv@paulv_r400_linux_marlboro

The include I removed, while its okay for simulation, is not okay for synthesis.

Change 95533 on 2003/04/14 by paulv@paulv_r400_linux_marlboro

Removed an include and added another.

Change 95531 on 2003/04/14 by cbrennan@cbrennan_r400_linux_marlboro

Merge new TC on top of old TC.
Contains changes for tp4_tc and tc testbenches as well.

Change 95530 on 2003/04/14 by sallen@sallen_r400_lin_marlboro

ferret: manually built files....

Change 95498 on 2003/04/14 by scamlin@scamlin_crayola_unix_orl

typo

Change 95490 on 2003/04/14 by vromaker@vromaker_r400_linux_marlboro

fix for CFSM end-of-clause detection

Change 95457 on 2003/04/14 by danh@danh_crayola_linux_orl

	Initial Release.

Change 95432 on 2003/04/14 by mmantor@mmantor_crayola_linux_orl

<removed duplicate declaration>

Change 95423 on 2003/04/14 by jayw@jayw_r400_linux_marlboro

Fix for when src is a subnorm in 2nd pass of 2pass fog.

Change 95404 on 2003/04/14 by rramsey@rramsey_crayola_linux_orl

Temporary fix to let flush events flow through the SC if they are not
preceded by a draw_init.
	Note flushes are still broken if you want to use them for syncing state changes,
	for example changing bad_pipe.

```
Change 95396 on 2003/04/14 by wlawless@wlawless_r400_linux_marlboro

fragment mslock probe stuff

Change 95391 on 2003/04/14 by rramsey@rramsey_crayola_linux_orl

Change SQ_DEBUSSY option to control only SQ dumping
Add SP_DEBUSSY option to control dumping of SPs
       Add some internal trackers
       Fix width on tp_sqsp_thread_id

Change 95278 on 2003/04/11 by jayw@jayw_r400_linux_marlboro

Fix 2 bit alpha channel deformat round.

Change 95254 on 2003/04/11 by paulv@paulv_r400_linux_marlboro

Added include of rb_reg.v

Change 95252 on 2003/04/11 by tien@tien_r400_devel_marlboro

Fix for max clamp on mults
Added flop in wake_up sig

Change 95189 on 2003/04/11 by jayw@jayw_r400_linux_marlboro

Fixed missing 'not' for Alpha Saturate.

Change 95174 on 2003/04/11 by hartogs@fl_hartogs

Added hooked up new "thread_type" signal from SQ module. Enhanced timeout detection.

Change 95115 on 2003/04/11 by nkociuk@nkociuk_r400_linux_marl

more updates

Change 95093 on 2003/04/11 by rramsey@rramsey_crayola_linux_orl

Regen with new genperfcode

Change 95029 on 2003/04/10 by paulv@paulv_r400_linux_marlboro

Minor code simplification.

Change 95000 on 2003/04/10 by tien@tien_r400_devel_marlboro

Some LEDA cleanup
Fix for unnormed coords
```

Got FMT_32_32_32_32_FLOAT working for one test :-)

Change 94999 on 2003/04/10 by ygiang@ygiang_r400_pv2_marlboro

fixed: sq perf counter "sq_vertex_vectors_sub"

Change 94990 on 2003/04/10 by askende@askende_r400_linux_marlboro

renamed the sp_vsr_ctl to spi_vsr_ctl

Change 94962 on 2003/04/10 by johnchen@johnchen_r400_linux_marlboro_rbrc

correct memory operations for standard hier_stencil

Change 94953 on 2003/04/10 by wlawless@wlawless_r400_linux_marlboro

fixed a probe bug found in r400rb_rb/standard_z by Paul

Change 94951 on 2003/04/10 by askende@askende_r400_linux_marlboro

removing redundant files.

Change 94950 on 2003/04/10 by askende@askende_r400_linux_marlboro

removing redundant files. The module are now part of the spi block

Change 94947 on 2003/04/10 by paulv@paulv_r400_linux_marlboro

Fixed the event_cache_flush, context_done and flush_and_invalidate signals to account for surface_enabled.

Change 94936 on 2003/04/10 by paulv@paulv_r400_linux_marlboro

Fixed typo in ARGB1555 format, number UINTEGER for alpha channel.

Change 94920 on 2003/04/10 by ygiang@ygiang_r400_pv2_marlboro

changed: naming of sx perf counters

Change 94917 on 2003/04/10 by bhankins@bhankins_crayola_win_orl

move sample time negedge clk

Change 94916 on 2003/04/10 by paulv@paulv_r400_linux_marlboro

Two major fixes. The first is in the RBM for external queue logic. The second is the consolidation of registers in tile and small part of depth.

Change 94913 on 2003/04/10 by paulv@paulv_r400_linux_marlboro

Fixed negative zeroes mux.

Change 94901 on 2003/04/10 by bhankins@bhankins_crayola_win_orl

initial add

Change 94873 on 2003/04/10 by askende@askende_r400_linux_marlboro

releasing the following changes:
1. creation of the new SPI block
2. top level changes to support 8 SP instances
3. tracker changes to support a few IO name changes

Change 94867 on 2003/04/10 by bhankins@bhankins_crayola_win_orl

update to enable injector to generate back to back exports for more robust testing. currently disabled.

Change 94834 on 2003/04/09 by mmantor@mmantor_crayola_linux_orl

<fixed a problem in ptr_buff where he hangs on an event that is not a pixel event>

Change 94830 on 2003/04/09 by mmantor@mmantor_crayola_linux_orl

<SQ/SX/SP out of order thread completion and remove redundant storage in sp for sq/sx communitcations some sq cfs bug fixed and texture kill mask generation and other misc things>

Change 94820 on 2003/04/09 by johnchen@johnchen_r400_linux_marlboro_rbrc

fixes for random test hangs

Change 94798 on 2003/04/09 by nkociuk@nkociuk_r400_linux_marl

updates

Change 94780 on 2003/04/09 by hmonsef@hmonsef

No need

Change 94776 on 2003/04/09 by paulv@paulv_r400_linux_marlboro

Removed a file and added a file to the checklist.

Change 94775 on 2003/04/09 by paulv@paulv_r400_linux_marlboro

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LEDA fix.

Change 94767 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94766 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94765 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94764 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94762 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94761 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94760 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94759 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94758 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94757 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94756 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94755 on 2003/04/09 by hmonsef@hmonsef
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Worst case RTL file

Change 94754 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94753 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94752 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94751 on 2003/04/09 by hmonsef@hmonsef


Worst case RTL file

Change 94749 on 2003/04/09 by hmonsef@hmonsef

Worst case RTL file

Change 94748 on 2003/04/09 by hmonsef@hmonsef

Worst case rtl file

Change 94747 on 2003/04/09 by hmonsef@hmonsef

Replaced by 16x34

Change 94744 on 2003/04/09 by hmonsef@hmonsef

Replaced with 8x111

Change 94740 on 2003/04/09 by hmonsef@hmonsef

Replaced by 16x228

Change 94730 on 2003/04/09 by askende@askende_r400_linux_marlboro

timing fix

Change 94727 on 2003/04/09 by jayw@jayw_r400_linux_marlboro

Fix for 1555 format with alpha channel masked out.

Change 94724 on 2003/04/09 by mzini@mzini_crayola_linux_orl
```

New SQ trackers

Change 94718 on 2003/04/09 by viviana@viviana_crayola_linux_orl

SQ trackers for the sequencer control flow instructions.

Change 94706 on 2003/04/09 by wlawless@wlawless_r400_linux_marlboro

Changed the fragment probe to work with a probe mask instead of a coarse mask
for each fragment....

Change 94685 on 2003/04/09 by askende@askende_r400_linux_marlboro

adding the file to the perforce tree

Change 94648 on 2003/04/09 by bhankins@bhankins_crayola_win_orl

remove unused tracker

Change 94619 on 2003/04/08 by tien@tien_r400_devel_marlboro

Another fix for unnormed coords

Change 94617 on 2003/04/08 by johnchen@johnchen_r400_linux_marlboro_rbrc

update tile_id and qc_index for cacheline hits because these values can change in tile
block

Change 94518 on 2003/04/08 by vromaker@vromaker_r400_linux_marlboro

fix for bug caused by resource change between EXEC control flow
instructions

Change 94505 on 2003/04/08 by rramsey@rramsey_crayola_linux_orl

don't inc vtx thread counter if thread is an event

Change 94480 on 2003/04/08 by bhankins@bhankins_crayola_win_orl

update to current test hierarchy

Change 94468 on 2003/04/08 by jayw@jayw_r400_linux_marlboro_rbrc

Fix for Alpha Saturate precision bug.

Change 94467 on 2003/04/08 by bhankins@bhankins_crayola_win_orl

reduce random wait time

Change 94448 on 2003/04/08 by paulv@paulv_r400_linux_marlboro

Fixed some readability issues.

Change 94436 on 2003/04/08 by bhankins@bhankins_crayola_win_orl

parameterize random wait times

Change 94409 on 2003/04/08 by nkociuk@nkociuk_r400_linux_marl

initial checkin of tp_addresser testbench

Change 94399 on 2003/04/08 by bhankins@bhankins_crayola_win_orl

1. fix bug in tbmod_fake_rb to properly read request size value from dumps.2. fix test bench to properly detect a good end of test condition.

Change 94394 on 2003/04/08 by bhankins@bhankins_crayola_win_orl

remove unused signal

Change 94378 on 2003/04/07 by jayw@jayw_r400_linux_marlboro_rbrc

Fixed prescale to ignore zero subterms.

Change 94239 on 2003/04/07 by bhankins@bhankins_crayola_win_orl

add some randomization to parameter cache deallocs

Change 94228 on 2003/04/07 by jayw@jayw_r400_linux_marlboro_rbrc

resetting q_is_largest_or_equal to ONE.

Change 94223 on 2003/04/07 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Got rid off bunch of adder/subtract functions

Change 94222 on 2003/04/07 by bhankins@bhankins_crayola_win_orl

fix to allow the issue of parameter cache deallocates regardless of the number of lines available.

Change 94211 on 2003/04/07 by hartogs@fl_hartogs

Template Debussy waveform file.

Change 94198 on 2003/04/07 by jayw@jayw_r400_linux_marlboro

Pass sign through for neg zero, max and min functions. hang fix.

Change 94193 on 2003/04/07 by paulv@paulv_r400_linux_marlboro

Fixed blendon wiring.

Change 94187 on 2003/04/07 by bhankins@bhankins_crayola_win_orl

1. accomodate the pc_channel_mask column that was added to sp_sx.dmp2. remove references to sq_sx_pc.dmp (former home of pc_channel_mask)

Change 94178 on 2003/04/07 by bhankins@bhankins_crayola_win_orl

misc changes

Change 94118 on 2003/04/06 by johnchen@johnchen_r400_linux_marlboro_rbrc

fix a cache write conflict

Change 94063 on 2003/04/04 by jayw@jayw_r400_linux_marlboro

missing comma from Mark's checkin.

Change 94062 on 2003/04/04 by msprague@msprague_r400_synth

Update to reflect timing changes with comments retained

Change 94054 on 2003/04/04 by tien@tien_r400_devel_marlboro

Fixed issue with unnormed coords in tp_addresser

Change 94022 on 2003/04/04 by hmonsef@hmonsef

Wrong file name

Change 94021 on 2003/04/04 by hmonsef@hmonsef

Replaces 8x128

Change 94001 on 2003/04/04 by johnchen@johnchen_r400_linux_marlboro_rbrc

bug fix for figuring out when to expand and some stencile support

Change 93999 on 2003/04/04 by wlawless@wlawless_r400_linux_marlboro

fixed the previous fix... ooops

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Change 93998 on 2003/04/04 by hmonsef@hmonsef

Replace 8x128 wirh 8x136

Change 93997 on 2003/04/04 by hmonsef@hmonsef

Replaced 8x128 with 8x136

Change 93995 on 2003/04/04 by hmonsef@hmonsef

Replaced 8x128 with 8x136

Change 93994 on 2003/04/04 by hmonsef@hmonsef

Replaces 8x128

Change 93993 on 2003/04/04 by askende@askende_r400_linux_marlboro

checked in a timing fix

Change 93988 on 2003/04/04 by wlawless@wlawless_r400_linux_marlboro

changed a muc cnt

Change 93985 on 2003/04/04 by hmonsef@hmonsef

Replaced 8x128 with 8x136

Change 93984 on 2003/04/04 by hmonsef@hmonsef

Replaced 8x128 with 8x136

Change 93972 on 2003/04/04 by msprague@msprague_r400_synth

Incorporated timing and area changes into pre-vpp version, so comments are kept

Change 93959 on 2003/04/04 by vromaker@vromaker_r400_linux_marlboro

temporarily disabled PVPS src select swizzle because it was causing SP tests
       from Andi's mini_regress to fail

Change 93957 on 2003/04/04 by hmonsef@hmonsef_r400_linux_marlboro_rbrc

Reduced the number of comparators by rewriting the code

Change 93951 on 2003/04/04 by bhankins@bhankins_crayola_win_orl
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fix to properly get to end of file

Change 93945 on 2003/04/04 by sallen@sallen_r400_lin_marlboro

ferret: TC tb, force manual creation of tcf_no_tpc.v and tpc_empty,v
              (requires manual updating)

Change 93934 on 2003/04/04 by wlawless@wlawless_r400_linux_marlboro

Addressing bug when flushing fragment bits

Change 93929 on 2003/04/04 by sallen@sallen_r400_lin_marlboro

ferret: create empty overrides.cfg if it doesn't exist
           delete manually created tcf_no_tpc.v

Change 93914 on 2003/04/04 by paulv@paulv_r400_linux_marlboro

Timing fix.

Change 93845 on 2003/04/04 by jayw@jayw_r400_linux_marlboro

adding new file

Change 93801 on 2003/04/03 by jayw@jayw_r400_linux_marlboro

Mark Sprague's timing, power and area reduction updates.

Change 93788 on 2003/04/03 by dougd@dougd_r400_linux_marlboro

added event_context register to correctly capture context when sending a vtx event to
the thread buffer.

Change 93640 on 2003/04/03 by hartogs@fl_hartogs

Added include file "vgt_reg.v" to prevent compiler errors during Modelsim compile.
   Fixed wire definition to match output port definition.

Change 93627 on 2003/04/03 by jayw@jayw_r400_linux_marlboro_rbrc

resolve pixelpair signal for hang fix.

Change 93626 on 2003/04/03 by jayw@jayw_r400_linux_marlboro_rbrc

Fixes for hangs.

Change 93591 on 2003/04/03 by paulv@paulv_r400_linux_marlboro
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Fixed logic for the cacheline dirty vector.

Change 93585 on 2003/04/03 by dougd@dougd_r400_linux_marlboro

move event filters to inputs of SQ in ptr_buff and vtx_ctl and remove from
thread_buff_cntl, modify cntx0-17 busy counters in ptr_buff to use new event logic, add
RST_VTX_CNT functionality to sq_vtx_ctl, add SQ_CP_event and SQ_RB event functionality
to pix_thread_buff and vtx_thread_buf, remove obsolete SQ_CP_event functionality from
thread_buff_cntl.

Change 93489 on 2003/04/02 by vromaker@vromaker_r400_linux_marlboro

added end of clause detection for serialization and resource change to CFSM;
fix for first_in_clause related to PVPS detection;
added SQ_SP_thread_type and SQ_TP_thread_type outputs to sq.v;
added predicate to Tex IQ - now predicate goes from TCFS, thru TIF, thru TIQ, to the
TIS;
removed q1 pipeline stage for SP predicate data in AIS Output;

Change 93483 on 2003/04/02 by subad@subad_r400_linux_marlboro

added 2D tiled for fmt00 and fmt01

Change 93462 on 2003/04/02 by tien@tien_r400_devel_marlboro

Somes fixes for sign issues in LOD deriv

Change 93450 on 2003/04/02 by wlawless@wlawless_r400_linux_marlboro

it was using the allocated addr for the second tile in a hit line

Change 93427 on 2003/04/02 by wlawless@wlawless_r400_linux_marlboro

Update multisample for 2 and 4 sample

Change 93426 on 2003/04/02 by askende@askende_r400_linux_marlboro

changes related to renaming of these modules to spi_*

Change 93419 on 2003/04/02 by askende@askende_r400_linux_marlboro

deleting a file that it is no longer used

Change 93417 on 2003/04/02 by askende@askende_r400_linux_marlboro

various changes and additions

Change 93402 on 2003/04/02 by jayw@jayw_r400_linux_marlboro
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Fixes for hang and clamping

Change 93335 on 2003/04/02 by bhankins@bhankins_crayola_win_orl

misc fixes

Change 93215 on 2003/04/01 by askende@askende_r400_linux_marlboro

deleting

Change 93210 on 2003/04/01 by vbhatia@vbhatia_r400_linux_marlboro

Added new tests

Change 93208 on 2003/04/01 by askende@askende_r400_linux_marlboro

adding new files under the spi tree

Change 93207 on 2003/04/01 by askende@askende_r400_linux_marlboro

adding new files under spi tree

Change 93206 on 2003/04/01 by askende@askende_r400_linux_marlboro

creating a new directory under parts_lib (TOTT) representing the spi (shader pipe
interpolators)

Change 93196 on 2003/04/01 by paulv@paulv_r400_linux_marlboro

For non-surface-enabled tiles, hiz_quad_state_mask should be set to zeroes.

Change 93181 on 2003/04/01 by johnchen@johnchen_r400_linux_marlboro_rbrc

add smask_enable and zmask_enable to request register

Change 93160 on 2003/04/01 by askende@askende_r400_linux_marlboro

      checking in a timing (tentative) fix

Change 93113 on 2003/04/01 by nkociuk@nkociuk_r400_linux_marl

flops for signals going to perfmon block to simplify tcd timing...

Change 93099 on 2003/04/01 by hartogs@fl_hartogs

Fixed logic that holds off SC injector.
   Fixed bug in threaded empty signal for tp_sqsp_dmp_not_empty.
```

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   Hacked logic that frees state contexts so that it sorta works.

Change 93069 on 2003/04/01 by paulv@paulv_r400_linux_marlboro

Changed definition of upper quad_state_mask bit (per quad).  Also added no_detail_mask
qualifier to output fifo to RBD.

Change 93063 on 2003/04/01 by jayw@jayw_r400_linux_marlboro

Fix for neg zero propogating for very small neg IEEE.

Change 93054 on 2003/04/01 by rramsey@rramsey_crayola_linux_orl

PV/PS determinations need to be made on post-swizzled component selects

Change 93053 on 2003/04/01 by dougd@dougd_r400_linux_marlboro

added context_id or state to event info stored in the status_reg to correct a bug in
the state logic supporting cntx0 and cntx17 busy

Change 93040 on 2003/04/01 by tien@tien_r400_devel_marlboro

Another LOD fix in 16-bit multiply (pos 0 output always)

Change 93026 on 2003/03/31 by grayc@grayc_crayola_linux_orl

   minor changes for gc testbench

Change 93012 on 2003/03/31 by tien@tien_r400_devel_marlboro

LOD fix MAX_INT

Change 93010 on 2003/03/31 by askende@askende_r400_linux_marlboro

change related to :
                 matching the latency of the predicate and kill on both scalar and
vector engines (7 cycles)

Change 92977 on 2003/03/31 by paulv@paulv_r400_linux_marlboro

HiZ fixes.

Change 92970 on 2003/03/31 by dougd@dougd_r400_linux_marlboro

added pix event_id to qualify events to increment the cntx17 busy counter. Also added
`include "vgt_reg.v" and removed hard coded parameters.

Change 92965 on 2003/03/31 by jayw@jayw_r400_linux_marlboro
```

Added missing include.

Change 92957 on 2003/03/31 by jayw@jayw_r400_linux_marlboro_rbrc

a fix for sending 16-float minus zero for small_multi_rect_no_tb_no_z b54b31ba

Change 92910 on 2003/03/31 by vbhatia@vbhatia_r400_linux_marlboro

Few more tests

Change 92904 on 2003/03/31 by hartogs@fl_hartogs

Added TP_SP latency controls requested by Mantor.

Change 92903 on 2003/03/31 by jayw@jayw_r400_linux_marlboro_rbrc

Fix for small_multi_with_no_tb_no_z 85080ce7 src alpha precision 2 pass fog

Change 92885 on 2003/03/31 by paulv@paulv_r400_linux_marlboro

Fixed some other_tiledata logic.

Change 92884 on 2003/03/31 by hartogs@fl_hartogs

Cleaned-up some "TODO" items.

Change 92727 on 2003/03/29 by tien@tien_r400_devel_marlboro

MOre LOD fixes

Change 92721 on 2003/03/28 by johnchen@johnchen_r400_linux_marlboro_rbrc

quaddata even flush happen independent of z_enable or stencile_enable

Change 92693 on 2003/03/28 by paulv@paulv_r400_linux_marlboro

Fixed bug where quad cache was being read even though mask was 0.

Change 92679 on 2003/03/28 by hartogs@fl_hartogs

Hooked-up new thread-id ports on SQ. Testbench should now handle most tests.

Change 92674 on 2003/03/28 by hmonsef@hmonsef

Replaces 16x32 with 16x34

Change 92671 on 2003/03/28 by hmonsef@hmonsef

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Replaces 16x32 with 16x34

Change 92667 on 2003/03/28 by hmonsef@hmonsef

Replaced 16x32 with 16x34

Change 92666 on 2003/03/28 by hmonsef@hmonsef

replaced 16x32 with 16x34

Change 92665 on 2003/03/28 by hmonsef@hmonsef

replaced 16x32 with 16x34

Change 92664 on 2003/03/28 by hmonsef@hmonsef

Replaces 16x32

Change 92656 on 2003/03/28 by jayw@jayw_r400_linux_marlboro

New AB fixes for avoiding neg zero out of blender.

Change 92655 on 2003/03/28 by askende@askende_r400_linux_marlboro

changes related to :
          1. NaN propagation in case of DOT products
          2. qualifying the inf detection on the input of the scalar engine for operand
b with ~single_operand_instruction

Change 92649 on 2003/03/28 by paulv@paulv_r400_linux_marlboro

Fix to flush logic (again).

Change 92622 on 2003/03/28 by bhankins@bhankins_crayola_win_orl

misc fixes and cleanup

Change 92617 on 2003/03/28 by johnchen@johnchen_r400_linux_marlboro_rbrc

update szmask request interface

Change 92615 on 2003/03/28 by bhankins@bhankins_crayola_win_orl

initial add.  very simple.  probably will need work.

Change 92611 on 2003/03/28 by hmonsef@hmonsef
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Replaced 16x224 with 16x228

Change 92610 on 2003/03/28 by grayc@grayc_crayola_linux_orl

   new tracker

Change 92609 on 2003/03/28 by hmonsef@hmonsef

Replaced 16x224 with 16x228

Change 92608 on 2003/03/28 by hmonsef@hmonsef

Replaced 16x224 with 16x228

Change 92607 on 2003/03/28 by hmonsef@hmonsef

Replaced 16x224 with 16x228

Change 92606 on 2003/03/28 by hmonsef@hmonsef

Replaced 16x224 with 16x228

Change 92605 on 2003/03/28 by hmonsef@hmonsef

Replaced 16x224 with 16x228

Change 92590 on 2003/03/28 by hmonsef@hmonsef

Replaces 16x224.

Change 92586 on 2003/03/28 by tien@tien_r400_devel_marlboro

Sign fix LOD

Change 92582 on 2003/03/28 by paulv@paulv_r400_linux_marlboro

Bunch of fixes, including fixes to the quad cache cacheline allocation and the flush
logic between the quad and tile cache.

Change 92573 on 2003/03/28 by nkociuk@nkociuk_r400_linux_marl

initial checkin or tp_registers testbench...

Change 92554 on 2003/03/28 by bhankins@bhankins_crayola_win_orl

misc fixes and updates.  passes mini-regress tests.

Change 92534 on 2003/03/27 by askende@askende_r400_linux_marlboro
```

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added/updated comments...

Change 92521 on 2003/03/27 by dclifton@dclifton_crayola_linux_orl

Fixed treatment of denorm floats

Change 92515 on 2003/03/27 by askende@askende_r400_linux_marlboro

changes related to :
         1.infinity propagation in case of DOT product
         2.ignoring the NaN inputs in SrcC when dealing with two-operand opcodes

Change 92496 on 2003/03/27 by johnchen@johnchen_r400_linux_marlboro_rbrc

remove surface_enable quaddata even flush

Change 92466 on 2003/03/27 by jayw@jayw_r400_linux_marlboro

more signal name renaming...

Change 92454 on 2003/03/27 by rramsey@rramsey_crayola_linux_orl

add reset for mp_snd and mp_loop regs

Change 92451 on 2003/03/27 by hartogs@fl_hartogs

Added several missing input ports to sub-modules.

Change 92435 on 2003/03/27 by johnchen@johnchen_r400_linux_marlboro_rbrc

add surface_enable to quaddata even flush

Change 92428 on 2003/03/27 by hartogs@fl_hartogs

Deleted reduntant wire declaration that was causing an error in modelsim.
   Added explicit declarations for a bunch of implicitly used wires. The lack of the
explicit declarations was causing warnings in Modelsim.

Change 92424 on 2003/03/27 by jayw@jayw_r400_linux_marlboro

removed last pixel of quad, never used, regnerated.

Change 92423 on 2003/03/27 by jayw@jayw_r400_linux_marlboro

renamed many sigs. fixed a hold_non_fog pulling in wrong cycle data.

Change 92415 on 2003/03/27 by johnchen@johnchen_r400_linux_marlboro_rbrc
```

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add flush bits to the quaddata interface

Change 92356 on 2003/03/27 by smoss@smoss_crayola_linux_orl

   removed space limiting on mismatch display

Change 92353 on 2003/03/27 by nkociuk@nkociuk_r400_linux_marl

change instantiations to match newer module revs...

Change 92324 on 2003/03/27 by dougd@dougd_r400_linux_marlboro

fixed bug with address wrapping in the gpr_wr_addr generation for pix and vtx

Change 92314 on 2003/03/27 by jayw@jayw_r400_linux_marlboro

Fix for color mask and plane mask.

Change 92303 on 2003/03/27 by mmantor@mmantor_crayola_linux_orl

<export_id expanded from one to four bit, end_of_clause added to CFS-TIF interface and
last_in_clause flag passed down with instruction to eventually trigger a free_done.
thread_id outputs added to the SQ_SP and SQ_TP interfaces for testbench, and added
sq_sx control signals for exp_table read >

Change 92288 on 2003/03/26 by jayw@jayw_r400_linux_marlboro

fix for color mask and color swap set.

Change 92262 on 2003/03/26 by hartogs@fl_hartogs

Added untested code for random backpressure on the SQ_TP interface.
   Added untested code for random starve pressure on the TP_SP interface.

Change 92221 on 2003/03/26 by jayw@jayw_r400_linux_marlboro

LEDA fixes.

Change 92210 on 2003/03/26 by paulv@paulv_r400_linux_marlboro

Several fixes in the HiZ tile and quad checkers and the quad cache (cachelines weren't
being flushed because inflight counts weren't going to zero).  Also removed
RBD_RBT_quaddata_z_enable (it wasn't needed).

Change 92203 on 2003/03/26 by askende@askende_r400_linux_marlboro

reverting the previous change.
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Change 92192 on 2003/03/26 by bhankins@bhankins_crayola_win_orl

obsolete

Change 92191 on 2003/03/26 by bhankins@bhankins_crayola_win_orl

ongoing work.  some perf and sp tests pass.paramater cache reads pass, but
tbmod_fake_int.v may need some work.

Change 92185 on 2003/03/26 by vbhatia@vbhatia_r400_linux_marlboro

Added default dump file and turned off default dumping

Change 92178 on 2003/03/26 by subad@subad_r400_linux_marlboro

timing fix for ftfconv path

Change 92177 on 2003/03/26 by nkociuk@nkociuk_r400_linux_marl

update perfmon blocks with new genperfcode (1.6)

Change 92176 on 2003/03/26 by nkociuk@nkociuk_r400_linux_marl

update testbench with tp_pipe_valids block, allowing emulator to avoid dealing with
hardware implementation specifics
   in this case, this is the color-channel format encoding used in the tp_hicolor block
 also added some additional runtime parameters

Change 92158 on 2003/03/26 by wlawless@wlawless_r400_linux_marlboro

Added the 2 & 4 sample logic

Change 92142 on 2003/03/25 by hartogs@fl_hartogs

This version passes milestone_tri. Trackers and injectors are ready for multi-threading
when those signals become available.

Change 92139 on 2003/03/25 by hartogs@fl_hartogs

This version passes the "milestone_tri" test completely. First working version for
texture fetch.

Change 92135 on 2003/03/25 by vbhatia@vbhatia_r400_linux_marlboro

Updated

Change 92095 on 2003/03/25 by sallen@sallen_r400_lin_marlboro
```

```
ferret: snapshot TC testbench development

Change 92092 on 2003/03/25 by tien@tien_r400_devel_marlboro

Removed hi-latency stuff.  Still need to clean up

Change 92080 on 2003/03/25 by johnchen@johnchen_r400_linux_marlboro_rbrc

add the dk bit to the pipeline

Change 92018 on 2003/03/25 by askende@askende_r400_linux_marlboro

releasing a fix related to detecting an overflow and clamping to max_float in the
scalar engine multiplier

Change 92000 on 2003/03/25 by hartogs@fl_hartogs

Un-did previous change so that I would have to listen to Skende whine about it.

Change 91979 on 2003/03/25 by hartogs@fl_hartogs

Put the "USE_BEHAVE_MEM" (dum_mem_p2) model back in.

Change 91978 on 2003/03/25 by hartogs@fl_hartogs

Incremental check-in. This version will run "milestone_tri" to completion (including
injecting the texture fetch data); however the simulation mismatches on the SPSX
tracker.

Change 91977 on 2003/03/25 by hartogs@fl_hartogs

Changed "check flags" on one of the SQ memories to minimize garbage output during
simulation.

Change 91976 on 2003/03/25 by hartogs@fl_hartogs

Changed dump file name from tp_sq.dmp to tp_sqsp.dmp.

Change 91926 on 2003/03/24 by tien@tien_r400_devel_marlboro

Fix in tp_hicolor for INT mode
Removed fast vfetch logic

Change 91920 on 2003/03/24 by paulv@paulv_r400_linux_marlboro

leda fixes
```

```
Change 91890 on 2003/03/24 by johnchen@johnchen_r400_linux_marlboro_rbrc

get the right tile_id when expand

Change 91876 on 2003/03/24 by paulv@paulv_r400_linux_marlboro

LEDA fixes.

Change 91872 on 2003/03/24 by hmonsef@hmonsef

replaced 8x110 with 8x111

Change 91869 on 2003/03/24 by hmonsef@hmonsef

replaced 8x110 with 8x111

Change 91868 on 2003/03/24 by hmonsef@hmonsef

Replaced 8x110 with 8x111

Change 91867 on 2003/03/24 by hmonsef@hmonsef

Repalced 8x110 with 8x111

Change 91866 on 2003/03/24 by hmonsef@hmonsef

Repalces 8x110

Change 91865 on 2003/03/24 by hmonsef@hmonsef

Replaced 8x110 with 8x111

Change 91864 on 2003/03/24 by hmonsef@hmonsef

Replaced 8x110 with 8x111

Change 91845 on 2003/03/24 by wlawless@wlawless_r400_linux_marlboro

Added a 64 bit signal of line_in_read_cam to block it from being
allocated

Change 91820 on 2003/03/24 by paulv@paulv_r400_linux_marlboro

Added RBT_RBC_c_frag_color_sel.

Change 91818 on 2003/03/24 by paulv@paulv_r400_linux_marlboro

Multiple fixes and some additions.
```

Change 91811 on 2003/03/24 by nkociuk@nkociuk_r400_linux_marl

initial checkin

Change 91808 on 2003/03/24 by wlawless@wlawless_r400_linux_marlboro

new stuff for ms_lock color cache

Change 91763 on 2003/03/24 by hartogs@fl_hartogs

Qualified use of "q_skid_rbbm_a" with "!q_skid_empty". This was done to avoid X's on "sel_gfx_vgt_draw_initiator" which corrupted a counter "map_copy_cntr". The corruption of "map_copy_cntr" could only be corrected by reset.

Change 91754 on 2003/03/24 by rramsey@rramsey_crayola_linux_orl

Fix for gpr write tracker

Change 91746 on 2003/03/24 by jayw@jayw_r400_linux_marlboro

More LEDA 'fixes'.

Change 91737 on 2003/03/23 by jayw@jayw_r400_linux_marlboro

Many LEDA fixes and added one missing include to rb_rbd_cache_access.v

Change 91706 on 2003/03/23 by jayw@jayw_r400_linux_marlboro

LEDA fixes and important subnorm result fix in ab_format.v

Change 91689 on 2003/03/22 by askende@askende_r400_linux_marlboro

reverting a change made to the swizzle logic in sp_macc.v rev.56

Change 91601 on 2003/03/21 by askende@askende_r400_linux_marlboro

releasing a fix related to maskgt opcode

Change 91599 on 2003/03/21 by jayw@jayw_r400_linux_marlboro

fix for irc_cp_cache_flush as suggested by Alexander Ashkar.

Change 91569 on 2003/03/21 by dougd@dougd_r400_linux_marlboro

added Real Time input to each of the constant store to enable the correct addressing of RT constants from the SQ

```
Change 91566 on 2003/03/21 by askende@askende_r400_linux_marlboro

fix related to a  typo in the swizzle logic when different channels of the same operand
are
selected from different sources (GPR vs. Previous result vs. Constant)

Change 91546 on 2003/03/21 by paulv@paulv_r400_linux_marlboro

Fixed pixel_mask to account for 16-bit/channel bypassed signals.

Change 91529 on 2003/03/21 by dclifton@dclifton_r400

Generated with version 1.6 of genperfcode--syntax issues possibly causing unknowns in
gate sims are fixed

Change 91513 on 2003/03/21 by rramsey@rramsey_crayola_linux_orl

connect sc_rtr up to signal from SC when not running pa_block_sim

Change 91475 on 2003/03/21 by rmanapat@rmanapat_r400_sun_marlboro

Was missing value for [9]

Change 91472 on 2003/03/21 by rmanapat@rmanapat_r400_sun_marlboro

fix synthesized latches

Change 91453 on 2003/03/21 by bhankins@bhankins_crayola_win_orl

snoop into the sx's to get an rtr to throttle requests from the fake pa so as not to
blow out the request fifo in the sx.

Change 91426 on 2003/03/20 by johnchen@johnchen_r400_linux_marlboro_rbrc

freeing cachelines independent of tag...temporary fix....might not work when multiple
cachelines need freeing

Change 91422 on 2003/03/20 by dougd@dougd_r400_linux_marlboro

fixed bugs in the rbi_rd_state machine

Change 91383 on 2003/03/20 by johnchen@johnchen_r400_linux_marlboro_rbrc

probe cache hit compare fix

Change 91352 on 2003/03/20 by hmonsef@hmonsef

Replaced 16x223 with 16x224
```

Change 91348 on 2003/03/20 by kmeekins@kmeekins_crayola_linux_orl

Changed to use the default filenames created by build scripts.

Change 91346 on 2003/03/20 by subad@subad_r400_linux_marlboro

fix for special case 2

Change 91339 on 2003/03/20 by hmonsef@hmonsef

Replaced 16x223 with 16x224

Change 91338 on 2003/03/20 by hmonsef@hmonsef

Replaced 16x223 with 16x224

Change 91337 on 2003/03/20 by hmonsef@hmonsef

Replaced 16x223 with 16x224

Change 91336 on 2003/03/20 by paulv@paulv_r400_linux_marlboro

A previous fix had tiles coming out every cycle, which shouldn't happen. This has been fixed.

Change 91335 on 2003/03/20 by hmonsef@hmonsef

Replaces 16x223

Change 91331 on 2003/03/20 by hmonsef@hmonsef

Replaced 16x223 by 16x224

Change 91330 on 2003/03/20 by hmonsef@hmonsef

replaced 16x223 by 16x224

Change 91312 on 2003/03/20 by subad@subad_r400_linux_marlboro

fix for 16B expand formats to do float to fixed conversion

Change 91303 on 2003/03/20 by jayw@jayw_r400_linux_marlboro_rbrc

non-blend not set at allocation

Change 91278 on 2003/03/20 by paulv@paulv_r400_linux_marlboro

Fixed bypass fifo from overflowing and slightly modified the stall signal for the head.

Change 91267 on 2003/03/20 by bhankins@bhankins_crayola_win_orl

get in sync with gui.

Change 91266 on 2003/03/20 by bhankins@bhankins_crayola_linux_orl

ok for now, but still needs work in properly detecting which pixels to track.

Change 91238 on 2003/03/20 by bhankins@bhankins_crayola_linux_orl

seems to be working.

Change 91234 on 2003/03/20 by bhankins@bhankins_crayola_linux_orl

seems to be working.

Change 91233 on 2003/03/20 by bhankins@bhankins_crayola_linux_orl

update. showing signs of life.

Change 91232 on 2003/03/20 by bhankins@bhankins_crayola_linux_orl

do paramater cache reads

Change 91230 on 2003/03/20 by bhankins@bhankins_crayola_linux_orl

starting to show signs of working

Change 91219 on 2003/03/20 by dougd@dougd_r400_linux_marlboro

fix bug in real time write address logic

Change 91208 on 2003/03/20 by paulv@paulv_r400_linux_marlboro

A few other minor fixes.

Change 91205 on 2003/03/20 by jayw@jayw_r400_linux_marlboro_rbrc

Fix dst exp when MIN or MAX.

Change 91199 on 2003/03/20 by paulv@paulv_r400_linux_marlboro

Code fixes and optimizations.

Change 91177 on 2003/03/20 by donaldl@fl_donaldl_p4

```
Removed IO_SC and IO_SC_B partition scan input/output signals.

Change 91126 on 2003/03/19 by dougd@dougd_r400_linux_marlboro

fixed bug in incrementing pix_cntx17_cnt with back to back events

Change 91104 on 2003/03/19 by tien@tien_r400_devel_marlboro

Fixed cmask for hicolor fast floats
Added test ports

Change 91060 on 2003/03/19 by dclifton@dclifton_r400

Reverted width of IO_PA_scan and PA_IO_scan back to 15 bits.

Change 91059 on 2003/03/19 by dclifton@dclifton_r400

Reverted width of IO_PA_scan and PA_IO_scan back to 15 bits.

Change 91037 on 2003/03/19 by dclifton@dclifton_r400

Changed width of IO_PA_scan and PA_IO_scan to 14 bits.

Change 91033 on 2003/03/19 by dclifton@dclifton_r400

Changed number of IO_PA_scan and PA_IO_scan pins to 14 each.

Change 91024 on 2003/03/19 by hmonsef@hmonsef

Added SCAN ports as requested by Jim B.

Change 91017 on 2003/03/19 by kevino@kevino_r400_linux_marlboro

         Added bist ports.  Changed io_tc*_scan to 14 bits (from 25).
            removed io_tcf_patition_scan signals (now part of scan signal)

Change 91010 on 2003/03/19 by bhankins@fl_bhankins_r400_win

work in progress. dont use.

Change 90997 on 2003/03/19 by bhankins@bhankins_crayola_linux_orl

temp version; work in progress.  do not use.

Change 90988 on 2003/03/19 by askende@askende_r400_linux_marlboro

fix related to KILL (MASK) scalar instruction
```

```
Change 90972 on 2003/03/19 by askende@askende_r400_linux_marlboro

releasing changes to top level related to SoCBIST

Change 90960 on 2003/03/19 by smoss@smoss_crayola_linux_orl

   added new sq trackers

Change 90935 on 2003/03/19 by paulv@paulv_r400_linux_marlboro

Intermediate check-in.  Main fix is fixing surface_enabled in the HiZ logic to only
care about z-related surfaces.

Change 90931 on 2003/03/19 by kmeekins@kmeekins_r400_win

Changed the ROM_BAD_PIPE_DISABLE_REGISTER logic to only check those
disable bit fields associated with pixel processing.

Change 90929 on 2003/03/19 by wlawless@wlawless_r400_linux_marlboro

found a bit width typo in the tile inflight decrement logic...

Change 90915 on 2003/03/19 by dougd@dougd_r400_linux_marlboro

added I/O TEST PORTS for bist and scan

Change 90899 on 2003/03/19 by rmanapat@rmanapat_r400_sun_marlboro

Forgotten files for bug 1500

Change 90897 on 2003/03/19 by hmonsef@hmonsef

Added scan ports as requested by Jim Bosco

Change 90895 on 2003/03/19 by bhankins@fl_bhankins_r400_win

add test signals

Change 90875 on 2003/03/19 by bhankins@fl_bhankins_r400_win

mods

Change 90865 on 2003/03/19 by bhankins@fl_bhankins_r400_win

updates

Change 90862 on 2003/03/19 by bhankins@fl_bhankins_r400_win
```

```
add common_dft test ports

Change 90861 on 2003/03/19 by rramsey@rramsey_crayola_linux_orl

Changes to sp_sel and valid logic to get bad_pipe working

Change 90807 on 2003/03/18 by donaldl@fl_donaldl_p4

Added common test ports.

Change 90803 on 2003/03/18 by paulv@paulv_r400_linux_marlboro

Fixed the quad cache to prevent HiZ from starving RBD requests (although some better
method may be needed) and fixed the quad_cache_cline signal for HiZ writes to quad
cache.

Change 90797 on 2003/03/18 by paulv@paulv_r400_linux_marlboro

Minor code simplification.

Change 90786 on 2003/03/18 by askende@askende_r400_linux_marlboro

fixes related to:
            1.vector MAX4 instruction
            2.TRUNC/FLOOR vector instruction

Change 90773 on 2003/03/18 by dougd@dougd_r400_linux_marlboro

added logic to drive SQ_CNTX0_BUSY, SQ_CNTX17_BUSY. This change should complete this
functionality.

Change 90747 on 2003/03/18 by paulv@paulv_r400_linux_marlboro

Tile optimizations and a few bug fixes.

Change 90740 on 2003/03/18 by paulv@paulv_r400_linux_marlboro

All inputs to blender now have an IEEE 8-bit exponent.  Some other minor fixes.

Change 90733 on 2003/03/18 by dougd@dougd_r400_linux_marlboro

added counters and control for pix cntx0, cntx17 busy

Change 90718 on 2003/03/18 by rmanapat@rmanapat_r400_sun_marlboro

Fix for bug1500

Change 90624 on 2003/03/17 by askende@askende_r400_linux_marlboro
```

releasing a change related to NaN propagation in case of one-operand scalar instructions

Change 90622 on 2003/03/17 by hartogs@fl_hartogs_linux

First crack at VCS build script for tb_sqsp

Change 90594 on 2003/03/17 by grayc@grayc_crayola_linux_orl

   changed number of pipe stages for valid to 8

Change 90551 on 2003/03/17 by dougd@dougd_r400_linux_marlboro

added code in sq_status_reg to decement the thread counters in sq_vtx_cntl used for SQ_CNTX0_busy, SQ_CNTX17_busy

Change 90460 on 2003/03/17 by bhankins@fl_bhankins_r400_win

fixed to ignore don't care transfers

Change 90313 on 2003/03/14 by hartogs@fl_hartogs

Added multi-threaded code to tbtrk_sqtp.v. (Thread id and type are hard-coded to 0 and 1, respectively, until these signals are available from the sq.)
   Fixed port name typos in tbtrk_spsx.v.

Change 90308 on 2003/03/14 by kmeekins@kmeekins_r400_win

Conditioned the use_polymode_grad mux select with the Real-Time
stream enable such that the stored polymode gradient is never used
during RTS. The dx and dy gradients are supplied during RTS so using
the stored value is not necessary.

Change 90271 on 2003/03/14 by jayw@jayw_r400_linux_marlboro

Fix for 128 bit linear pixels.

Change 90253 on 2003/03/14 by bhankins@fl_bhankins_r400_win

revert back to earlier version until new version is tested

Change 90250 on 2003/03/14 by bhankins@fl_bhankins_r400_win

obsolete

Change 90249 on 2003/03/14 by bhankins@fl_bhankins_r400_win

initial checkin

Change 90247 on 2003/03/14 by bhankins@fl_bhankins_r400_win

mods

Change 90245 on 2003/03/14 by askende@askende_r400_linux_marlboro

various changes

Change 90242 on 2003/03/14 by wlawless@wlawless_r400_linux_marlboro

Removed the LSb from the cam lookup the blend bypass for the num_quads_in_pipe only

Change 90199 on 2003/03/14 by johnchen@johnchen_r400_linux_marlboro_rbrc

compare the complete centerz value..not just the mantisa

Change 90171 on 2003/03/14 by askende@askende_r400_linux_marlboro

fixes related to pred_pop instruction

Change 90106 on 2003/03/13 by johnchen@johnchen_r400_linux_marlboro_rbrc

turn off request registers for plane4

Change 90101 on 2003/03/13 by paulv@paulv_r400_linux_marlboro

Timing fix.

Change 90086 on 2003/03/13 by johnchen@johnchen_r400_linux_marlboro_rbrc

memory request for plane4

Change 90069 on 2003/03/13 by jayw@jayw_r400_linux_marlboro

More LEDA.

Change 90053 on 2003/03/13 by johnchen@johnchen_r400_linux_marlboro_rbrc

use stencil clear when surface enable is on

Change 90029 on 2003/03/13 by kmeekins@kmeekins_r400_win

Created script to convert Modelsim .do wave files to nWave .rc files.

Change 90026 on 2003/03/13 by paulv@paulv_r400_linux_marlboro

```
Timing and area optimizations.

Change 90002 on 2003/03/13 by viviana@viviana_crayola_linux_orl

Corrected some signal paths to work at the gc level testench.

Change 90001 on 2003/03/13 by tien@tien_r400_devel_marlboro

cmask fixes, EMU still incorrect

Change 89992 on 2003/03/13 by jayw@jayw_r400_linux_marlboro

LEDA fixes.

Change 89972 on 2003/03/13 by paulv@paulv_r400_linux_marlboro

Fixed timing loop and the stall_head_addr_calc_b signal for the quad_cache_tc_rtr
signal.

Change 89954 on 2003/03/13 by viviana@viviana_crayola_linux_orl

Tracker to test the interface between the Vertex Input Control of the sq and the
   VSR's of the SP, during a write.

Change 89943 on 2003/03/13 by askende@askende_r400_linux_marlboro

releasing fix related to param gen inputs into the interpolators

Change 89936 on 2003/03/13 by bhankins@fl_bhankins_r400_win

add comment

Change 89935 on 2003/03/13 by bhankins@fl_bhankins_r400_win

simplify.

Change 89887 on 2003/03/12 by vbhatia@vbhatia_r400_linux_marlboro

Initial checkin

Change 89863 on 2003/03/12 by mmantor@mmantor_crayola_linux_orl

<Fix bug in the sx export buffers that prevents data corruption.  Single color exports
should now work also added a test to the sq_regress file to check export buffer back
pressure>

Change 89848 on 2003/03/12 by askende@askende_r400_linux_marlboro
```

```
1. added opcode decoding to detect PRED_POP,INV, CLR and RESTORE in sp_macc.v
       2. routed the results of the above opcodes into the outputs of the scalar engine

Change 89835 on 2003/03/12 by jayw@jayw_r400_linux_marlboro

Clean LEDA errors.

Change 89810 on 2003/03/12 by hartogs@fl_hartogs

Minor corrections to tbtrk_sqtp.
   Modularized the SP/SX tracker.

Change 89808 on 2003/03/12 by wlawless@wlawless_r400_linux_marlboro

separated the probe and flush completely... Made the first flush
addr free flowing and locked when flush is busy..

Change 89804 on 2003/03/12 by jayw@jayw_r400_linux_marlboro

up to date..

Change 89778 on 2003/03/12 by askende@askende_r400_linux_marlboro

fix related to :
         1. vector pixel kill
         2. infinity propagation in case of DOT2ADD vector opcode

Change 89766 on 2003/03/12 by paulv@paulv_r400_linux_marlboro

Performance optimization for tile cache.

Change 89762 on 2003/03/12 by johnchen@johnchen_r400_linux_marlboro_rbrc

cache write problem when planes are almost filled up

Change 89746 on 2003/03/12 by hartogs@fl_hartogs

Modularized the SQTP tracker (per Chris Gray's request).

Change 89740 on 2003/03/12 by hartogs@fl_hartogs

Somehow this one slipped through the cracks. This one should have been changed when the
"pc_free_cnt_q" signal width
   was increased from 7 to 8 bits.

Change 89686 on 2003/03/12 by rmanapat@rmanapat_r400_sun_marlboro
```

```
fixed a syntax mistake

Change 89654 on 2003/03/11 by jayw@jayw_r400_linux_marlboro

Fix for sample mask zero killed quads and cache inflight coherency.

Change 89588 on 2003/03/11 by hartogs@fl_hartogs

Added tp_sq.dmp to list.

Change 89538 on 2003/03/11 by hartogs@fl_hartogs

Interim Check-in

Change 89518 on 2003/03/11 by hartogs@fl_hartogs

Dummy files currently uses by tb_sqsp testbench.

Change 89516 on 2003/03/11 by hartogs@fl_hartogs

Interim check-in.

Change 89515 on 2003/03/11 by hartogs@fl_hartogs

Changed "pc_free_cnt_q" to 8 bits so that it could represent the maximum free count of
128. Propagated this change to
   ss/sq_status_reg.v and to ss/sq_vtx_thread_buff.v. Added ifdef SIM code to check for
overflow and underflow of this
   counter.
   Added condition for simultaneous occurrance of pc_alloc and pb_dealloc_vld.

Change 89510 on 2003/03/11 by kmeekins@kmeekins_r400_win

Changed compareScSq to not compare pixel mask on events or dealloc.

Change 89498 on 2003/03/11 by paulv@paulv_r400_linux_marlboro

Fixed state machine and read_quad_cache signal to take into account the empty
propagation delay for the hiz data fifo.

Change 89491 on 2003/03/11 by vbhatia@vbhatia_r400_linux_marlboro

Example stimulus generation tests

Change 89479 on 2003/03/11 by paulv@paulv_r400_linux_marlboro

Removed unused bit from i/o of conversion logic.
```

Change 89474 on 2003/03/11 by vromaker@vromaker_r400_linux_marlboro

change to make texture requests wait on alu_instr_pending

Change 89448 on 2003/03/10 by mmantor@mmantor_crayola_linux_orl

<1. Added timestamp to dum_mem read and write from same location error message. 2. Moved flat/gouroud shading and provoking vertex to sq-pc from the sx and worked on ptr instead of data 3.Added control for the texture cylinderical wrapsubcycling. 4. Add rt parameter cache ptr selection in sq 5.Clamped and wrapped pc_ptrs in sq 6. Added support for points and lines in the parameter cache ptr determination. 7. prep seperate write address for export to memory 8. tmp fix for deallocation of export memory deallocation. 9. remove some old comment out code and redundant logic >

Change 89419 on 2003/03/10 by jayw@jayw_r400_linux_marlboro

Fixes for very 16 bit srepeat and urepeat precision. hang fix, bad state for tiling, unknowns for rc cache signal

Change 89412 on 2003/03/10 by wlawless@wlawless_r400_linux_marlboro

changes how the ms_lock is sent on probe

Change 89390 on 2003/03/10 by tien@tien_r400_devel_marlboro

Fix for min/mag determination

Change 89374 on 2003/03/10 by johnchen@johnchen_r400_linux_marlboro

plane_in_cache fix for multi cache access quads

Change 89352 on 2003/03/10 by bhankins@fl_bhankins_r400_win

edits

Change 89344 on 2003/03/10 by bhankins@fl_bhankins_r400_win

changes

Change 89341 on 2003/03/10 by bhankins@bhankins_crayola_linux_orl

changes

Change 89340 on 2003/03/10 by bhankins@bhankins_crayola_linux_orl

changes

Change 89330 on 2003/03/10 by askende@askende_r400_linux_marlboro

```
change related to flushing to zero the mantissa of the result when the exp <= 0

Change 89222 on 2003/03/09 by askende@askende_r400_linux_marlboro

fix related to SETGT instruction in the vector engine

Change 89136 on 2003/03/07 by johnchen@johnchen_r400_linux_marlboro

probe hit does not depend on if the cacheline is free or not.  Even if it is free,
it'll still be a hit

Change 89131 on 2003/03/07 by askende@askende_r400_linux_marlboro

releasing changes related to :
          1. CUBE opcode .
          2. forcing to zero the mantissa for denorm float results.

Change 89082 on 2003/03/07 by paulv@paulv_r400_linux_marlboro

Needed to loop back the alpha sat winner signal when doing 2-pass fog.

Change 89074 on 2003/03/07 by johnchen@johnchen_r400_linux_marlboro

fix typo

Change 89065 on 2003/03/07 by tien@tien_r400_devel_marlboro

Tied request_latency returning from TC to 0
min/mag fix.

Change 89061 on 2003/03/07 by rmanapat@rmanapat_r400_sun_marlboro

Tied request_latency back to 0 until problem is fixed or
signal is removed

Change 89049 on 2003/03/07 by johnchen@johnchen_r400_linux_marlboro

handful of compression fixes

Change 89043 on 2003/03/07 by nkociuk@nkociuk_r400_linux_marl

more register changes.  almost done...  just some top-level connections remaining

Change 89042 on 2003/03/07 by nkociuk@nkociuk_r400_linux_marl

extend busy...
```

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Change 89041 on 2003/03/07 by paulv@paulv_r400_linux_marlboro

Slight code simplification to the previous timing fix.

Change 89040 on 2003/03/07 by nkociuk@nkociuk_r400_linux_marl

cleanup

Change 89039 on 2003/03/07 by dougd@dougd_r400_linux_marlboro

added `include "register_addr.v"

Change 89031 on 2003/03/07 by paulv@paulv_r400_linux_marlboro

Minor timing fixes.

Change 89022 on 2003/03/07 by sallen@sallen_r400_lin_marlboro

ferret: tp/tc testbench getting closer

Change 88999 on 2003/03/07 by rramsey@rramsey_crayola_linux_orl

fix dum_mem instance to be 128 deep

Change 88996 on 2003/03/07 by wlawless@wlawless_r400_linux_marlboro

juat some small changes for multisample

Change 88989 on 2003/03/07 by bhankins@bhankins_crayola_linux_orl

update

Change 88929 on 2003/03/06 by vromaker@vromaker_r400_linux_marlboro

fix to CFS that prevents a new thread from entering when the thread ID
in the input pipe stage is different than the thread ID in the output pipe stage;
also changed triangle size to 150 for sq_tests test case pred_eq_vec

Change 88918 on 2003/03/06 by jayw@jayw_r400_linux_marlboro

Fix for rop_2d_using_shadow

Change 88895 on 2003/03/06 by subad@subad_r400_linux_marlboro

Tien's fix for some formats

Change 88886 on 2003/03/06 by nkociuk@nkociuk_r400_linux_marl
```

small fix...

Change 88884 on 2003/03/06 by nkociuk@nkociuk_r400_linux_marl

timing fix for perfmon stuff

Change 88866 on 2003/03/06 by paulv@paulv_r400_linux_marlboro

Fix for subnorm 16-bit floats.

Change 88839 on 2003/03/06 by nkociuk@nkociuk_r400_linux_marl

adding what will be the register interface for tcr

Change 88838 on 2003/03/06 by nkociuk@nkociuk_r400_linux_marl

more register changes..

Change 88836 on 2003/03/06 by nkociuk@nkociuk_r400_linux_marl

move some counters to tcf, where they belong...

Change 88833 on 2003/03/06 by donaldl@fl_donaldl_p4

Wrapper around ati_lrp_state_storage to register RBIU interface signals.

Change 88830 on 2003/03/06 by donaldl@fl_donaldl_p4

Delayed by 1 clk some of RBIU inputs/outputs to state storage modules (ie. w_addr[2:0], we, sel, cp, w_data[31:0], r_addr[2:0], re, r_data[31:0]). Done to reduce large fanout in post layout netlist.

Change 88816 on 2003/03/06 by dougd@dougd_r400_linux_marlboro

added ports to support cntx0_busy, cntx17_busy

Change 88814 on 2003/03/06 by askende@askende_r400_linux_marlboro

releasing a fix related to generation of an R400_FP_NAN when dealing with neg values in the case of SQRT instruction

Change 88811 on 2003/03/06 by nkociuk@nkociuk_r400_linux_marl

l2 lowhigh and high latency counters..

Change 88804 on 2003/03/06 by jayw@jayw_r400_linux_marlboro

Added comment.

```
Change 88801 on 2003/03/06 by jayw@jayw_r400_linux_marlboro

Fix for r400rb_color_channels and r400rb_tb

Change 88791 on 2003/03/06 by cbrennan@cbrennan_r400_linux_marlboro

Timing fixes on l2 tag generation.

Change 88777 on 2003/03/06 by paulv@paulv_r400_linux_marlboro

Fixed the sign of the final 22-bit rb fp result.

Change 88773 on 2003/03/06 by jayw@jayw_r400_linux_marlboro

Fix for r400rb_tb, breaks r400rb_mask_color_channels alpha.

Change 88762 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

updates

Change 88761 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

updates

Change 88760 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

updates

Change 88759 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

update to support 'size' field of sx_rb_quad.dmp

Change 88758 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

moved to ./tb_sx

Change 88756 on 2003/03/06 by bhankins@fl_bhankins_r400_win

moving to ./tb_sx

Change 88755 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

moved from ../

Change 88754 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

moved from ../
```

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Change 88753 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

moved from ../

Change 88752 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

initial checkin

Change 88750 on 2003/03/06 by wlawless@wlawless_r400_linux_marlboro

msaa fixes

Change 88745 on 2003/03/06 by bhankins@bhankins_crayola_linux_orl

added support for reading the 'size' field.  This is not a signal, and is not checked.

Change 88710 on 2003/03/05 by paulv@paulv_r400_linux_marlboro

Timing and a logic fix.

Change 88686 on 2003/03/05 by johnchen@johnchen_r400_linux_marlboro

hold off accesses to the cache when expand is not done

Change 88667 on 2003/03/05 by dclifton@dclifton_crayola_linux_orl

Fixed typo on red_addend0 for SREPEAT COLOR_4_4_4_4

Change 88659 on 2003/03/05 by jayw@jayw_r400_linux_marlboro

Bug fix for missing define.

Change 88639 on 2003/03/05 by vromaker@vromaker_r400_linux_marlboro

a few minor updates, mostly comment related; added q2 verison of
state_head_ptr for use in state read addr calcualtion in vtx thread buff

Change 88560 on 2003/03/05 by rramsey@RRAMSEY_P4_r400_win

only look at lower 5 bits of rbbm write data to get event id

Change 88556 on 2003/03/05 by kmeekins@kmeekins_r400_win

Modified quad select out and quad pair proc out trackers and dump
routines to handle and additional vector generation for last quad
pair of prim.
```

```
Change 88552 on 2003/03/05 by dougd@dougd_r400_linux_marlboro

needed to subtract RT base address (`SQ_FETCH_RT_0) from incoming address for RT writes
and reads.

Change 88548 on 2003/03/05 by rmanapat@rmanapat_r400_sun_marlboro

changes to request_latency signal instead of pulling but from q0_*_const[41]
during tfetch it pulled from q3_*const[41]

Change 88539 on 2003/03/05 by dclifton@dclifton_crayola_linux_orl

Fixed tmp_src_color18 assignment of overflow value

Change 88512 on 2003/03/05 by rramsey@rramsey_crayola_linux_orl

Fix a bug with the valid bit inits that was causing tri128_pix4 to fail
Change the vsr_ld machine to alternate between buf0 and buf1 so pattern
is deterministic and can be compared vs emulator

Change 88504 on 2003/03/05 by wlawless@wlawless_r400_linux_marlboro

some decrement inflight for fragment tiles stuff for the sample mask zero case

Change 88458 on 2003/03/04 by tien@tien_r400_devel_marlboro

Fixed for request_* signals

Change 88448 on 2003/03/04 by jayw@jayw_r400_linux_marlboro

Fix for non_blend not being set during allocation.

Change 88447 on 2003/03/04 by jayw@jayw_r400_linux_marlboro

Fix for DST.

Change 88435 on 2003/03/04 by subad@subad_r400_linux_marlboro

Tien's fixes for rf expansions for format 10_11_11, 11_11_10 and
       2_10_10_10

Change 88423 on 2003/03/04 by nkociuk@nkociuk_r400_linux_marl

perfmon..

Change 88414 on 2003/03/04 by johnchen@johnchen_r400_linux_marlboro

bug fixes for expand
```

```
Change 88411 on 2003/03/04 by rmanapat@rmanapat_r400_sun_marlboro

Added support for base addr calcs for cube mapping and
SOI fix for Kevin

Change 88400 on 2003/03/04 by vromaker@vromaker_r400_linux_marlboro

fix for dealloc_space width; status register and thread buffer updates for
status register writes; status register fix for clearing the event_valid (and all
other bits) on a pop; new_thread flag now generated in the instr fetch module and
send dowm thru the AIQ; fix for the setting of thread_valid status

Change 88399 on 2003/03/04 by paulv@paulv_r400_linux_marlboro

A few more possible timing fixes.

Change 88317 on 2003/03/04 by kevino@kevino_r400_linux_marlboro

        Added SOI counters at a few interfaces

Change 88289 on 2003/03/04 by nkociuk@nkociuk_r400_linux_marl

sensitivity list fix

Change 88223 on 2003/03/03 by tien@tien_r400_devel_marlboro

Fixes in tp_input and tpc_fifos in the selection of tex/vtx
Fixed connection of norm/denorm bits

Change 88203 on 2003/03/03 by nkociuk@nkociuk_r400_linux_marl

sensitivity list fix...

Change 88178 on 2003/03/03 by rmanapat@rmanapat_r400_sun_marlboro

ff was missing posedge in decleration

Change 88171 on 2003/03/03 by wlawless@wlawless_r400_linux_marlboro

fixed fragment fifo from being written when full//////

Change 88162 on 2003/03/03 by nkociuk@nkociuk_r400_linux_marl

more changes for perf counters

Change 88160 on 2003/03/03 by jbrady@jbrady_r400_win
```

```
gate build for pa using structural macros

Change 88152 on 2003/03/03 by wlawless@wlawless_r400_linux_marlboro

fixed a non_blend after blend from setting the non_blend bit

Change 88129 on 2003/03/03 by rmanapat@rmanapat_r400_sun_marlboro

Fix SOI behaviour in TCA

Change 88124 on 2003/03/03 by rmanapat@rmanapat_r400_sun_marlboro

Change signal name to match spec...mimic behavior of request_latency
signal from tp_input.v in tpc_fifos.v

Change 88117 on 2003/03/03 by hartogs@fl_hartogs

Added dum_mem_p2 model back into the code with USE_BEHAVE_MEM compiler directive.

Change 88096 on 2003/03/03 by smburu@smburu_r400_linux_marlboro

Changed cmdscout to output.

Change 88094 on 2003/03/03 by rramsey@RRAMSEY_P4_r400_win

Fix a bug related that was allowing non-rts/rts quads to get packed with rts/non-rts
quads when the switch happened with a quad in the overflow buf

Change 88074 on 2003/03/03 by wlawless@wlawless_r400_linux_marlboro

fixed the 128b thing correctly

Change 88058 on 2003/03/03 by kevino@kevino_r400_linux_marlboro

      Removed sequence based write counters from L2 logic and all the sequence-based
misscount>writecount signals from the pipe.  Seq num are still generated in L2 pipe and
should be removed

Change 88011 on 2003/03/03 by jayw@jayw_r400_linux_marlboro_rbrc

More random fixes for DST reads.

Change 88005 on 2003/03/03 by bhankins@fl_bhankins_r400_win

checkin ongoing work

Change 87997 on 2003/03/03 by dougd@dougd_r400_linux_marlboro
```

missing term in eqn for skid_re_hold for tex_rt_rd caused tex_rt_rd_req to assert for only 1 cycle and not wait for the data ack

Change 87995 on 2003/03/03 by kevino@kevino_r400_linux_marlboro

Send TPC/TP the request latency bit

Change 87990 on 2003/03/03 by wlawless@wlawless_r400_linux_marlboro

128b pixels needed to check both sides of cache to stop in blend mode

Change 87947 on 2003/03/02 by jayw@jayw_r400_linux_marlboro_rbrc

Merged my dst required state changes with Paul's.

Change 87946 on 2003/03/02 by jayw@jayw_r400_linux_marlboro_rbrc

blend dst required logic needed updating to handle blend on/off and more!

Change 87945 on 2003/03/02 by donaldl@donaldl_crayola_unix_orl

Fanout of state variable indices to help post layout timing.

Change 87944 on 2003/03/02 by donaldl@fl_donaldl_p4

Fanout of state variable indices to help post layout timing.

Change 87889 on 2003/03/01 by askende@askende_r400_linux_marlboro

fix related to :
1. NaN and Inf when executing MAX4 opcode

Change 87871 on 2003/03/01 by johnchen@johnchen_r400_linux_marlboro

z expand for planes overflow