





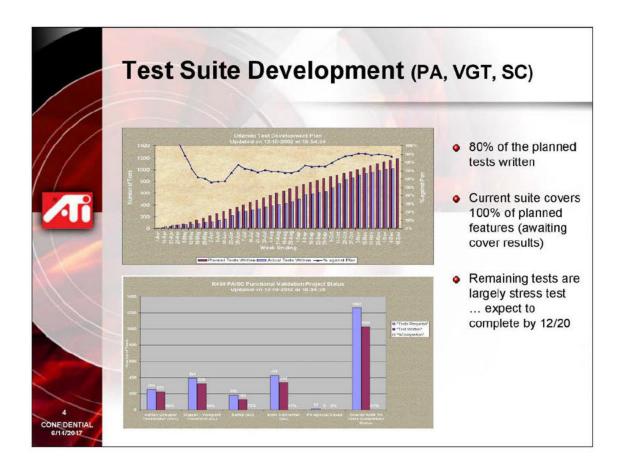
Orlando Hardware Status

- CP / RBBM / VGT / PA / SC / SC_B 100% coded
- Gate Level simulations of all blocks started
- Synthesis / Timing improvements in process
- Real Time Streams implemented
 - Status: Passed first RTS and mixed NRTS/RTS test
- Code Coverage results being reviewed for feedback to Validation team













Block Validation

Block Level Test Regressions

Test Bench	Tests Run	Tests Pass	% Pass	Report Date
VGT	2308	2308	100%	12/09/02
CP/RBBM	902	890	98%	12/10/02
sc	2308	2198	95%	12/10/02
PA	2309	2201	95%	12/10/02

- Block Level Random Testing
 - VGT / PA / SC Block Randoms coded & passing 100%
 - PA / SC Chip Randoms passing
 - VGT / CP Chip Randoms started



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