




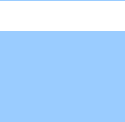
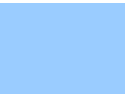
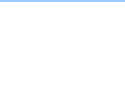
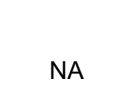








Design	RTL Coding	RTL regress	Gate regress	Area	Synthesis timing	Internal Worst timing	External Worst timing	Target timing	Violation
BIF	100%				SCLK				
MC	95%				SCLK				
HDP	100%				MCLK				
VIP/ROM/I2C	100%				SCLK				
Display	100%				FCP				
					SCLK				
					PIXCLK				
					P2GCLK				
					OV0CLK				
					TMDS				
					TVOUT				
					DVOCLK				
DFT/IO System	100%				NA				
	NA				NA	NA	NA	NA	NA

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Design		RTL specs	RTL coding	Emulation	Tests Written
display	dcp	100%	100%	100%	100%
	lb	100%	100%	98%	98%
	scl	100%	100%	98%	91%
	crtc	100%	100%	100%	100%
	dispout	100%	100%	100%	100%
	tvout	100%	100%	80%	50%
-----		-----	-----	-----	-----
dccg		100%	100%	no emu	no tests
dccif		100%	100%	no emu	no tests
rbbmif		100%	100%	no emu	no tests
dmif		100%	100%	no emu	no tests
vga		100%	100%	99%	100%
vip		100%	100%	100%	100%
VideolP(DC)					
BIF		90%	90%	90%	30%
IDCT		100%	100%	100%	100%
Total					

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Design		Clock	Area (mm2)	Area accuracy	Timing
display	dcp	2.25	2.41	100%	3.72
	lb	2.25	1.42	100%	3.25
	scl	2.25	1.39	100%	3.23
	crtc	2.25	0.25	100%	2.25
	dispout	2.25	0.67	100%	3.13
	tvout	10.00	0.93	100%	10.76
vga		2.25	0.39	100%	4.43
vip		2.25	0.49	100%	2.38
VideoIP(DC)			8.27	97%	
BIF		14.00	1.63	99%	12.39
		3.50			3.50
		2.25			2.78
IDCT		2.25	1.22	99%	2.90
Total					

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Design	features	EMU	Completed	Planned	Added
VidoeIP(DC)	display	100%	143	143	0
		#DIV/0!			
		100%	89	89	
		#DIV/0!			
		100%	54	54	
	#DIV/0!				
	vga	100%	100	100	
vip	100%	72	72		
Subtotal		100%	458	458	0
IDCT		100%	396	396	
Total		100%	854	854	0

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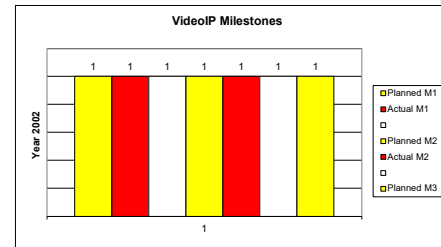
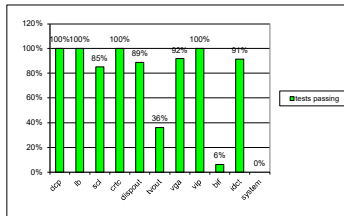
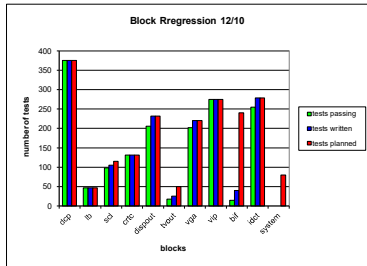
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Design	features	RTL regress	Tests passing	Tests Written	Tests Planned	Tests written
VideoP(DC)	DC					
	dcp	100%	375	375	375	100%
	lb	100%	47	47	47	100%
	scl	85%	98	105	115	91%
	crtc	100%	131	131	131	100%
	dispout	80%	206	232	232	100%
	tvout	36%	18	25	50	50%
	vga	92%	202	220	220	100%
	vip	100%	275	275	275	100%
	BIF	bif	6%	15	40	240
IDCT	idct	91%	255	279	279	100%
IDCT	system	0%	0	0	80	0%
Total		93%	1607	1689	1724	98%

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Design	features	RTL regress	Tests passing	Tests Written	Tests Planned	
VideoP(DC)	dcp	32%	57	180	202	
	lb	21%	3	14	18	
	scl	38%	3	8	78	
	crtc	44%	15	34	50	
	dispout	54%	29	54	79	
	tvout	54%	29	54	79	
	vga	65%	22	34	154	
	vip	100%	270	270	275	
	BIF		7%	15	225	240
	IDCT		86%	240	279	279
IDCT		86%	240	279	279	
Total		63%	495	783	798	

Design	features	Planned M1	Achieved M1	Planned M2	Achieved M2	Planned M2	Achieved M2
VideoP(DC)	dcp	30-Apr	31-May				
	lb	30-Apr	31-May				
	scl	30-Apr	31-May				
	crtc	30-Apr	31-May				
	dispout	30-Apr	31-May				
	tvout	30-Apr	31-May				
	vga	30-Apr	31-May				
	vip	30-Apr	31-May				
	BIF	bif	30-May				
	IDCT	idct	30-May	30-Jun			
IDCT	idct	30-May	30-Jun				
Total							



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