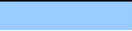









Design	RTL Coding	RTL regress	Gate regress	Area	Synthesis timing	Internal Worst timing	External Worst timing	Target timing	Violation
BIF	100%				SCLK BCLK AGPCLK				
MC	95%				MCLK SCLK MCLK				
HDP	100%				SCLK BCLK				
VIP/ROM/I2C	100%				SCLK FCP				
Display	100%				SCLK PIXCLK P2GCLK OV0CLK TMDS TVOUT DVOCLK				
DFT/IO System	100% NA				NA NA	NA	NA	NA	NA

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Design		RTL specs	RTL coding	Emulation	Tests Written
display	dcp	100%	100%	100%	100%
	lb	100%	100%	100%	98%
	scl	100%	100%	100%	98%
	crtc	100%	100%	100%	100%
	dispout	100%	100%	100%	100%
	tvout	100%	100%	80%	50%
vga		100%	100%	99%	100%
vip		100%	100%	100%	100%
BIF		95%	95%	90%	30%
IDCT		100%	100%	100%	100%

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Design		Clock	Area (mm2)	Area accuracy	Timing (flops)
display	dcp	2.50	1.81	99%	3.93
	lb	2.50	1.11	99%	2.07
	scl	2.50	1.36	99%	4.58
	crtc	2.50	0.23	99%	2.19
	dispout	2.50	0.58	99%	2.16
	tvout	10.00	0.81	99%	21.81
vga		2.50	0.35	99%	4.27
vip		2.50	0.49	100%	2.94
VideolP(DC)			7.04	99%	
BIF		14.00	1.63	98%	14.00
		3.50			2.96
		2.50			2.10
IDCT		2.50	1.22	99%	2.33

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Design	features	EMU	Completed	Planned	Added
VideolP(DC)	display	100%	143	143	0
		#DIV/0!			
		100%	89	89	
		#DIV/0!			
		100%	54	54	
		#DIV/0!			
	vga	100%	100	100	
vip	100%	72	72		
Subtotal		100%	458	458	0
IDCT		100%	396	396	
Total		100%	854	854	0

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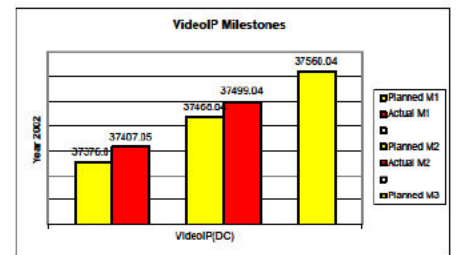
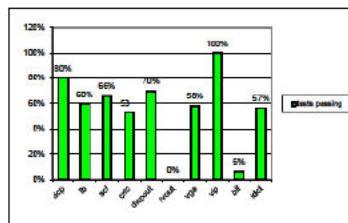
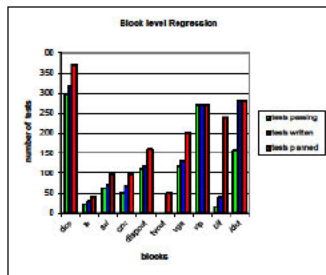
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Design	features	RTL reg/rets	Tests passing	Tests Written	Tests Planned	Test written %
	dcp	80%	296	315	310	86%
	ip	60%	24	30	42	75%
	act	66%	64	73	97	75%
	crfc	53%	51	68	96	71%
	dispout	70%	112	119	160	74%
	ivout	0%	0	0	50	0%
	vga	60%	117	131	202	60%
	vip	100%	271	271	271	100%
BIF	bif	6%	15	40	240	17%
IDCT	idct	57%	158	279	279	100%
Total		61%	1100	1329	1895	

Design	features	RTL reg/rets	Tests passing	Tests Written	Tests Planned
	dcp	32%	57	160	202
	ip	21%	3	14	18
	act	30%	3	8	79
	crfc	44%	15	34	50
	dispout	54%	29	54	79
	dispout	54%	29	54	79
	vga	60%	22	34	164
	vip	100%	270	270	275
BIF	bif	7%	15	235	240
IDCT	idct	85%	240	279	279
Total		51%	259	564	518

Design	features	Planned M1	Achieved M1	Planned M2	Achieved M2	Planned M3	Achieved M3
	dcp	30-Apr	31-May		31-Jul	31-Aug	31-Oct
	ip	30-Apr	31-May		31-Jul	31-Aug	31-Oct
	act	30-Apr	31-May		31-Jul	31-Aug	31-Oct
	crfc	30-Apr	31-May		31-Jul	31-Aug	31-Oct
	dispout	30-Apr	31-May		31-Jul	31-Aug	31-Oct
	dispout	30-Apr	31-May		31-Jul	31-Aug	31-Oct
	vga	30-Apr	31-May		31-Jul	31-Aug	31-Oct
	vip	30-Apr	31-May		31-Jul	31-Aug	31-Oct
BIF	bif	30-May					
IDCT	idct	30-May	30-Jun				
Total							

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