

Α

Δ

DOCKET

Author: Clay Taylor	
Issue To:	Copy No:
R400 Prir	nitive Assembly
Block Overvie	w VGT / CL / SU / SC
	ver 0.1
Overview:	
AUTOMATICALLY UPDATED FIELDS: Document Location: Document1 Current Intranet Search Title : R400 Generic	Spec
Name/Dept	APPROVALS Signature/Date
Remarks:	
THIS DOCUMENT CONTAINS SUBSTANTIALLY DETRIMENTAL INC. THROUGH UNAUT	INFORMATION THAT COULD BE TO THE INTEREST OF ATI TECHNOLOGIES HORIZED USE OR DISCLOSURE.
"Copyright 2000, ATI Technologies Inc. All rights re work created in 2000. The use of this copyright not unpublished work. The copyright notice is not an adm proprietary information and trade secrets of ATI. No p form or by any means without the prior written permis	eserved. The material in this document constitutes an unpublished tice is intended to provide notice that ATI owns a copyright in this hission that publication has occurred. This work contains confidential part of this document may be used, reproduced, or transmitted in any sion of ATI Technologies Inc."
R400_Orlando_Top.doc 💷 7198 Bytes*** ©	Reference Copyright Notice on Cover Page © ***

11/01/01 11:57 AM

AMD1044 0182535



Table Of Contents

1.1 Features 6 1.2 Performance 6 2. EXTERNAL INTERFACES 6 2.1 An interface 6 3. BLOCK DIAGRAM 7 4. ? 7 5. LOGIC DESCRIPTION 7 5.1 Description of each subblock 8 6. REGISTER SPECIFICATION 8 6.1 Performance/Debug 8 7. PHYSICAL DESIGN 8 8. AREA ESTIMATE 8 9 PEREORMANCE ISSUES 8	1.	OVERVIEW	. 6
1.2 Performance. 6 2. EXTERNAL INTERFACES 6 2.1 An interface. 6 3. BLOCK DIAGRAM. 7 4. ? 7 5. LOGIC DESCRIPTION 7 5.1 Description of each subblock 8 6. REGISTER SPECIFICATION 8 6.1 Performance/Debug 8 7. PHYSICAL DESIGN 8 8. AREA ESTIMATE 8 9. PEREORMANCE ISSUES 8	1.1	Features	. 6
2. EXTERNAL INTERFACES 6 2.1 An interface 6 3. BLOCK DIAGRAM 7 4. ? 7 5. LOGIC DESCRIPTION 7 5.1 Description of each subblock 8 6. REGISTER SPECIFICATION 8 6.1 Performance/Debug 8 7. PHYSICAL DESIGN 8 8. AREA ESTIMATE 8 9. PEREORMANCE ISSUES 8	1.2	Performance	. 6
2.1 An interface 6 3. BLOCK DIAGRAM 7 4. ? 7 5. LOGIC DESCRIPTION 7 5.1 Description of each subblock 8 6. REGISTER SPECIFICATION 8 6.1 Performance/Debug 8 7. PHYSICAL DESIGN 8 8. AREA ESTIMATE 8 9. PEREORMANCE ISSUES 8	2.	EXTERNAL INTERFACES	. 6
3. BLOCK DIAGRAM	2.1	An interface	.6
4. ?	3.	BLOCK DIAGRAM	.7
5. LOGIC DESCRIPTION 7 5.1 Description of each subblock 8 6. REGISTER SPECIFICATION 8 6.1 Performance/Debug 8 7. PHYSICAL DESIGN 8 8. AREA ESTIMATE 8 9. PERFORMANCE ISSUES 8	4.	?	.7
5.1 Description of each subblock 8 6. REGISTER SPECIFICATION 8 6.1 Performance/Debug 8 7. PHYSICAL DESIGN 8 8. AREA ESTIMATE 8 9. PERFORMANCE ISSUES 8	5.	LOGIC DESCRIPTION	.7
6. REGISTER SPECIFICATION 8 6.1 Performance/Debug 8 7. PHYSICAL DESIGN 8 8. AREA ESTIMATE 8 9. PERFORMANCE ISSUES 8	5.1	Description of each subblock	. 8
6.1 Performance/Debug .8 7. PHYSICAL DESIGN .8 8. AREA ESTIMATE .8 9. PERFORMANCE ISSUES .8	6.	REGISTER SPECIFICATION	. 8
7. PHYSICAL DESIGN	6.1	Performance/Debug	. 8
8. AREA ESTIMATE	7.	PHYSICAL DESIGN	. 8
9 PERFORMANCE ISSUES 8	8.	AREA ESTIMATE	. 8
	9.	PERFORMANCE ISSUES	. 8

R400_Orlando_Top.doc 🗆 7198 Bytes*** ©

DOCKET

Α

LARM

eference Copyright Notice on Cover Page @ ***

11/01/01 11:57 AM

AMD1044 0182536

Find authenticated court documents without watermarks at docketalarm.com.



Revision Changes:

Rev 0.0 (Clay Taylor) Date: October 29,2001 Initial revision. Document started

R400_Orlando_Top.doc 0 7198 Bytes*** ©

Reference Copyright Notice on Cover Page © ***

11/01/01 11:57 AM

AMD1044 0182537



Find authenticated court documents without watermarks at <u>docketalarm.com</u>.



Introduction

This document will briefly describe at a top level the interfaces, requirements and motivations for the Primitive Assembly group of blocks of the R400 chip. The primary goal of this document is to provide a first-tier description of the blocks which are being designed by the Orlando site and their relative location within the graphics pipeline.

The acronym PA (Primitive Assembly) is being used to encompass many of the Orlando-owned blocks. The individual blocks will be identified as follows:

- 1. Command Processor (CP). (Not considered to be part of PA)
- 2. Vertex Grouper Tesselator (VGT).
- 3. Clipper & Viewport Transform (CL).
- 4. Setup Engine (SU).
- 5. Scan Converter Barycentric Interpolator (SC)

There will be a separate spec for each of these blocks which will be maintained by the block owners. The details of the functionality, internal interfaces, etc can be found in the individual specifications.

1.1 Requirements & Functional Descriptions

The R400 3D pipe is similar in function to previous ATI designs in that it takes in primitives (typically triangles), performs vertex processing (Index Reuse Detection, Vertex Fetching, Transform, Lighting, PVS, Viewport Xform), performs primitive processing (Clipping and Setup), rasterizes primitives into pixels (Scan Conversion and Perspective Correct Barycentric Coord Calculation), performs pixel processing (Texture Lookup, Pixel Shaders, Alpha Blend/Test, Z Test, Stencil, etc). In ALU architecture it is most similar to R300 in that it uses Vertex Shaders and Pixel Shaders only for Vertex and Pixel processing, but varies significantly from R300 in pipeline architecture. Because of this, there may be significant reuse of R300 logic for several blocks in the design (i.e. setup, viewport transform, barycentric interpolation), but there is very little commonality in block-level interfaces, etc.

Many of the requirements for the CP/PA blocks are quite similar to the equivalent blocks' requirements for R300. The top-level requirements of the blocks are as follows (see individual specs for real details):

Command Processor

The CP has many functions. It's primary role is to fetch command stream data (which includes state updates, draw packets, 2D packets, IDCT packets, etc) and deliver it to the various blocks in the chip. Please see the CP spec for details of requirements, functionality, interfaces, etc.

Vertex Grouper / Tesselator

This block has two distinct functions, vertex reuse/grouping and tesselation.

The first, and most frequently used is the vertex reuse/grouping. The functionality is very similar to the R100/R200/R300 vertex reuse block. The requirement is that the block detect vertex index reuse within the previous 16 (or 14 or 15 TBD) vertex indices. If a hit is detected, this vertex is not resubmitted for vertex processing. The vertex grouper will gather together 64 (32 or 16 for RV400, RL400) vertices for submission to the unified shader (vertex shader). This group of 64 vertices is processed as one "unit" in the shader pipeline. Partial units will be submitted when an end of packet is detected. This block will send primitives to the CLIP block to perform clipping, etc on the post-shaded vertices.

Tesselation is not well defined currently. This block will be used to tessellate primitives and create indices and/or weights to assist in the tessellation process. The base requirements are that at least discrete and continuous N-Patch tessellation be supported. Many methods have been discussed, but no detailed requirements have been formulated. There is also an undefined requirement that the tessellation engine be programmable.

Clipper & Viewport Transform

This block has two distinct functions, clipping and viewport transform.

The clipping process is similar to that of R100,R200,R300 with the notable exception that only position and barycentric weights are clipped/created, none of the triangle (vertex) attributes are clipped.

The viewport transform process is very similar to previous generations, with the possible exception that viewport transform may be performed prior to clipping.

Setup Engine

DOCKE

R400_Orlando_Top.doc 💷 7198 Bytes*** 🤅

RM

Reference Copyright Notice on Cover Page © ***

11/01/01 11:57 AM

AMD1044 0182538

Find authenticated court documents without watermarks at docketalarm.com.

ORIGINATE DATE	EDIT DATE	DOCUMENT-REV. NUM.	PAGE
29 October, 2001	[date \@ "d MMMM,	R400 Generic Spec	5 of 8

The requirements are very similar to that of the R300 setup engine with the notable exception (again) that none of the primitive (vertex) attribute data other than position (x,y,z,w) and barycentric weights are processed in the setup engine. The fact that the clipper no longer clips attribute data requires that the setup engine be able to compute barycentric weight gradients for triangles with non-0/non-1 barycentric values at the vertices (probably at a reduced rate). This block is also responsible for computing start-points and gradients for Z, and the barycentric weights (I,J,K). It is also responsible for back-face culling, scissor-culling, fill-mode conversion (tri->point, tri->wireframe), polygon (z) offset, and line-stipple texture coordinate calculations.

Scan Converter / Barycentric Interpolator

The functional requirements of the R400 scan converter are similar to that of R300 except that the performance and tiling requirements are different due to the single SC of R400 versus the multi-SC of R300. The scan converter must determine which 8x8 pixel "tiles" are "hit" by a primitive and submit these tiles to the Render Backend for hierarchical z culling. It must determine which 2x2 pixel "quads" are "hit" by a primitive for submission to the pixel shader pipeline. These quads must be assembled into a group of 16 quads (64 pixels) in an order which is advantageous to texture caching (TBD). It must produce 2 quads per clock (8 pixels per clock) in order to keep up with the render backend desired rate of 8 pixels per clock. The SC must support points, lines, triangles, and rects, line stipple, poly stipple, line antialiasing, and polygon antialiasing?. It must support walking algorithms advantageous to 3D as well as 2D overlapping blits. It must conform to fill rules for both DX and OGL.

The SC (BI) must also compute the perspective-correct barycentric weights for each of the pixels that it outputs to the pixel shader (sequencer).

R400_Orlando_Top.doc 🗆 7198 Bytes*** G

DOCKE

Reference Copyright Notice on Cover Page © ***

11/01/01 11:57 AM

AMD1044 0182539

Find authenticated court documents without watermarks at docketalarm.com.

DOCKET



Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time** alerts and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

