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R400 Primitive Assembly

Block Overview VGT / CL / SU / SC

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Introduction

This document will briefly describe at a top level the interfaces, requirements and motivations for the Primitive Assembly group of blocks of the R400 chip. The primary goal of this document is to provide a first-tier description of the blocks which are being designed by the Orlando site and their relative location within the graphics pipeline.

The acronym PA (Primitive Assembly) is being used to encompass many of the Orlando-owned blocks. The individual blocks will be identified as follows:

1. Command Processor (CP). (Not considered to be part of PA)
2. Vertex Grouper Tesselator (VGT).
3. Clipper & Viewport Transform (CL).
4. Setup Engine (SU).
5. Scan Converter Barycentric Interpolator (SC)

There will be a separate spec for each of these blocks which will be maintained by the block owners. The details of the functionality, internal interfaces, etc can be found in the individual specifications.

1.1 Requirements & Functional Descriptions

The R400 3D pipe is similar in function to previous ATI designs in that it takes in primitives (typically triangles), performs vertex processing (Index Reuse Detection, Vertex Fetching, Transform, Lighting, PVS, Viewport Xform), performs primitive processing (Clipping and Setup), rasterizes primitives into pixels (Scan Conversion and Perspective Correct Barycentric Coord Calculation), performs pixel processing (Texture Lookup, Pixel Shaders, Alpha Blend/Test, Z Test, Stencil, etc). In ALU architecture it is most similar to R300 in that it uses Vertex Shaders and Pixel Shaders only for Vertex and Pixel processing, but varies significantly from R300 in pipeline architecture. Because of this, there may be significant reuse of R300 logic for several blocks in the design (i.e. setup, viewport transform, barycentric interpolation), but there is very little commonality in block-level interfaces, etc.

Many of the requirements for the CP/PA blocks are quite similar to the equivalent blocks' requirements for R300. The top-level requirements of the blocks are as follows (see individual specs for real details):

Command Processor

The CP has many functions. It's primary role is to fetch command stream data (which includes state updates, draw packets, 2D packets, IDCT packets, etc) and deliver it to the various blocks in the chip. Please see the CP spec for details of requirements, functionality, interfaces, etc.

Vertex Grouper / Tesselator

This block has two distinct functions, vertex reuse/grouping and tesselation.

The first, and most frequently used is the vertex reuse/grouping. The functionality is very similar to the R100/R200/R300 vertex reuse block. The requirement is that the block detect vertex index reuse within the previous 16 (or 14 or 15 TBD) vertex indices. If a hit is detected, this vertex is not resubmitted for vertex processing. The vertex grouper will gather together 64 (32 or 16 for RV400, RL400) vertices for submission to the unified shader (vertex shader). This group of 64 vertices is processed as one "unit" in the shader pipeline. Partial units will be submitted when an end of packet is detected. This block will send primitives to the CLIP block to perform clipping, etc on the post-shaded vertices.

Tesselation is not well defined currently. This block will be used to tessellate primitives and create indices and/or weights to assist in the tessellation process. The base requirements are that at least discrete and continuous N-Patch tessellation be supported. Many methods have been discussed, but no detailed requirements have been formulated. There is also an undefined requirement that the tessellation engine be programmable.

Clipper & Viewport Transform

This block has two distinct functions, clipping and viewport transform.

The clipping process is similar to that of R100,R200,R300 with the notable exception that only position and barycentric weights are clipped/created, none of the triangle (vertex) attributes are clipped.

The viewport transform process is very similar to previous generations, with the possible exception that viewport transform may be performed prior to clipping.

Setup Engine

The requirements are very similar to that of the R300 setup engine with the notable exception (again) that none of the primitive (vertex) attribute data other than position (x,y,z,w) and barycentric weights are processed in the setup engine. The fact that the clipper no longer clips attribute data requires that the setup engine be able to compute barycentric weight gradients for triangles with non-0/non-1 barycentric values at the vertices (probably at a reduced rate). This block is also responsible for computing start-points and gradients for Z, and the barycentric weights (I,J,K). It is also responsible for back-face culling, scissor-culling, fill-mode conversion (tri->point, tri->wireframe), polygon (z) offset, and line-stipple texture coordinate calculations.

Scan Converter / Barycentric Interpolator

The functional requirements of the R400 scan converter are similar to that of R300 except that the performance and tiling requirements are different due to the single SC of R400 versus the multi-SC of R300. The scan converter must determine which 8x8 pixel "tiles'" are "hit" by a primitive and submit these tiles to the Render Backend for hierarchical z culling. It must determine which 2x2 pixel "quads" are "hit" by a primitive for submission to the pixel shader pipeline. These quads must be assembled into a group of 16 quads (64 pixels) in an order which is advantageous to texture caching (TBD). It must produce 2 quads per clock (8 pixels per clock) in order to keep up with the render backend desired rate of 8 pixels per clock. The SC must support points, lines, triangles, and rects, line stipple, poly stipple, line antialiasing, and polygon antialiasing?. It must support walking algorithms advantageous to 3D as well as 2D overlapping blits. It must conform to fill rules for both DX and OGL.

The SC (BI) must also compute the perspective-correct barycentric weights for each of the pixels that it outputs to the pixel shader (sequencer).

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