



R400 Program Review

December 11, 2002

ATI Corporate Presentation

Emulator

- ◆ SQ/SP/SX
 - Debugging HW / EMU numerical mismatches
- ◆ TP/TC
 - Debugging 3D/Volume textures
 - Debugging HW / EMU numerical mismatches
- ◆ RB/RC
 - Debugging MSAA Resolve
 - Shader depth export and Zpass counter not implemented
- ◆ MC/MH
 - Debugging ATI GART

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HW Verification (directed tests)

Block	Planned	% Written	% Running	% Passing
MC / MH	2300	96%	100%	94%
RB / RC	870	91%	86%	86%
SQ/SX/SP	1700	97%	100%	81%
TP / TC	5500	85%	13%	25%
*GC	4183			63%



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Random Validation

- GC/Chip level random validation library in place
 - Currently running ~200 tests/night on GC
 - Mostly RB, SP interpolator type tests
 - Running ~750 tests/night on RB/RC
 - Able to start random shaders in ~2-3 weeks
- MC / MH running ~740 test/night
- Need more machines and sim licenses



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Notes

- ◆ R400 Performance Verification Web Site

- Created a web site for the dissemination of R400 performance information and analysis
- Includes images from playback, dump files, synthetic test results, information on tools, links to drivers and emulators, etc...
- See <http://www.ma.atitech.com/r400/perfver/index.htm>



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R400 Capture & Playback Tools

● QS Capture Functionality

- The capture tool has fixed several issues and is now able to capture R400 PM4 packet streams and associated indirect data (VB's, Set State's, etc) from the OpenGL and D3D drivers
- Several benchmarks have had frames captured successfully including Quake3 and 3DWinbench2000 (Rust Valley and Hanger)
- Redesigned how VB's are captured to get around situations where the size of the data is essentially unknown by the driver (immediate mode, vertex buffer objects, etc)
- New CRC checking seems to be helping to keep the size of the bin files down somewhat by preventing the capturing of duplicate VB's and textures

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R400 Capture & Playback (con't)

• Playback Status

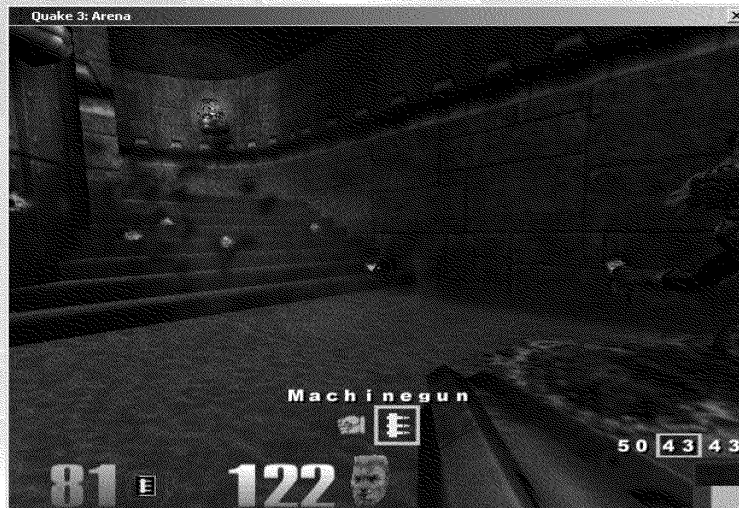
- R400 playback is now working!
- Have demonstrated the ability to playback a captured dump file on the emulator with minimal issues
- Playback on the simulator does not currently function properly
- Have played back frames of Quake3, 3DWinBench2000 (Rust Valley and Hanger)
- Have tried to capture frames of Doom3, 3DMark2001 and 2003 but these still have issues preventing them from emulating properly
- Support from QS/CMM, TO HWPG, and the driver folks has been wonderful and allowed all this to happen
- Images are on the web site

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R400 Capture & Playback (con't)

- ◆ Quake3 four.dm_68 (frame 40) emulated



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R400 Capture & Playback (con't)

- ◆ Quake3 four.dm_68 (frame 40) playback

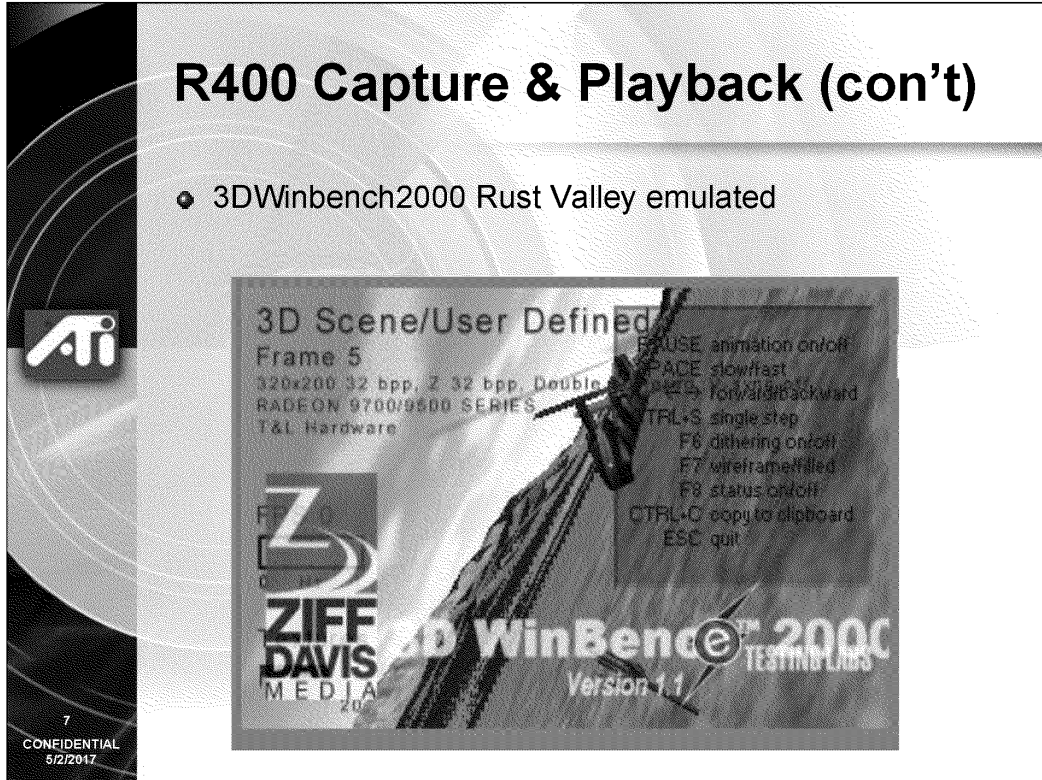


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R400 Capture & Playback (con't)

- ◆ 3DWinbench2000 Rust Valley emulated



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R400 Capture & Playback (con't)

- ◆ 3DWinbench2000 Rust Valley playback



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R400 Capture & Playback (con't)

◆ Capture and Playback Issues

- Working with QS/CMM and TO HWPG groups to solve capture and playback issues
- So far have addressed problems with CRC checks, LCC data capture, and a few other issues
- Still working on texture issue (see Q3 image) and Rust Valley problems – making good progress

◆ Driver Issues

- Working with the driver groups to solve problems with capture and playback of benchmarks that may be driver related
- To date, the driver folks have fixed a handful of relatively minor issues in their code ranging from bad assertions and memory leaks to initialization issues

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R400 Capture & Playback (con't)

◆ Simulator Playback Issues

- Have not been able to playback anything through the simulator ☹
- Have found and worked around several issues including lack of app support in the gc testbench and a (potential) issue with non zero FB start
- Latest theory is the shaders produced by the driver/compiler are hitting functionality in the hw that is not working properly; attempting to validate this by using simpler, known to work shaders...
- Lack of (standalone) shader assemblers and disassemblers make this tedious work; the compiler folks are helping out and creating a standalone disassembler to help out here...

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R400 Capture & Playback Tools

● Parser Tools

- TO HWPG have been continuing to support the R400 in the parser tools
- Next addition will be disassembly support for shaders using the same standalone disassembler that the compiler folks are working on...
- Some minor issues regarding GART support and ring buffer location are also expected

● Misc

- All participating groups are continuing weekly meetings to discuss schedules, implementation details, etc
- 2D capture and playback implementation is mostly complete; working on issues related to buffer location, etc...

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R400 Tools

• Optimizer Tool (PM4Opt)

- Will parse dump files from D3D and OpenGL drivers, analyze the render states, shader programs, etc, and update new dump file for playback
- Allows performance verification work to proceed without creating a dependency on the driver folks; information gleaned can be fed back to the R400 driver and compiler groups
- Based on R400 parser library tools; modeled against the R300 program
- With dump files now available and issues that may require this type of functionality, this tool will become more important

• Frame/Scissor Tools (DX8Logger, GLWrapper)

- Actively used as part of the perf ver process

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Performance Counters

● Current Status

- Most blocks have implemented performance counters including MH, VGT, SX(2), SQ, SC, RB(4), and PA (CP in but needs to use genperf tool hook into dumping mechanism)
- MC, TP/TC are still being worked on
- Over 400 counters total so far
- This includes “phantom” counters; not synthesized but allow dumping of all information after simulation

● Analysis

- Have not done much analysis with the counter information as of yet; this is somewhat gated by the gc and sim playback issues
- Plan is to be able to post process dumps to provide support for analysis of simulations, benchmark runs, etc

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Performance Counter Output

◆ Sample SC and RB Counts

```
----- start of module sc count -----
testbench.top.gc.gc.sc.usc_perfmon_qm_num_quads_low,      4096
testbench.top.gc.gc.sc.usc_perfmon_qm_covered_hi6_low,   256
testbench.top.gc.gc.sc.usc_perfmon_hier_num_quads_low,   4096
testbench.top.gc.gc.sc.usc_perfmon_det_num_quads_low,    4096
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h0_low,      0
testbench.top.gc.gc.sc.usc_perfmon_det_mask_hi_low,      0
----- end of module sc count -----
----- start of module rb count -----
testbench.top.gc.gc.rb_3_urb_perfmon_wrapper.urb_perfmon_rb_cntx17_busy_low,      4527
testbench.top.gc.gc.rb_3_urb_perfmon_wrapper.urb_perfmon_num_quads_passed_z_low,   1024
testbench.top.gc.gc.rb_3_urb_perfmon_wrapper.urb_perfmon_num_quads_failed_z_low,   1
testbench.top.gc.gc.rb_3_urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_exp_low, 0
testbench.top.gc.gc.rb_3_urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_sep_low, 0
testbench.top.gc.gc.rb_3_urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_low, 0
testbench.top.gc.gc.rb_3_urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_sep, 0
----- end of module rb count -----
```

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Directed Tests

● Gathering Data

- Have been primarily focusing on the capture and playback functionality and therefore not running too many directed tests
- Started running some compressed depth tests; the functionality is not quite there yet.
- Have spec'ed out several new directed tests to run focused on stressing the various caches in the RB and TC...

● Analysis

- Color fills still appear to be achieving peak goal of 8 pix/clock
- Blends are currently not hitting the peak numbers (~6 pix/clock) but have improved in the last few weeks by approx 10%; this is still under investigation

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Directed Tests (con't)

● Issues

- There are still some issues (known) that are preventing some of the performance tests from running properly (eg depth compression)
- Still want to use GC for all performance measurements; however, GC is not fully optimal yet preventing peak measurements for many directed tests...
- Need more time spent on back end processing of data; currently the process is too manual

● What's next

- Texturing tests, depth tests, stencil tests, etc
- Small batch tests, scissoring tests, shadows?, shaders?

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Application Tests

• Tgl to primlib port

- Allows R300 synthetic and high level (complex) tests to be run on R400 (SiV); will complement the directed tests
- Scripting language (dv) allows for large numbers of test variations
- Have been working towards getting more complex iterations of these tests to run on the emulator and simulator.

• Pseudo-benchmark apps

- Simpler apps that are designed to emulate known algorithms used in benchmarks
- Have Doom3 final shader pass and stencil shadow algorithms; R300 perfsuite complex tests will complement these tests

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Benchmark Tests

◆ 3DWinbench 2000

- Older DirectX tests...
- Several of these tests are being emulated, captured and played back with varying levels of success

◆ 3DMark 2001/2003

- Have DX7, DX8, and DX9 tests with most emphasis on the DX9 test (2003), also have some fill rate and geometry tests
- These tests are not working with enough functionality to consider capture and playback

◆ Quake3/Doom3

- Have been able to successfully emulate, capture, and playback frames of one Q3 demo
- Doom3 not ready yet...

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What does this all mean?

- ◆ We are now ready to begin running the actual driver dump files through the simulator
- ◆ This is a major goal of the performance verification team and a significant milestone for the project
- ◆ Tapeout should be gated by the functional verification of these benchmarks
- ◆ The performance analysis of these benchmark runs should also be considered as part of the readiness criteria



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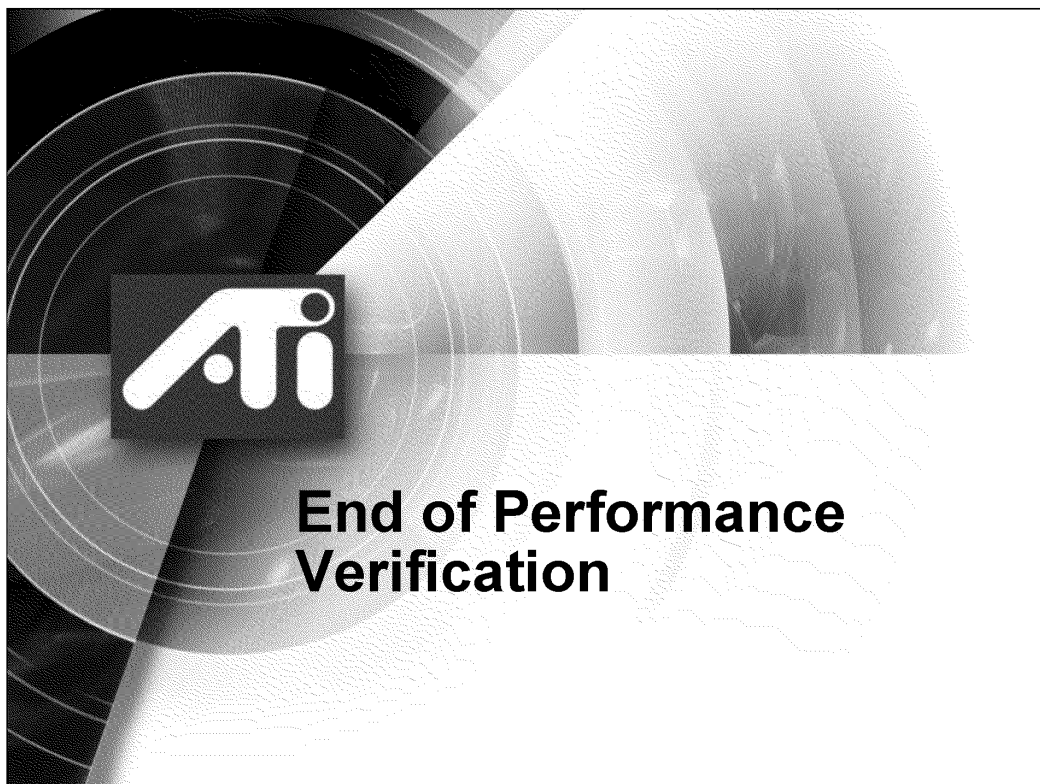
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Next Month...

- ◆ Continue to debug capture and playback tools
- ◆ Get playback on the simulator operational!!!
- ◆ Continue debug and analysis of benchmark (et al) applications – need to have 3DMark2003 and Doom3 working by the end of the month
- ◆ Focus more on directed tests – need gc operational both functionally and performant
- ◆ Run more of the perfsuite tests
- ◆ Provide hardware and software folks with useful performance information!!!
- ◆ Include set of performance regression tests as part of nightly build
- ◆ Continue to work with driver folks to facilitate benchmark runs on the simulator
- ◆ Successful implementation of R400 optimizer tool

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Directed Tests

Test	Planned	Written	% Written	Analyzed	% Analyzed
pv_triangle	28	21	75%	.5	0%
pv_texture	27	27	100%	0	0%
pv_texture_multi	12	4	33%	0	0%
pv_scissor	3	3	100%	0	0%
pv_fog	8	4	50%	0	0%
pv_line	8	4	50%	0	0%
pv_point	8	1	12%	0	0%
pv_rb	19	19	100%	0	0%
pv_tcache	12?	0	0%	0	0%
pv_hiz_sten	10?	0	0%	0	0%
pv_shader	12?	0	0%	0	0%
miscellaneous	20?	0	0%	0	0%
Total	167	83	50%	.5	0%

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Directed Tests

- Sample Data (RBRC color fills)

R400 Fill Rate Tests
Updated 1/15/2003

Test	Size	Grid (nxn)	RBRC				Pix/Clk (noflush)	R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
			Pixels	Clks	Pix/Clk						
rectmesh_wc32	64	1	4096	827	4.952842	7.17338	8	89.67%			
rectmesh_wc32	64	4	65536	8543	7.67131	7.90829	8	98.85%			
rectmesh_wc32	128	1	16384	2383	6.875367	7.702868	8	96.29%			
rectmesh_wc32	128	2	65536	8527	7.685704	7.923588	8	99.04%			
rectmesh_wc32	256	1	65536	8527	7.685704	7.923588	8	99.04%	7.871	100.66%	
trimesh_wc32	64	1	4096	862	4.75174	6.759076	8	84.49%			
trimesh_wc32	64	4	65536	8795	7.451507	7.674903	8	95.94%			
trimesh_wc32	128	1	16384	2407	6.806813	7.616922	8	95.21%			
trimesh_wc32	128	2	65536	8526	7.686606	7.924547	8	99.06%			
trimesh_wc32	256	1	65536	8585	7.63378	7.868412	8	98.36%			

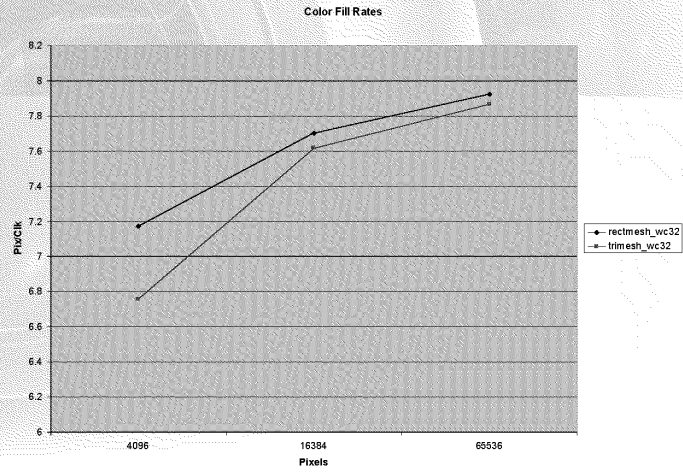
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Directed Tests

- RBRC color fill (increasing pixels)

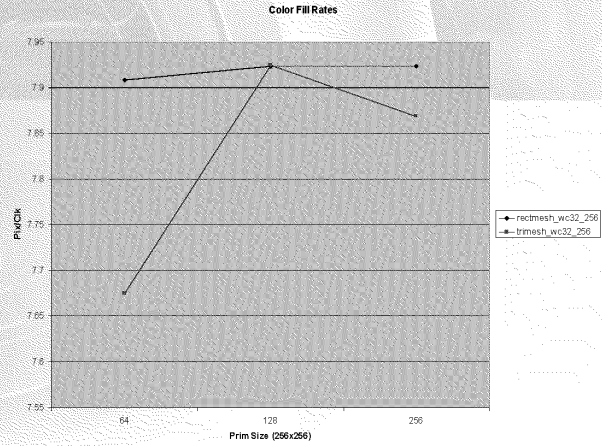


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Directed Tests

- ◆ RBRC color fill (constant pixels)



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Directed Tests

- Sample Data (RBRC blends)

R400 Fill Rate Tests
Updated 1/15/2003

Test	Size	Grid (nxn)	RBRC				R400 (Exp)	% R400 (Exp)	R300 (Sim)	% R300 (Sim)
			Pixels	Clks	Pix/Clk	Pix/Clk (noflush)				
rectmesh_rwc32	128	1	16384	2704	6.0591716	6.69281	8	75.74%		
rectmesh_rwc32	128	2	65536	11656	5.622512	5.748772	8	70.28%		
rectmesh_rwc32	256	1	65536	11272	5.8140525	5.949165	8	72.68%	7.0981	81.91%
trimesh_rwc32	128	1	16384	3095	5.2936995	5.771046	8	66.17%		
trimesh_rwc32	128	2	65536	11909	5.5030649	5.623959	8	68.79%		
trimesh_rwc32	256	1	65536	11571	5.6638147	5.791958	8	70.80%		

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```

----- start of module sc count -----
testbench.top.gc.gc.sc.usc_perfmon_qm_num_quads_low,      4096
testbench.top.gc.gc.sc.usc_perfmon_qm_covered_hl6_low,   256
testbench.top.gc.gc.sc.usc_perfmon_hier_num_quads_low,   4096
testbench.top.gc.gc.sc.usc_perfmon_det_num_quads_low,    4096
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h0_low,      0
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h1_low,      0
.
----- end of module sc count -----
----- start of module rb count -----
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_rb_cntx17_busy_low,      4527
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_passed_z_low,   1024
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_failed_z_low,    1
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_exp_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_sep_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_sep, 0
.
----- end of module rb count -----

```

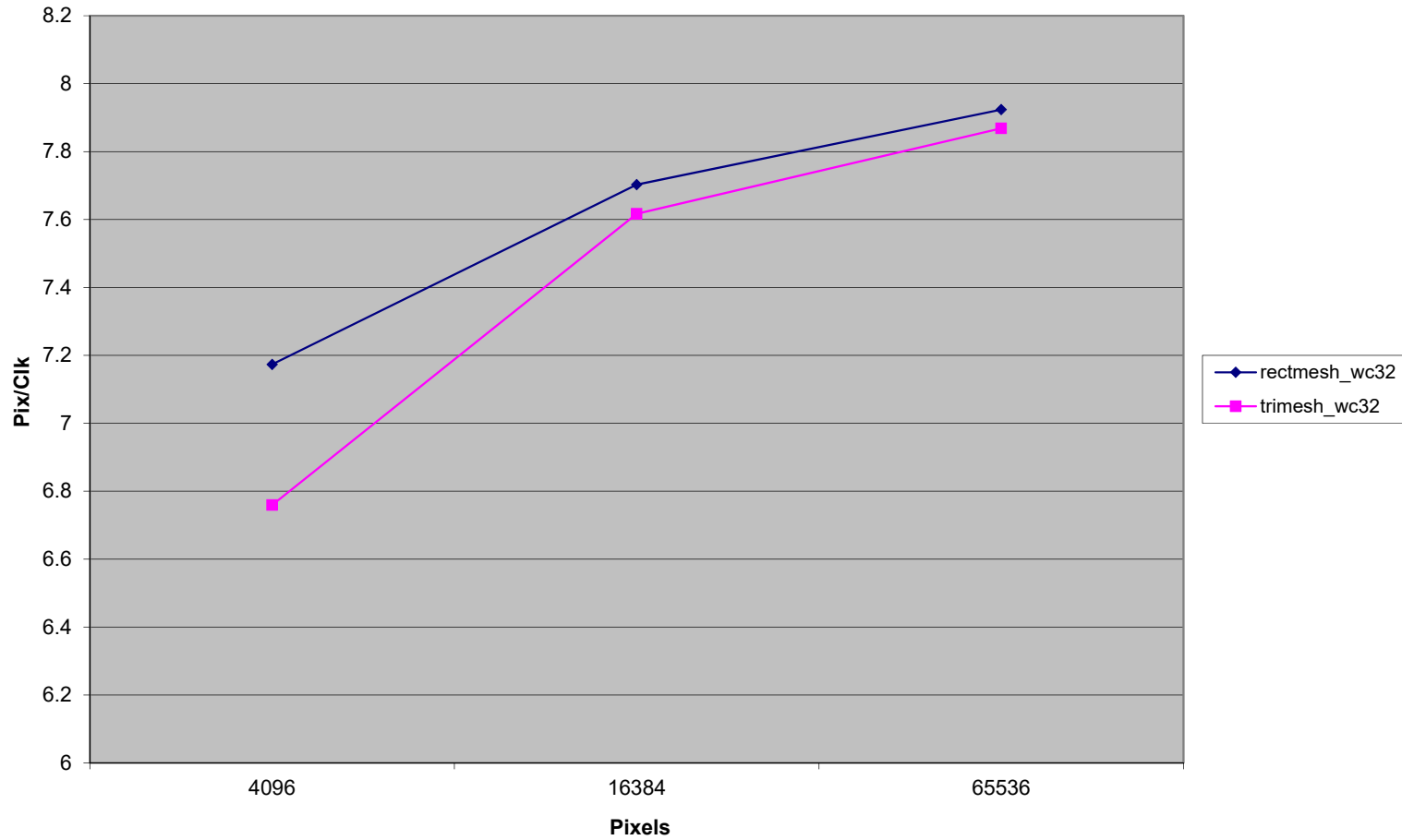
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R400 Fill Rate Tests
Updated 1/15/2003

RBRC										
Test	Size	Grid		Clks	Pix/Clk	Pix/Clk (noflush)	R400	% R400	R300	% R300
		(nxn)	Pixels				(Exp)	Expected	(Sim)	Simulated
rectmesh_wc32	64	1	4096	827	4.952842	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.67131	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.875367	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.685704	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.685704	7.923588	8	99.04%	7.871	100.66%
trimesh_wc32	64	1	4096	862	4.75174	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.451507	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.806813	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.686606	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.63378	7.868412	8	98.36%		

PROTECTIVE ORDER

Color Fill Rates



PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/xx/2003

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid Size (nxn)	RBRC		Test	Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
		Clks (all_bsys)	Pix/Clk							
rectmesh_wc32	64 1	827	4.9528	rectmesh_wc32	4096 7.17338	8	89.67%			
rectmesh_wc32	64 4	8543	7.6713	rectmesh_wc32	65536 7.90829	8	98.85%			
rectmesh_wc32	128 1	2383	6.8754	rectmesh_wc32	16384 7.702868	8	96.29%			
rectmesh_wc32	128 2	8527	7.6857	rectmesh_wc32	65536 7.923588	8	99.04%			
rectmesh_wc32	256 1	8527	7.6857	rectmesh_wc32	65536 7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64 1	862	4.7517	trimesh_wc32	4096 6.759076	8	84.49%			
trimesh_wc32	64 4	8795	7.4515	trimesh_wc32	65536 7.674903	8	95.94%			
trimesh_wc32	128 1	2407	6.8068	trimesh_wc32	16384 7.616922	8	95.21%			
trimesh_wc32	128 2	8526	7.6866	trimesh_wc32	65536 7.924547	8	99.06%			
trimesh_wc32	256 1	8585	7.6338	trimesh_wc32	65536 7.868412	8	98.36%			
rectmesh_wc32	64 1	827	4.9528	rectmesh_wc32	4096 7.17338	8	89.67%			
rectmesh_wc32	64 4	8543	7.6713	rectmesh_wc32	65536 7.90829	8	98.85%			
rectmesh_wc32	128 1	2383	6.8754	rectmesh_wc32	16384 7.702868	8	96.29%			
rectmesh_wc32	128 2	8527	7.6857	rectmesh_wc32	65536 7.923588	8	99.04%			
rectmesh_wc32	256 1	8527	7.6857	rectmesh_wc32	65536 7.923588	8	99.04%	7.871268	100.66%	
rectmesh_wc32	64 1	827	4.9528	rectmesh_wc32	4096 7.17338	8	89.67%			
rectmesh_wc32	128 1	2383	6.8754	rectmesh_wc32	16384 7.702868	8	96.29%			
rectmesh_wc32	256 1	8527	7.6857	rectmesh_wc32	65536 7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64 1	862	4.7517	trimesh_wc32	4096 6.759076	8	84.49%			
trimesh_wc32	128 1	2407	6.8068	trimesh_wc32	16384 7.616922	8	95.21%			
trimesh_wc32	256 1	8585	7.6338	trimesh_wc32	65536 7.868412	8	98.36%			

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R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid		GC		RBRC			R400	% R400	R300	% R300	Notes
	Size	(nxn)	Pixels	Cntx17 busy	Pix/Cik	Clks (all_busys)	Pix/Cik	(noflush)	Expected	Expected	Simulated	
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%		
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%		
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%		
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%		
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%		

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R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid		GC		RBRC			R400	% R400	R300	% R300	Notes
	Size	(nxn) Pixels	Cntx17 busy	Pix/Clk	Clks (all_busys)	Pix/Clk	Pix/Clk (noflush)	Expected	Expected	Simulated	Simulated	
rectmesh_wc32	64	1 4096			827	4.9528	7.17338	8	89.67%			
rectmesh_wc32	64	4 65536			8543	7.6713	7.90829	8	98.85%			
rectmesh_wc32	128	1 16384			2383	6.8754	7.702868	8	96.29%			
rectmesh_wc32	128	2 65536			8527	7.6857	7.923588	8	99.04%			
rectmesh_wc32	256	1 65536			8527	7.6857	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64	1 4096			862	4.7517	6.759076	8	84.49%			
trimesh_wc32	64	4 65536			8795	7.4515	7.674903	8	95.94%			
trimesh_wc32	128	1 16384			2407	6.8068	7.616922	8	95.21%			
trimesh_wc32	128	2 65536			8526	7.6866	7.924547	8	99.06%			
trimesh_wc32	256	1 65536			8585	7.6338	7.868412	8	98.36%			
rectmesh_rwc32	128	1 16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2 65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1 65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1 16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2 65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1 65536			11571	5.6638		8	70.80%			
rectmesh_wc32_t128pt	64	1 4096	2705	1.5142				6.4				
rectmesh_wc32_t128pt	64	4 65536						6.4				
rectmesh_wc32_t256pt	128	1 16384						6.4				
rectmesh_wc32_t256pt	128	2 65536						6.4				
rectmesh_wc32_t256pt	256	1 65536						6.4				
trimesh_wc32_t256pt	128	1 16384						6.4				apparent hang (RB->MC)
trimesh_wc32_t256pt	128	2 65536						6.4				
trimesh_wc32_t256pt	256	1 65536						6.4				
rectmesh_wc32_rwz	256	1 65536			271400000	2.4147						currently unoptimized
rectmesh_wc32_rwz	128	2 65536			286520000	2.2873						currently unoptimized

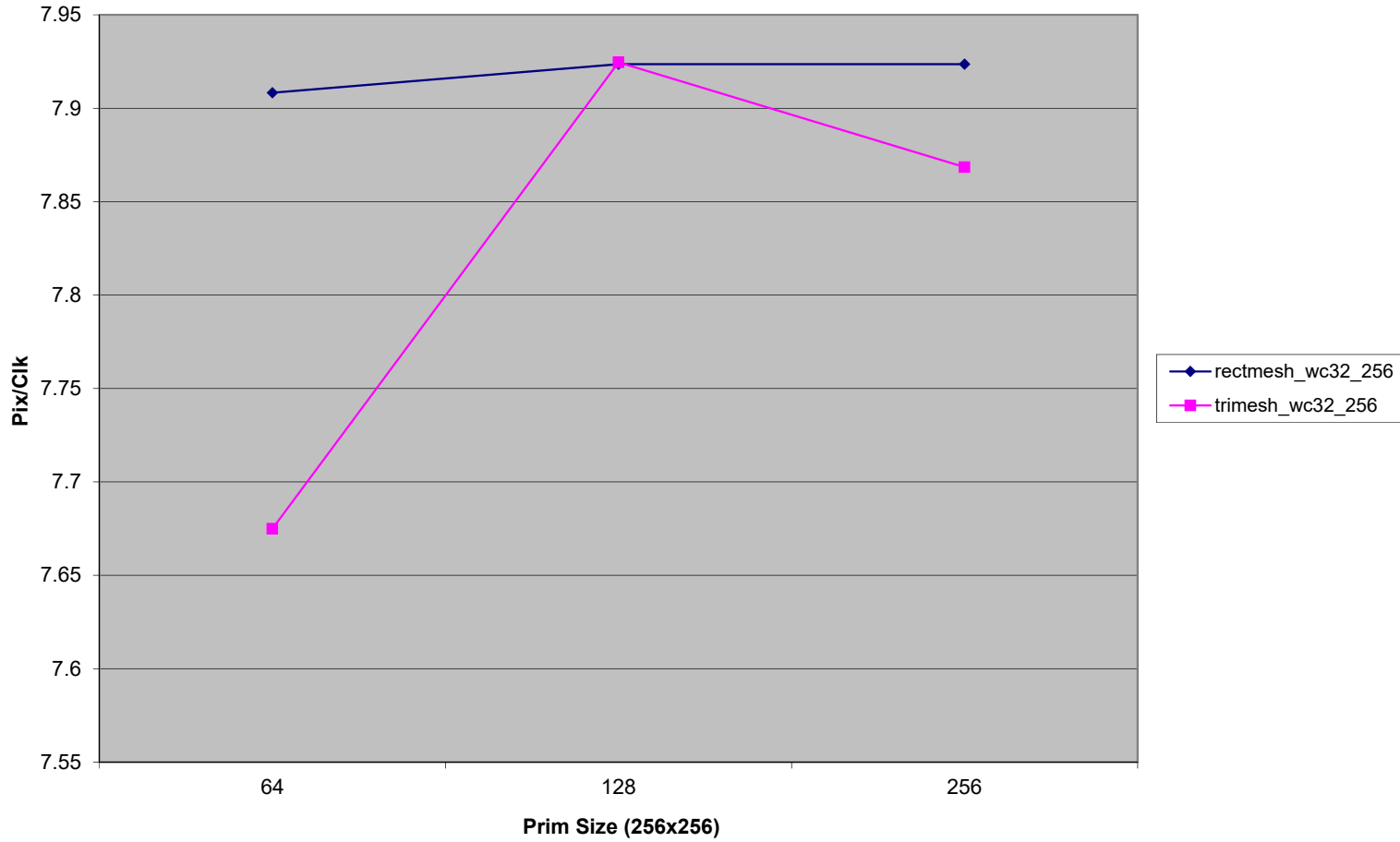
PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/15/2003

Test	RBRC						R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
	Grid Size (nxn)	Pixels	Clks	Pix/Clk	Pix/Clk (noflush)					
rectmesh_wc32	64	1	4096	827	4.9528	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.6713	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.8754	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.6857	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.6857	7.923588	8	99.04%	7.871 100.66%	
trimesh_wc32	64	1	4096	862	4.7517	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.4515	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.8068	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.6866	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.6338	7.868412	8	98.36%		

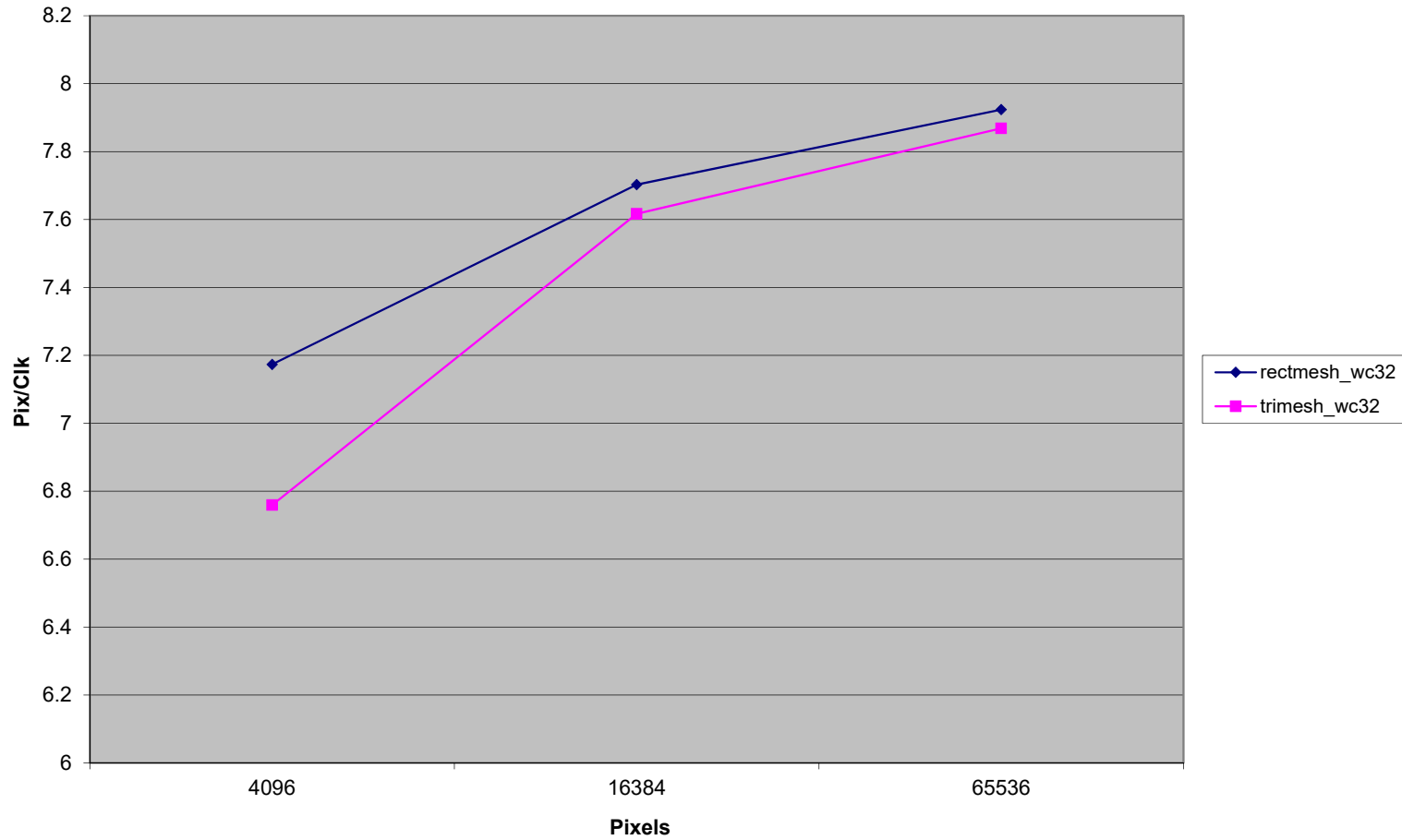
PROTECTIVE ORDER

Color Fill Rates



PROTECTIVE ORDER

Color Fill Rates



PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/xx/2003

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid		RBRC		Pix/Clk		R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
	Size (nxn)		Clocks (all_bsys)	Pix/Clk	Test	Pixels (noflush)					
rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32	65536	7.90829	8	98.85%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	1	862	4.7517	trimesh_wc32	4096	6.759076	8	84.49%		
trimesh_wc32	64	4	8795	7.4515	trimesh_wc32	65536	7.674903	8	95.94%		
trimesh_wc32	128	1	2407	6.8068	trimesh_wc32	16384	7.616922	8	95.21%		
trimesh_wc32	128	2	8526	7.6866	trimesh_wc32	65536	7.924547	8	99.06%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32	65536	7.868412	8	98.36%		
rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32	65536	7.90829	8	98.85%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	1	862	4.7517	trimesh_wc32	4096	6.759076	8	84.49%		
trimesh_wc32	128	1	2407	6.8068	trimesh_wc32	16384	7.616922	8	95.21%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32	65536	7.868412	8	98.36%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32_256	65536	7.90829	8	98.85%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32_256	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32_256	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	4	8795	7.4515	trimesh_wc32_256	65536	7.674903	8	95.94%		
trimesh_wc32	128	2	8526	7.6866	trimesh_wc32_256	65536	7.924547	8	99.06%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32_256	65536	7.868412	8	98.36%		

PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid		GC		RBRC			R400	% R400	R300	% R300	Notes	
	Size	(nxn)	Pixels	Cntx17 busy	Pix/Cik	Clks (all_busys)	Pix/Cik	(noflush)	Expected	Expected	Simulated		Simulated
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%			

PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid		GC		RBRC			R400	% R400	R300	% R300	Notes
	Size	(nxn) Pixels	Cntx17 busy	Pix/Clk	Clks (all_busys)	Pix/Clk	Pix/Clk (noflush)	Expected	Expected	Simulated	Simulated	
rectmesh_wc32	64	1 4096			827	4.9528	7.17338	8	89.67%			
rectmesh_wc32	64	4 65536			8543	7.6713	7.90829	8	98.85%			
rectmesh_wc32	128	1 16384			2383	6.8754	7.702868	8	96.29%			
rectmesh_wc32	128	2 65536			8527	7.6857	7.923588	8	99.04%			
rectmesh_wc32	256	1 65536			8527	7.6857	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64	1 4096			862	4.7517	6.759076	8	84.49%			
trimesh_wc32	64	4 65536			8795	7.4515	7.674903	8	95.94%			
trimesh_wc32	128	1 16384			2407	6.8068	7.616922	8	95.21%			
trimesh_wc32	128	2 65536			8526	7.6866	7.924547	8	99.06%			
trimesh_wc32	256	1 65536			8585	7.6338	7.868412	8	98.36%			
rectmesh_rwc32	128	1 16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2 65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1 65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1 16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2 65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1 65536			11571	5.6638		8	70.80%			
rectmesh_wc32_t128pt	64	1 4096	2705	1.5142				6.4				
rectmesh_wc32_t128pt	64	4 65536						6.4				
rectmesh_wc32_t256pt	128	1 16384						6.4				
rectmesh_wc32_t256pt	128	2 65536						6.4				
rectmesh_wc32_t256pt	256	1 65536						6.4				
trimesh_wc32_t256pt	128	1 16384						6.4				apparent hang (RB->MC)
trimesh_wc32_t256pt	128	2 65536						6.4				
trimesh_wc32_t256pt	256	1 65536						6.4				
rectmesh_wc32_rwz	256	1 65536			271400000	2.4147						currently unoptimized
rectmesh_wc32_rwz	128	2 65536			286520000	2.2873						currently unoptimized

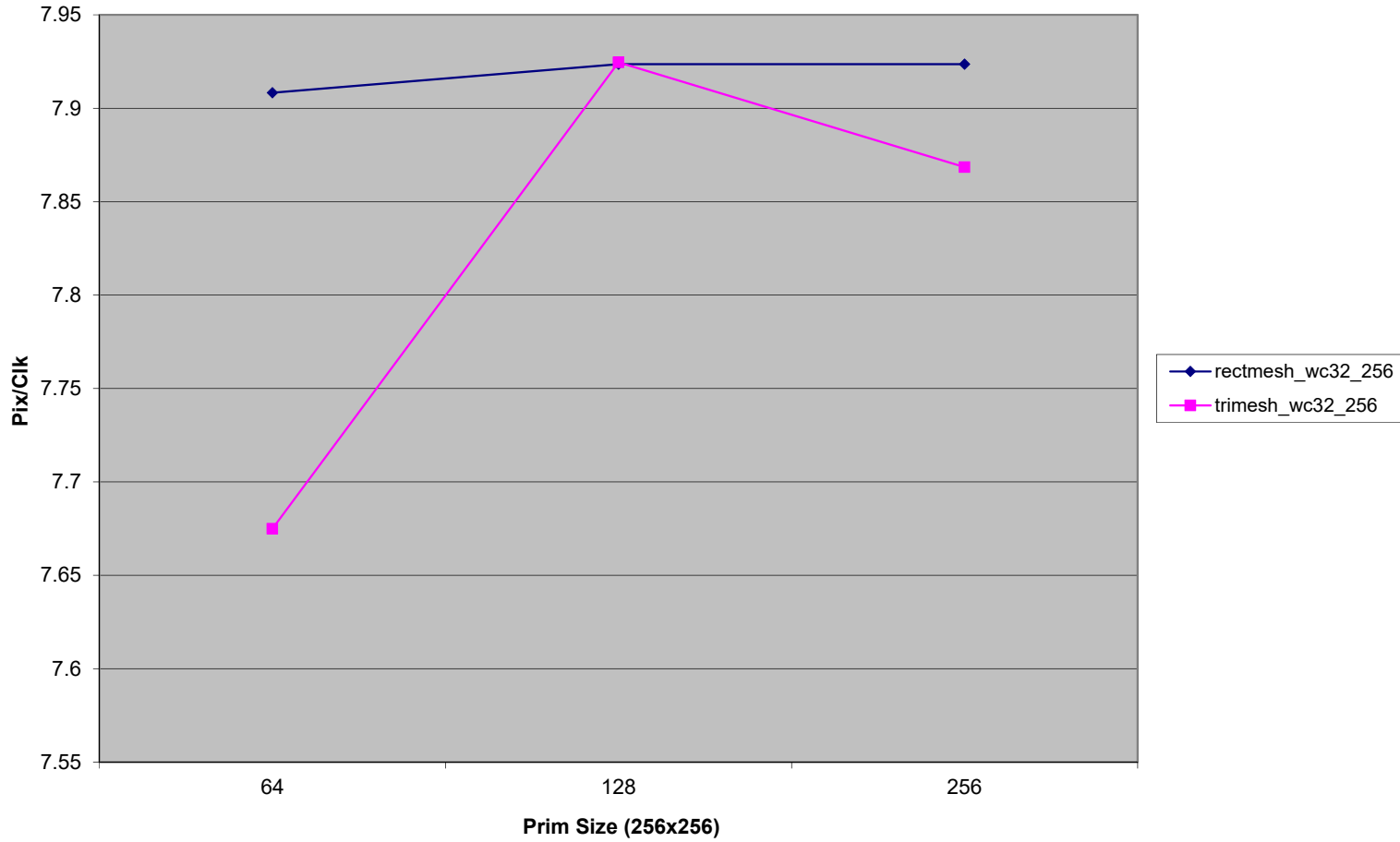
PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/15/2003

Test	RBRC						R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
	Grid Size (nxn)	Pixels	Clks	Pix/Clk	Pix/Clk (noflush)					
rectmesh_wc32	64	1	4096	827	4.9528	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.6713	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.8754	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.6857	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.6857	7.923588	8	99.04%	7.871	100.66%
trimesh_wc32	64	1	4096	862	4.7517	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.4515	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.8068	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.6866	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.6338	7.868412	8	98.36%		

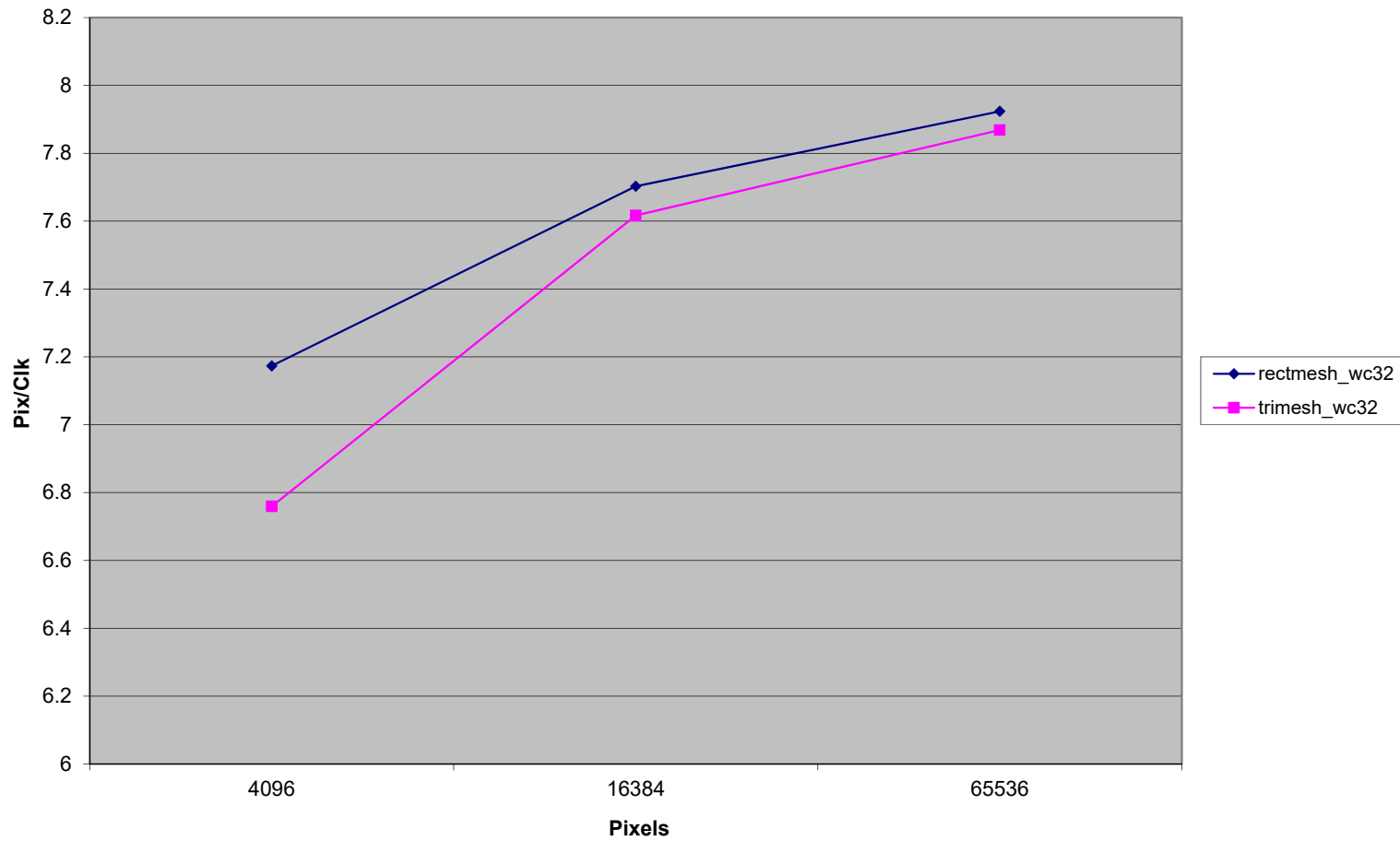
PROTECTIVE ORDER

Color Fill Rates



PROTECTIVE ORDER

Color Fill Rates



PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/xx/2003

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid		RBRC		Pix/Clk		R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
	Size (nxn)		Clks (all_bsys)	Pix/Clk	Pixels	(noflush)					
rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32	65536	7.90829	8	98.85%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	1	862	4.7517	trimesh_wc32	4096	6.759076	8	84.49%		
trimesh_wc32	64	4	8795	7.4515	trimesh_wc32	65536	7.674903	8	95.94%		
trimesh_wc32	128	1	2407	6.8068	trimesh_wc32	16384	7.616922	8	95.21%		
trimesh_wc32	128	2	8526	7.6866	trimesh_wc32	65536	7.924547	8	99.06%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32	65536	7.868412	8	98.36%		
rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32	65536	7.90829	8	98.85%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	1	862	4.7517	trimesh_wc32	4096	6.759076	8	84.49%		
trimesh_wc32	128	1	2407	6.8068	trimesh_wc32	16384	7.616922	8	95.21%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32	65536	7.868412	8	98.36%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32_256	65536	7.90829	8	98.85%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32_256	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32_256	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	4	8795	7.4515	trimesh_wc32_256	65536	7.674903	8	95.94%		
trimesh_wc32	128	2	8526	7.6866	trimesh_wc32_256	65536	7.924547	8	99.06%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32_256	65536	7.868412	8	98.36%		

PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/15/2003

Test	Size	Grid (nxn)	RBRC				R400 (Exp)	% R400 (Exp)	R300 (Sim)	% R300 (Sim)
			Pixels	Clks	Pix/Clk	Pix/Clk (noflush)				
rectmesh_rwc32	128	1	16384	2704	6.0591716	6.69281	8	75.74%		
rectmesh_rwc32	128	2	65536	11656	5.622512	5.748772	8	70.28%		
rectmesh_rwc32	256	1	65536	11272	5.8140525	5.949165	8	72.68%	7.0981 81.91%	
trimesh_rwc32	128	1	16384	3095	5.2936995	5.771046	8	66.17%		
trimesh_rwc32	128	2	65536	11909	5.5030649	5.623959	8	68.79%		
trimesh_rwc32	256	1	65536	11571	5.6638147	5.791958	8	70.80%		

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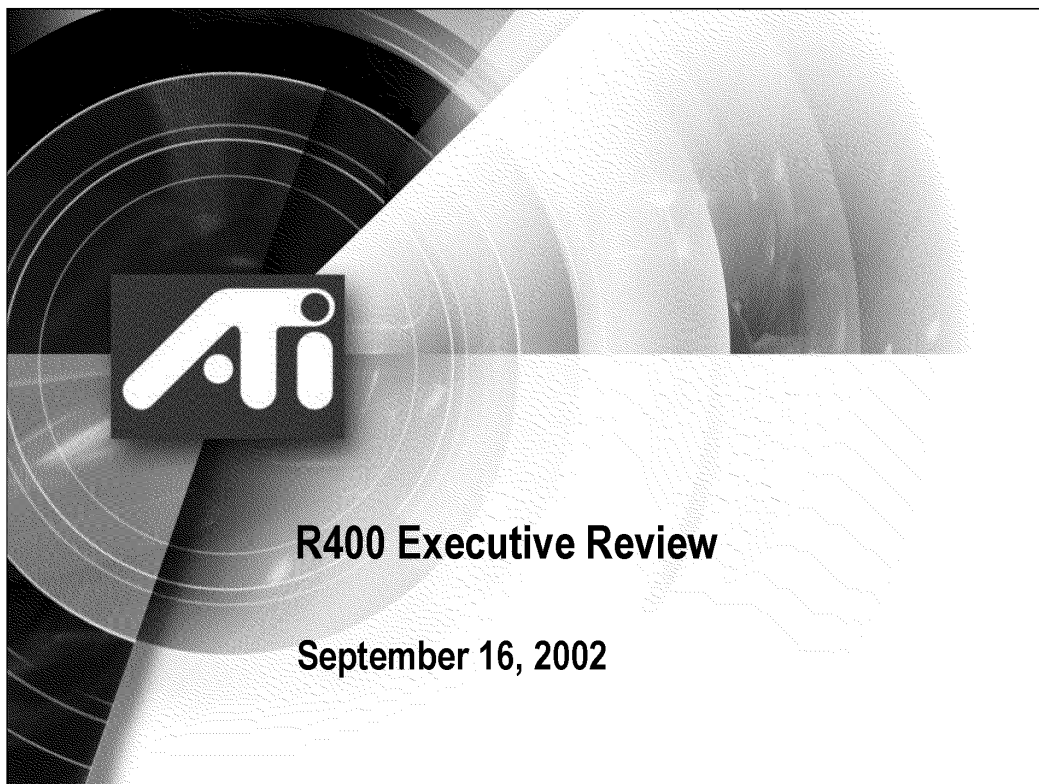
R400 Fill Rate Tests
Updated 1/xx/2003

Test	Grid		GC		RBRC			R400	% R400	R300	% R300	Notes	
	Size	(nxn)	Pixels	Cntx17 busy	Pix/Clk	Clks (all_busys)	Pix/Clk	(noflush)	Expected	Expected	Simulated		Simulated
rectmesh_wc32	64	1	4096			827	4.9528	7.17338	8	89.67%			
rectmesh_wc32	64	4	65536			8543	7.6713	7.90829	8	98.85%			
rectmesh_wc32	128	1	16384			2383	6.8754	7.702868	8	96.29%			
rectmesh_wc32	128	2	65536			8527	7.6857	7.923588	8	99.04%			
rectmesh_wc32	256	1	65536			8527	7.6857	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64	1	4096			862	4.7517	6.759076	8	84.49%			
trimesh_wc32	64	4	65536			8795	7.4515	7.674903	8	95.94%			
trimesh_wc32	128	1	16384			2407	6.8068	7.616922	8	95.21%			
trimesh_wc32	128	2	65536			8526	7.6866	7.924547	8	99.06%			
trimesh_wc32	256	1	65536			8585	7.6338	7.868412	8	98.36%			
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%			
rectmesh_wc32_t128pt	64	1	4096	2705	1.5142				6.4				
rectmesh_wc32_t128pt	64	4	65536						6.4				
rectmesh_wc32_t256pt	128	1	16384						6.4				
rectmesh_wc32_t256pt	128	2	65536						6.4				
rectmesh_wc32_t256pt	256	1	65536						6.4				
trimesh_wc32_t256pt	128	1	16384						6.4				
trimesh_wc32_t256pt	128	2	65536						6.4				apparent hang (RB->MC)
trimesh_wc32_t256pt	256	1	65536						6.4				
rectmesh_wc32_rwz	256	1	65536			271400000	2.4147						currently unoptimized
rectmesh_wc32_rwz	128	2	65536			286520000	2.2873						currently unoptimized

PROTECTIVE ORDER

R400 Fill Rate Tests
Updated 1/15/2003

Test	Grid Size (nxn)	Pixels	RBRC				R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
			Clks	Pix/Clk	Pix/Clk (noflush)					
rectmesh_wc32	64	1	4096	827	4.9528	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.6713	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.8754	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.6857	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.6857	7.923588	8	99.04%	7.871 100.66%	
trimesh_wc32	64	1	4096	862	4.7517	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.4515	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.8068	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.6866	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.6338	7.868412	8	98.36%		



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Block Logic Design and Timing

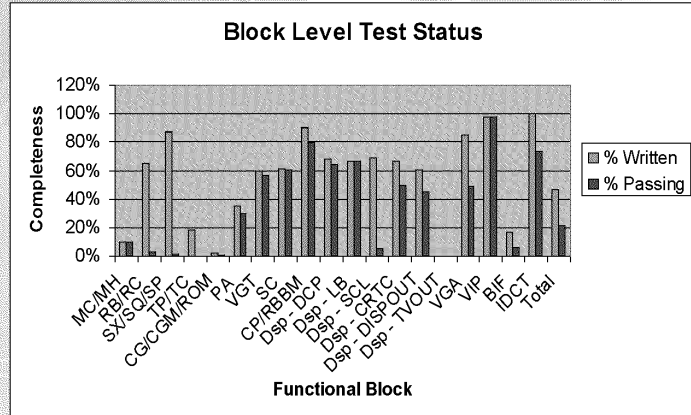
Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14.1nS)	
MC/MH	95% / 95%	9/23 - 9/16	N/A	10%	MC: 4.46; MH: 4.72	MCLK: 2.39	55 / 643
RB/RC	85% / 95%	9/30	95%	54%	RB: 8.2; RC: 2.5		16689 / 0
SXSQ	90%	9/16 - 9/30	99%	88%	SX: 2.74; SQ: 2.5		0 / 0
SP	100%	9/16	97%		SP: 2.5		0
TP/TC	97% / 95%	9/16	92%	18%	TP: 2.55; TC: 2.5		0 / 0
CG/CGM/ROM	100%	9/16	N/A	2%	CG: 2.5; CGM: 2.5; DBG: 2.5		0
PA	100%	9/16	100%	35%	PA: 2.69		110
VGT	100%	9/16	100%	59%	VGT: 2.75		33
SC	90%	9/16	95%	61%	SC: 2.73		140
RBBM	95%	9/16	N/A		RBBM: 2.95		95
CP	95%	9/16	90%	90%	CP: 2.85		439
Display - DCP	100%	9/16	90%	65%	Display: 11	PIXCLK: 2.5	8207
Display - LB	100%	9/16	100%	65%			
Display - SCL	70%	9/20	85%	65%			
Display - CRTG	100%	9/16	80%	65%			
Display - DISPOUT	95%	9/16	65%	65%			
Display - TVOUT	100%	9/16	30%	0%			
VGA	100%	9/16	99%	85%			
VIP	100%	9/16	100%	100%			
BIF	100%	9/16	90%	15%	BIF: 4.47	BCLK: 14.1	228
IDCT	100%	9/16	97%	97%	IDCT: 4.23		2898

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5/2/2017

ATI Corporate Presentation
Confidential

Block Level Test

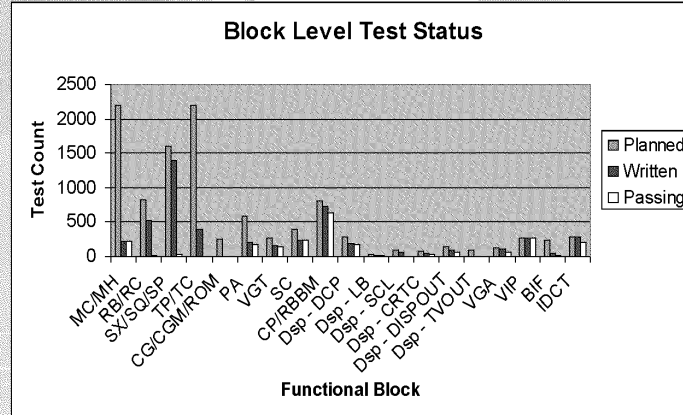


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CONFIDENTIAL
5/2/2017

ATI Corporate Presentation
Confidential

Block Level Test



4
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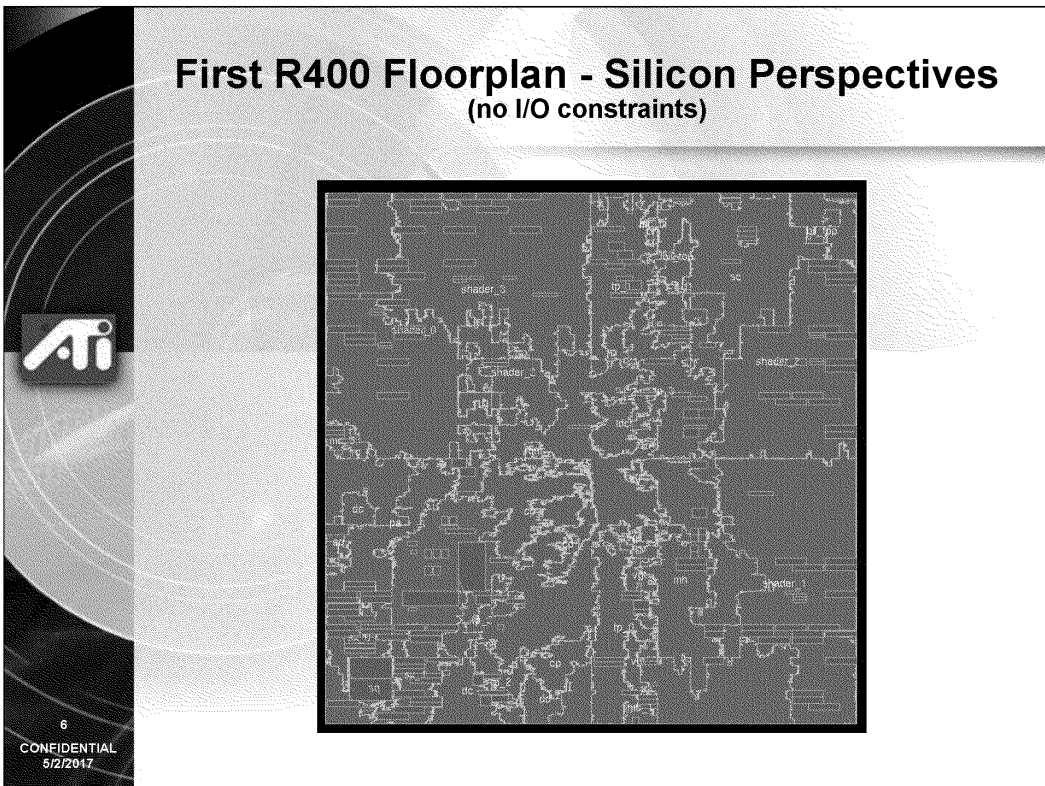
Synthesis & Physical Design

- **Hardware Emulation**
 - Initial IKOS compilation has begun to attempt R400 fit into a V15M
- **Synthesis continuing ...**
 - Blocks focusing on feature complete, not timing
 - Some blocks have made significant progress
 - Working top level interconnect issues
 - Working synthesis interface into physical design
- **Physical design**
 - Working group inter-relationships SiV<>Marlboro
 - Meeting often to synchronize teams
 - Physical Design web page under construction
- **Floorplan**
 - Initial padout done, needs to be reviewed
 - Initial netlist successfully read into SPC
 - Generated floorplan from SPC (no I/O constraint)

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First R400 Floorplan - Silicon Perspectives (no I/O constraints)



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Software Status (2D / MM)

- **Display Driver**

- BIOS: Design scope nearly complete, significant work identified, detailed plan is available
- CAIL: Design scope completed, ~15% implemented
- DAL/GXO: Design scope completed, significant work identified, work underway
- CMM/QS: Design scope completed, ~5% implemented
- 2D/NTx: Design scope completed, ~10% implemented
- 2D/9x: Design scope completed, ~5% implemented

- **Multimedia**

- Staffing and re-org complete; development work in progress.
- Schedule complete; under review.
- Design specs partially complete.
- MRD review meeting scheduled on Thursday.

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Software Status (3D)

- **D3D**

- BLT ~80% implemented
- Abstract state, state cache, surface create and drawing functions ~60% implemented
- Z/Stencil/Color ~50% implemented
- Texture ~40% implemented
- AA / HOS not yet begun

- **OpenGL**

- Multiple texture and texture state 80% complete
- IL to R400 binary translator 100% complete
- Z, stencil and alpha operations complete
- Vertex and fragment shaders complete

- **Compiler**

- Compiler integrated with SSM and D3D Driver 100%
- Triangle through compiler on emulator 100%

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R400 Area Summary

R400 Area Estimate (0.13)

Block	Pre Route Logic Area	Utilization	Post Route Logic Unit Area	Macro Area	Total Unit Area	R400 Qty	R400 Total	RV400 Qty	RV400 Total	
BIF (Bus Interface)	1,488,988	0.70	2,126,968	0	2,126,968	1	2,126,968	1.00	2,126,968	1%
DC (Display Controller)	2,277,800	0.70	3,825,429	1,775,349	5,605,377	1	5,605,377	1.00	5,605,377	4%
VP (Video In Port)	518,368	0.70	740,527	47,892	788,419	4	788,419	1.00	788,419	1%
CC (Clock Orig)	346,703	0.70	493,714	224,000	717,714	3	717,714	1.00	717,714	0%
ROM (ROM and debug controller)	193,104	0.70	275,363	0	275,363	1	275,363	1.00	275,363	0%
TSTC (Test Controller)	9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714	1%
CP (Control Processor)	3,369,939	0.70	4,804,484	1,497,941	6,302,925	1	6,302,925	1.00	6,302,925	4%
RBBM (Register Backbone Manager)	221,702	0.70	316,717	0	316,717	1	316,717	1.00	316,717	0%
MH (Memory Hub)	9,183,174	0.70	4,591,677	916,232	5,239,808	3	5,239,808	0.75	3,929,862	3%
VDI (Memory Hub)	347,452	0.70	2,10,946	84,403	1,295,049	1	1,295,049	1.00	1,295,049	1%
VGT (Vertex Group and Tessellate)	818,890	0.70	1,187,129	331,893	1,498,822	3	1,498,822	1.00	1,498,822	1%
PA (Viewport Memm Clip and Setup)	2,373,377	0.70	4,255,253	680,018	4,935,271	1	4,935,271	1.00	4,935,271	3%
SC (Scan Converter)	6,558,352	0.70	9,393,074	598,187	9,991,261	1	9,991,261	0.60	5,995,357	6%
SP (Shader Pipe)	3,922,400	0.70	6,703,429	2,013,708	8,717,138	4	8,717,138	2.00	16,434,276	21%
SD (Sampler)	1,173,596	0.70	1,953,692	3,380,846	4,084,338	1	4,084,338	1.00	4,084,338	3%
TP (Texture Pipe)	2,210,278	0.70	3,157,541	881,432	3,838,973	4	3,838,973	2.00	7,677,946	10%
TC (Texture Cache)	13,044,218	0.70	18,591,739	5,302,014	23,893,751	1	23,893,751	0.60	14,348,251	15%
RB (Render Backend)	3,194,000	0.70	5,120,000	1,519,000	6,639,000	4	6,639,000	2.00	13,278,000	18%
RC (Render Central)	40,000	0.70	57,143	200,000	267,143	1	267,143	1.00	267,143	0%
EX (Shader Export)	424,378	0.70	743,891	1,519,000	2,262,891	2	2,262,891	1.00	2,262,891	3%
MC (Memory Controller)	143,312	0.70	778,180	426,767	1,204,917	4	1,204,917	2.00	2,409,834	3%
Analog							6,545,640		6,154,400	4%
Total Core (um²)							157,103,674		102,178,949	
Current Pad separation (um)				90						
Current Pad height (um)				360						
Scribe				0.18						
Core mm/side							12.63		10.11	
Total mm/side							13.98		10.99	
RV450 in 0.09 (estimated)										
Core mm/side									8.45	
Total mm/side									9.07	

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R400 Risks / Issues Summary

- **R400 Technology**
 - Proceeding with TSMC 0.13 Low-K; need to continue to monitor status
- **Chip Integration**
 - Virage STAR compiler - functional compiler delivery late
 - Impacting completeness of next netlist release
 - Chip level simulation environment stabilizing - impacting debug of non-GC blocks
- **Physical Design**
 - Resource rollovers from RV350 to R400
 - Logic Design netlist delivery to the Physical team
 - New flow will be a risk; only partially exercised on RV350
- **Software**
 - Compiler progressing (slower than planned)
 - Software MRD reviews completing; need review of integrated SW schedules
- **Overall**
 - Debug progressing slowly in some areas
 - February tapeout target.

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R400 Program Schedule

Task	Plan	Actual	Forecast
Emulator Test template Complete	01-18-02	01-18-02	
GC Emulator integration – 1 triangle	02-22-02	02-21-02	
Core Emulator pixel / shader tests run	03-15-02	03-19-02	
Block Testing Begins	04-16-02	05-01-02	
GC/Chip Integration Start	05-17-02	05-15-02	
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	
First Syntheses	07-12-02	08-03-03	
Verilog Feature Complete	09-16-02		09-30-02
IKOS Emulation start	10-11-02		10-11-02
Begin early block delivery	11-08-02		11-15-02
IKOS Emulation (w/ Software) begins	11-11-02		11-11-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02		11-30-02
A11 Base Layers Tapeout	01-10-03		02-28-03
A11 Metal Layers Tapeout	01-24-03	03-14-03	
First Samples for Engineering			05-23-03
A12 Tapeout		06-28-03	
A12 Samples for Engineering			07-26-03
R400 Customer Samples			08-02-03
Product Delivery			09-02-03

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PROTECTIVE ORDER

R400 Area Estimate (0.13)

Block	Pre Route		Post Route Logic Unit Area	Macro Area	Total Unit Area	R400 Qty	R400 Total	RV400 Qty	RV400 Total	
	Logic Area	Utilization								
BIF (Bus Interface)	1,488,869	0.70	2,126,956	0	2,126,956	1	2,126,956	1.00	2,126,956	1% BIF (Bus Interface)
DC (Display Controller)	2,677,800	0.70	3,825,429	1,779,948	5,605,377	1	5,605,377	1.00	5,605,377	4% DC (Display Controller)
VIP (Video In Port)	518,369	0.70	740,527	47,892	788,419	1	788,419	1.00	788,419	1% VIP (Video In Port)
CG (Clock Gen)	340,700	0.70	486,714	224,000	710,714	1	710,714	1.00	710,714	0% CG (Clock Gen)
ROM (ROM and debug controller)	193,104	0.70	275,863	0	275,863	1	275,863	1.00	275,863	0% ROM (ROM and debug controller)
TSTC (Test Controller)	9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714	1% VIP (Video In Port)
CP (Control Processor)	3,366,639	0.70	4,809,484	1,497,341	6,306,825	1	6,306,825	1.00	6,306,825	4% CP (Control Processor)
RBBM (Register Backbone Manager)	221,702	0.70	316,717	0	316,717	1	316,717	1.00	316,717	0% RBBM (Register Backbone Manager)
MH (Memory Hub)	3,193,174	0.70	4,561,677	675,232	5,236,909	1	5,236,909	0.75	3,927,682	3% MH (Memory Hub)
IDCT	847,452	0.70	1,210,646	84,403	1,295,049	1	1,295,049	1.00	1,295,049	1% IDCT
VGT (Vertex Group and Tessellate)	816,990	0.70	1,167,129	331,693	1,498,822	1	1,498,822	1.00	1,498,822	1% VGT (Vertex Group and Tessellate)
PA(Viewport Xform,Clip and Setup)	2,979,377	0.70	4,256,253	580,018	4,836,271	1	4,836,271	1.00	4,836,271	3% PA(Viewport Xform,Clip and Setup)
SC (Scan Converter)	6,558,352	0.70	9,369,074	568,187	9,937,261	1	9,937,261	0.60	5,962,357	6% SC (Scan Converter)
SP (Shader Pipe)	3,992,400	0.70	5,703,429	2,613,709	8,317,138	4	33,268,552	2.00	16,634,276	21% SP (Shader Pipe)
SQ (Sequencer)	1,178,584	0.70	1,683,692	2,380,646	4,064,338	1	4,064,338	1.00	4,064,338	3% SQ (Sequencer)
TP (Texture Pipe)	2,210,279	0.70	3,157,541	681,432	3,838,973	4	15,355,891	2.00	7,677,945	10% TP (Texture Pipe)
TC (Texture Cache)	13,014,218	0.70	18,591,739	5,322,011	23,913,751	1	23,913,751	0.60	14,348,251	15% TC (Texture Cache)
RB (Render Backend)	3,584,000	0.70	5,120,000	1,233,000	6,353,000	4	25,412,000	2.00	12,706,000	16% RB (Render Backend)
RC (Render Central)	40,000	0.70	57,143	200,000	257,143	1	257,143	1.00	257,143	0% RC (Render Central)
SX (Shader Export)	524,928	0.70	749,897	1,516,000	2,265,897	2	4,531,794	1.00	2,265,897	3% SX (Shader Export)
MC (Memory Controller)	543,312	0.70	776,160	426,757	1,202,917	4	4,811,668	2.00	2,405,834	3% MC (Memory Controller)
Analog							6,545,540		8,154,400	4% Analog
Total Core (um2)							157,109,574		102,178,849	

Current Pad separation (um)	80		
Current Pad height (um)	350		
Scribe	0.18		
Core mm/side		12.53	10.11
Total mm/side		13.98	10.99
RV450 in 0.09 (estimated)			
Core mm/side			8.15
Total mm/side			9.07

PROTECTIVE ORDER

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14.1nS)	
MC/MH	95% / 95%	9/23 - 9/16	N/A	10%	MC:4.46; MH: 4.72	MCLK: 2.39	55 / 643
RB/RC	85% / 95%	9/30	95%	54%	RB: 8.2; RC 2.5		16689 / 0
SX/SQ	90%	9/16 - 9/30	99%	88%	SX: 2.74; SQ: 2.5		0 / 0
SP	100%	9/16	97%		SP: 2.5		0
TP/TC	97% / 95%	9/16	92%	18%	TP: 2.55; TC: 2.5		0 / 0
CG/CGM/ROM	100%	9/16	N/A	2%	CG: 2.5; CGM:2.5; DBG:2.5		0
PA	100%	9/16	100%	35%	PA: 2.69		110
VGT	100%	9/16	100%	59%	VGT: 2.75		33
SC	90%	9/16	95%	61%	SC:2.73		140
RBBM	95%	9/16	N/A		RBBM: 2.95		95
CP	95%	9/16	90%	90%	CP: 2.85		439
Display - DCP	100%	9/16	90%	65%	Display: 11	PIXCLK: 2.5	8207
Display - LB	100%	9/16	100%	65%			
Display - SCL	70%	9/20	85%	65%			
Display - CRTC	100%	9/16	80%	65%			
Display - DISPOUT	95%	9/16	65%	65%			
Display - TVOUT	100%	9/16	30%	0%			
VGA	100%	9/16	99%	85%			
VIP	100%	9/16	100%	100%			
BIF	100%	9/16	90%	15%	BIF 4.47	BCLK: 14.1	228
IDCT	100%	9/16	97%	97%	IDCT: 4.23		2898

Tests Planned	Tests Written	Tests Passing
2200	225	215
720	390	22
1600	1400	27
2200	400	0
253	5	2
584	206	175
263	156	149
389	239	236
800	722	635
280	190	179
30	20	20
97	67	5
75	50	37
150	91	68
130	110	64
275	270	270
240	40	15
279	279	204