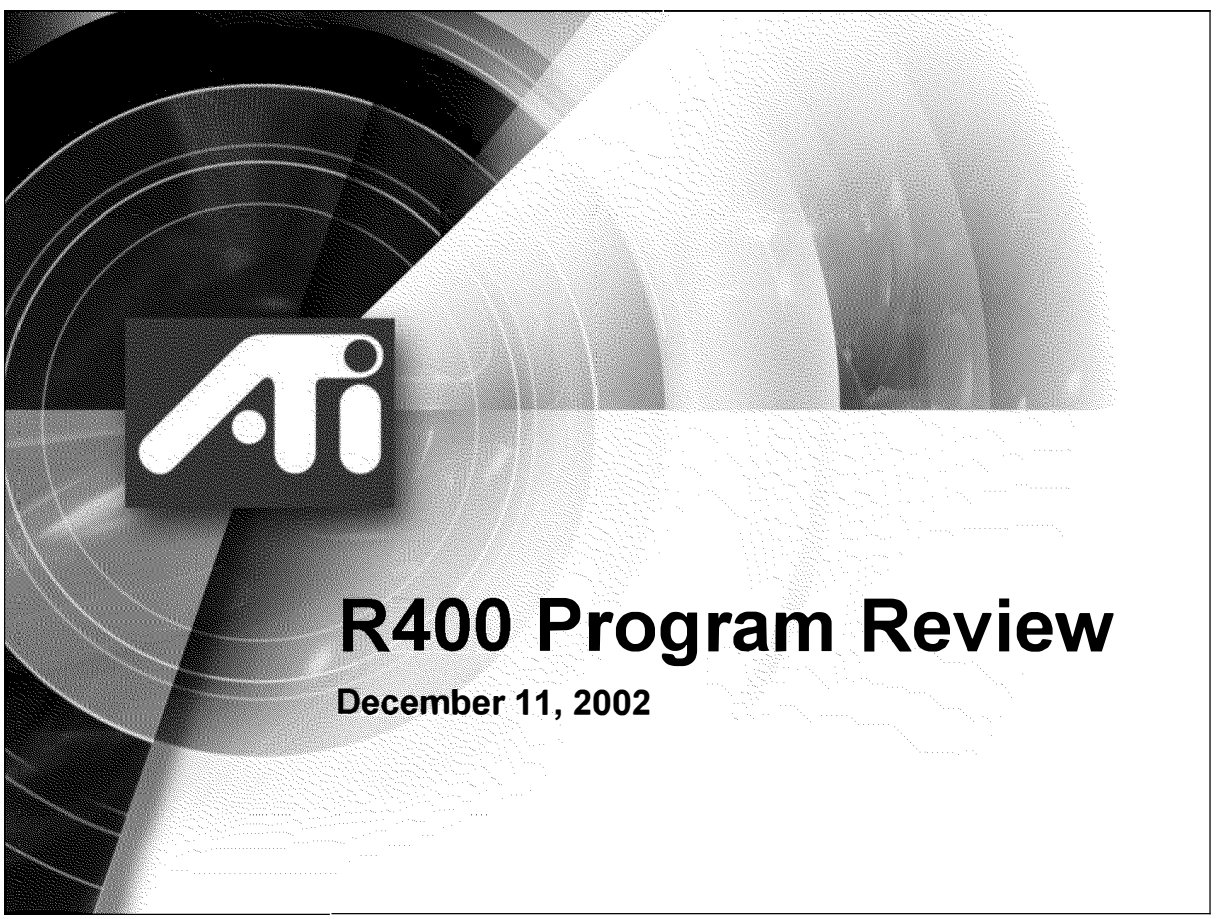


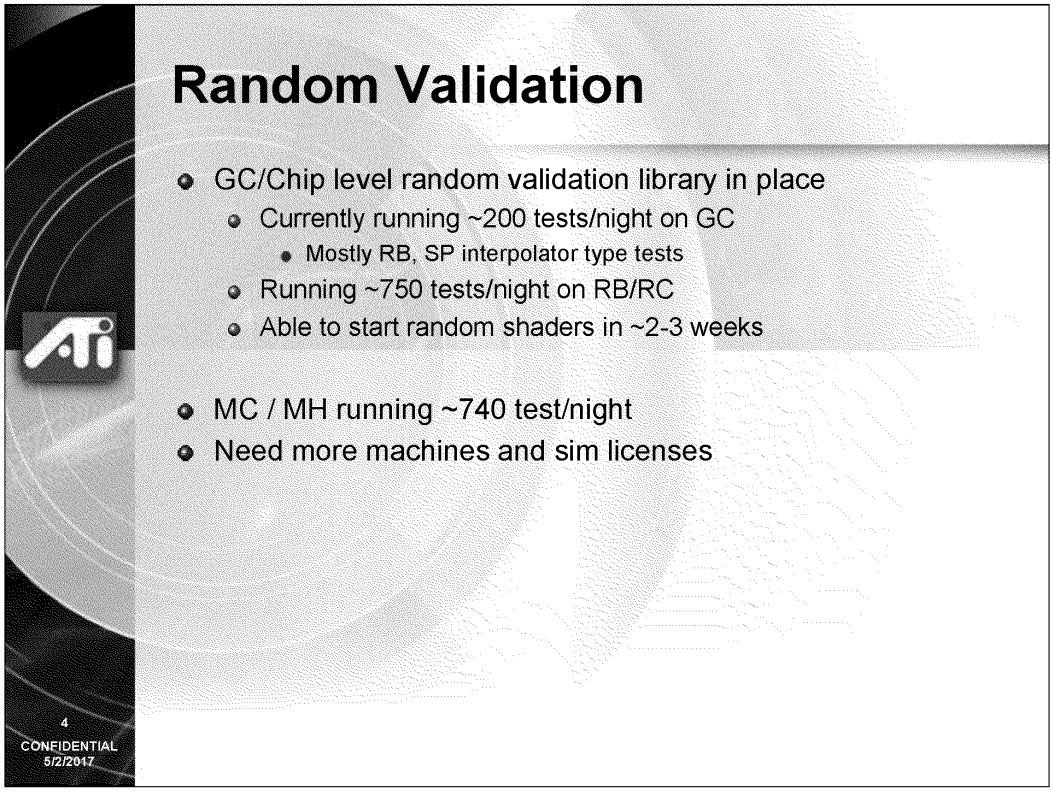
ATI Corporate Presentation

Emulator

- SQ/SP/SX
  - Debugging HW / EMU numerical mismatches
- TP/TC
  - Debugging 3D/Volume textures
  - Debugging HW / EMU numerical mismatches
- RB/RC
  - Debugging MSAA Resolve
  - Shader depth export and Zpass counter not implemented
- MC/MH
  - Debugging ATI GART

HW Verification (directed tests)

Block	Planned	% Written	% Running	% Passing
MC / MH	2300	96%	100%	94%
RB / RC	870	91%	86%	86%
SQ/SX/SP	1700	97%	100%	81%
TP / TC	5500	85%	13%	25%
*GC	4183			63%



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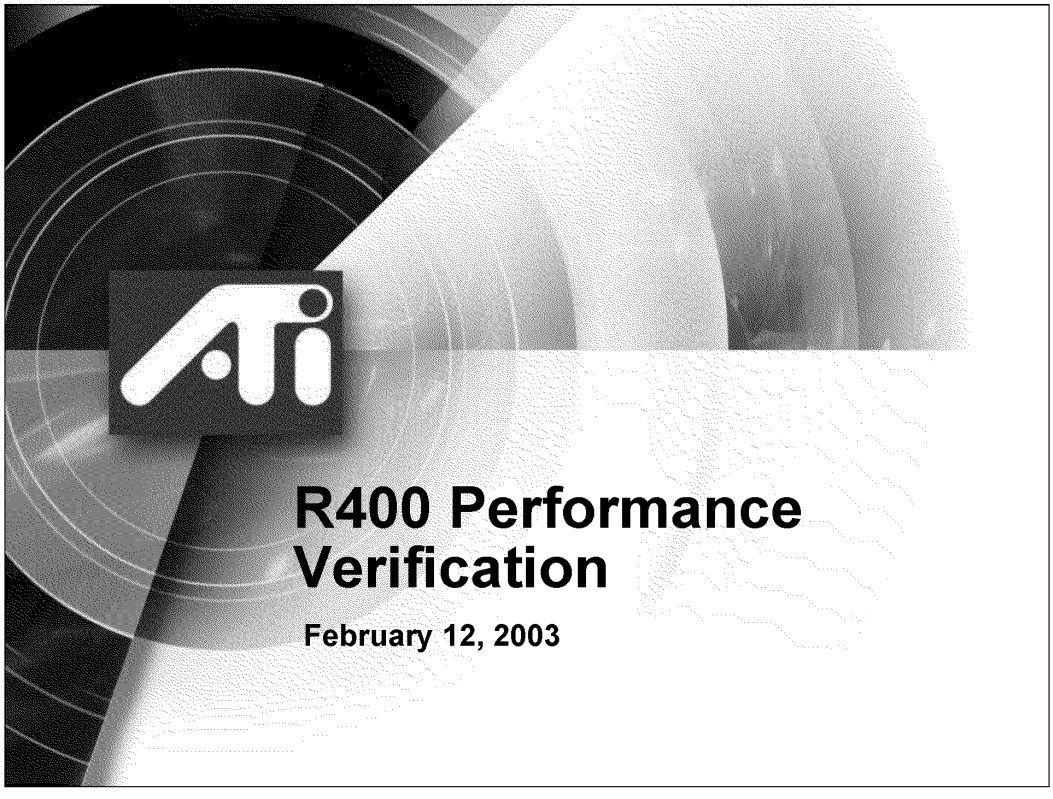

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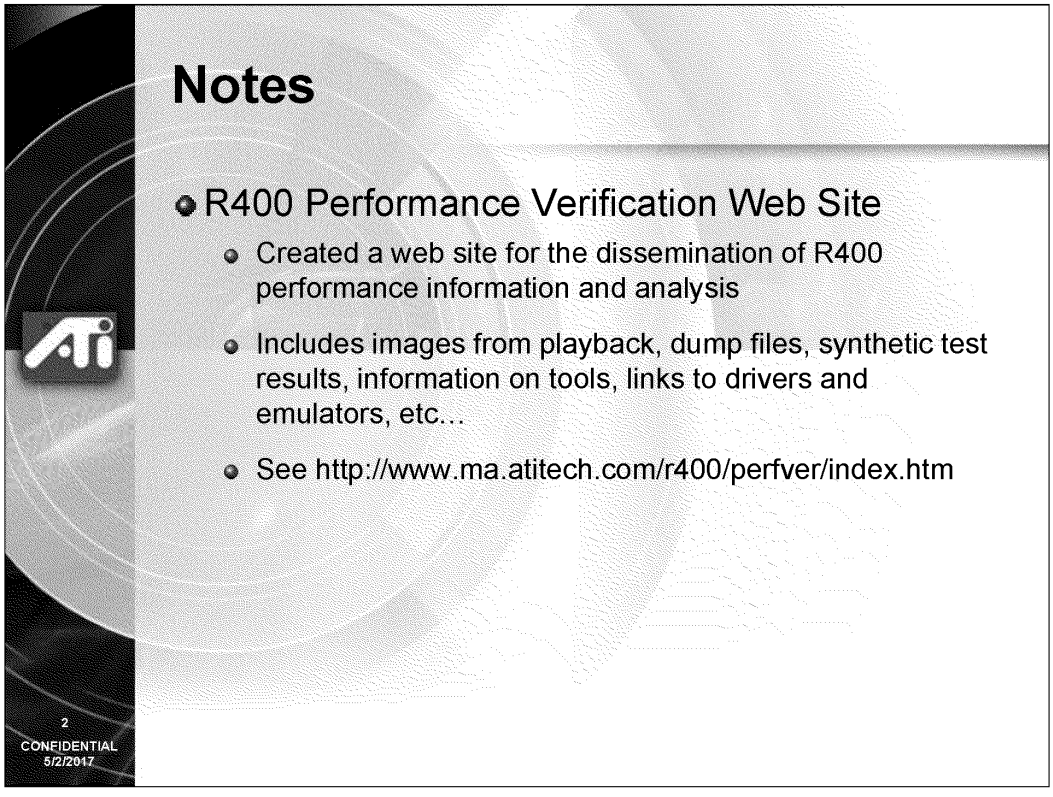
Notes
R400 Performance Verification Web Site
Created a web site for the dissemination of R400 performance information and analysis
Includes images from playback, dump files, synthetic test results, information on tools, links to drivers and emulators, etc…
See http://www.ma.atitech.com/r400/perfver/index.htm
2
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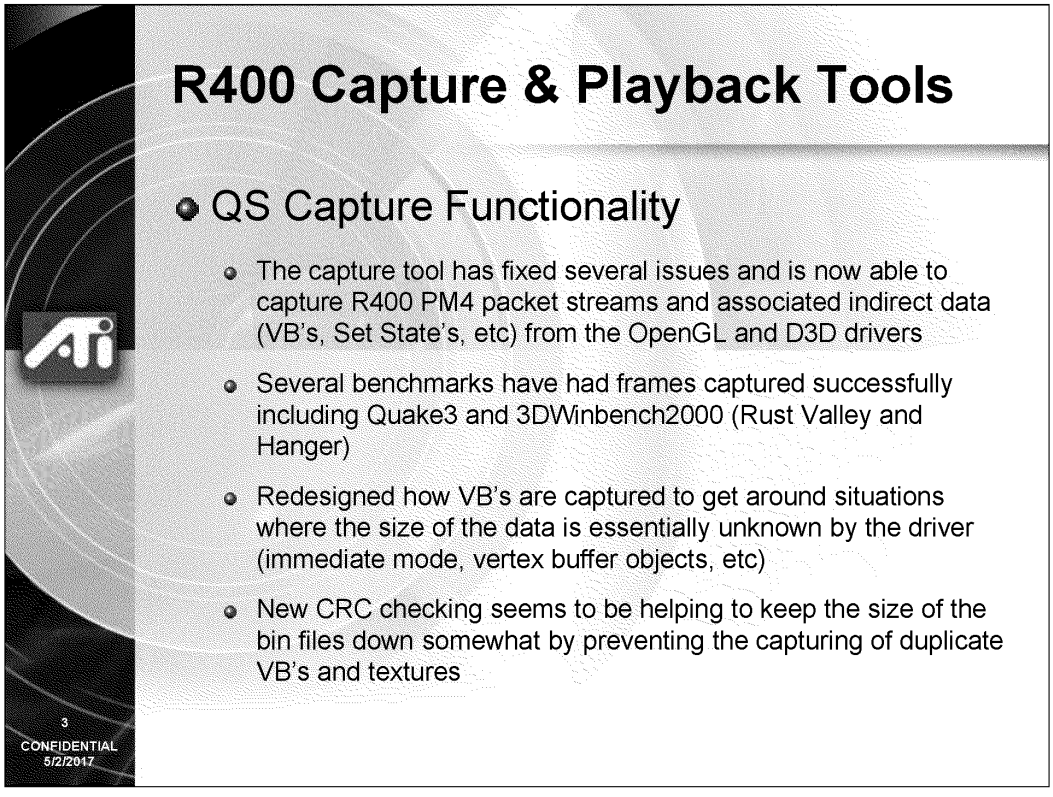

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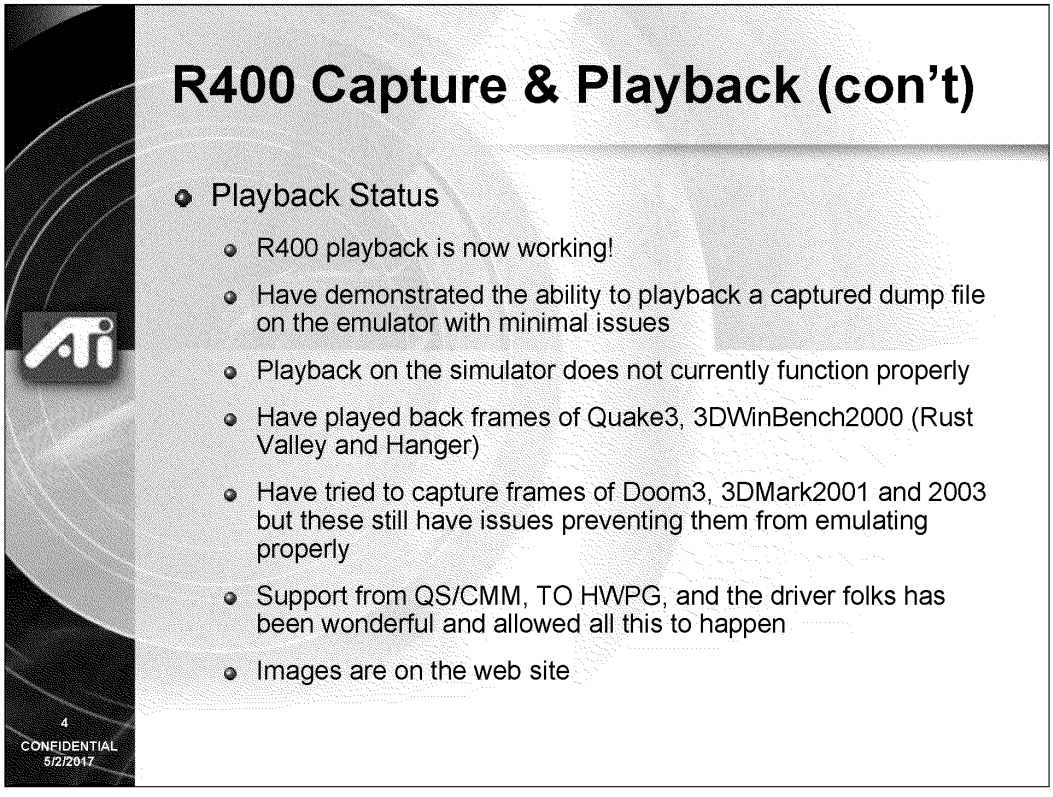
Confidential



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R400 Capture & Playback (con't)

- Quake3 four.dm_68 (frame 40) emulated

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R400 Capture & Playback (con't)

- Quake3 four.dm_68 (frame 40) playback

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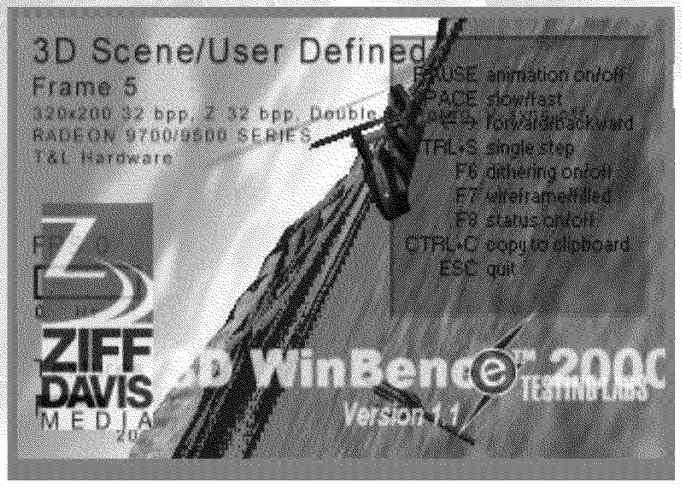
R400 Capture & Playback (con't)

- 3DWinbench2000 Rust Valley emulated



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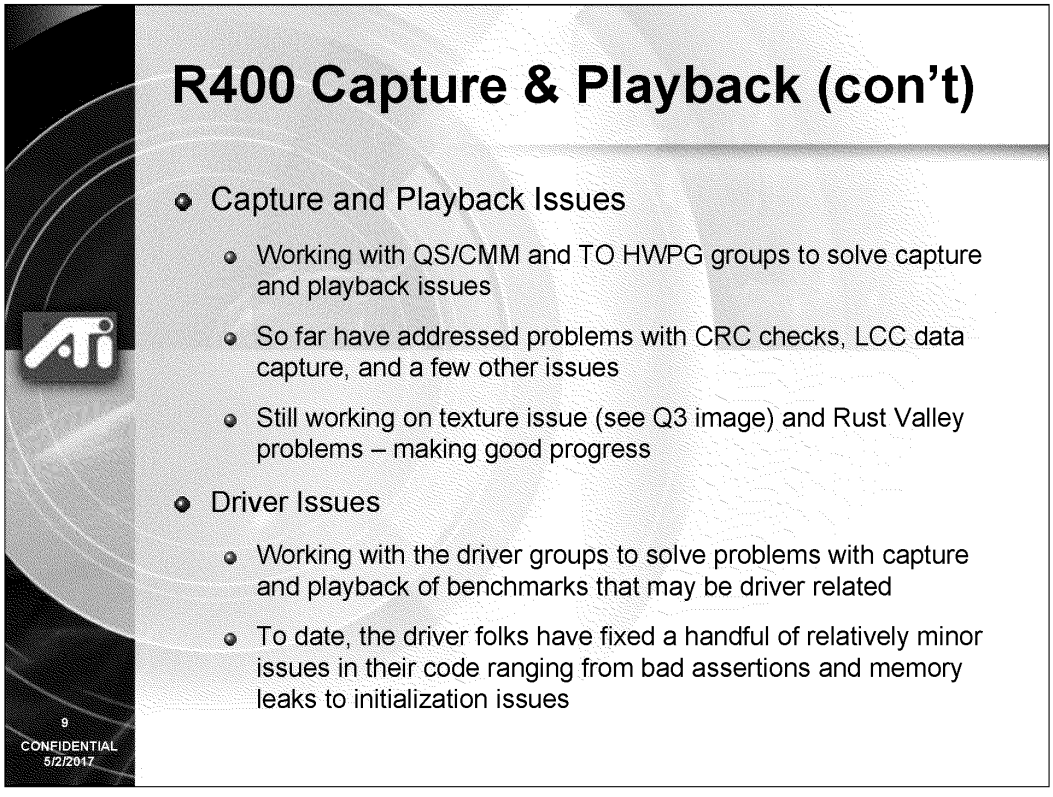
R400 Capture & Playback (con't)

- 3DWinbench2000 Rust Valley playback



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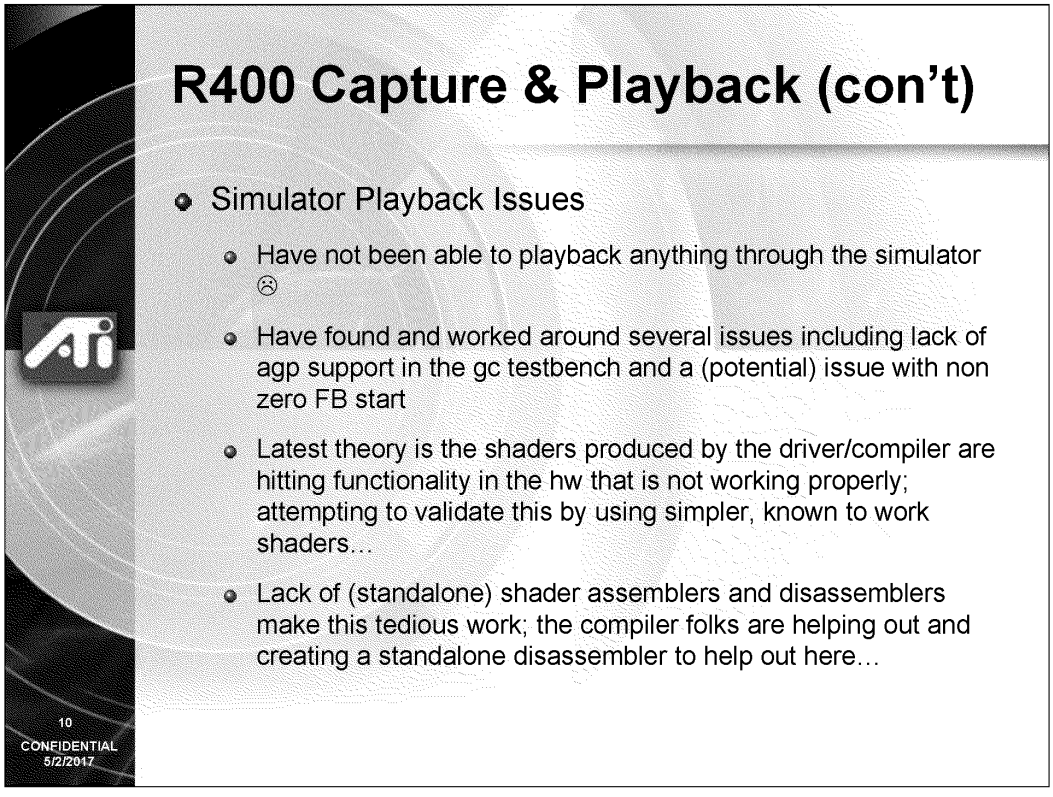
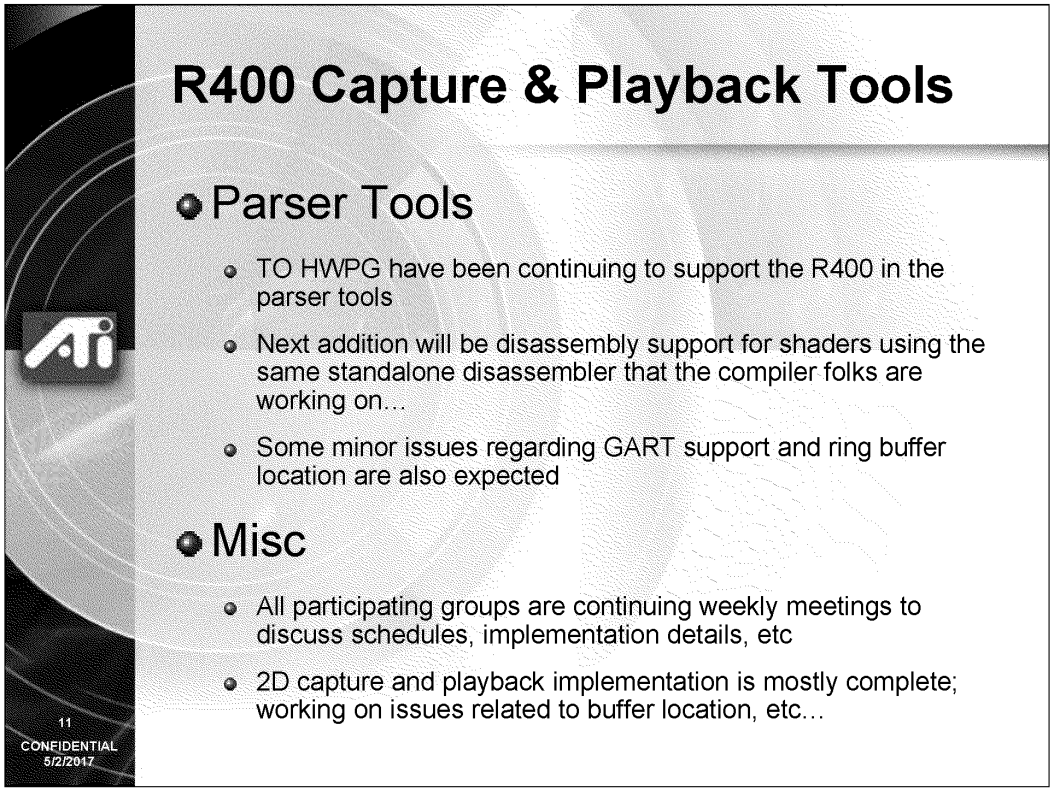
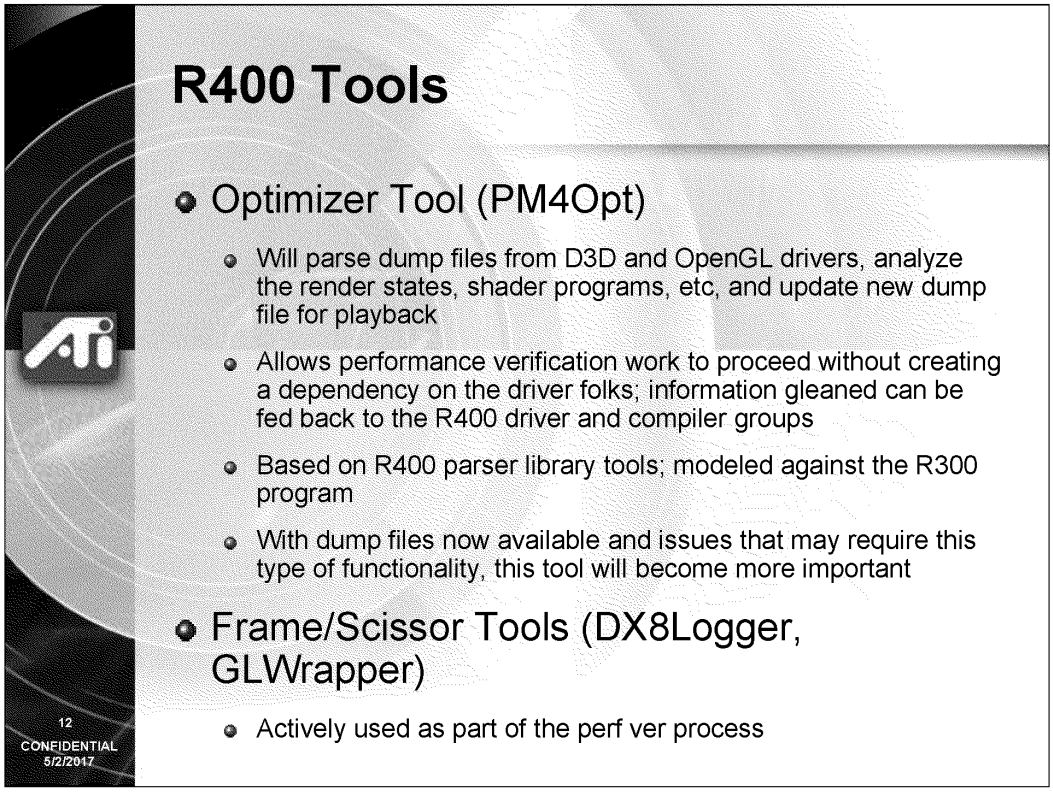


ATI Corporate Presentation
Confidential



ATI Corporate Presentation
Confidential



ATI Corporate Presentation
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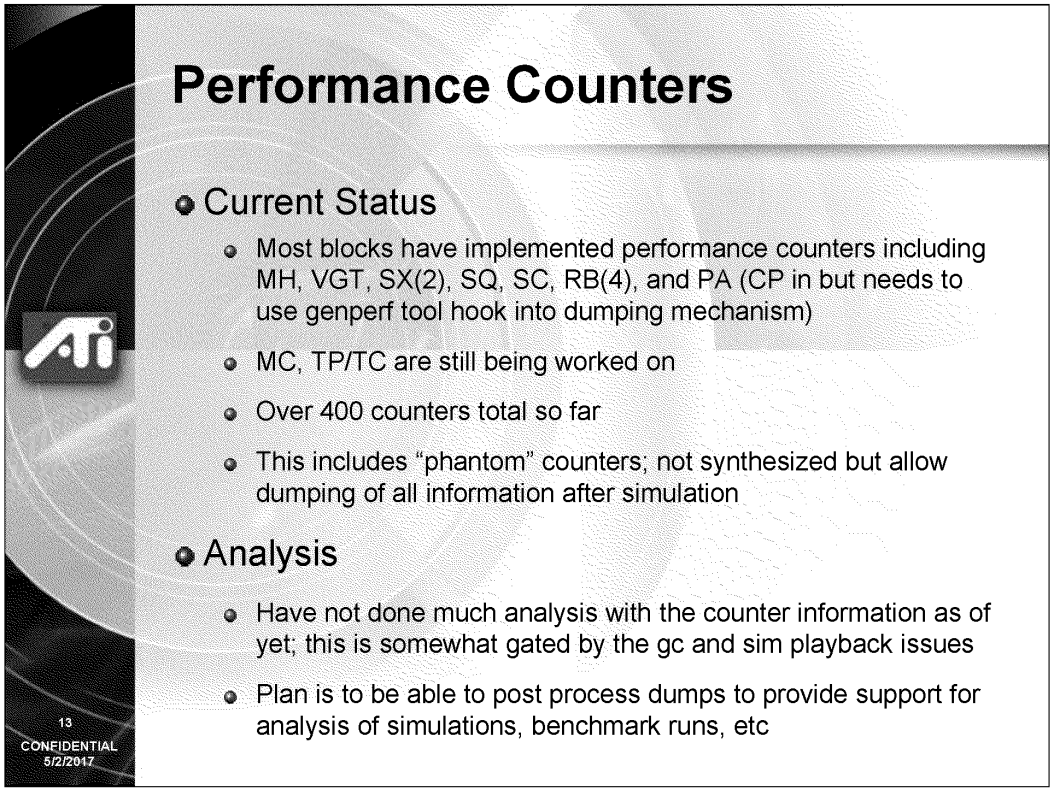
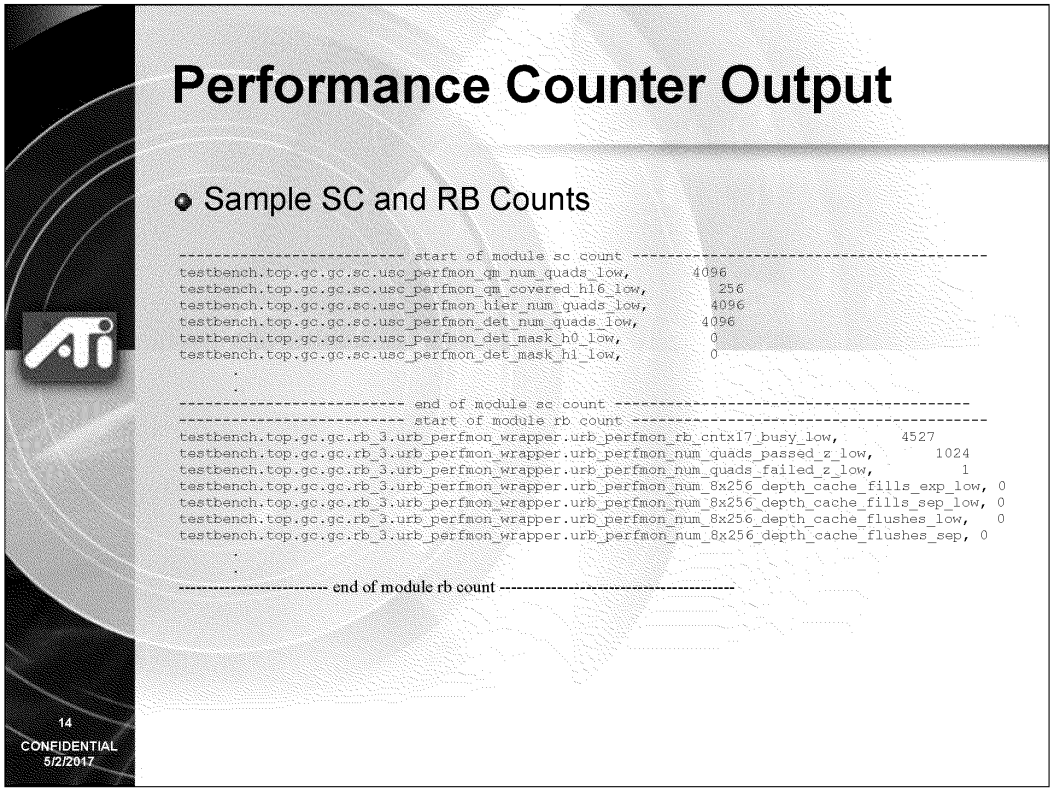


ATI Corporate Presentation
Confidential



ATI Corporate Presentation
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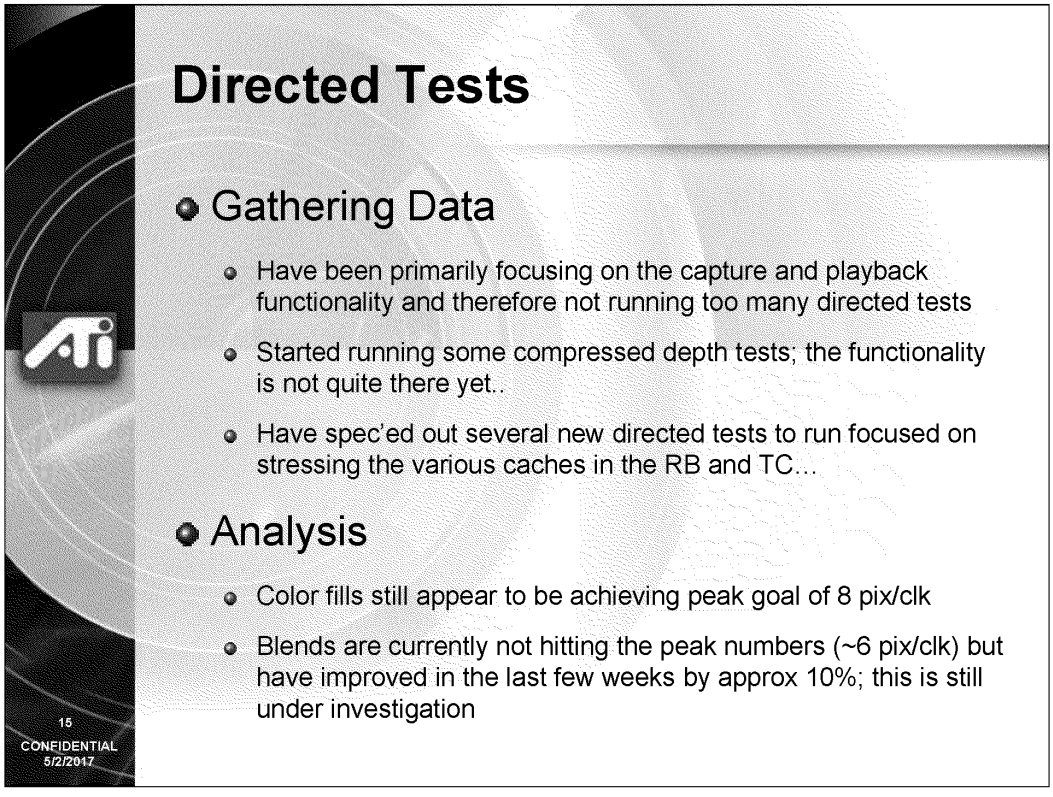
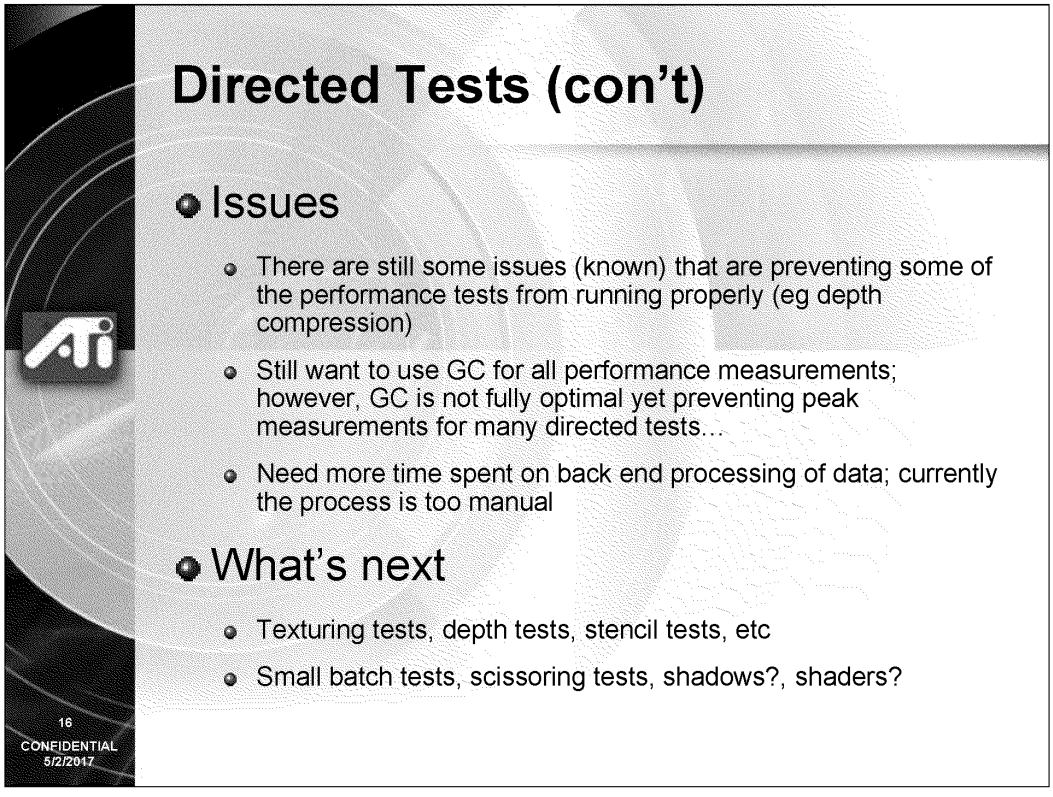
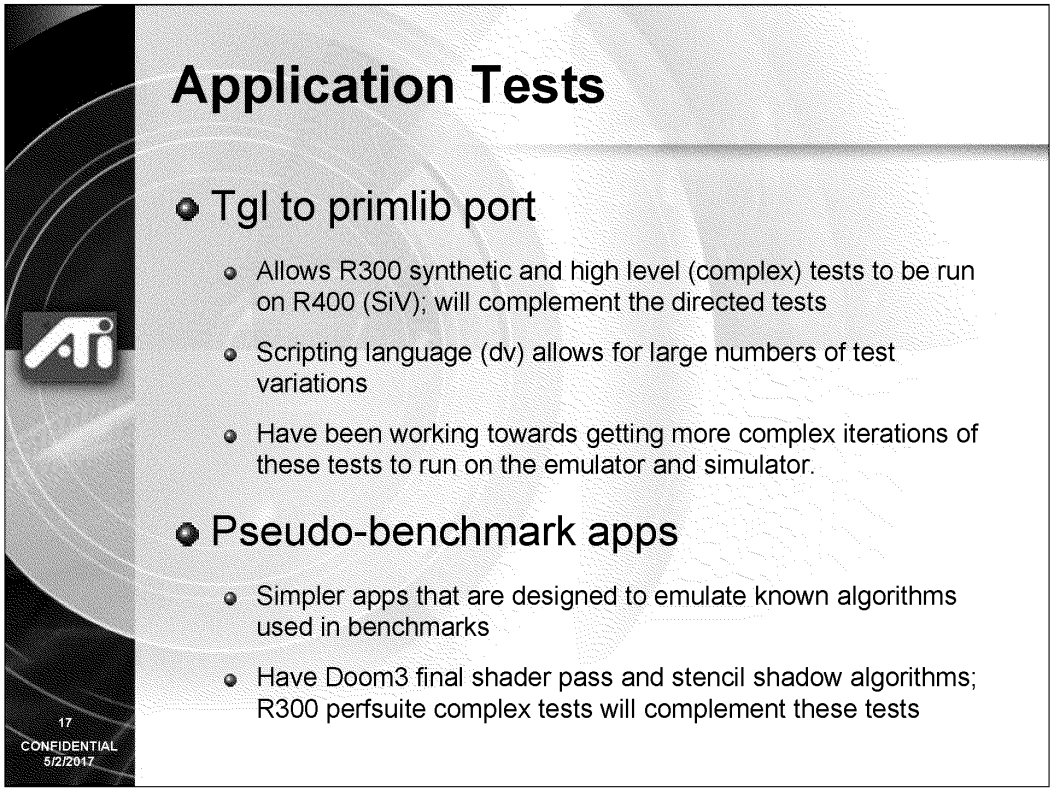


ATI Corporate Presentation
Confidential



ATI Corporate Presentation
Confidential



ATI Corporate Presentation
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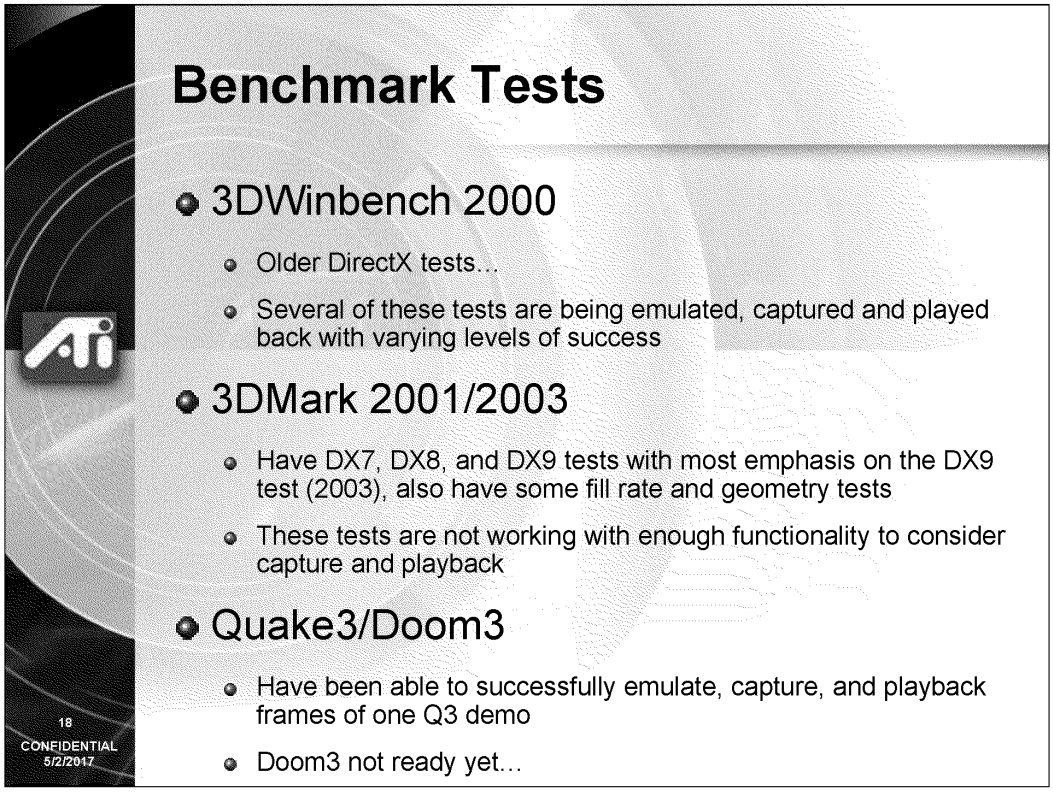
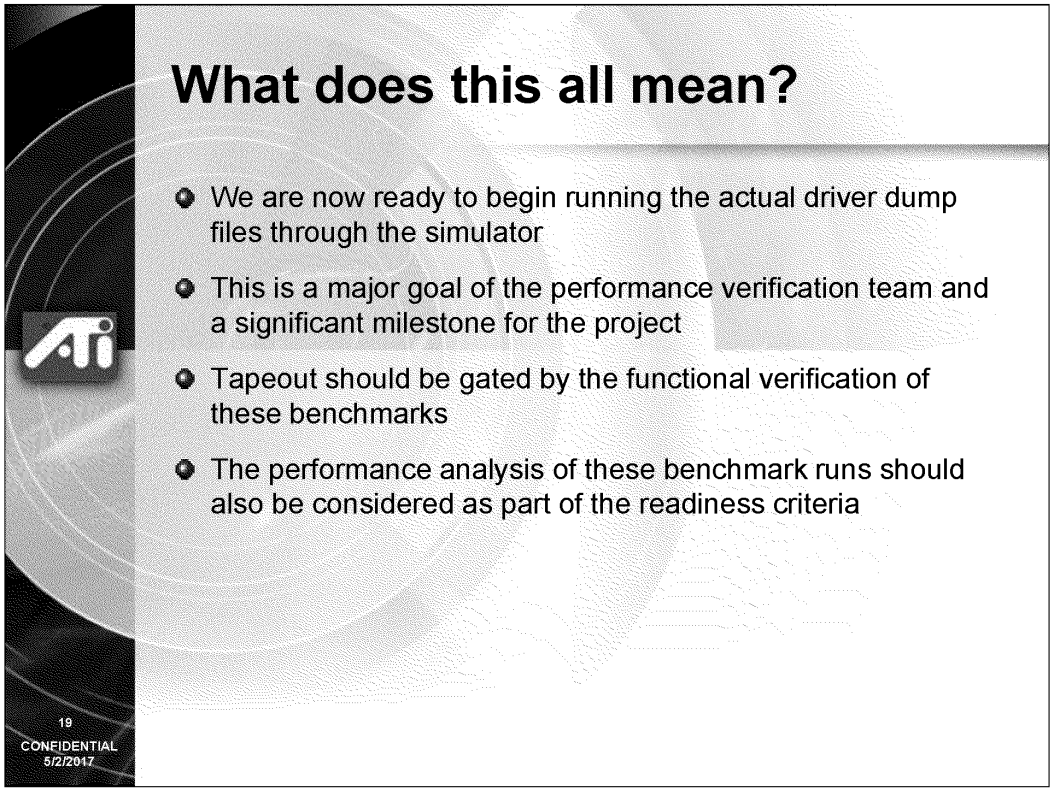
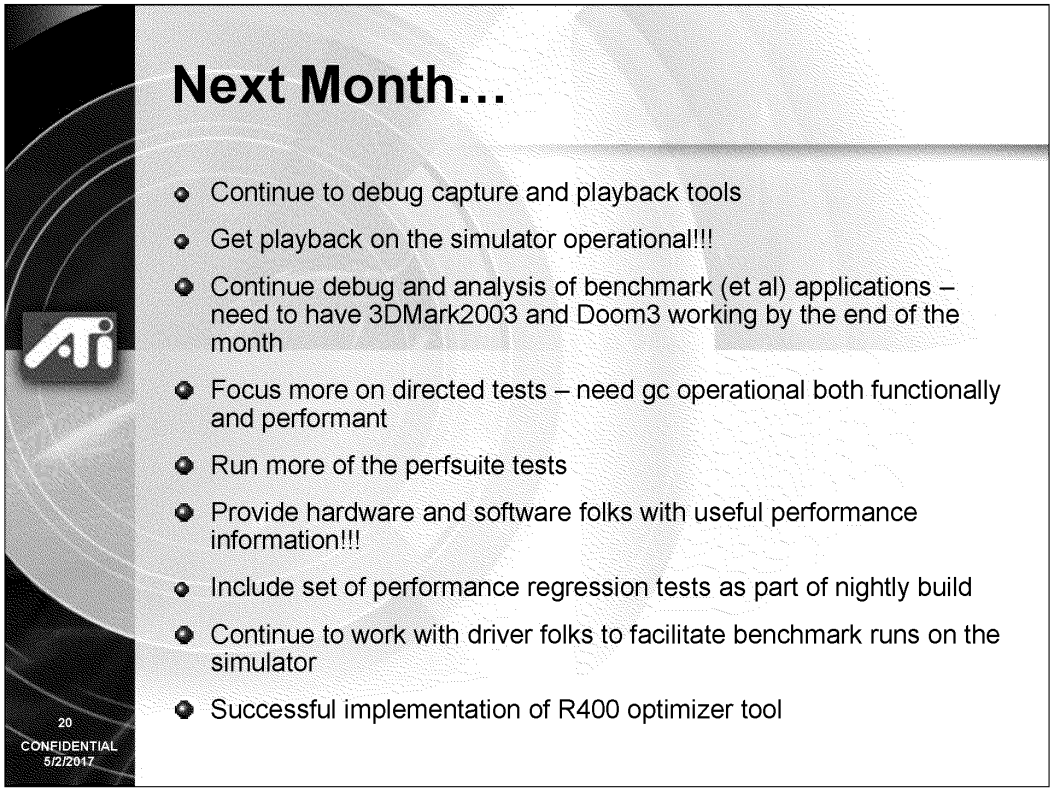


ATI Corporate Presentation
Confidential



ATI Corporate Presentation
Confidential



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ATI Corporate Presentation
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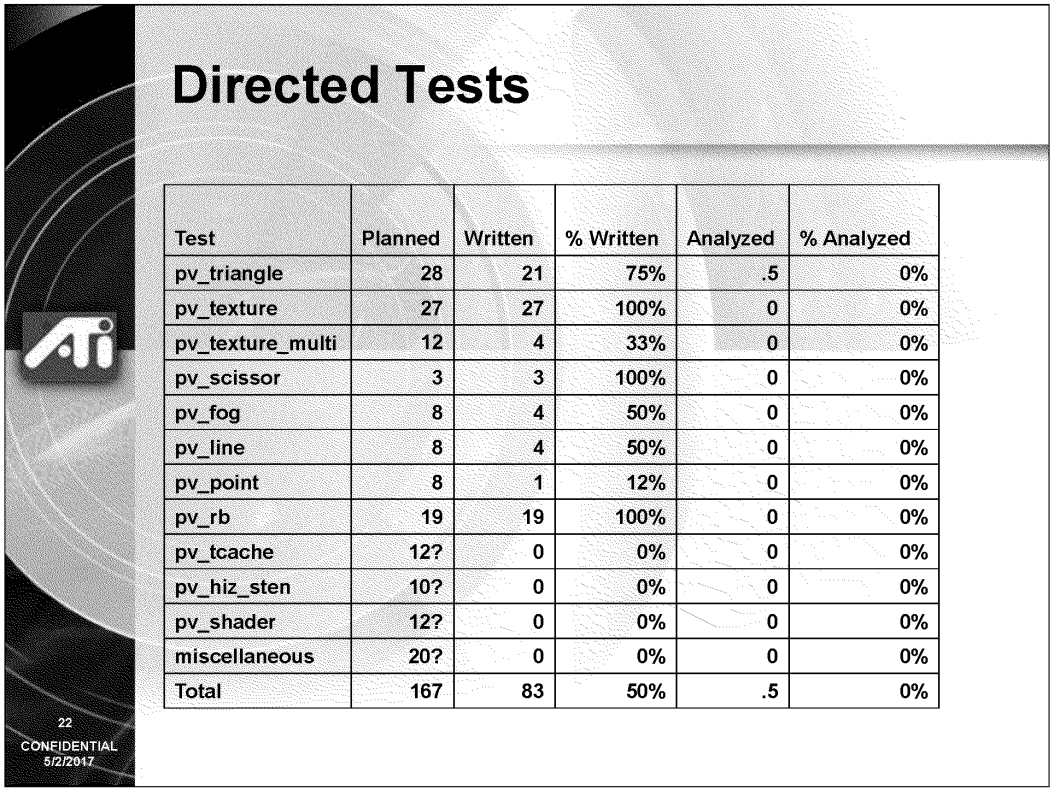
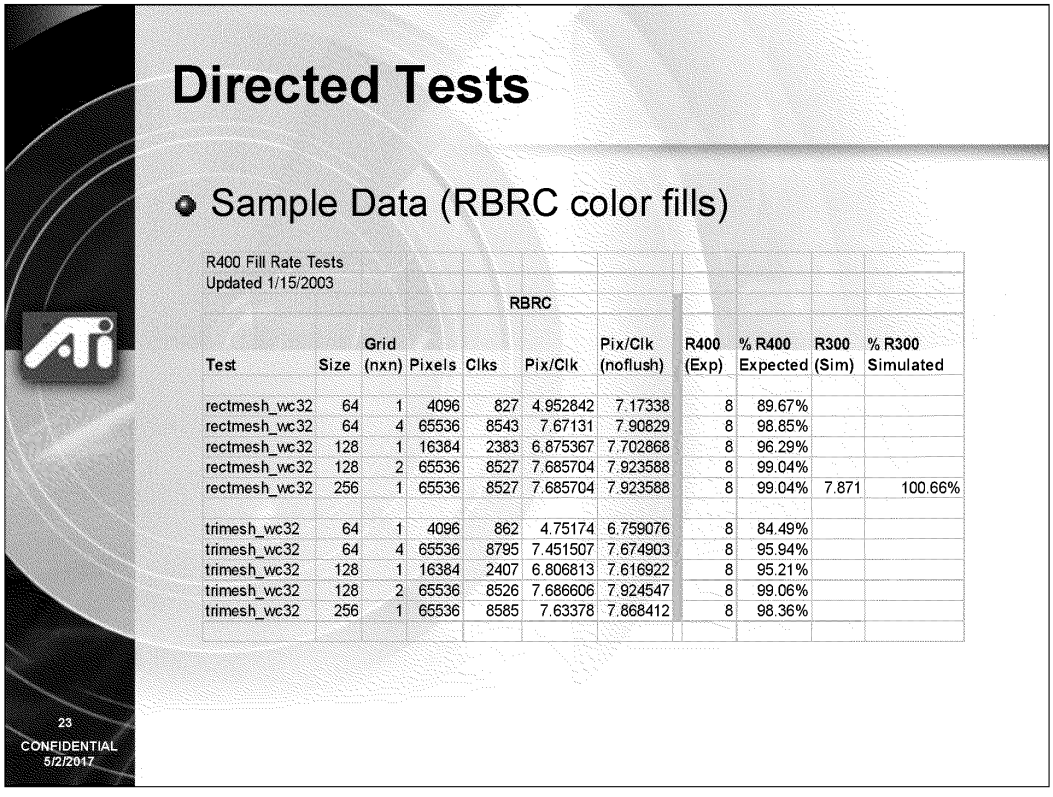


ATI Corporate Presentation
Confidential



ATI Corporate Presentation
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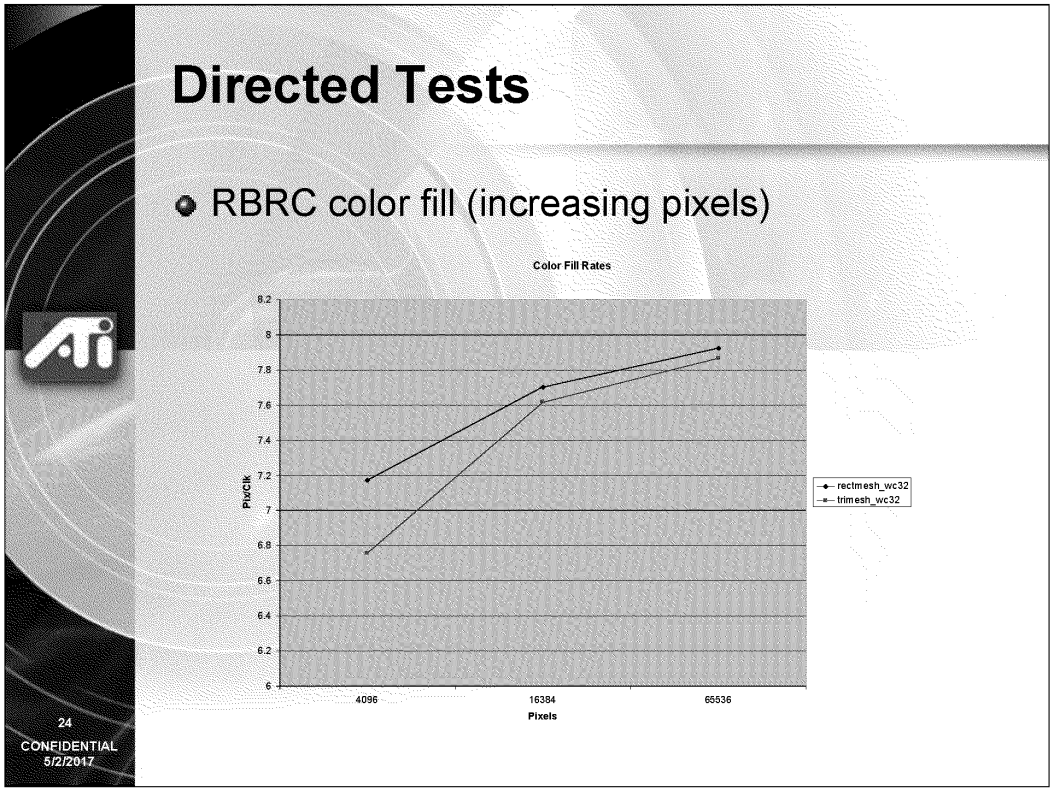
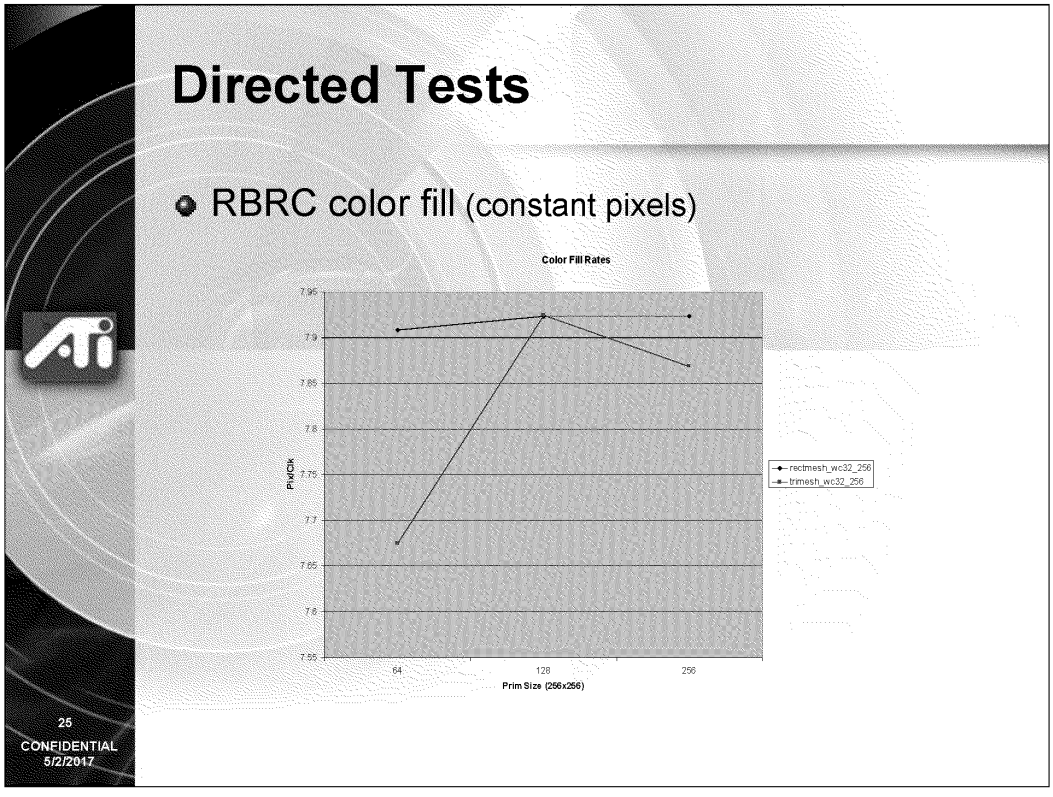
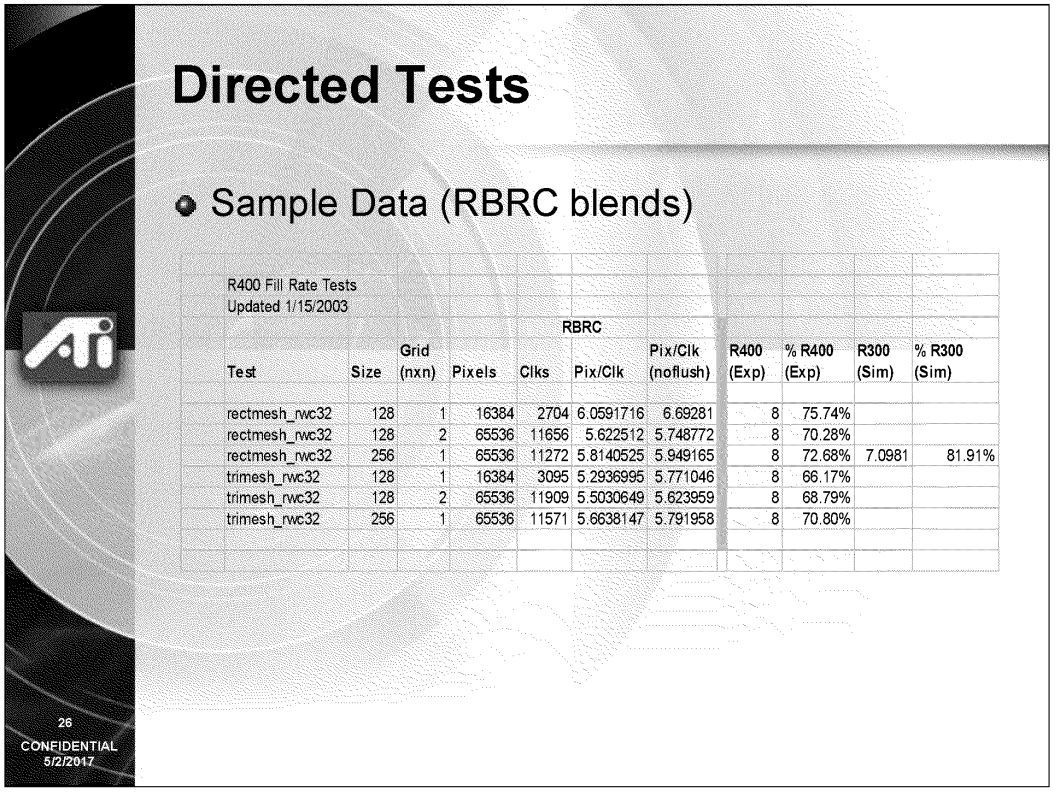


ATI Corporate Presentation
Confidential



ATI Corporate Presentation
Confidential



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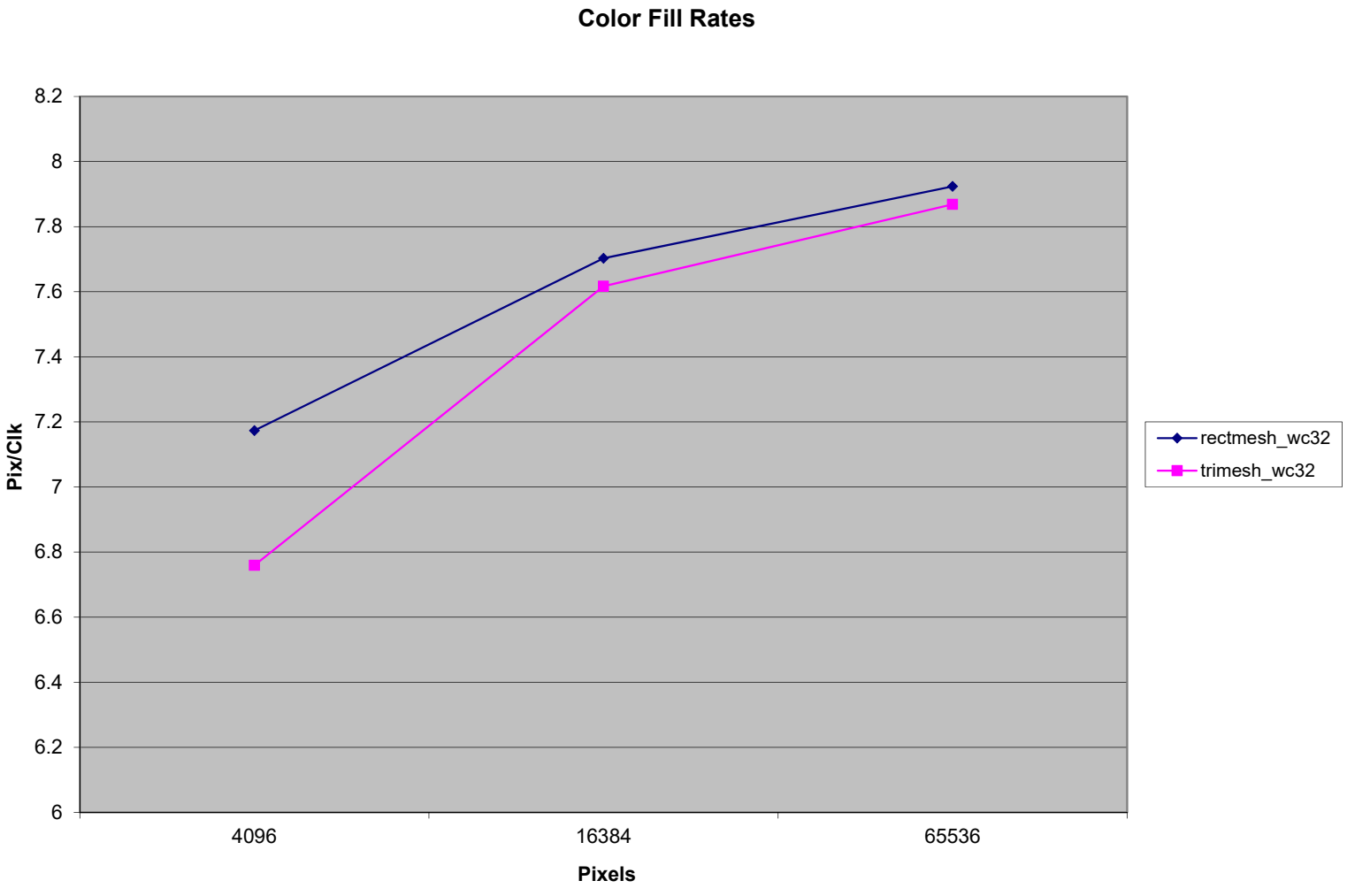
```
-------------------------- start of module sc count ----------------------------------------
testbench.top.gc.gc.sc.usc_perfmon_qm_num_quads_low,       4096
testbench.top.gc.gc.sc.usc_perfmon_qm_covered_h16_low,        256
testbench.top.gc.gc.sc.usc_perfmon_hier_num_quads_low,       4096
testbench.top.gc.gc.sc.usc_perfmon_det_num_quads_low,       4096
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h0_low,          0
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h1_low,          0
      .
      .
-------------------------- end of module sc count ------------------------------------------
-------------------------- start of module rb count ----------------------------------------
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_rb_cntx17_busy_low,       4527
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_passed_z_low,       1024
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_failed_z_low,          1
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_exp_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_sep_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_low,   0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_sep, 0
      .
      .
------------------------- end of module rb count -----------------------------------------
```

R400 Fill Rate Tests
Updated 1/15/2003

Test	Size	Grid (nxn)	Pixels	Clks	RBRC Pix/Clk	RBRC Pix/Clk (noflush)	R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
rectmesh_wc32	64	1	4096	827	4.952842	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.67131	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.875367	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.685704	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.685704	7.923588	8	99.04%	7.871	100.66%
trimesh_wc32	64	1	4096	862	4.75174	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.451507	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.806813	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.686606	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.63378	7.868412	8	98.36%		


Color Fill Rates
8.2
8
7.8
7.6
7.4
7.2
7
6.8
6.6
6.4
6.2
6
Pix/Clk
4096
16384
65536
Pixels
rectmesh_wc32
trimesh_wc32

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Size	Grid (nxn)	RBRC Clks (all_busys)	Pix/Clk
rectmesh_wc32	64	1	827	4.9528
rectmesh_wc32	64	4	8543	7.6713
rectmesh_wc32	128	1	2383	6.8754
rectmesh_wc32	128	2	8527	7.6857
rectmesh_wc32	256	1	8527	7.6857
trimesh_wc32	64	1	862	4.7517
trimesh_wc32	64	4	8795	7.4515
trimesh_wc32	128	1	2407	6.8068
trimesh_wc32	128	2	8526	7.6866
trimesh_wc32	256	1	8585	7.6338

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Pixels	Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_wc32	4096	7.17338	8	89.67%			
rectmesh_wc32	65536	7.90829	8	98.85%			
rectmesh_wc32	16384	7.702868	8	96.29%			
rectmesh_wc32	65536	7.923588	8	99.04%			
rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	4096	6.759076	8	84.49%			
trimesh_wc32	65536	7.674903	8	95.94%			
trimesh_wc32	16384	7.616922	8	95.21%			
trimesh_wc32	65536	7.924547	8	99.06%			
trimesh_wc32	65536	7.868412	8	98.36%			

rectmesh_wc32	4096	7.17338	8	89.67%			
rectmesh_wc32	65536	7.90829	8	98.85%			
rectmesh_wc32	16384	7.702868	8	96.29%			
rectmesh_wc32	65536	7.923588	8	99.04%			
rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%	
rectmesh_wc32	4096	7.17338	8	89.67%			
rectmesh_wc32	16384	7.702868	8	96.29%			
rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	4096	6.759076	8	84.49%			
trimesh_wc32	16384	7.616922	8	95.21%			
trimesh_wc32	65536	7.868412	8	98.36%			

R400 Fill Rate Tests
Updated 1/xx/2003

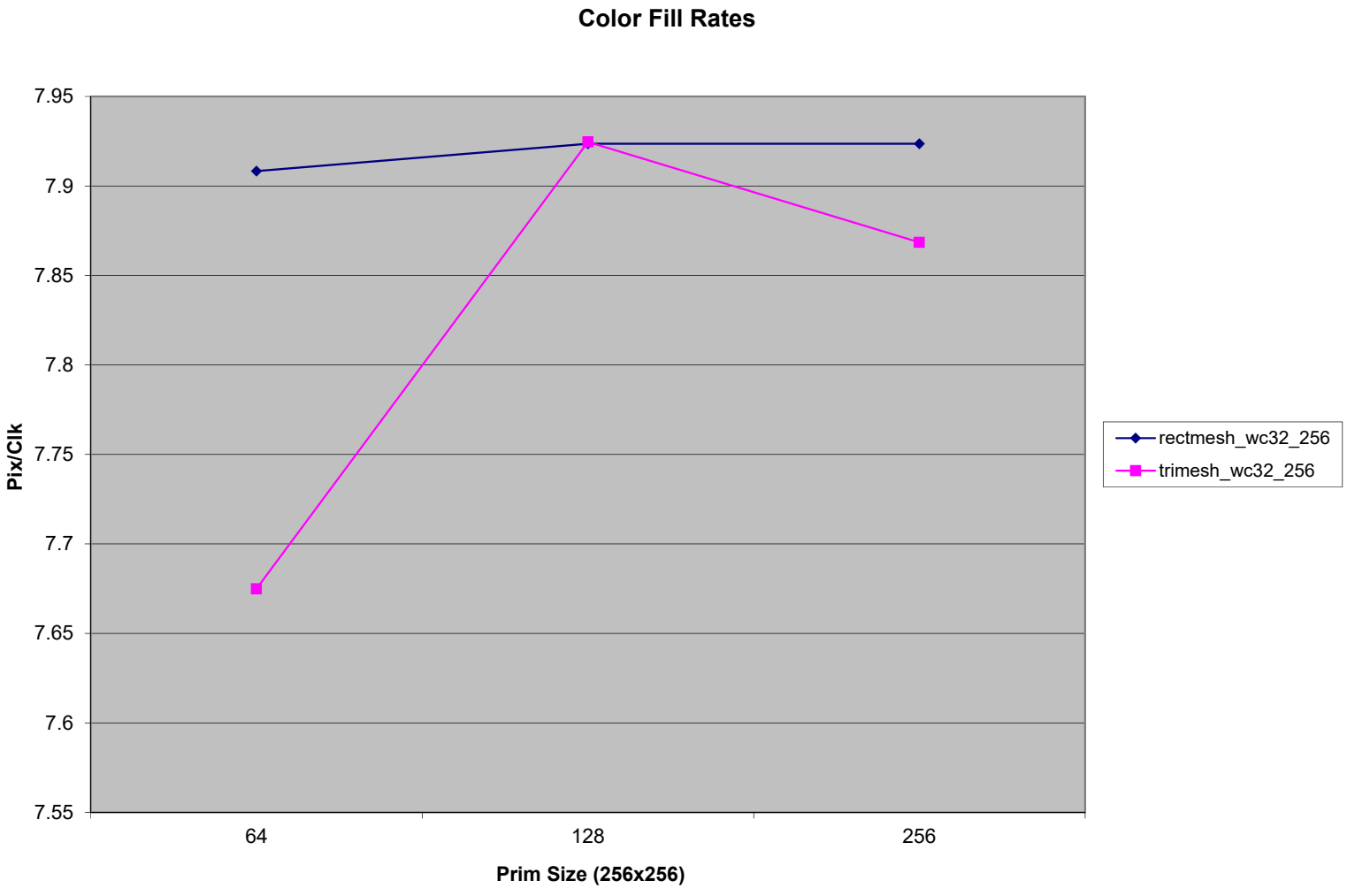
Test	Size	Grid (nxn)	Pixels	GC Cntx17 busy	GC Pix/Clk	RBRC Clks (all_busys)	RBRC Pix/Clk	Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%			

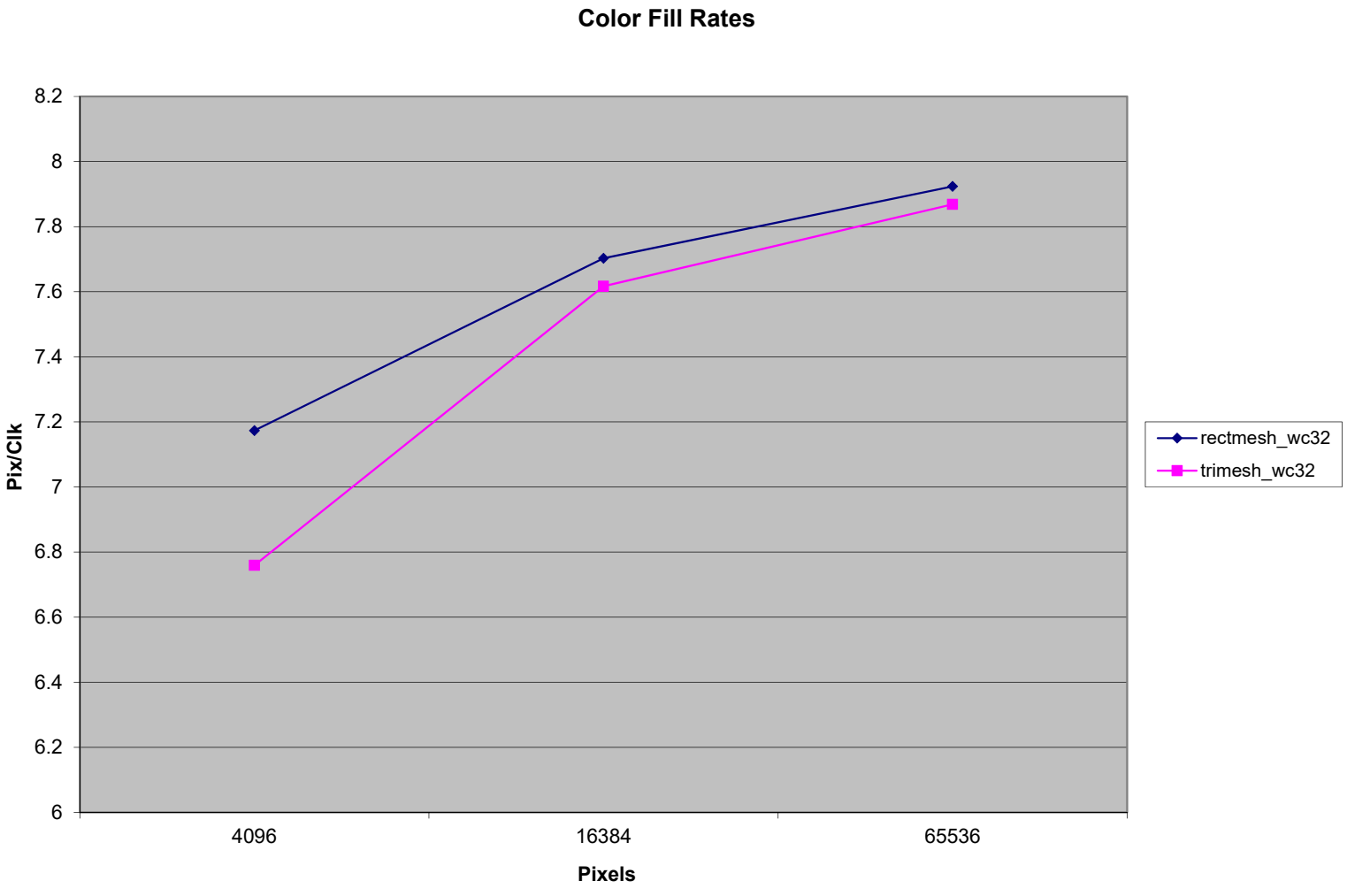
R400 Fill Rate Tests
Updated 1/xx/2003

Test	Size	Grid (nxn)	Pixels	GC Cntx17 busy	GC Pix/Clk	RBRC Clks (all_busys)	RBRC Pix/Clk	RBRC Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_wc32	64	1	4096			827	4.9528	7.17338	8	89.67%			
rectmesh_wc32	64	4	65536			8543	7.6713	7.90829	8	98.85%			
rectmesh_wc32	128	1	16384			2383	6.8754	7.702868	8	96.29%			
rectmesh_wc32	128	2	65536			8527	7.6857	7.923588	8	99.04%			
rectmesh_wc32	256	1	65536			8527	7.6857	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64	1	4096			862	4.7517	6.759076	8	84.49%			
trimesh_wc32	64	4	65536			8795	7.4515	7.674903	8	95.94%			
trimesh_wc32	128	1	16384			2407	6.8068	7.616922	8	95.21%			
trimesh_wc32	128	2	65536			8526	7.6866	7.924547	8	99.06%			
trimesh_wc32	256	1	65536			8585	7.6338	7.868412	8	98.36%			
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%			
rectmesh_wc32_t128pt	64	1	4096	2705	1.5142				6.4				
rectmesh_wc32_t128pt	64	4	65536						6.4				
rectmesh_wc32_t256pt	128	1	16384						6.4				
rectmesh_wc32_t256pt	128	2	65536						6.4				
rectmesh_wc32_t256pt	256	1	65536						6.4				
trimesh_wc32_t256pt	128	1	16384						6.4				apparent hang (RB->MC)
trimesh_wc32_t256pt	128	2	65536						6.4				
trimesh_wc32_t256pt	256	1	65536						6.4				
rectmesh_wc32_rwz	256	1	65536			271400000	2.4147						currently unoptimized
rectmesh_wc32_rwz	128	2	65536			286520000	2.2873						currently unoptimized

R400 Fill Rate Tests
Updated 1/15/2003

Test	Size	Grid (nxn)	Pixels	RBRC Clks	RBRC Pix/Clk	RBRC Pix/Clk (noflush)	R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
rectmesh_wc32	64	1	4096	827	4.9528	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.6713	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.8754	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.6857	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.6857	7.923588	8	99.04%	7.871	100.66%
trimesh_wc32	64	1	4096	862	4.7517	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.4515	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.8068	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.6866	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.6338	7.868412	8	98.36%		


Color Fill Rates
7.95
7.9
7.85
7.8
7.75
7.7
7.65
7.6
7.55
Pix/Clk
64
128
256
Prim Size (256x256)
rectmesh_wc32_256
trimesh_wc32_256


Color Fill Rates
8.2
8
7.8
7.6
7.4
7.2
7
6.8
6.6
6.4
6.2
6
Pix/Clk
4096
16384
65536
Pixels
rectmesh_wc32
trimesh_wc32

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Size	Grid (nxn)	RBRC Clks (all_busys)	RBRC Pix/Clk
rectmesh_wc32	64	1	827	4.9528
rectmesh_wc32	64	4	8543	7.6713
rectmesh_wc32	128	1	2383	6.8754
rectmesh_wc32	128	2	8527	7.6857
rectmesh_wc32	256	1	8527	7.6857
trimesh_wc32	64	1	862	4.7517
trimesh_wc32	64	4	8795	7.4515
trimesh_wc32	128	1	2407	6.8068
trimesh_wc32	128	2	8526	7.6866
trimesh_wc32	256	1	8585	7.6338

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Pixels	Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_wc32	4096	7.17338	8	89.67%			
rectmesh_wc32	65536	7.90829	8	98.85%			
rectmesh_wc32	16384	7.702868	8	96.29%			
rectmesh_wc32	65536	7.923588	8	99.04%			
rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	4096	6.759076	8	84.49%			
trimesh_wc32	65536	7.674903	8	95.94%			
trimesh_wc32	16384	7.616922	8	95.21%			
trimesh_wc32	65536	7.924547	8	99.06%			
trimesh_wc32	65536	7.868412	8	98.36%			

rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32	65536	7.90829	8	98.85%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
rectmesh_wc32	64	1	827	4.9528	rectmesh_wc32	4096	7.17338	8	89.67%		
rectmesh_wc32	128	1	2383	6.8754	rectmesh_wc32	16384	7.702868	8	96.29%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	1	862	4.7517	trimesh_wc32	4096	6.759076	8	84.49%		
trimesh_wc32	128	1	2407	6.8068	trimesh_wc32	16384	7.616922	8	95.21%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32	65536	7.868412	8	98.36%		
rectmesh_wc32	64	4	8543	7.6713	rectmesh_wc32_256	65536	7.90829	8	98.85%		
rectmesh_wc32	128	2	8527	7.6857	rectmesh_wc32_256	65536	7.923588	8	99.04%		
rectmesh_wc32	256	1	8527	7.6857	rectmesh_wc32_256	65536	7.923588	8	99.04%	7.871268	100.66%
trimesh_wc32	64	4	8795	7.4515	trimesh_wc32_256	65536	7.674903	8	95.94%		
trimesh_wc32	128	2	8526	7.6866	trimesh_wc32_256	65536	7.924547	8	99.06%		
trimesh_wc32	256	1	8585	7.6338	trimesh_wc32_256	65536	7.868412	8	98.36%		

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Size	Grid (nxn)	Pixels	GC Cntx17 busy	GC Pix/Clk	RBRC Clks (all_busys)	RBRC Pix/Clk	Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%			

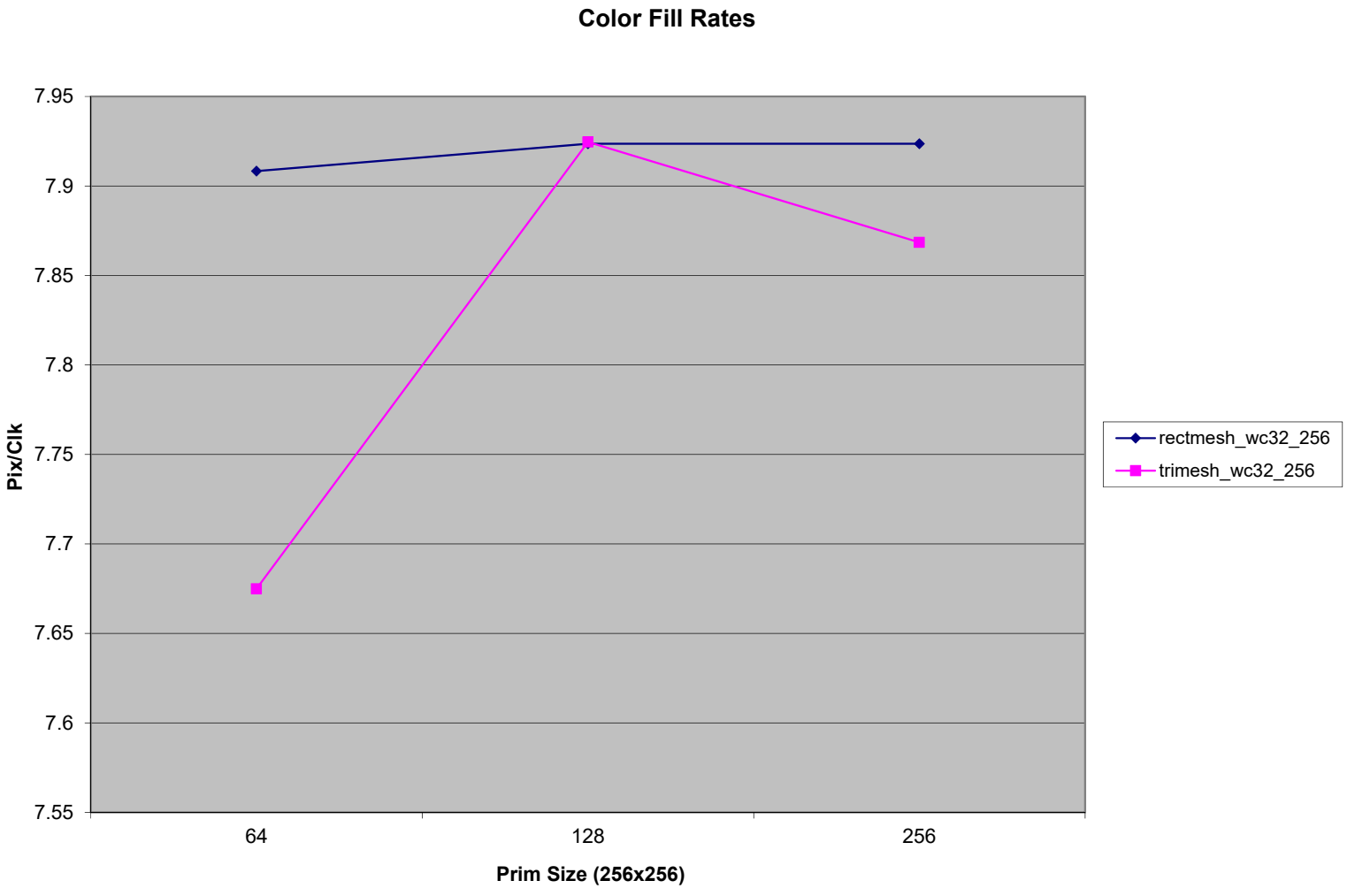
R400 Fill Rate Tests
Updated 1/xx/2003

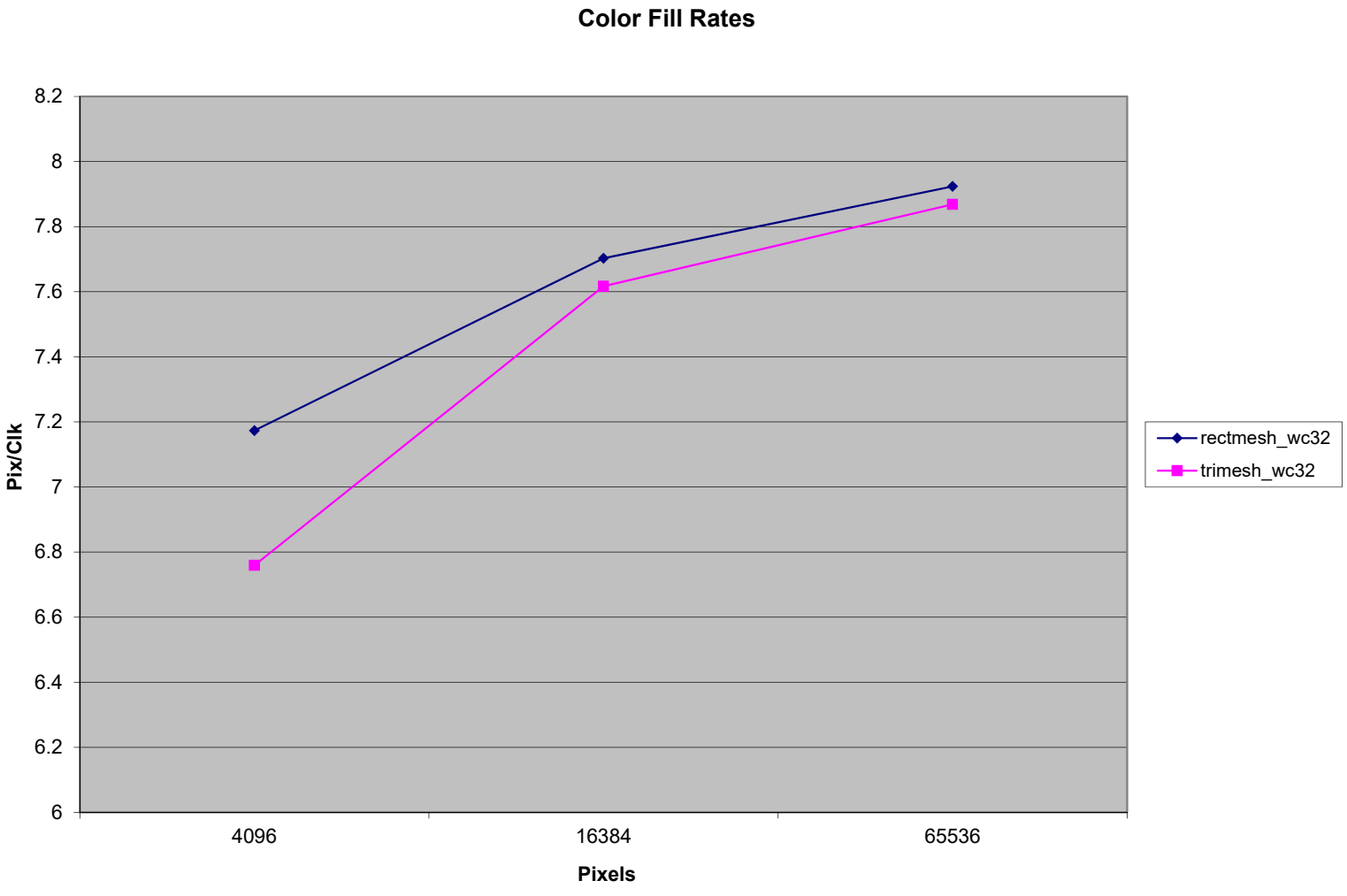
Test	Size	Grid (nxn)	Pixels	GC Cntx17 busy	GC Pix/Clk	RBRC Clks (all_busys)	RBRC Pix/Clk	RBRC Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_wc32	64	1	4096			827	4.9528	7.17338	8	89.67%			
rectmesh_wc32	64	4	65536			8543	7.6713	7.90829	8	98.85%			
rectmesh_wc32	128	1	16384			2383	6.8754	7.702868	8	96.29%			
rectmesh_wc32	128	2	65536			8527	7.6857	7.923588	8	99.04%			
rectmesh_wc32	256	1	65536			8527	7.6857	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64	1	4096			862	4.7517	6.759076	8	84.49%			
trimesh_wc32	64	4	65536			8795	7.4515	7.674903	8	95.94%			
trimesh_wc32	128	1	16384			2407	6.8068	7.616922	8	95.21%			
trimesh_wc32	128	2	65536			8526	7.6866	7.924547	8	99.06%			
trimesh_wc32	256	1	65536			8585	7.6338	7.868412	8	98.36%			
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%			
rectmesh_wc32_t128pt	64	1	4096	2705	1.5142				6.4				
rectmesh_wc32_t128pt	64	4	65536						6.4				
rectmesh_wc32_t256pt	128	1	16384						6.4				
rectmesh_wc32_t256pt	128	2	65536						6.4				
rectmesh_wc32_t256pt	256	1	65536						6.4				
trimesh_wc32_t256pt	128	1	16384						6.4				apparent hang (RB->MC)
trimesh_wc32_t256pt	128	2	65536						6.4				
trimesh_wc32_t256pt	256	1	65536						6.4				
rectmesh_wc32_rwz	256	1	65536			271400000	2.4147						currently unoptimized
rectmesh_wc32_rwz	128	2	65536			286520000	2.2873						currently unoptimized

R400 Fill Rate Tests
Updated 1/15/2003

RBRC

Test	Size	Grid (nxn)	Pixels	Clks	Pix/Clk	Pix/Clk (noflush)	R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
rectmesh_wc32	64	1	4096	827	4.9528	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.6713	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.8754	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.6857	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.6857	7.923588	8	99.04%	7.871	100.66%
trimesh_wc32	64	1	4096	862	4.7517	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.4515	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.8068	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.6866	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.6338	7.868412	8	98.36%		


Color Fill Rates
7.95
7.9
7.85
7.8
7.75
7.7
7.65
7.6
7.55
Pix/Clk
64
128
256
Prim Size (256x256)
rectmesh_wc32_256
trimesh_wc32_256


Color Fill Rates
8.2
8
7.8
7.6
7.4
7.2
7
6.8
6.6
6.4
6.2
6
Pix/Clk
4096
16384
65536
Pixels
rectmesh_wc32
trimesh_wc32

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Size	Grid (nxn)	RBRC Clks (all_busys)	RBRC Pix/Clk
rectmesh_wc32	64	1	827	4.9528
rectmesh_wc32	64	4	8543	7.6713
rectmesh_wc32	128	1	2383	6.8754
rectmesh_wc32	128	2	8527	7.6857
rectmesh_wc32	256	1	8527	7.6857
trimesh_wc32	64	1	862	4.7517
trimesh_wc32	64	4	8795	7.4515
trimesh_wc32	128	1	2407	6.8068
trimesh_wc32	128	2	8526	7.6866
trimesh_wc32	256	1	8585	7.6338

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Pixels	Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_wc32	4096	7.17338	8	89.67%			
rectmesh_wc32	65536	7.90829	8	98.85%			
rectmesh_wc32	16384	7.702868	8	96.29%			
rectmesh_wc32	65536	7.923588	8	99.04%			
rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	4096	6.759076	8	84.49%			
trimesh_wc32	65536	7.674903	8	95.94%			
trimesh_wc32	16384	7.616922	8	95.21%			
trimesh_wc32	65536	7.924547	8	99.06%			
trimesh_wc32	65536	7.868412	8	98.36%			

Test	Size	Grid (nxn)	Clks (all_busys)	Pix/Clk
rectmesh_wc32	64	1	827	4.9528
rectmesh_wc32	64	4	8543	7.6713
rectmesh_wc32	128	1	2383	6.8754
rectmesh_wc32	128	2	8527	7.6857
rectmesh_wc32	256	1	8527	7.6857
rectmesh_wc32	64	1	827	4.9528
rectmesh_wc32	128	1	2383	6.8754
rectmesh_wc32	256	1	8527	7.6857
trimesh_wc32	64	1	862	4.7517
trimesh_wc32	128	1	2407	6.8068
trimesh_wc32	256	1	8585	7.6338
rectmesh_wc32	64	4	8543	7.6713
rectmesh_wc32	128	2	8527	7.6857
rectmesh_wc32	256	1	8527	7.6857
trimesh_wc32	64	4	8795	7.4515
trimesh_wc32	128	2	8526	7.6866
trimesh_wc32	256	1	8585	7.6338

Test	Pixels	Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_wc32	4096	7.17338	8	89.67%			
rectmesh_wc32	65536	7.90829	8	98.85%			
rectmesh_wc32	16384	7.702868	8	96.29%			
rectmesh_wc32	65536	7.923588	8	99.04%			
rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%	
rectmesh_wc32	4096	7.17338	8	89.67%			
rectmesh_wc32	16384	7.702868	8	96.29%			
rectmesh_wc32	65536	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	4096	6.759076	8	84.49%			
trimesh_wc32	16384	7.616922	8	95.21%			
trimesh_wc32	65536	7.868412	8	98.36%			
rectmesh_wc32_256	65536	7.90829	8	98.85%			
rectmesh_wc32_256	65536	7.923588	8	99.04%			
rectmesh_wc32_256	65536	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32_256	65536	7.674903	8	95.94%			
trimesh_wc32_256	65536	7.924547	8	99.06%			
trimesh_wc32_256	65536	7.868412	8	98.36%			

R400 Fill Rate Tests
Updated 1/15/2003

Test	Size	Grid (nxn)	Pixels	Clks	RBRC Pix/Clk	Pix/Clk (noflush)	R400 (Exp)	% R400 (Exp)	R300 (Sim)	% R300 (Sim)
rectmesh_rwc32	128	1	16384	2704	6.0591716	6.69281	8	75.74%		
rectmesh_rwc32	128	2	65536	11656	5.622512	5.748772	8	70.28%		
rectmesh_rwc32	256	1	65536	11272	5.8140525	5.949165	8	72.68%	7.0981	81.91%
trimesh_rwc32	128	1	16384	3095	5.2936995	5.771046	8	66.17%		
trimesh_rwc32	128	2	65536	11909	5.5030649	5.623959	8	68.79%		
trimesh_rwc32	256	1	65536	11571	5.6638147	5.791958	8	70.80%		

R400 Fill Rate Tests
Updated 1/xx/2003

Test	Size	Grid (nxn)	Pixels	GC Cntx17 busy	GC Pix/Clk	RBRC Clks (all_busys)	RBRC Pix/Clk	RBRC Pix/Clk (noflush)	R400 Expected	% R400 Expected	R300 Simulated	% R300 Simulated	Notes
rectmesh_wc32	64	1	4096			827	4.9528	7.17338	8	89.67%			
rectmesh_wc32	64	4	65536			8543	7.6713	7.90829	8	98.85%			
rectmesh_wc32	128	1	16384			2383	6.8754	7.702868	8	96.29%			
rectmesh_wc32	128	2	65536			8527	7.6857	7.923588	8	99.04%			
rectmesh_wc32	256	1	65536			8527	7.6857	7.923588	8	99.04%	7.871268	100.66%	
trimesh_wc32	64	1	4096			862	4.7517	6.759076	8	84.49%			
trimesh_wc32	64	4	65536			8795	7.4515	7.674903	8	95.94%			
trimesh_wc32	128	1	16384			2407	6.8068	7.616922	8	95.21%			
trimesh_wc32	128	2	65536			8526	7.6866	7.924547	8	99.06%			
trimesh_wc32	256	1	65536			8585	7.6338	7.868412	8	98.36%			
rectmesh_rwc32	128	1	16384			2704	6.0592		8	75.74%			
rectmesh_rwc32	128	2	65536			11656	5.6225		8	70.28%			
rectmesh_rwc32	256	1	65536			11272	5.8141		8	72.68%	7.098056	81.91%	
trimesh_rwc32	128	1	16384			3095	5.2937		8	66.17%			
trimesh_rwc32	128	2	65536			11909	5.5031		8	68.79%			
trimesh_rwc32	256	1	65536			11571	5.6638		8	70.80%			
rectmesh_wc32_t128pt	64	1	4096	2705	1.5142				6.4				
rectmesh_wc32_t128pt	64	4	65536						6.4				
rectmesh_wc32_t256pt	128	1	16384						6.4				
rectmesh_wc32_t256pt	128	2	65536						6.4				
rectmesh_wc32_t256pt	256	1	65536						6.4				
trimesh_wc32_t256pt	128	1	16384						6.4				apparent hang (RB->MC)
trimesh_wc32_t256pt	128	2	65536						6.4				
trimesh_wc32_t256pt	256	1	65536						6.4				
rectmesh_wc32_rwz	256	1	65536			271400000	2.4147						currently unoptimized
rectmesh_wc32_rwz	128	2	65536			286520000	2.2873						currently unoptimized

R400 Fill Rate Tests
Updated 1/15/2003

RBRC

Test	Size	Grid (nxn)	Pixels	Clks	Pix/Clk	Pix/Clk (noflush)	R400 (Exp)	% R400 Expected	R300 (Sim)	% R300 Simulated
rectmesh_wc32	64	1	4096	827	4.9528	7.17338	8	89.67%		
rectmesh_wc32	64	4	65536	8543	7.6713	7.90829	8	98.85%		
rectmesh_wc32	128	1	16384	2383	6.8754	7.702868	8	96.29%		
rectmesh_wc32	128	2	65536	8527	7.6857	7.923588	8	99.04%		
rectmesh_wc32	256	1	65536	8527	7.6857	7.923588	8	99.04%	7.871	100.66%
trimesh_wc32	64	1	4096	862	4.7517	6.759076	8	84.49%		
trimesh_wc32	64	4	65536	8795	7.4515	7.674903	8	95.94%		
trimesh_wc32	128	1	16384	2407	6.8068	7.616922	8	95.21%		
trimesh_wc32	128	2	65536	8526	7.6866	7.924547	8	99.06%		
trimesh_wc32	256	1	65536	8585	7.6338	7.868412	8	98.36%		

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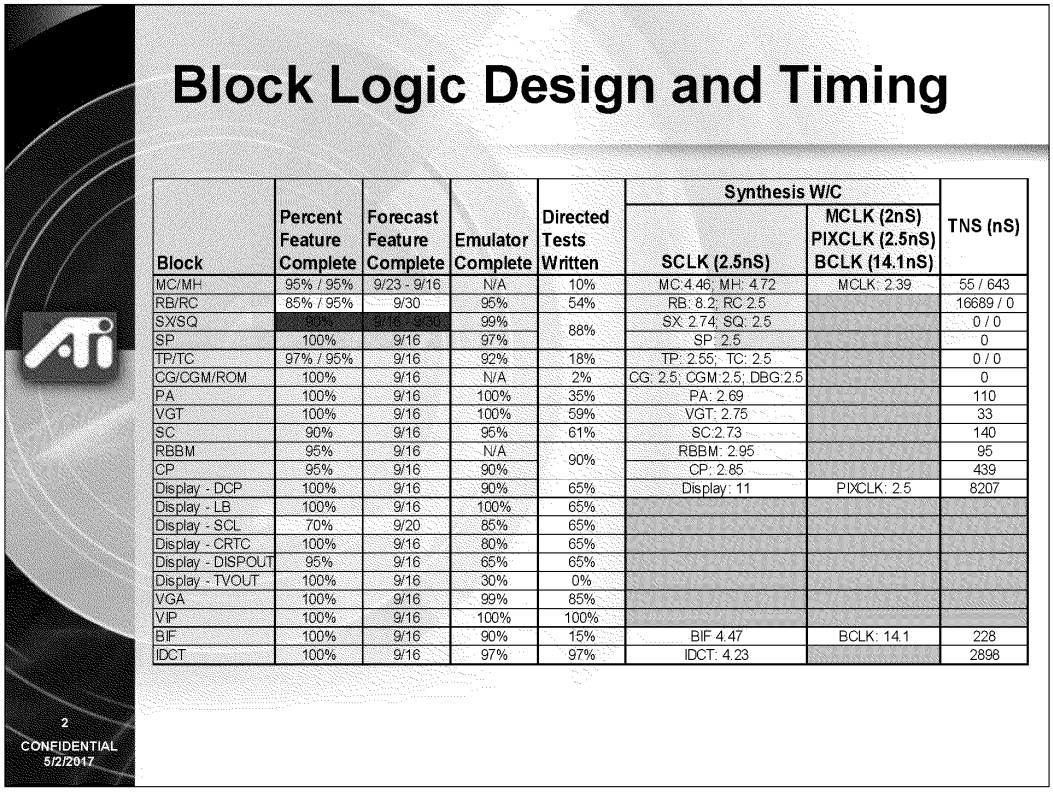

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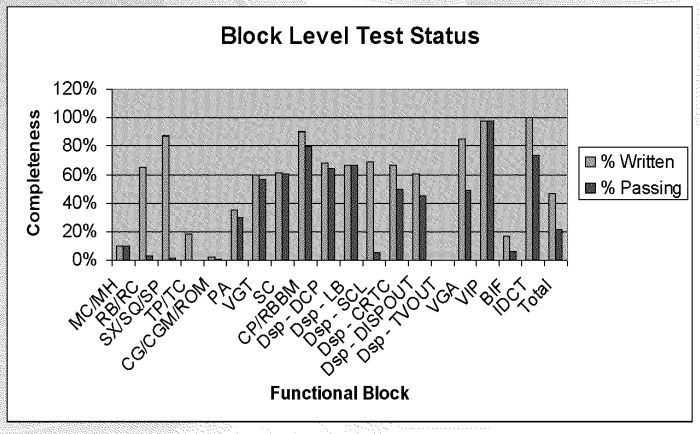
Block Level Test



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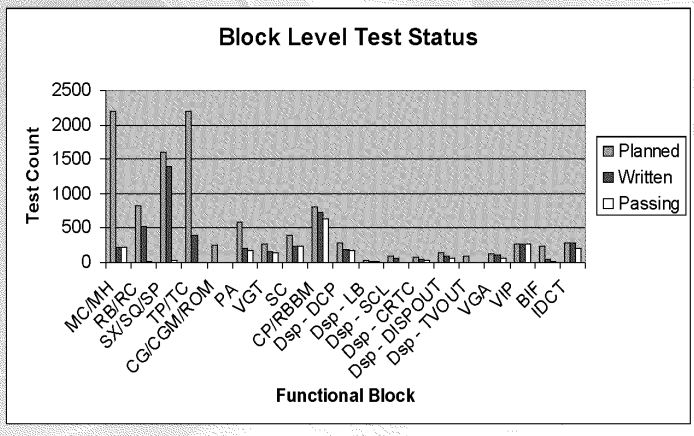
Block Level Test



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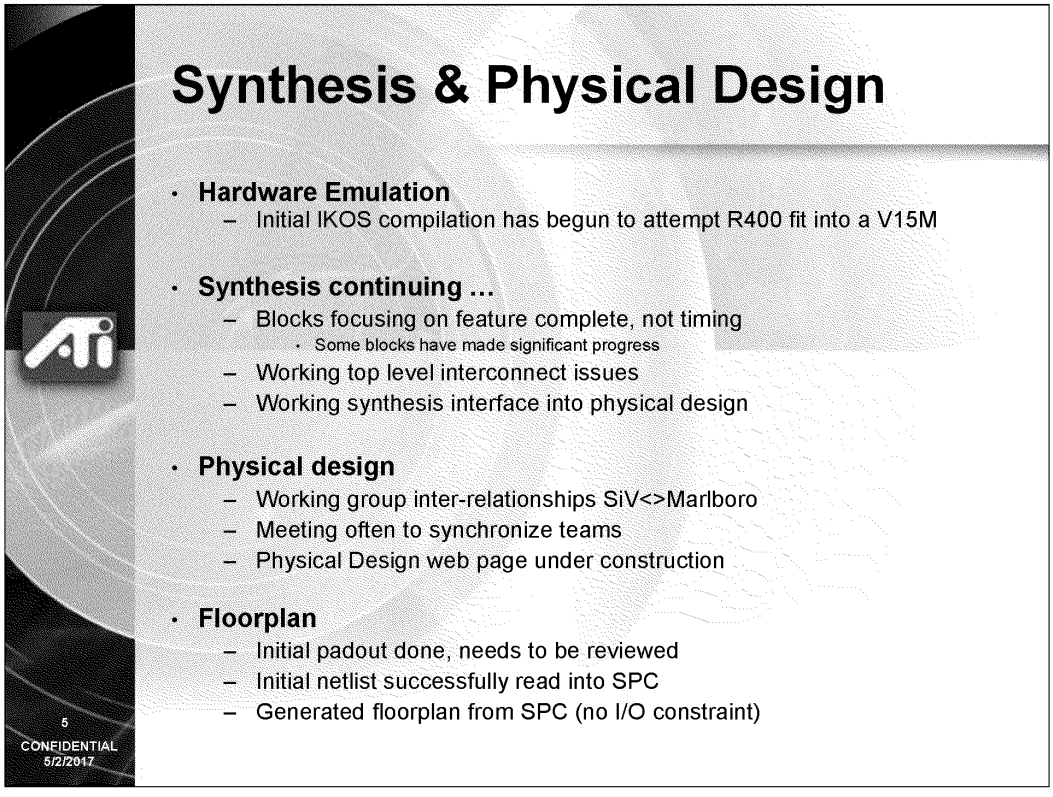

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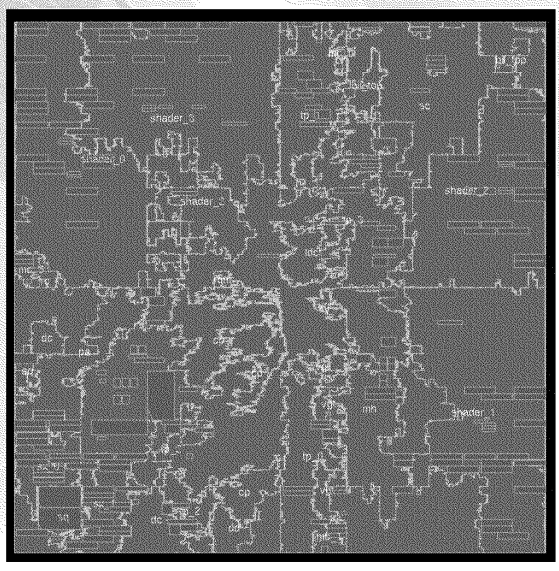
First R400 Floorplan - Silicon Perspectives
(no I/O constraints)



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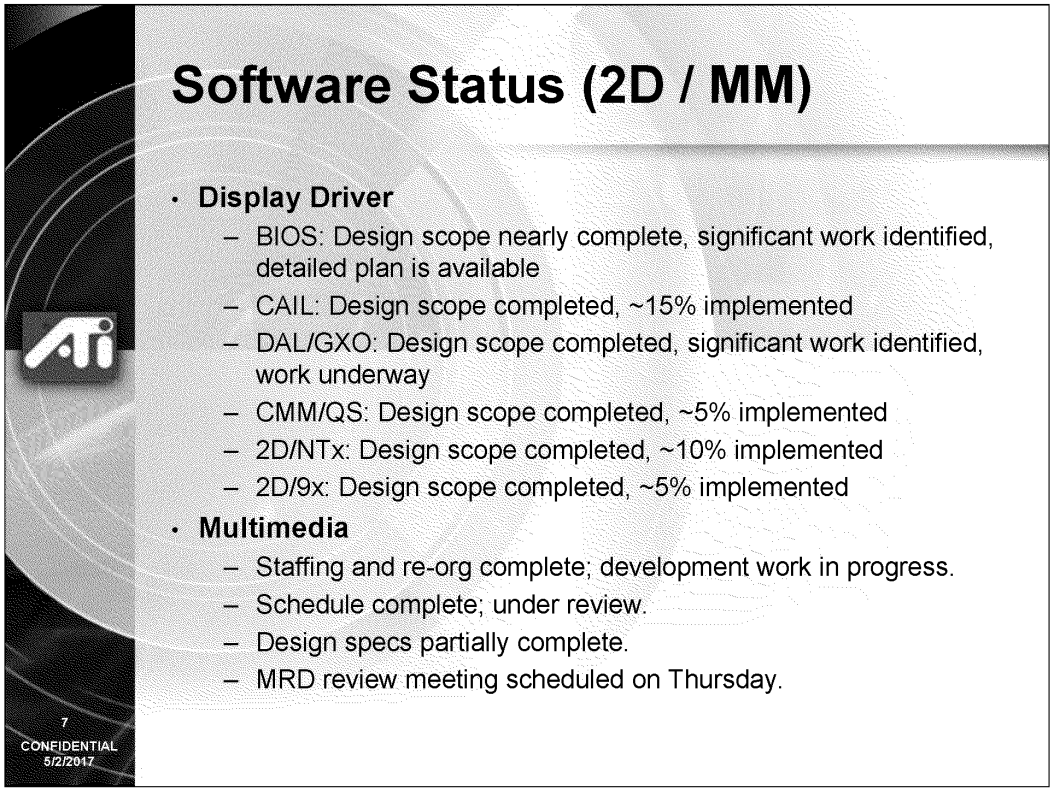

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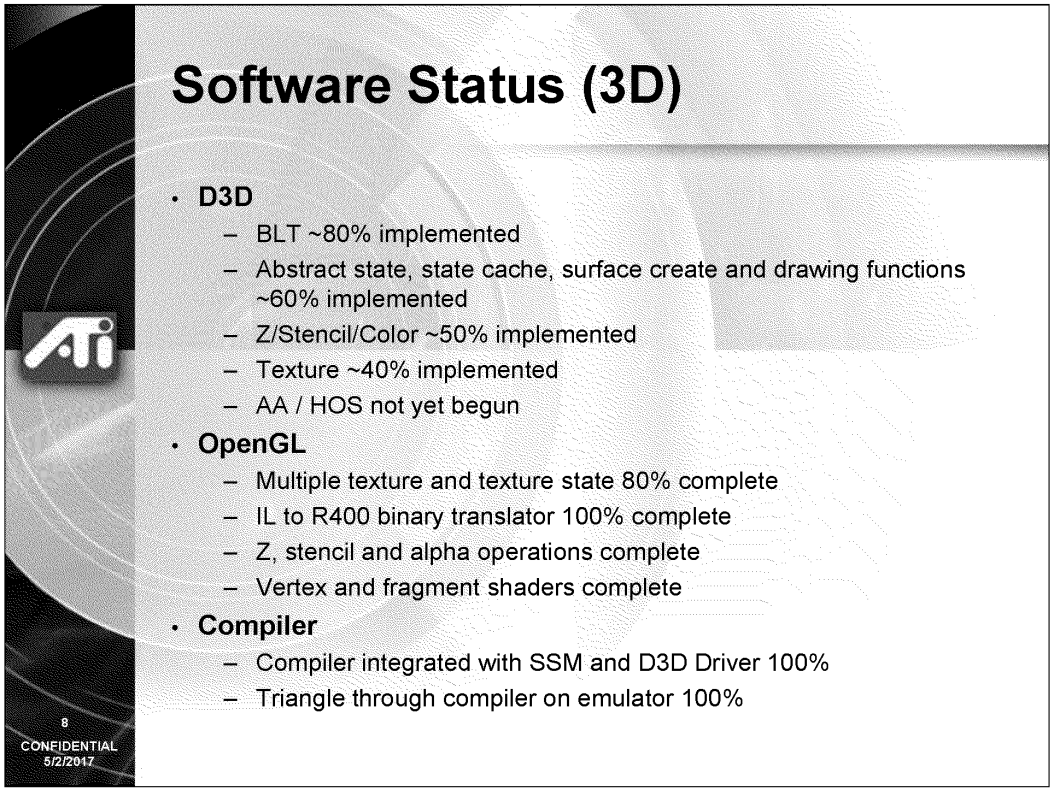

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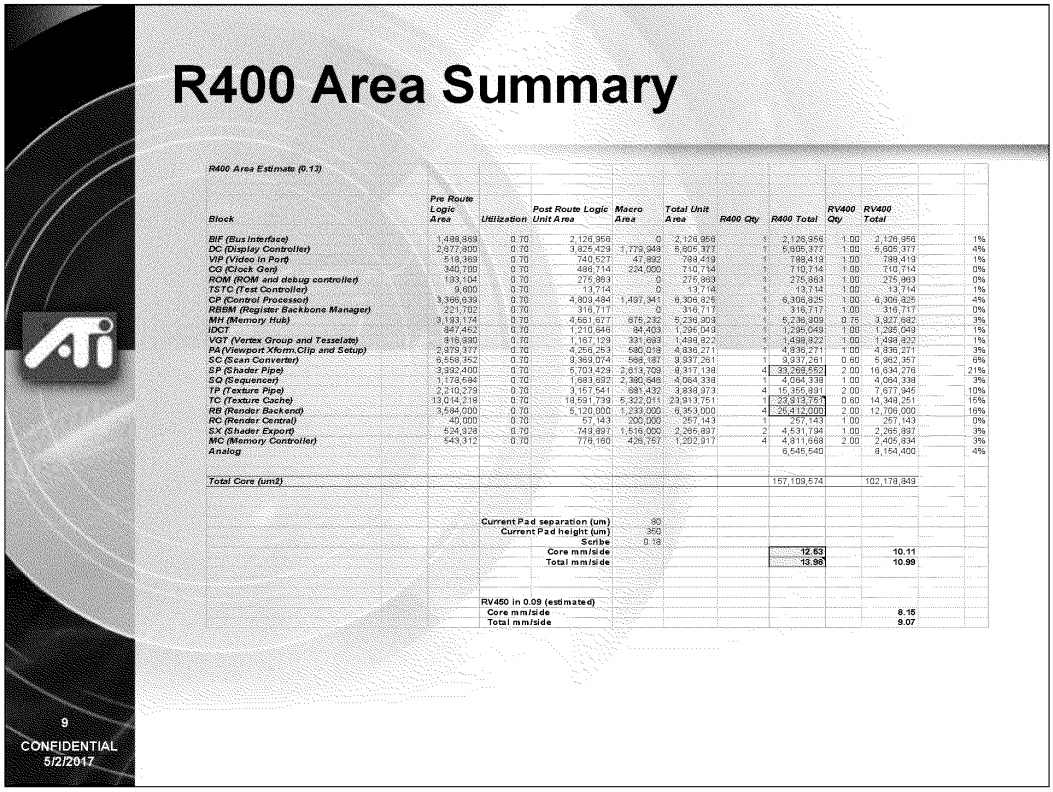

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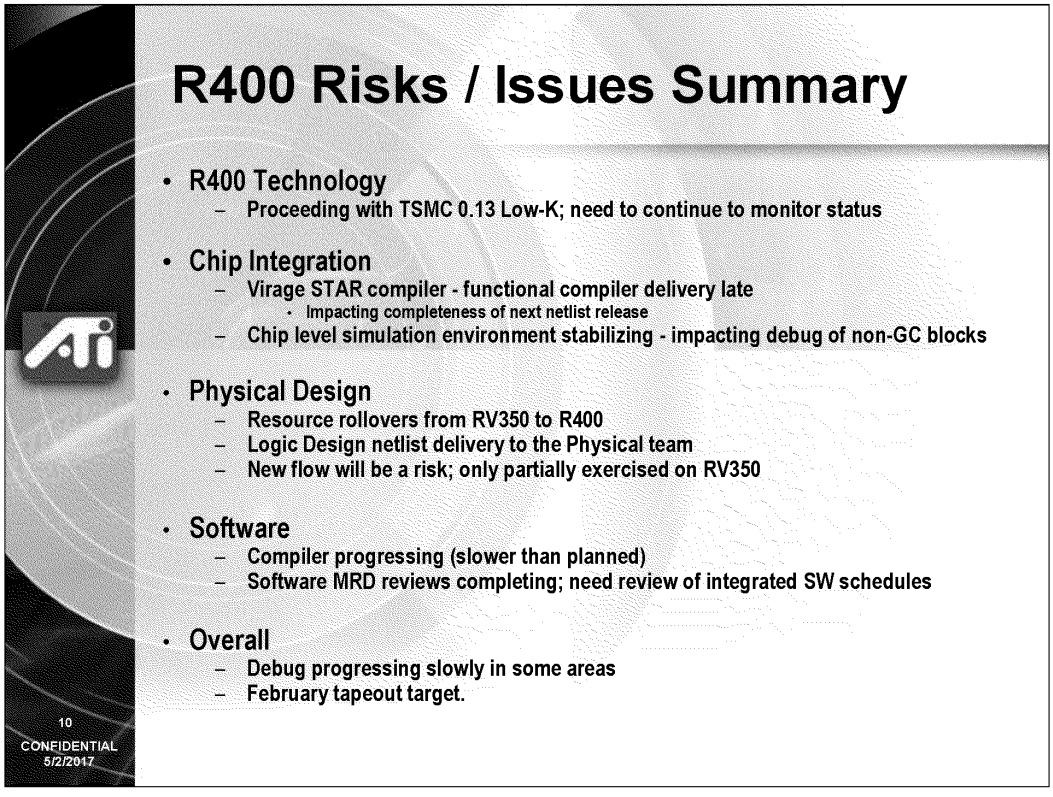

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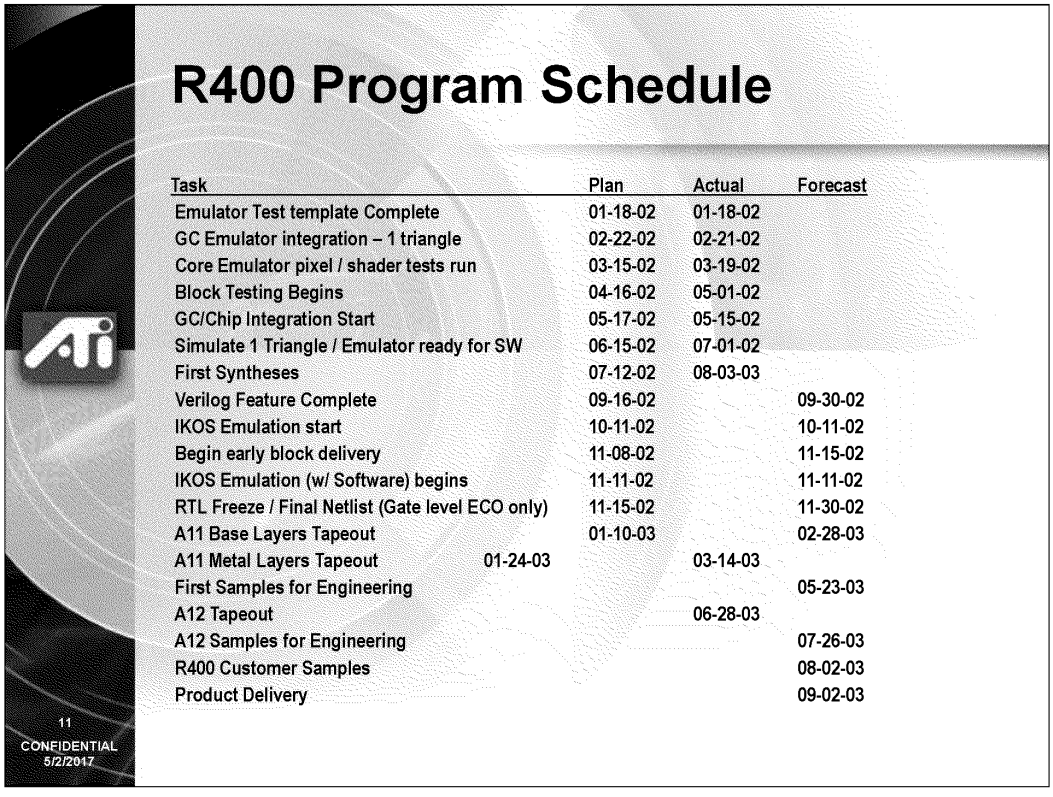

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R400 Area Estimate (0.13)

Block	Pre Route Logic Area	Utilization	Post Route Logic Unit Area	Macro Area	Total Unit Area	R400 Qty	R400 Total	RV400 Qty	RV400 Total	
BIF (Bus Interface)	1,488,869	0.70	2,126,956	0	2,126,956	1	2,126,956	1.00	2,126,956	1% BIF (Bus Interface)
DC (Display Controller)	2,677,800	0.70	3,825,429	1,779,948	5,605,377	1	5,605,377	1.00	5,605,377	4% DC (Display Controller)
VIP (Video In Port)	518,369	0.70	740,527	47,892	788,419	1	788,419	1.00	788,419	1% VIP (Video In Port)
CG (Clock Gen)	340,700	0.70	486,714	224,000	710,714	1	710,714	1.00	710,714	0% CG (Clock Gen)
ROM (ROM and debug controller)	193,104	0.70	275,863	0	275,863	1	275,863	1.00	275,863	0% ROM (ROM and debug controller)
TSTC (Test Controller)	9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714	1% VIP (Video In Port)
CP (Control Processor)	3,366,639	0.70	4,809,484	1,497,341	6,306,825	1	6,306,825	1.00	6,306,825	4% CP (Control Processor)
RBBM (Register Backbone Manager)	221,702	0.70	316,717	0	316,717	1	316,717	1.00	316,717	0% RBBM (Register Backbone Manager)
MH (Memory Hub)	3,193,174	0.70	4,561,677	675,232	5,236,909	1	5,236,909	0.75	3,927,682	3% MH (Memory Hub)
IDCT	847,452	0.70	1,210,646	84,403	1,295,049	1	1,295,049	1.00	1,295,049	1% IDCT
VGT (Vertex Group and Tesselate)	816,990	0.70	1,167,129	331,693	1,498,822	1	1,498,822	1.00	1,498,822	1% VGT (Vertex Group and Tesselate)
PA(Viewport Xform,Clip and Setup)	2,979,377	0.70	4,256,253	580,018	4,836,271	1	4,836,271	1.00	4,836,271	3% PA(Viewport Xform,Clip and Setup)
SC (Scan Converter)	6,558,352	0.70	9,369,074	568,187	9,937,261	1	9,937,261	0.60	5,962,357	6% SC (Scan Converter)
SP (Shader Pipe)	3,992,400	0.70	5,703,429	2,613,709	8,317,138	4	33,268,552	2.00	16,634,276	21% SP (Shader Pipe)
SQ (Sequencer)	1,178,584	0.70	1,683,692	2,380,646	4,064,338	1	4,064,338	1.00	4,064,338	3% SQ (Sequencer)
TP (Texture Pipe)	2,210,279	0.70	3,157,541	681,432	3,838,973	4	15,355,891	2.00	7,677,945	10% TP (Texture Pipe)
TC (Texture Cache)	13,014,218	0.70	18,591,739	5,322,011	23,913,751	1	23,913,751	0.60	14,348,251	15% TC (Texture Cache)
RB (Render Backend)	3,584,000	0.70	5,120,000	1,233,000	6,353,000	4	25,412,000	2.00	12,706,000	16% RB (Render Backend)
RC (Render Central)	40,000	0.70	57,143	200,000	257,143	1	257,143	1.00	257,143	0% RC (Render Central)
SX (Shader Export)	524,928	0.70	749,897	1,516,000	2,265,897	2	4,531,794	1.00	2,265,897	3% SX (Shader Export)
MC (Memory Controller)	543,312	0.70	776,160	426,757	1,202,917	4	4,811,668	2.00	2,405,834	3% MC (Memory Controller)
Analog							6,545,540		8,154,400	4% Analog
Total Core (um2)							157,109,574		102,178,849	

Current Pad separation (um)	80		
Current Pad height (um)	350		
Scribe	0.18		
Core mm/side		**12.53**	**10.11**
Total mm/side		**13.98**	**10.99**

RV450 in 0.09 (estimated)

Core mm/side	**8.15**
Total mm/side	**9.07**

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)	Tests Planned	Tests Written	Tests Passing
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14.1nS)				
MC/MH	95% / 95%	9/23 - 9/16	N/A	10%	MC:4.46; MH: 4.72	MCLK: 2.39	55 / 643	2200	225	215
RB/RC	85% / 95%	9/30	95%	54%	RB: 8.2; RC 2.5		16689 / 0	720	390	22
SX/SQ	90%	9/16 - 9/30	99%	88%	SX: 2.74; SQ: 2.5		0 / 0	1600	1400	27
SP	100%	9/16	97%		SP: 2.5		0			
TP/TC	97% / 95%	9/16	92%	18%	TP: 2.55; TC: 2.5		0 / 0	2200	400	0
CG/CGM/ROM	100%	9/16	N/A	2%	CG: 2.5; CGM:2.5; DBG:2.5		0	253	5	2
PA	100%	9/16	100%	35%	PA: 2.69		110	584	206	175
VGT	100%	9/16	100%	59%	VGT: 2.75		33	263	156	149
SC	90%	9/16	95%	61%	SC:2.73		140	389	239	236
RBBM	95%	9/16	N/A	90%	RBBM: 2.95		95			
CP	95%	9/16	90%		CP: 2.85		439	800	722	635
Display - DCP	100%	9/16	90%	65%	Display: 11	PIXCLK: 2.5	8207	280	190	179
Display - LB	100%	9/16	100%	65%				30	20	20
Display - SCL	70%	9/20	85%	65%				97	67	5
Display - CRTC	100%	9/16	80%	65%				75	50	37
Display - DISPOUT	95%	9/16	65%	65%				150	91	68
Display - TVOUT	100%	9/16	30%	0%					0	
VGA	100%	9/16	99%	85%				130	110	64
VIP	100%	9/16	100%	100%				275	270	270
BIF	100%	9/16	90%	15%	BIF 4.47	BCLK: 14.1	228	240	40	15
IDCT	100%	9/16	97%	97%	IDCT: 4.23		2898	279	279	204