R400 Program Review

Jan 15, 2003

ATI Corporate Presentation

Target Milestones in Last Month

- **R400 Program Milestones**
    - Whole chip code freeze by 11/23

- **Toronto R400 revised milestones**
    - Achieve 100% passing in block regression by 12/13 with tvout being 1/6.
    - Start IKOS debug 12/20.
    - Achieve revised timing goals by 12/30.
    - Achieve 50% regression passing in chip by 12/30, 100% by 1/30.
    - Start Gate level simulation in Jan.
    - Complete system tests & debugged by 1/30
    - Deliver final netlist 1/30.

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What Have We Achieved

- **Status Summary**
  - ✓ Achieved 100% passing on block level regression on Dec 30 with the exception of tvout and bif
  - ✓ Achieved over 50% passing on chip level regression on Dec 30
  - ✓ PCI configuration cycles passed on IKOS validation on netlist 2.0
  - ✓ System tests are on track to be delivered & debugged
  - ✓ Emulation work in bif & tvout are on track. The completion dates are Jan 24 for tvout and Feb 7 for bif
  - ✓ Synthesis timing/area closure is in progress
  - ✓ Deliver IDCT final netlist on Jan 24

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What Have We Achieved (specs, coding, emulation, tests)

- Coding is 100% complete with 2% outstanding in BIF(agp 64byte write & perf counter).
- Emulation is 100% completed with vga(tiled mem dump) and bif.
- Tests are 100% released with lb, tvout, bif & system outstanding, covering RT, hdtv, bif changes.

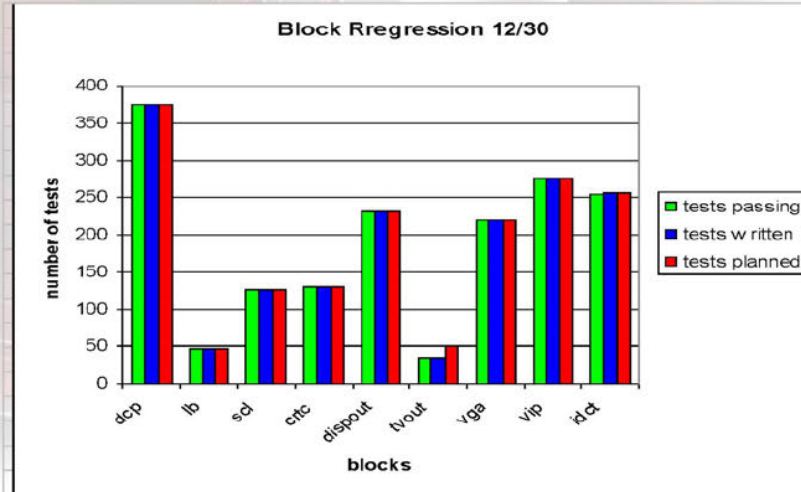| Design		RTL specs	RTL coding	Emulation	Tests Written
display	dcp	100%	100%	100%	100%
	lb	100%	100%	100%	98%
	scl	100%	100%	100%	100%
	crtc	100%	100%	100%	100%
	dispout	100%	100%	100%	100%
	tvout	100%	100%	100%	80%
vga		100%	100%	99%	100%
vip		100%	100%	100%	100%
BIF		96%	98%	90%	50%
IDCT		100%	100%	100%	100%
system					35%

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What Have We Achieved (block RTL regression)

- All blocks are 100% passing
- Tvout reached 80% passing and plan to complete by Jan24

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