R400 Program Review

Feb 12, 2003

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Target Milestones in Last Month

- **Toronto R400 revised milestones**
- ➤ Deliver IDCT final netlist by Jan 24
- ➤ Achieve DC 100% passing in chip level regression by Jan 30
- ➤ IKOS validation on netlist 3.0.
- ➤ Achieve DC timing goals by Jan 30.
- ➤ Deliver DC final netlist by Feb 15.
- ➤ Start Gate level simulation in Jan.
- ➤ Close bif timing & existing tests issues by 1/30.
- ➤ Deliver BIF final netlists by Feb 28

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What Have We Achieved

- **Status Summary**
  - ✓ Delivered final idct netlist on Feb 5 with meeting timing target & validation target. Although there are 4 chip level tests failing we believe it is not idct issue.
  - ✓ Achieved 84% chip level regression passing.
  - ✓ Register cycles passing on ikos with netlist 3.0 but having problems with memory interface.
  - ✓ Worked out DC synthesis issues with Rob and the cell count is reduced to 382k from 400k and the worst timinig violation is down to –0.15ns.
  - ✓ 98% existing bif tests passing in emulation with a number of 2D related tests failing, while 30% existing bif tests passing in chip level simulation
  - ✓ Bif new feature related emulation work to follow.

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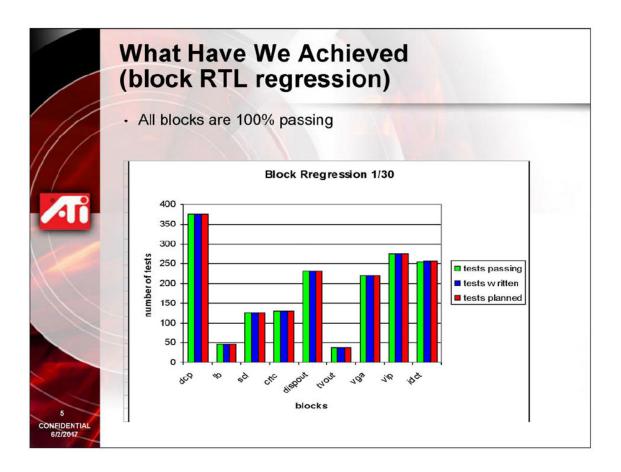# What Have We Achieved (specs, coding, emulation, tests)

- Spec is 100% complete in display & idct while bif is 98% complete.
- Coding is 100% complete.
- Emulation is 100% completed with vga(tiled mem dump) and bif outstanding.
- Tests are 100% released with 10% bif & system tests outstanding.

Design		RTL specs	RTL coding	Emulation	Tests Written
display	dcp	100%	100%	100%	100%
	lb	100%	100%	100%	100%
	scl	100%	100%	100%	100%
	crtc	100%	100%	100%	100%
	dispout	100%	100%	100%	100%
	tvout	100%	100%	100%	100%
vga		100%	100%	99%	100%
vip		100%	100%	100%	100%
BIF		98%	100%	95%	90%
IDCT		100%	100%	100%	100%
system					90%

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What Have We Achieved (block RTL regression)

- All blocks are 100% passing

Block Rregression 1/30

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