Change 138566 on 2003/12/19 by fliljero@fl_frank

Added 3 new packets for improved type-0 packet processing:
Incremental_Update_State/Const/Instr

Change 137750 on 2003/12/16 by fliljero@fl_knarf

Added optimized Event_Write* packets & new opcodes

Change 137101 on 2003/12/12 by fliljero@fl_frank

Added Wait_Reg_Eq & Wait_Reg_Gte PM4 packet descriptions

Change 137025 on 2003/12/11 by fliljero@fl_knarf

updated documentation on error checking and removed reference to type-1 packet.

Change 136800 on 2003/12/10 by fliljero@fl_knarf

Updated description for MEM_WRITE_CNTR to include how to change the core clock interval
from 1 <--> 16.

Change 136780 on 2003/12/10 by fliljero@fl_knarf

Updated Me_Init packet for Header Dumps & Error checking...added note about recompiling
microcode to enable these debug only features.

Change 136762 on 2003/12/10 by fliljero@fl_knarf

Updates related to CP_MEQ

Change 136302 on 2003/12/08 by fliljero@fl_frank

Updates to MEQ related registers & busy signals

Change 135746 on 2003/12/05 by fliljero@fl_knarf

Updated CP Interrupt packet for performance

Change 134564 on 2003/12/01 by fliljero@fl_knarf

Max Buffer Size in Indirect Buffer Packets is [19:0]...Spec had [22:0]

Change 130037 on 2003/11/04 by fliljero@fl_knarf

Added registers and PM4 packet changes related to the Software Managed Instruction
Store...



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Change 124599 on 2003/10/02 by fliljero@fl_knarf

no change

Change 123990 on 2003/09/30 by fliljero@fl_knarf

added changes to set_state and load_constant_context

Change 123315 on 2003/09/25 by fliljero@fl_knarf

Updated Const_Prefetch packet to issue only once per LCC packet. When the LCC ordinals repeat, they also repeat in the Const_Prefetch packet. Formerly, there was a new Const_Prefetch packet for each repeat of the ordinals.

Change 123064 on 2003/09/24 by fliljero@fl_knarf

Updated Subblk_Prefetch packet to send the Header only once, followed optionally by each ordinal on a mismatch.

Change 122800 on 2003/09/23 by fliljero@fl_knarf

made drawing change to reflect changes to SRC0 & SRC1 removal of MICROM, MRL & MRM as possible sources. also removed the BOOLEANs as a possible source for SRC1.

Change 120795 on 2003/09/11 by fliljero@fl_knarf

added zpass_done info to the event_write packet

Change 120303 on 2003/09/09 by fliljero@fl_knarf

added predicated bin test results (RT/nRT) to State Management register w/index=0xD

Change 120271 on 2003/09/09 by fliljero@fl_knarf

Update Event Write packet for new functionality for the zpass_done event ... clears the context valid flag, which in turn will cause the context to be rolled on the next state packet.

Change 119939 on 2003/09/08 by fliljero@fl_knarf

added 128-bit write enable to the MH field to the CP_DEBUG register.

Change 119726 on 2003/09/05 by fliljero@fl_knarf

added predicate_disable bit to CP_DEBUG

Change 119667 on 2003/09/05 by fliljero@fl_knarf



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```
removed DATA ordinal from the MEM_WRITE_CNTR packet description

Change 119663 on 2003/09/05 by fliljero@fl_knarf

added MEM_WRITE_CNTR opcode
moved SET_BIN_MASK/SELECT opcodes to unused locations

Change 119301 on 2003/09/03 by fliljero@fl_knarf

made updates to the event write packet and added new associated register:
CP_ME_CF_EVENT_SRC

Change 119223 on 2003/09/03 by fliljero@fl_knarf

added CP_PROG_COUNTER,
related update to CP_ME_CNTL,
related update to EVENT_WRITE packet, &
related new PM4 packet MEM_WRITE_CNTR

Change 118709 on 2003/08/29 by fliljero@fl_fliljeros

added real-time versions of the predicate registers: BIN_MASK & BIN_SELECT

Change 118408 on 2003/08/27 by fliljero@fl_knarf

updated/added coherency registers and interface
updated/added predicate registers and description

Change 118362 on 2003/08/27 by fliljero@fl_knarf

added type-3 predicated packet related information

Change 115561 on 2003/08/08 by fliljero@fl_knarf

renamed references from R400 to Crayola

Change 115547 on 2003/08/08 by fliljero@fl_knarf

Removed all references to PIO/Push mode and its associated registers:
CP_CSQ_CNTL
CP_ 'RING | INDIRECT1 | INDIRECT2 | REAL_TIME | IB_ST | RT_ST'_PUSH

Change 115546 on 2003/08/08 by fliljero@fl_knarf

renamed to use Crayola rather than R400

Change 115463 on 2003/08/07 by fliljero@fl_knarf
```



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Baseline for the PM4 Spec (after the start of Xenos)

Change 115462 on 2003/08/07 by fliljero@fl_knarf

added note to cover to see PM4 Spec Crayola for the latest PM4 data

Change 115461 on 2003/08/07 by fliljero@fl_knarf

Baseline for Crayola CP Spec (after the start of Xenos)

Change 115460 on 2003/08/07 by fliljero@fl_knarf

added note on cover to see CP Spec Crayola for the latest CP data.

Change 114564 on 2003/08/01 by aashkar@aashkar2_crayola_win

Updated Spec with the addition of bit 19 in the interrupt registers for the software interrupt (SW_INT). This interrupt is moving to the CP from the MH.

Change 108824 on 2003/07/02 by jacarey@fl_jcarey_desktop

Update Min / Max functions in emulator to match hardware.
Hardware produces a 32-bit signed extended result of 16-bit comparision value.

Change 108680 on 2003/07/01 by jacarey@fl_jcarey_desktop

Add section documenting CP Idling before writing certain control registers.

Change 104633 on 2003/06/06 by jacarey@fl_jcarey_desktop

Document resetting of read registers to zero on reset.

Change 104324 on 2003/06/05 by jacarey@fl_jcarey_desktop

Reset VS & PS De-alloc fifos when ME overwrites the *_Avail_Count counters

Change 104014 on 2003/06/04 by jacarey@fl_jcarey_desktop

Documentation for new debug bit in the CP.

Change 103099 on 2003/05/29 by jacarey@fl_jcarey_desktop

Added oper=comp to document.

Change 101923 on 2003/05/21 by jacarey@fl_jcarey_desktop

Clarification that Isync flushing occurs only before the first "draw" packet after the transition.



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Change 101800 on 2003/05/20 by jacarey@fl_jcarey_desktop

Correction to Gradfill prim type for rectangles.

Change 101625 on 2003/05/19 by jacarey@fl_jcarey_desktop

Miscellaneous Corrections to documents w.r.t. 2D Coherency Rectangle Updates.

Change 101380 on 2003/05/16 by jacarey@fl_jcarey_desktop

Clarifications to pre-write-timer and pre-write-limit usage.

Change 100945 on 2003/05/14 by jacarey@fl_jcarey_desktop

Clarifications to Set_Constant and LCC packets w.r.t. write enables for each CONST_ID type.

Change 100549 on 2003/05/12 by jacarey@fl_jcarey_desktop

Microcode Update for 2D surface coherency

Change 100159 on 2003/05/09 by jacarey@fl_jcarey_desktop

Document setting of bit 20 in 2D Booleans as Default_Sel

Change 99510 on 2003/05/07 by jacarey@fl_jcarey_desktop

Updates to document for usage of "flush done" flag in the microcode.

Change 99386 on 2003/05/06 by jacarey@fl_jcarey_desktop

Update

Change 99380 on 2003/05/06 by jacarey@fl_jcarey_desktop

Fix for 2D Coherency (Flushing TC)

Change 98285 on 2003/04/30 by fliljero@fl_frank

latest updates

Change 96875 on 2003/04/22 by fliljero@fl_frank

changed data from one pass to the next to better insure proper validation

Change 96851 on 2003/04/22 by jacarey@fl_jcarey_desktop



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