Change 138566 on 2003/12/19 by fliljero@fl frank

Added 3 new packets for improved type-0 packet processing: Incremental Update State/Const/Instr

Change 137750 on 2003/12/16 by fliljero@fl knarf

Added optimized Event Write\* packets & new opcodes

Change 137101 on 2003/12/12 by fliljero@fl frank

Added Wait Reg Eq & Wait Reg Gte PM4 packet descriptions

Change 137025 on 2003/12/11 by fliljero@fl knarf

updated documentation on error checking and removed reference to type-1 packet.

Change 136800 on 2003/12/10 by fliljero@fl knarf

Updated description for MEM\_WRITE\_CNTR to include how to change the core clock interval from 1 < --> 16.

Change 136780 on 2003/12/10 by fliljero@fl knarf

Updated Me\_Init packet for Header Dumps & Error checking...added note about recompiling microcode to enable these debug only features.

Change 136762 on 2003/12/10 by fliljero@fl knarf

Updates related to CP MEQ

Change 136302 on 2003/12/08 by fliljero@fl frank

Updates to MEQ related registers & busy signals

Change 135746 on 2003/12/05 by fliljero@fl knarf

Updated CP Interrupt packet for performance

Change 134564 on 2003/12/01 by fliljero@fl\_knarf

Max Buffer Size in Indirect Buffer Packets is [19:0]...Spec had [22:0]

Change 130037 on 2003/11/04 by fliljero@fl\_knarf

Added registers and PM4 packet changes related to the Software Managed Instruction Store...



AMD1044 0166380

Change 124599 on 2003/10/02 by fliljero@fl knarf

no change

Change 123990 on 2003/09/30 by fliljero@fl knarf

added changes to set\_state and load\_constant\_context

Change 123315 on 2003/09/25 by fliljero@fl knarf

Updated Const\_Prefetch packet to issue only once per LCC packet. When the LCC ordinals repeat, they also repeat in the Const\_Prefetch packet. Formerly, there was a new Const\_Prefetch packet for each repeat of the ordinals.

Change 123064 on 2003/09/24 by fliljero@fl knarf

Updated Subblk\_Prefetch packet to send the Header only once, followed optionally by each ordinal on a mismatch.

Change 122800 on 2003/09/23 by fliljero@fl knarf

made drawing change to reflect changes to SRC0 & SRC1 removal of MICROM, MRL & MRM as possible sources. also removed the BOOLEANs as a possible source for SRC1.

Change 120795 on 2003/09/11 by fliljero@fl knarf

added zpass\_done info to the event\_write packet

Change 120303 on 2003/09/09 by fliljero@fl knarf

added predicated bin test results (RT/nRT) to State Management register w/index=0xD

Change 120271 on 2003/09/09 by fliljero@fl knarf

Update Event Write packet for new functionality for the zpass\_done event ... clears the context valid flag, which in turn will cause the context to be rolled on the next state packet.

Change 119939 on 2003/09/08 by fliljero@fl knarf

added 128-bit write enable to the MH field to the CP DEBUG register.

Change 119726 on 2003/09/05 by fliljero@fl\_knarf

added predicate\_disable bit to CP\_DEBUG

Change 119667 on 2003/09/05 by fliljero@fl\_knarf



```
removed DATA ordinal from the MEM WRITE CNTR packet description
Change 119663 on 2003/09/05 by fliljero@fl knarf
added MEM WRITE CNTR opcode
moved SET BIN MASK/SELECT opcodes to unused locations
Change 119301 on 2003/09/03 by fliljero@fl knarf
made updates to the event write packet and added new associated register:
CP ME CF EVENT SRC
Change 119223 on 2003/09/03 by fliljero@fl_knarf
added CP PROG COUNTER,
related update to CP ME CNTL,
related update to EVENT_WRITE packet, &
related new PM4 packet MEM WRITE CNTR
Change 118709 on 2003/08/29 by fliljero@fl fliljeros
added real-time versions of the predicate registers: BIN_MASK & BIN_SELECT
Change 118408 on 2003/08/27 by fliljero@fl knarf
updated/added coherency registers and interface
updated/added predicate registers and description
Change 118362 on 2003/08/27 by fliljero@fl knarf
added type-3 predicated packet related information
Change 115561 on 2003/08/08 by fliljero@fl knarf
renamed references from R400 to Crayola
Change 115547 on 2003/08/08 by fliljero@fl knarf
Removed all references to PIO/Push mode and its associated registers:
CP CSQ CNTL
CP 'RING | INDIRECT1 | INDIRECT2 | REAL TIME | IB ST | RT ST' PUSH
Change 115546 on 2003/08/08 by fliljero@fl_knarf
renamed to use Crayola rather than R400
Change 115463 on 2003/08/07 by fliljero@fl_knarf
```



Baseline for the PM4 Spec (after the start of Xenos)

Change 115462 on 2003/08/07 by fliljero@fl knarf

added note to cover to see PM4 Spec Crayola for the latest PM4 data

Change 115461 on 2003/08/07 by fliljero@fl\_knarf

Baseline for Crayola CP Spec (after the start of Xenos)

Change 115460 on 2003/08/07 by fliljero@fl\_knarf

added note on cover to see CP Spec Crayola for the latest CP data.

Change 114564 on 2003/08/01 by aashkar@aashkar2\_crayola\_win

Updated Spec with the addition of bit 19 in the interrupt registers for the software interrupt (SW INT). This interrupt is moving to the CP from the MH.

Change 108824 on 2003/07/02 by jacarey@fl jcarey desktop

Update Min / Max functions in emulator to match hardware. Hardware produces a 32-bit signed extended result of 16-bit comparision value.

Change 108680 on 2003/07/01 by jacarey@fl\_jcarey\_desktop

Add section documenting CP Idling before writing certain control registers.

Change 104633 on 2003/06/06 by jacarey@fl jcarey desktop

Document resetting of read registers to zero on reset.

Change 104324 on 2003/06/05 by jacarey@fl jcarey desktop

Reset VS & PS De-alloc fifos when ME overwrites the \* Avail Count counters

Change 104014 on 2003/06/04 by jacarey@fl jcarey desktop

Documentation for new debug bit in the CP.

Change 103099 on 2003/05/29 by jacarey@fl jcarey desktop

Added oper=comp to document.

Change 101923 on 2003/05/21 by jacarey@fl jcarey desktop

Clarification that Isync flushing occurs only before the first "draw" packet after the transition.



Change 101800 on 2003/05/20 by jacarey@fl jcarey desktop Correction to Gradfill prim type for rectangles. Change 101625 on 2003/05/19 by jacarey@fl jcarey desktop Miscellaneous Corrections to documents w.r.t. 2D Coherency Rectangle Updates. Change 101380 on 2003/05/16 by jacarey@fl jcarey desktop Clarifications to pre-write-timer and pre-write-limit usage. Change 100945 on 2003/05/14 by jacarey@fl jcarey desktop Clarifications to Set Constant and LCC packets w.r.t. write enables for each CONST ID type. Change 100549 on 2003/05/12 by jacarey@fl jcarey desktop Microcode Update for 2D surface coherency Change 100159 on 2003/05/09 by jacarey@fl jcarey desktop Document setting of bit 20 in 2D Booleans as Default\_Sel Change 99510 on 2003/05/07 by jacarey@fl jcarey desktop Updates to document for usage of "flush done" flag in the microcode. Change 99386 on 2003/05/06 by jacarey@fl jcarey desktop Update Change 99380 on 2003/05/06 by jacarey@fl\_jcarey\_desktop Fix for 2D Coherency (Flushing TC) Change 98285 on 2003/04/30 by fliljero@fl frank latest updates Change 96875 on 2003/04/22 by fliljero@fl\_frank changed data from one pass to the next to better insure proper validation Change 96851 on 2003/04/22 by jacarey@fl\_jcarey\_desktop



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