



ORIGINATE DATE

11 March, 2001

EDIT DATE

[date \@ "d MMMM,

DOCUMENT-REV. NUM.

GEN-CXXXXX-REVA

PAGE

1 of 34

Author: Steve Morein

Issue To:

Copy No:

R400 Top Level Specification

ver 0.2

Overview: This replaces the R400 architecture specification.

AUTOMATICALLY UPDATED FIELDS:

Document Location: Document1

Current Intranet Search Title: R400 Top Level Spec

APPROVALS

Name/Dept

Signature/Date

Remarks:

THIS DOCUMENT CONTAINS INFORMATION THAT COULD BE
SUBSTANTIALLY DETRIMENTAL TO THE INTEREST OF ATI TECHNOLOGIES
INC. THROUGH UNAUTHORIZED USE OR DISCLOSURE.

"Copyright 2000, ATI Technologies Inc. All rights reserved. The material in this document constitutes an unpublished work created in 2000. The use of this copyright notice is intended to provide notice that ATI owns a copyright in this unpublished work. The copyright notice is not an admission that publication has occurred. This work contains confidential, proprietary information and trade secrets of ATI. No part of this document may be used, reproduced, or transmitted in any form or by any means without the prior written permission of ATI Technologies Inc."



ORIGINATE DATE
11 March, 2001

EDIT DATE
[date \@ "d MMMM,
****]

DOCUMENT-REV. NUM.
R400 Top Level Spec

PAGE
2 of 34

Table Of Contents

1. FEATURES 7

1.1 AGP 8x 7

1.2 256 Bit Memory Interface 7

1.3 Unified Processing pipe 7

1.4 Front end scaling 7

1.5 Real-Time drawing command ability 7

1.6 3D Features 8

1.6.1 Noise Textures 8

1.6.2 Shadow buffers 8

1.6.3 Sort Independent Transparency 8

1.6.4 Anti-Aliasing 8

1.6.5 Texture compression 8

1.6.6 Z compression 8

1.6.7 Texture Filtering 8

1.6.8 Curved Surface Support 9

1.6.9 Displacement maps 9

1.7 High color depth 9

2. PERFORMANCE 9

3. SCHEDULE 9

4. PROCESS 9

5. GENERAL CHIP OPERATION 9

5.1 Unified Shader 9

5.2 3D Rendering 10

5.3 Real Time Rendering 12

5.4 State Management 13

5.5 Bad Data 13

5.6 Display operation 14

6. BLOCK DIAGRAM 15

7. BLOCKS 15

8. BLOCK DESCRIPTONS 16

8.1 HBIU – host bus interface unit 16

8.1.1 Description 16

8.1.2 Major interfaces 16

8.1.3 Block diagram 17

8.2 CP – control processor 17


8.2.1 Description 17

8.2.2 Major interfaces 18


8.2.3 Block diagram 18

8.3 RBBM – register interface manager 19


8.3.1 Description 19

	ORIGINATE DATE 11 March, 2001	EDIT DATE [date \@ "d MMMM, ****]	DOCUMENT-REV. NUM. GEN-CXXXXX-REVA	PAGE 3 of 34
--	----------------------------------	---	---------------------------------------	-----------------

8.3.2	Major interfaces.....	19
8.3.3	Block diagram.....	20
8.3.4	RBBM operation.....	20
8.4	CLK – clock generator.....	21
8.4.1	Description.....	21
8.4.2	Major interfaces.....	21
8.4.3	Block diagram.....	22
8.5	TC – test controller.....	22
8.5.1	Description.....	22
8.5.2	Major interfaces.....	22
8.5.3	Block diagram.....	22
8.6	VIP – Video input port.....	22
8.6.1	Description.....	22
8.6.2	Major interfaces.....	22
8.6.3	Block diagram.....	22
8.7	ROM – boot rom.....	22
8.7.1	Description.....	22
8.7.2	Major interfaces.....	22
8.7.3	Block diagram.....	22
8.8	I2C – I2C interface.....	22
8.8.1	Description.....	22
8.8.2	Major interfaces.....	22
8.8.3	Block diagram.....	23
8.9	DU – Display.....	23
8.9.1	Description.....	23
8.9.2	Major interfaces.....	23
8.9.3	Block diagram.....	24
8.10	MH – Memory Hub.....	24
8.10.1	Description.....	24
8.10.2	Major interfaces.....	24
8.10.3	Block diagram.....	24
8.11	HDP – Host Data Path.....	24
8.11.1	Description.....	25
8.11.2	Major interfaces.....	25
8.11.3	Block diagram.....	25
8.12	IDCT – Mpeg decoder.....	25
8.12.1	Description.....	25
8.12.2	Major interfaces.....	25
8.12.3	Block diagram.....	25

	ORIGINATE DATE 11 March, 2001	EDIT DATE [date \@ 'd MMM, ****]	DOCUMENT-REV. NUM. R400 Top Level Spec	PAGE 4 of 34
--	----------------------------------	--	---	-----------------

8.13	PA – Primitive Assembly	25
8.13.1	Description	25
8.13.2	Major interfaces	25
8.13.3	Block diagram	26
8.14	TD – Texture Decompression	26
8.14.1	Description	26
8.14.2	Major interfaces	27
8.14.3	Block diagram	27
8.15	RE – Raster Engine	27
8.15.1	Description	27
8.15.2	Major interfaces	28
8.15.3	Block diagram	29
8.16	SP – Shader Pipe	30
8.16.1	Description	30
8.16.2	Major interfaces	30
8.16.3	Block diagram	31
8.17	TP – Texture Pipe	32
8.17.1	Description	32
8.17.2	Major interfaces	32
8.17.3	Block diagram	32
8.18	RB – Render Backend	32
8.18.1	Description	32
8.18.2	Major interfaces	32
8.18.3	Block diagram	32
8.19	MC – Memory Controller	32
8.19.1	Description	32
8.19.2	Major interfaces	32
8.19.3	Block diagram	32
9.	COMMON FOUNDATIONS	32
9.1	Logic Design	32
9.1.1	Data formats	32
9.1.2	Register Bus	32
9.1.3	Block Communication protocol	32
9.2	Software	32

	ORIGINATE DATE 11 March, 2001	EDIT DATE [date \@ "d MMMM, ****]	DOCUMENT-REV. NUM. GEN-CXXXXX-REVA	PAGE 5 of 34
--	----------------------------------	---	---------------------------------------	-----------------

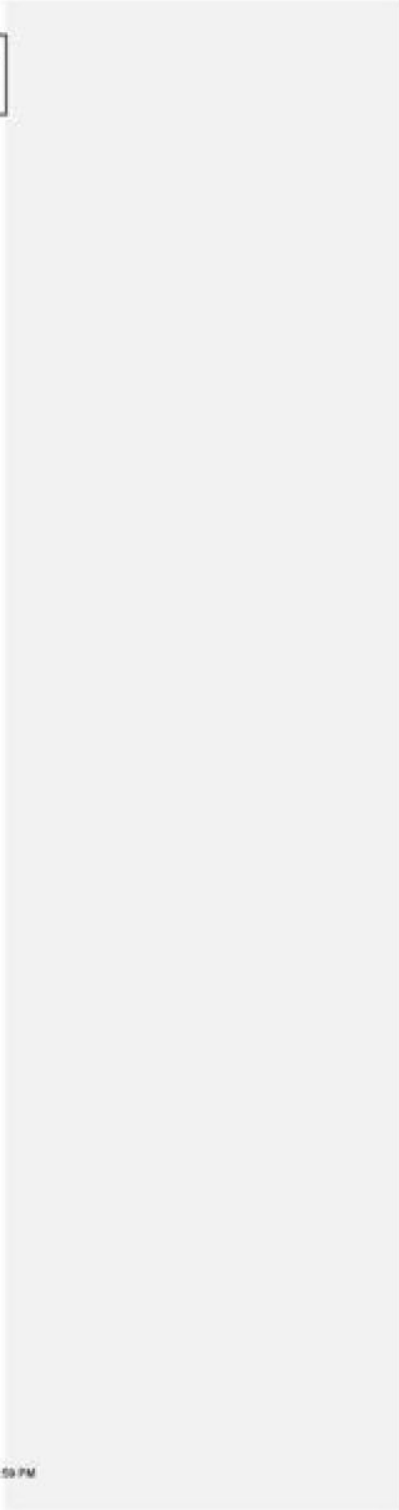
Revision Changes:

Rev 0.0 (Steve Morein)
Date: March 11, 2001
Initial revision.

Document recreated from earlier documents

Date March 14, 2001
April 21, 2001

Finally got back to editing it.
Upated texture path, hopefully this one works.



Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.