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GFXIP_9x SX

Micro-Architecture Specification

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Revision History

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2/12/2014	Dong Yiao	0.1	Initial Copy from gfx8
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Table of Contents

Preface

A micro-architecture (or block level) specification serves many purposes.

- The micro-architecture specification is used by design verification teams to build block and system level verification environments (test benches, test scenarios, test cases and testing methodologies/strategies). Although, a document is clearly not the ONLY vehicle used by design verification teams, it is a critical piece of the verification planning process in that it provides valuable data to support the test plan meetings between design and verification teams.
- The micro-architecture specification is also a useful tool for peer and block design reviews. Interfacing blocks require explicit details of control and handling of data being transferred, transformed between blocks. The specification is the obvious resource that peer teams go to for this type of information.
- This specification is also used by post-silicon verification teams and in the creation of documentation (such as programming guidelines, etc.) that must be prepared for external customers.
- This documentation is also useful when designs are transferred to other teams. For example, derivatives of a graphics core are used in many other products that include an integrated core, hand held devices, etc.

Each new major architecture should contain a micro-architecture specification for each block in the subsystem. In the case where a design is derived from a previous project, that previous project specification would be updated and checked into the new project revision control documentation area. All the delta features would be described in the feature section of the micro-architecture specification and the document in general should be updated to match the new project updated block design.

A template is provided as a means of describing the detail required by all teams that use the micro-architecture specification and to drive consistency between the specifications from one block to another. This template was created by the Design Verification Workgroup which is comprised of representatives across all AMDBusiness Units. This template has been and will be distributed to other Business Units and Design, Design Verification and Architecture teams for review and feedback. This template was created from a review of many of the existing micro-architecture specifications. Examples are pulled from these documents and presented here to illustrate the type of information that is required. To distinguish between the descriptions of content and examples, all examples appear in *italics*.

1 Introduction

The SX (shader export) block is responsible to receive and re-order color and position exports from the shader core and forward them to the correct client: PA for position, and the correct DB for color. The SX is also a conduit for parameter and GDS exports and in this role forwards the data unchanged to the PC (parameter cache) block.

The main input for the SX block is the shader output bus which is 2 busses each 16x32 bits wide. The SX output busses are:

1) 128 bits wide bus to the PA (primitive assembler) block supporting 1 position per clock
2) 256 bits to each DB (supporting up to 4 DB per SX) thus supporting 4 "compressed" pixels per clock (64 bpp) or 2 uncompressed pixels per clock (128 bpp).
3) 16x32 bit bus to PC/GDS.

1.1 Definitions / glossary of terms

Thread – *one instance of a shader program being executed on a vector of pixels, vertices, or primitives. Each thread has its own state which is unique from any other thread.*

Clause – *a group of instructions all of the same type (all ALU, all texture-fetch, etc.) executed as a group; part of a thread.*

Wave – *one instruction operates on a wave of pixels/vertices/primitives over 4 clock cycles. This is the basic unit of work. The size of a vector depends on the system configuration, but is always 4 clock cycles.*

SIMD – *Single Instruction, Multiple Data. Here, a SIMD refers to one slice of the SP machine which all receives the same instruction and operates on a vector of data. Most implementations will have multiple SIMDs. Each SIMD receives a separate instruction from the SQ.*

1.2 Top Level Diagram

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