

ATI Corporate Presentation

AMD1044 0051184

Block Logic Design and Timing

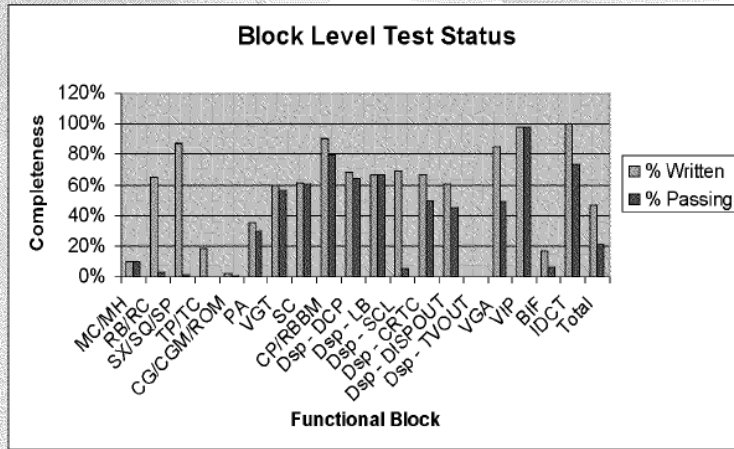
Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (ns)
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14.1nS)	
MC/MH	95% / 95%	9/23 - 9/16	N/A	10%	MC: 4.46; MH: 4.72	MCLK: 2.39	55 / 643
RB/RC	85% / 95%	9/30	95%	54%	RB: 8.2; RC: 2.5		16689 / 0
SXSQ			99%	88%	SX: 2.74; SQ: 2.5		0 / 0
SP	100%	9/16	97%		SP: 2.5		0
TP/TC	97% / 95%	9/16	92%	18%	TP: 2.55; TC: 2.5		0 / 0
CG/CGM/ROM	100%	9/16	N/A	2%	CG: 2.5; CGM: 2.5; DBG: 2.5		0
PA	100%	9/16	100%	35%	PA: 2.69		110
VGT	100%	9/16	100%	59%	VGT: 2.75		33
SC	90%	9/16	95%	61%	SC: 2.73		140
RBBM	95%	9/16	N/A		RBBM: 2.95		95
CP	95%	9/16	90%	90%	CP: 2.85		439
Display - DCP	100%	9/16	90%	65%	Display: 11	PIXCLK: 2.5	8207
Display - LB	100%	9/16	100%	65%			
Display - SCL	70%	9/20	85%	65%			
Display - CRTIC	100%	9/16	80%	65%			
Display - DISFOUT	95%	9/16	65%	65%			
Display - TVOUT	100%	9/16	30%	0%			
VGA	100%	9/16	99%	85%			
VIP	100%	9/16	100%	100%			
BIF	100%	9/16	90%	15%	BIF: 4.47	BCLK: 14.1	228
IDCT	100%	9/16	97%	97%	IDCT: 4.23		2898

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Block Level Test



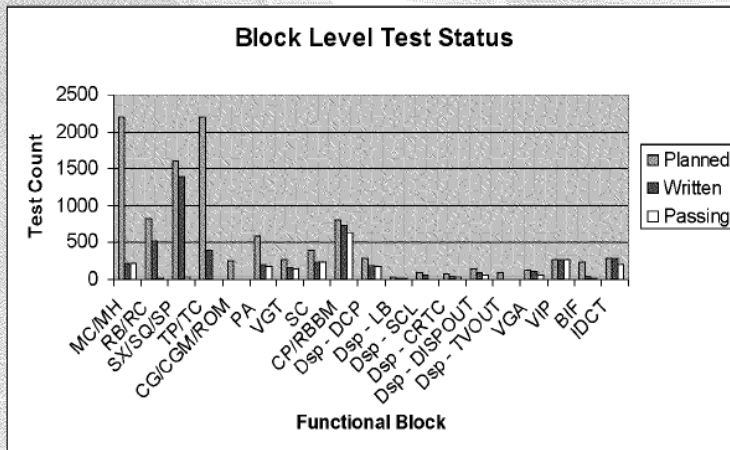
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Block Level Test



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Synthesis & Physical Design

- **Hardware Emulation**
 - Initial IKOS compilation has begun to attempt R400 fit into a V15M
- **Synthesis continuing ...**
 - Blocks focusing on feature complete, not timing
 - Some blocks have made significant progress
 - Working top level interconnect issues
 - Working synthesis interface into physical design
- **Physical design**
 - Working group inter-relationships SiV<>Marlboro
 - Meeting often to synchronize teams
 - Physical Design web page under construction
- **Floorplan**
 - Initial padout done, needs to be reviewed
 - Initial netlist successfully read into SPC
 - Generated floorplan from SPC (no I/O constraint)

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