ATI TECHNOLOGIES INC.

R400 I/O

February 12, 2003

May 2, 2017

R400 I/O Activities

- Pad ring review with Greg S. on 2/14 in SiV
- IO/NPL review on 2/25 & 2/26 in SiV with team from Marlborough
- Viper program

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May 2, 2017

Memory I/O & Clock

- First pass design of the memory I/O is complete.
- First pass design of the memory clock is complete.
- Layout schedule
  - Memory I/O – 2/13
  - Memory clock – 2/18
  - Memory calibration – 2/20
  - Memory strobe – 2/21
- Library files
  - Verilog – complete and checked into the tree
  - LEF of Memory I/O, clock, calibration, and strobe -- 2/18
  - TLF/LIB/DB of memory I/O, clock, calibration, and strobe – 2/21

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May 2, 2017

Memory Near Pad Logic

- RTL-to-schematic implementation
  - ADDR, DATA, DQSM, DQSS and HCLK are done first pass
  - All five pass LEC
  - Started timing simulations (HSPICE)
- Found bug in IO/NPL which required the NPL to be updated
  - Layout to start on 2/15 and complete on 3/15
- Library files (LEF, TLF, LIB, and DB) will be deliver on 3/1
- On going memory system timing – complete on 3/15

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May 2, 2017

Delay Line and misc layout

- Design is done
- Layout is complete
- Miscellaneous layout
  - ChrisV/KarenW started layout on the miscellaneous cells
  - PVREF
  - Corners
  - Spacers
  - Breaks
  - Complete on 3/1

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May 2, 2017

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