

ATI Corporate Presentation

AMD1044 0051103

R400 Review Action Summary

- Program – Next tentative review date is on March 12th

- Last Month

- R400 Software

- Plan support for packet dump capture – Complete
 - Quality goal needed for conformance of compression/coherency code - Open
 - IKOS Meeting with Ron White for SW – Complete

- R400 Hardware

- SDR 3.3V support on DVO port (requirements) – Closing, finalizing
 - RB break-up for Netlist delivery (NL4.0 vs NL5.0) – Planned for NL5
 - Code coverage analysis on all blocks – In process
 - DC dependency on MH bugs - Ken Correll focused on support
 - DC instance count – Instance count reduced, discussing with Mark Lee
 - SQ test coverage review – Complete

- Performance

- PA performance registers – Complete
 - GC testbench for better performance data – Not working yet, still debugging
 - Contractors to run/analyze tests – Ko Yu, Allen G. will pursue as necessary

- Chip Integration

- Power – Greg S. analyzing power
 - Operations – Update meeting held with Anita Siu, working fuse process
 - Pad – Review scheduled for end of February

- Physical Design

- Feedback from Netlist 3 needed – Mark Lee began, PD/LD meetings in process

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R400 Review Action Summary

- **This review**

- **R400 Software**

- Quality goal needed for conformance of compression/coherency code - **Open**
 - Is HW testing using Set_state or Type0 packets in tests – Mark Fowler
 - SW ran into problem recently

- **R400 Hardware**

- RB split for netlist 5 – Frank Hering
 - AB file dumps – Mike Mantor / Larry Seiler
 - Remove degamma from DXTC as a feature ?
 - Code coverage analysis on blocks – Mark Fowler
 - TC performance path – Steve Morein / Clay Taylor / Andy Gruber
 - DC instance count high – Lili S./Frank H. to close with Mark Lee
 - Assist with debug of 2D tests – Mark Earl / John Carey / Harry Wise
 - SQ/SX has risk, continue to monitor – Peter Pellerite
 - Review CP code
 - Rewrite of 2D Drivers for derivative area savings – Joe Cox
 - CP code removed, need to review – Andy Gruber / John Carey

- **Performance**

- Orlando to work more with playback – Chris Gray / Allen G.
 - GC testbench for better performance data – **Open**

- **Chip Integration**

- Thermal solution need overall owner
 - Boards group involvement priority (or window is lost)
 - Operations – give memory/fuse package to Anita for ASE
 - Pad – clock distribution in pads needs to be finalized with SIV

- **Physical Design**

- BIF description for R400 PD – Lili Sinclair
 - PD to LD communication mostly working (may need to expand/change list)
 - Clock insertion methodology – meeting 2/14

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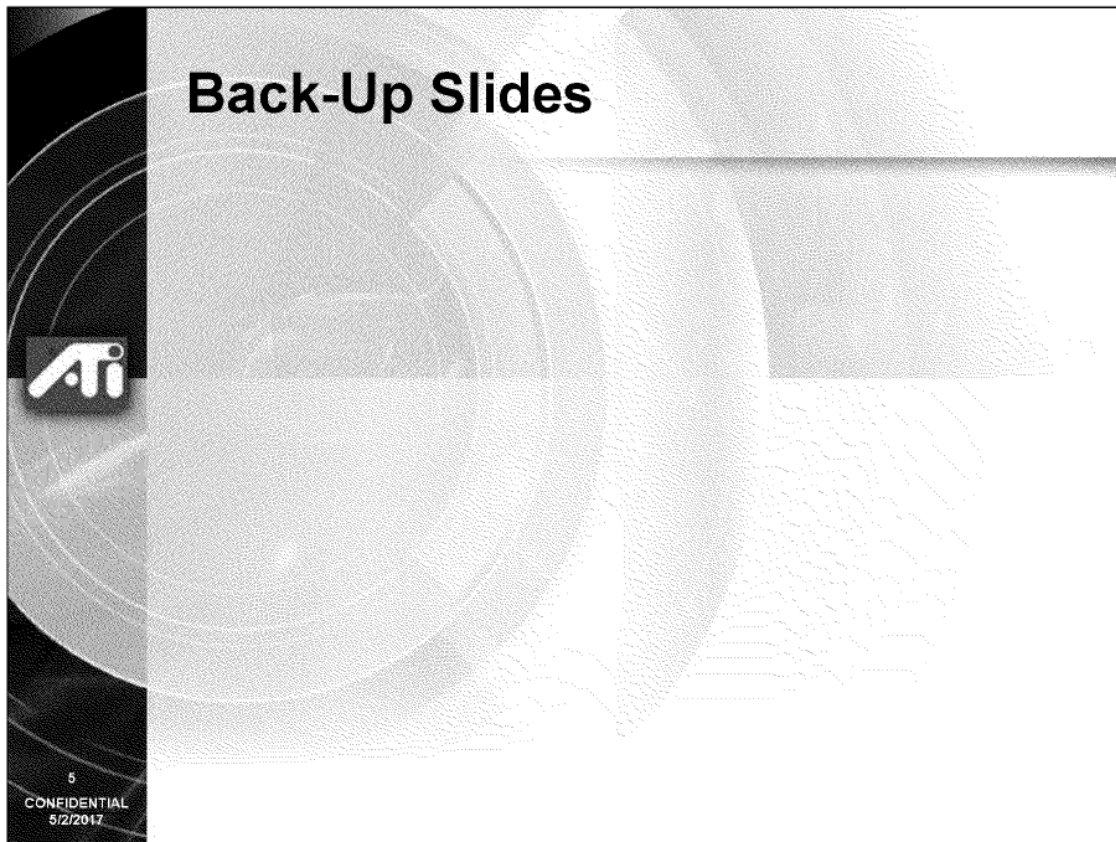
High Level Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-02	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
Netlist 4.0	02-14-03	02-07-03	02-12-03
Netlist 5.0	03-03-03	03-03-03	03-03-03
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	05-01-03
A11 Base Layers Tapeout	01-10-03	03-28-03	06-26-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	07-10-03
First Samples for Engineering		06-25-03	09-12-03
R400 First Customer Samples		07-16-03	10-03-03
A12 Tapeout		07-31-03	10-17-03
A12 Samples for Engineering		09-04-03	11-28-03
R400 Customer Samples		09-11-03	12-05-03
Product Delivery		10-04-03	12-29-03

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