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Shader Processor

Rev 1.2

Overview: This document describes the overall architecture of the Shaders, interfaces, partitioning into functional blocks as well as the timing of the shader pipeline. It's intended for use by hardware designers.

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Remarks

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Revision Changes:

Rev 0.0 (Steve Morein)
Date: Alpril, 2001
Initial revision.
Document started

Rev 0.1 (Andi Skende)
Date: May 09, 2001
Updated, added the instruction formant, initial block diagrams and preliminary interface description

Rev 0.2 (Andi Skende)
Date: May 21, 2001
A more detailed description of the SP<->TEX, RE/Sequencer <->SP interfaces.

Rev 0.3 (Andi Skende)
Date: June 19, 2001
Added the paragraph related to shader functional limitations that the compiler needs to be aware of.
A new updated and compressed version of ALU instruction format.

Rev 0.4 (Andi Skende)
Date: June 20, 2001
Updated the Introduction of this document. A new Pipeline Timing Diagram was inserted.

Rev 0.5 (Andi Skende)
Date: July 31, 2001
Merged in the Shader Hardware Spec. A more detailed description of the interfaces with the other blocks was added. Updated some of the diagrams to a more correct representation of the datapaths.

Rev 0.6 (Andi Skende)
Date: August 17,2001
A more detailed description/definition of Shader interfaces with the other blocks.
A more detailed description of the instruction supported by Shader Processor and it's relation to instruction set exposed at API level.

Rev 0.7 (Andi Skende)
Date: November 8, 2001
Updated the Alu instruction word definition and the list of the alu instruction opcodes supported by the shader pipe ALU unit.

Rev 0.8 (Andi Skende)
Date: November 27, 2001
Updated the definition of the External Interfaces

Rev 0.9 (Andi Skende)
Date: December 10, 2001
Updated the definition and naming of some of the external interfaces, rearranged the ALU instruction word definition such that the fields are dword aligned.
The instruction opcode definition was updated and expanded.

Rev 1.0 (Andi Skende)
Date: January 15, 2002
Updated most of the diagrams. Updated the External Interface definitions. Added a description of the Parameter Interpolation Units. Added a diagram desciption of the GPR write data paths.

Rev 1.1 (Andi Skende)
Date: January 21, 2002
Updated some of the external interface definitions.
Specified the expected behavior of hardware implementation of some shader opcode with some corner case values as input arguments. The MS Reference Rasterizer shader was used as guideline.

Rev 1.2 (Andi Skende)
Date: January 22, 2002
Updated some of the external interface definitions.

Introduction

Shader Pipe (SP) serves as the central Arithmetic and Logic Unit (ALU) for the R400 Graphics Processor. There are four identical Shader pipelines in the R400 architecture. Differently from previous ATI architectures, the R400 Shader Pipe truly represents an Unified Shader Architecture. In R400, both vertex and pixel shading operations are implemented through the shader units. The R400 Shader Pipe represents an SIMD architecture. All the shader units of each and every pipe execute the same ALU instruction on different sets of vertex parameters/pixel values. The building blocks of the R400 shader units execute operations on single precision IEEE floating-point values.

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