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Transcript of Hanspeter Pfister, Ph.D.

Date: February 16, 2024

Case: Realtek Semiconductor Corp. -v- ATI Technologies ULC (PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

Transcript of Hanspeter Pfister, Ph.D.
Conducted on February 16, 2024

1 (1 to 4)

1	3
1 UNITED STATES PATENT AND TRADEMARK OFFICE	1 C O N T E N T S
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD	2
3 -----x	3 EXAMINATION OF HANSPETER PFISTER, Ph.D. PAGE
4 REALTEK SEMICONDUCTOR CORP.,	4 By Mr. Dokhanchy 5
5 Petitioner,	5 By Mr. Johnson 132
6 v.	6
7 ATI TECHNOLOGIES ULC,	7
8 Patent Owner.	8 Exhibits - none marked in the deposition
9 -----x	9
10 Case No. IPR2023-00922	10
11	11
12 Videotaped deposition of Hanspeter Pfister, Ph.D.	12
13 Boston, Massachusetts	13
14 February 16, 2024	14
15 9:01 a.m.	15
16	16
17	17
18	18
19	19
20	20
21 Job No.: 524719	21
22 Pages: 1 - 135	22
23 Reported By: Alan H. Brock, RDR, CRR	23
24	24
25	25
2	4
1 A P P E A R A N C E S	1 February 16, 2024 9:01 a.m.
2 ON BEHALF OF PETITIONER:	2 P R O C E E D I N G S
3 BAKER BOTTS L.L.P.	3 THE VIDEOGRAPHER: Here begins Media No. 1
4 JEFFREY JOHNSON, ESQ.	4 in the videotaped deposition of Dr. Hanspeter Pfister,
5 910 Louisiana Street	5 in the matter of Realtek Semiconductor Corp. v. ATI
6 Houston, Texas 77002	6 Technologies ULC (PTAB), in the United States Patent
7 713.229.1234	7 and Trademark Office, Case No. IPR2023-00922. Today's
8 jeffrey.johnson@bakerbotts.com	8 date is February 16th, 2024. The time on the video
9	9 monitor is 9:02 a.m.
10 ON BEHALF OF PATENT OWNER:	10 The videographer today is Michael Safee,
11 MINTZ, LEVIN, COHN, FERRIS, GLOVSKY &	11 representing Planet Depos. This video deposition is
12 POPEO, P.C.	12 taking place at Orrick, Herrington & Sutcliffe LLP,
13 REZA DOKHANCHY, ESQ.	13 222 Berkeley Street, Suite 2000, Boston, Massachusetts
14 3580 Carmel Mountain Road, No. 300	14 02116.
15 San Diego, California 92130	15 Would counsel please voice-identify
16 858.314.1500	16 themselves and state whom they represent.
17 rdokhanchy@mintz.com	17 MR. DOKHANCHY: Reza Dokhanchy, of Mintz
18	18 Levin, on behalf of AMD/ATI.
19 ALSO PRESENT:	19 MR. JOHNSON: Jeffrey Johnson, Baker
20 Michael Safee, Videographer	20 Botts, on behalf of the Realtek defendants.
21	21 THE VIDEOGRAPHER: The court reporter
22	22 today is --
23	23 MR. JOHNSON: I'm sorry, Realtek
24	24 petitioners.
25	25 THE VIDEOGRAPHER: The court reporter

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<p>5</p> <p>1 today is Alan Brock, representing Planet Depos. The 2 witness will now be sworn. 3 HANSPETER PFISTER, PH.D., 4 being first duly sworn or affirmed to testify to the 5 truth, the whole truth, and nothing but the truth, was 6 examined and testified as follows: 7 EXAMINATION 8 BY MR. DOKHANCHY: 9 Q. Good morning, Dr. Pfister. 10 A. Good morning. 11 Q. I'm going to hand you copies of Exhibit 1001, 12 which is the '454 patent, and 1003. And Exhibit 1003 13 is your declaration in this matter; is that correct? 14 A. Yes, that's correct. 15 Q. If you could go to Paragraph 169 of your 16 report, please: It begins on Page 81. This is where 17 you begin your analysis in Ground 2 of the '454 18 patent, claim 2; is that right? 19 A. This is with regards to particular prior art, 20 and it seems to be the combination of Amantides and 21 Kohn. 22 Q. Okay. And in this section that starts at 23 Paragraph 167, you're addressing the claimed unified 24 shader of the '454 patent; right? 25 A. That's correct, with regards to Amantides and</p>	<p>7</p> <p>1 And so the i860 processor is basically the processor 2 in the Amantides system. So it does more, you know, 3 than just G/R processing. 4 Q. The thing you're calling the G/R unit, that's 5 a processor; right? 6 MR. JOHNSON: Objection, form. 7 A. Well, I call it a unit because I think that's 8 the term that Amantides uses. But if you could hand 9 me the Amantides reference, I can check that. 10 Q. Sure. I'm going to hand you Exhibit 1007, 11 which is the Amantides reference. 12 And I can point you to a particular place 13 if that would be helpful. 14 A. I found it. So in Amantides, Page 7 -- 15 sorry, Page -- well, which page should I use? I guess 16 I use the Bates Page 7? 17 Q. We can use 157. That's fine. 18 A. Page 157, on the bottom of the left column, 19 he describes these G/R units as the processors, or the 20 processor. So he uses the word "processor." You were 21 correct. 22 Q. So looking at Figure 3, there are multiple 23 G/R units. Those are, as we just saw, processors. 24 Each G/R unit is a processor; right? 25 A. That is correct.</p>
<p>6</p> <p>1 Kohn. 2 Q. Okay. And if you continue onto the next 3 page, in Paragraph 169, your allegation is that 4 Amantides termed the unified shader unit the G/R unit. 5 Do you see that? 6 A. Yes, correct. 7 Q. And so your allegation is that the Amantides 8 reference discloses a unified shader in the form of 9 the G/R unit; right? 10 A. Yes, the G/R unit or units, plural. 11 Q. You didn't say units plural in your report. 12 A. That's correct. I would say it's either the 13 singular or it's the collection of. 14 Q. In your report you said singular; correct? 15 A. That is correct. I used the singular in the 16 report, but I may have, you know, missed that 17 particular point. But I think either one is fine. 18 Q. And your -- withdrawn. The Amantides 19 reference states that the G/R unit is implemented as 20 an Intel i860 processor; right? 21 A. That is correct. 22 Q. So the G/R -- 23 A. So just to be clear: You know, I'm referring 24 now to Figure 4 on Page 83 of my declaration, and 25 Figure 4 shows the actual system diagram of Amantides.</p>	<p>8</p> <p>1 Q. And we see on the next page, 158, around the 2 middle of the page it says, "After exploring several 3 DSP microprocessors, we decided on the Intel i860"; 4 right? 5 A. Yes, that is correct. 6 Q. And so the authors are stating that the Intel 7 i860 is the processor selected as the G/R processor; 8 right? 9 A. Let me quickly check. I want to make sure 10 that we are still using the -- or Amantides is still 11 using the term "processor" in the same way. If you 12 don't mind, I'll quickly read that paragraph above. 13 Q. Yes. 14 A. I think it's a little ambiguous, just in the 15 sense that Amantides doesn't actually say that the 16 Intel i860 is just the G/R processor. The reason I 17 mention this is because, as I said earlier, in the 18 system diagram in Figure 4 the i860 appears as, you 19 know, the only processor within the graphics 20 processing unit, except for the host. So it 21 presumably will also have to do some other things. 22 And that's the only reason I bring this up. 23 Q. Okay. So looking at Figure 4, are you saying 24 that the G/R unit is coextensive with the i860, larger 25 than the i860, or smaller than the i860, or something</p>

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9	<p>1 else?</p> <p>2 MR. JOHNSON: Objection, form.</p> <p>3 A. I don't know what you mean by "larger than,"</p> <p>4 "smaller than," whatever terms you used.</p> <p>5 Q. Sure. So looking at Figure 4, what</p> <p>6 components would you consider parts of the G/R unit?</p> <p>7 A. Well, the G/R unit is clearly the i860,</p> <p>8 within the i860, because that's the, you know,</p> <p>9 one-to-one mapping to the previous diagram.</p> <p>10 Q. Okay. So that's what I meant by "smaller</p> <p>11 than": within.</p> <p>12 What else, if anything, is in the i860</p> <p>13 besides the G/R processor?</p> <p>14 A. Well, I wouldn't say, you know, "is within."</p> <p>15 I'm not sure what you mean by that term.</p> <p>16 Q. Well, that's the word you used. So I'm using</p> <p>17 your word.</p> <p>18 A. Oh, sorry. I said the G/R unit, you know, is</p> <p>19 basically within the i860. I mean, the i860 is -- is</p> <p>20 the G/R unit. It may also function as, you know, sort</p> <p>21 of--</p> <p>22 You know, it's a subtle distinction,</p> <p>23 because the G/R unit actually can also do some other</p> <p>24 processing. I was talking myself a little bit into a</p> <p>25 corner here, because I'm thinking, besides the</p>	11	<p>1 Q. Sure. I'm just looking at the claim</p> <p>2 language. We can talk about your mapping in a second.</p> <p>3 But my question simply is, "claim 2 requires a</p> <p>4 sequencer that maintains instructions; correct?"</p> <p>5 A. Yes.</p> <p>6 Q. And Paragraph 178 is where you discuss your</p> <p>7 allegations of why Amantides and Kohn disclose the</p> <p>8 claimed sequencer; is that correct?</p> <p>9 MR. JOHNSON: Objection, form.</p> <p>10 Q. I can just direct you to the first sentence.</p> <p>11 A. Yeah, I see the paragraph. What I'm actually</p> <p>12 saying is that both Amantides and Kohn disclose the</p> <p>13 claimed sequencer.</p> <p>14 Q. Okay. And in terms of what you identify, you</p> <p>15 say at the bottom -- the end of Paragraph 178, "The</p> <p>16 on-chip cache together with the memory unit comprise</p> <p>17 the claimed sequencer and sequencer circuitry of the</p> <p>18 '454 patent." Correct?</p> <p>19 A. So I think in order to understand this, we</p> <p>20 need to look at Kohn, because Kohn actually is</p> <p>21 referenced here, if I'm not mistaken, Exhibit 1008.</p> <p>22 Q. Well, let's just start with what you wrote.</p> <p>23 You wrote, "The on-chip cache together with the memory</p> <p>24 unit comprise the claimed sequencer and sequencer</p> <p>25 circuitry of the '454 patent." Did I read that</p>
10	<p>1 geometry and the rendering processing, there is some</p> <p>2 other processing happening. But that could be all</p> <p>3 part -- I mean, that is actually in Amantides all part</p> <p>4 of the G/R unit.</p> <p>5 So, you know, let's step back. I'm going</p> <p>6 to change -- basically, in my declaration, as I said,</p> <p>7 I think, the G/R unit is the i860.</p> <p>8 Actually, if you don't mind, I'll quickly</p> <p>9 check my declaration. I want to make sure I have that</p> <p>10 statement in here before I say I say that.</p> <p>11 Yeah, actually, I do say that.</p> <p>12 Q. Okay.</p> <p>13 A. So I say in Paragraph 172 on Page 892, "The</p> <p>14 claimed processor unit can be interpreted as each</p> <p>15 G/R," and then in parentheses, you know, the i860</p> <p>16 processor.</p> <p>17 Q. And let's talk about claim 2 of the '454</p> <p>18 patent. If you can open that up, please, or you may</p> <p>19 just remember it. But there is a sequencer claimed in</p> <p>20 the i860 -- excuse me. Withdrawn. Claim 2 requires a</p> <p>21 sequencer that maintains instructions. Do you see</p> <p>22 that?</p> <p>23 A. So claim 2 has several subclaims. I think</p> <p>24 we -- in my declaration I labeled them with A, B, C.</p> <p>25 So I think you're referring to the third or the C?</p>	12	<p>1 correctly?</p> <p>2 A. You read that correctly.</p> <p>3 Q. So let's talk about what you cite here. So</p> <p>4 you cite -- in this paragraph first you say,</p> <p>5 "Amantides at 157 to 158." Do you see that?</p> <p>6 A. Sorry, say that again. I'm sorry.</p> <p>7 Q. I'm looking at the first citation in</p> <p>8 Paragraph 178.</p> <p>9 A. Oh, yeah.</p> <p>10 Q. That's Amantides at Page 157 to 158; correct?</p> <p>11 A. That's the citation. That's not all we just</p> <p>12 talked about, just to be clear.</p> <p>13 Q. That's fine. I just want to -- we're going</p> <p>14 to go now look at that citation.</p> <p>15 A. Okay, yeah.</p> <p>16 Q. And then you have a quote saying, "As well,</p> <p>17 program space needs to be larger," dot dot dot. Let's</p> <p>18 go to that quote. Okay?</p> <p>19 A. Okay.</p> <p>20 Q. That's on Page 158 of Amantides. If you</p> <p>21 could go there, please. So this is one of your</p> <p>22 citations for why Amantides discloses the sequencer,</p> <p>23 which, as we just talked about, needs to maintain</p> <p>24 instructions. Correct?</p> <p>25 A. The sequencer needs to maintain instructions,</p>

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<p style="text-align: right;">13</p> <p>1 correct.</p> <p>2 Q. So where in this citation that you quoted,</p> <p>3 Page 158 -- where do you see a disclosure of storing</p> <p>4 instructions?</p> <p>5 A. I'm actually trying to find it on 157-158.</p> <p>6 Q. So the quote that you cited is about Line 8</p> <p>7 on 158. It starts "As well."</p> <p>8 A. Oh, yeah. Yeah, I think the relevant piece</p> <p>9 of that quote, or of that, you know, section in</p> <p>10 Amantides is that sentence at the end in my</p> <p>11 declaration, Paragraph 178, where I'm quoting. And in</p> <p>12 the sentence the quote says, "To get back to speed, we</p> <p>13 wanted the processor to have an on-chip cache." So</p> <p>14 that's what I'm referring to as the on-chip cache in</p> <p>15 Amantides.</p> <p>16 Q. Where does that say that what you're calling</p> <p>17 the sequencer stores instructions?</p> <p>18 A. If we look at Amantides, Page 158 -- also</p> <p>19 where my quote starts in my declaration: "As well,</p> <p>20 program space needs to be larger," et cetera.</p> <p>21 "Program space would be understood by a POSITA to mean</p> <p>22 memory for programs," and it's very clear that that</p> <p>23 includes instructions. So it would be clear to a</p> <p>24 POSITA that that program space which is stored in the</p> <p>25 on-chip cache is part of that cache, meaning the</p>	<p style="text-align: right;">15</p> <p>1 in the DRAM.</p> <p>2 Q. Does Amantides say one way or another whether</p> <p>3 the DRAM stores instructions?</p> <p>4 MR. JOHNSON: Objection, form.</p> <p>5 A. So, you know, you're directing me to this one</p> <p>6 paragraph in Amantides. And so to answer your</p> <p>7 question truthfully, I would have to look at, I think,</p> <p>8 the rest of the reference. You know, I don't recall.</p> <p>9 And I'd be happy to look through it if you like.</p> <p>10 Q. Yeah, why don't do you that. It's only</p> <p>11 discussed, I think, on that page, but you can feel</p> <p>12 free to correct me and look for the word "DRAM"</p> <p>13 throughout or whatever you want to look for.</p> <p>14 But my question is: Does Amantides say</p> <p>15 whether or not the DRAM stores instructions?</p> <p>16 MR. JOHNSON: Objection, form.</p> <p>17 A. So I think actually even within that</p> <p>18 paragraph that you directed me to, you know, if you</p> <p>19 read this carefully, Amantides points out that,</p> <p>20 "Program space needs to be larger as each processor</p> <p>21 does more work." Right? So he's pointing out the</p> <p>22 fact that, as we're combining the G/R into this one</p> <p>23 processor, it needs to do more work, and that means it</p> <p>24 also needs more program space. And then he talks</p> <p>25 about using DRAM.</p>
<p style="text-align: right;">14</p> <p>1 instructions are stored in that cache.</p> <p>2 Q. Okay. And it says originally, before</p> <p>3 considering the on-chip cache, there was a possibility</p> <p>4 of storing program space in SRAM or DRAM; is that</p> <p>5 right?</p> <p>6 A. Well, what Amantides actually points out is</p> <p>7 that he or they wanted to eliminate the need for SRAM</p> <p>8 and DRAM. So I guess you could say an alternative</p> <p>9 design would have been to store the instructions in</p> <p>10 SRAM and DRAM, but that's not --</p> <p>11 I'm sorry, in SRAM, sorry. I misquoted, I</p> <p>12 think. What he actually says or they say is that "we</p> <p>13 wanted to eliminate the need for SRAM, and use DRAM</p> <p>14 instead."</p> <p>15 And now I lost your question. I'm sorry.</p> <p>16 Q. Well, my question is: Does the DRAM in</p> <p>17 Amantides store instructions?</p> <p>18 A. It may also store instructions, simply</p> <p>19 because, you know, a cache is, if you will, kind of a</p> <p>20 temporary storage and typically limited in space. So,</p> <p>21 you know, it may not hold the whole program. And so</p> <p>22 it is possible.</p> <p>23 But Amantides does actually not disclose</p> <p>24 that. I think for a POSITA it would seem reasonable</p> <p>25 to say that it's possible that there are instructions</p>	<p style="text-align: right;">16</p> <p>1 So I think it's clear from just inferring</p> <p>2 this that he assumes that the program space will also</p> <p>3 be stored in the DRAM, since he points out that it can</p> <p>4 be large -- right? And a cache, as I mentioned</p> <p>5 before, is typically a temporary storage and is</p> <p>6 typically on or, you know -- I would say, yeah,</p> <p>7 typically not large enough to hold all of the program</p> <p>8 space.</p> <p>9 So I think it's reasonable to say that,</p> <p>10 yes, Amantides does say that the program space is</p> <p>11 stored in the DRAM, because that's large.</p> <p>12 Q. And you see in claim 2 there's a separate</p> <p>13 requirement from the sequencer, and that is a general</p> <p>14 purpose register block for maintaining data? Do you</p> <p>15 see that?</p> <p>16 A. Yes, the claim says that a sequencer is</p> <p>17 coupled to a general purpose register block, and then</p> <p>18 further down that, you know, that depicts a</p> <p>19 calculation of operations on the selected data</p> <p>20 maintained in the general purpose register block, is</p> <p>21 part of that, yes.</p> <p>22 Q. And could you actually look at the previous</p> <p>23 page at the bottom. It says "a unified shader,</p> <p>24 comprising a general purpose register block for</p> <p>25 maintaining data"; right?</p>

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