



(12) **United States Patent**
Swain et al.

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- (54) **READ LEVELING OF MEMORY UNITS DESIGNED TO RECEIVE ACCESS REQUESTS IN A SEQUENTIAL CHAINED TOPOLOGY**

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- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 110 days.
- (21) Appl. No.: **12/168,948**
- (22) Filed: **Jul. 8, 2008**

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- (51) **Int. Cl.**
GIIC 29/00 (2006.01)
GIIC 7/06 (2006.01)
- (52) **U.S. Cl.** **365/201**; 365/189.07; 714/718;
714/719
- (58) **Field of Classification Search** 365/201
See application file for complete search history.

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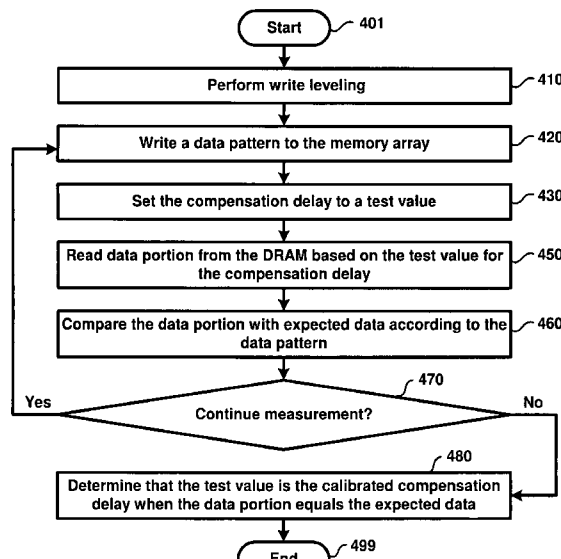
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(57) **ABSTRACT**
Read leveling of memory units designed to receive access requests in a sequential chained topology writing a data pattern to the memory array. In an embodiment, a memory controller first writes a desired pattern into the memory array of a memory unit and then iteratively determines the accurate calibrated delay by setting a compensation delay to a test value, reading a data portion from the memory array based on the test value for the compensation delay, comparing the data portion with an expected data, determining that the test value is a calibrated compensation delay for the memory unit if the data portion equals the expected value.

26 Claims, 5 Drawing Sheets



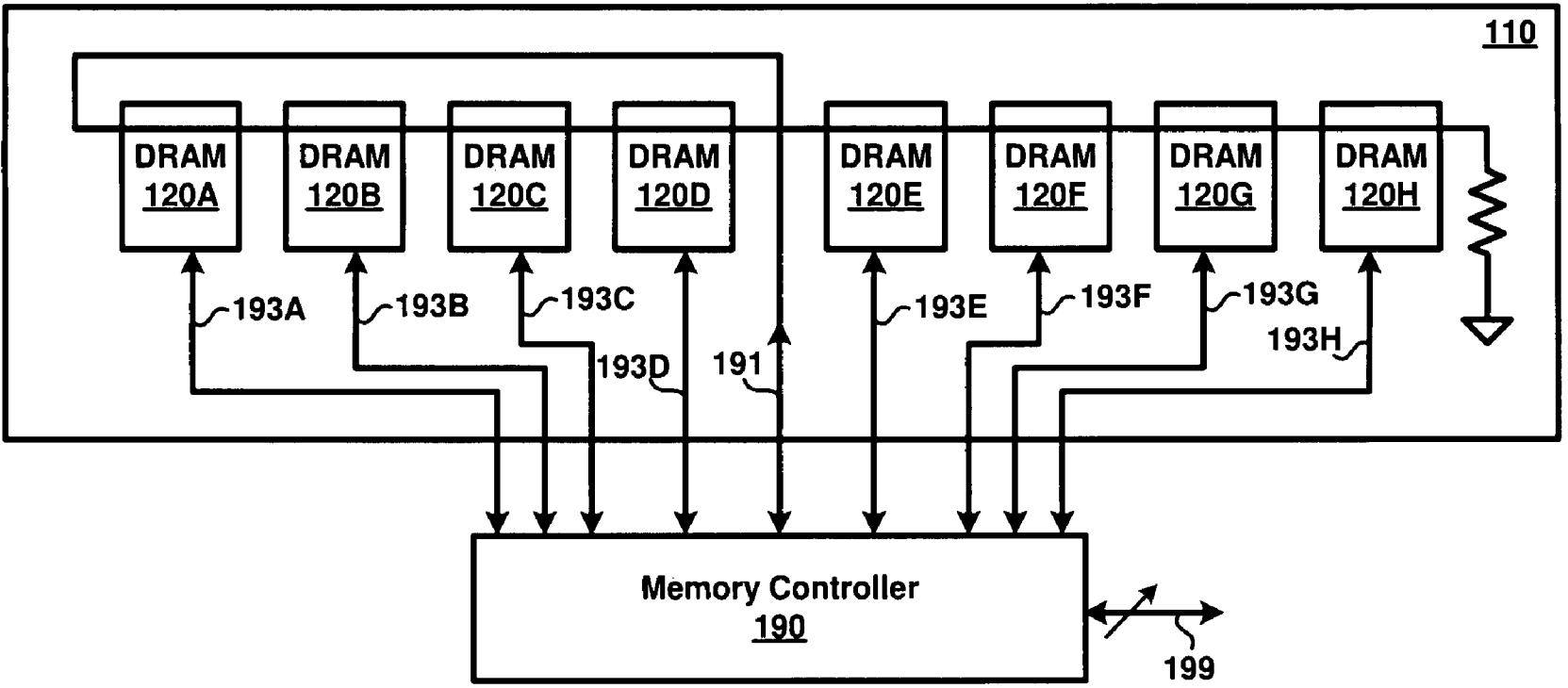
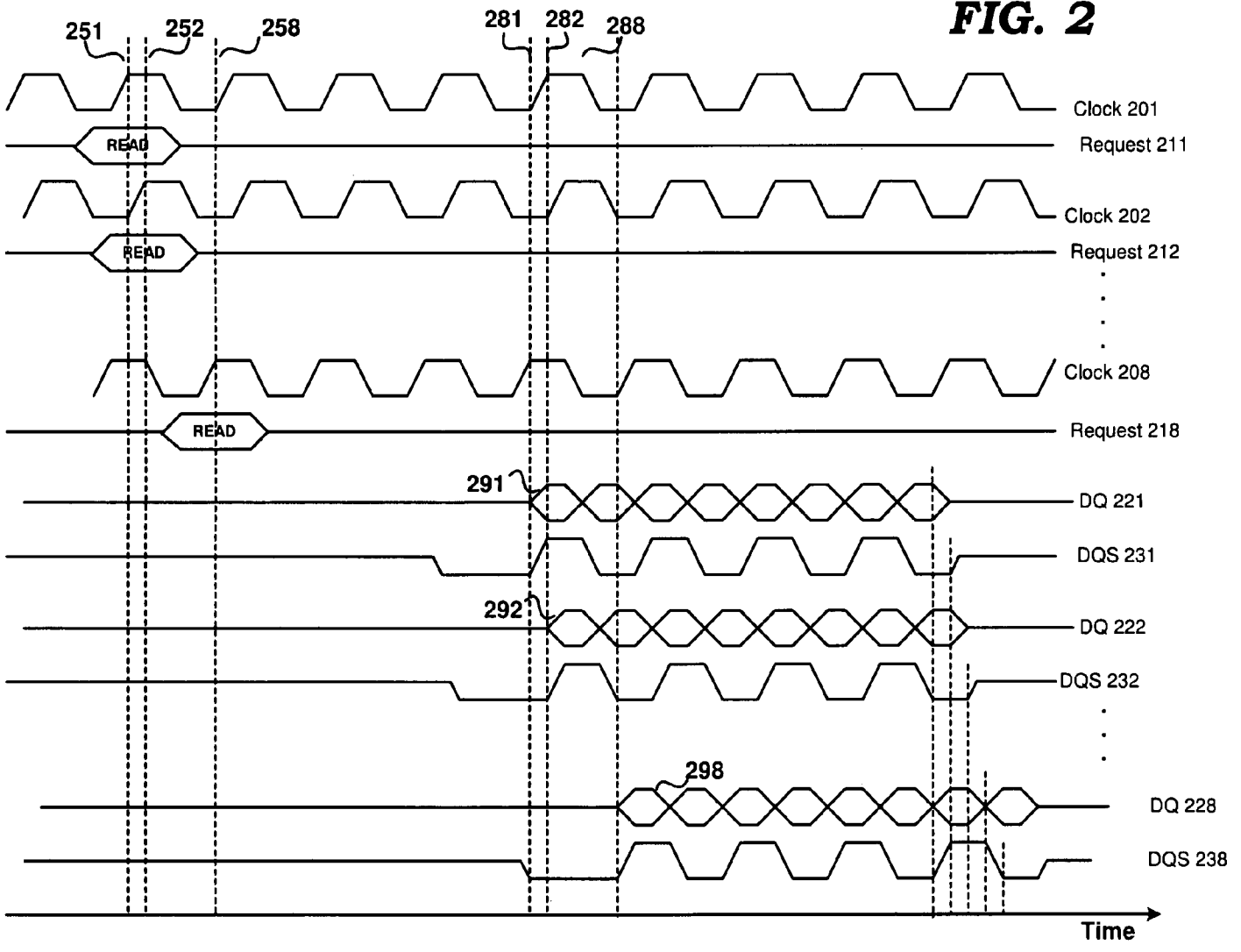


FIG. 1

FIG. 2



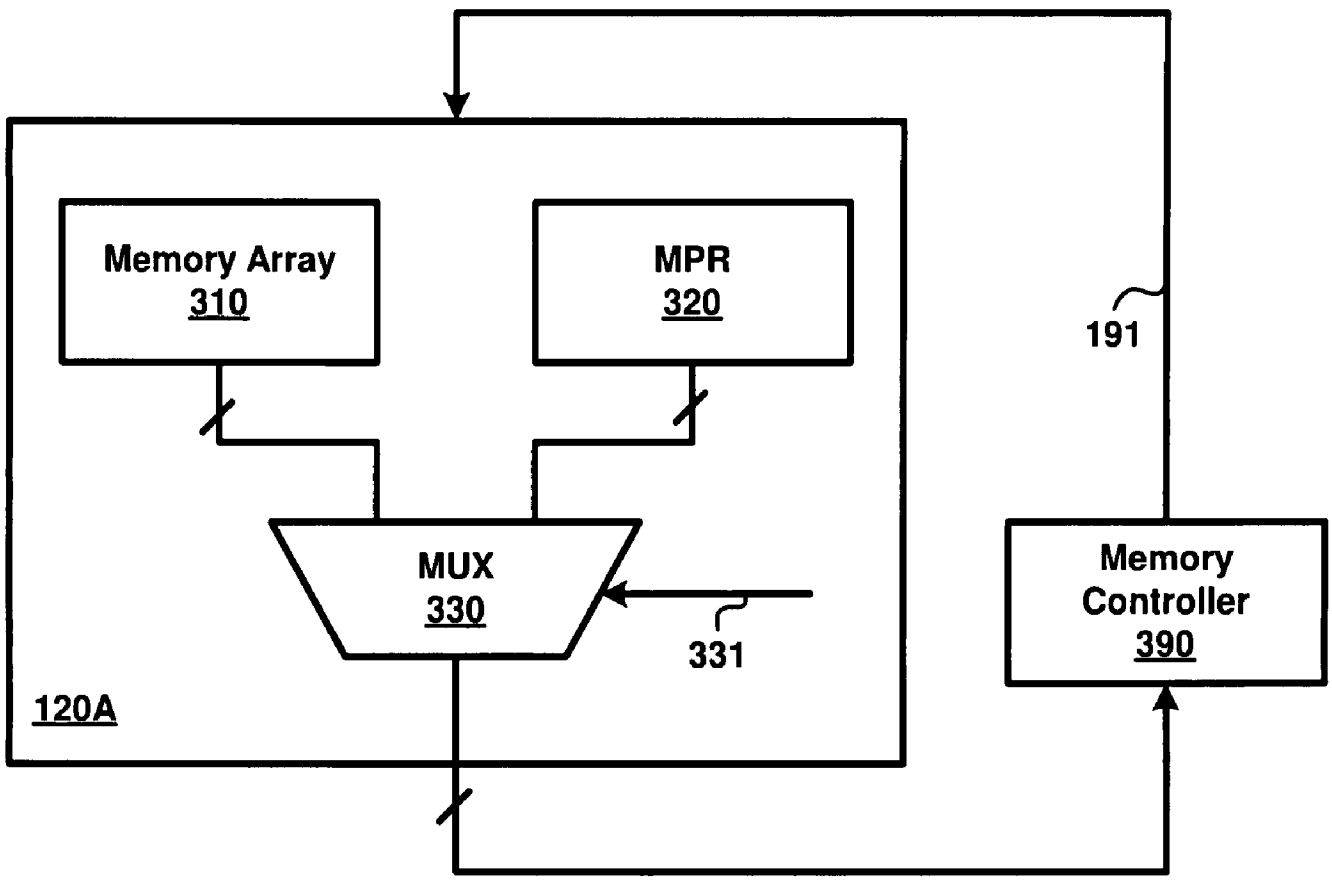


FIG. 3

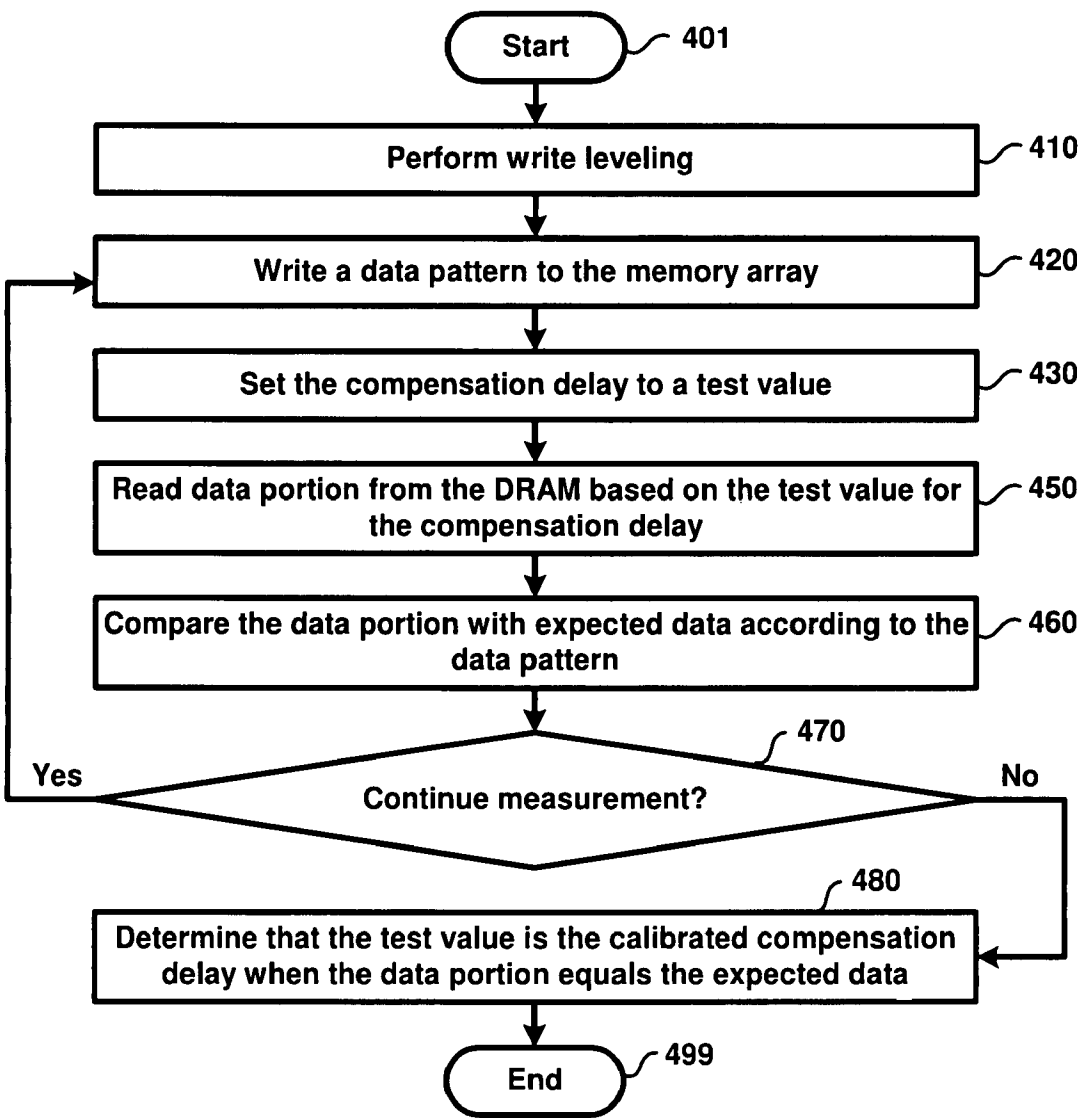


FIG. 4

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