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Trimberger et al.

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(54) **FPGA WITH TIME-MULTIPLEXED INTERCONNECT**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 140 days.

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(51) **Int. Cl.**
G06F 7/38 (2006.01)
H03K 19/173 (2006.01)

(52) **U.S. Cl.** **326/38**; 326/41; 326/47

(58) **Field of Classification Search** 326/37–47
See application file for complete search history.

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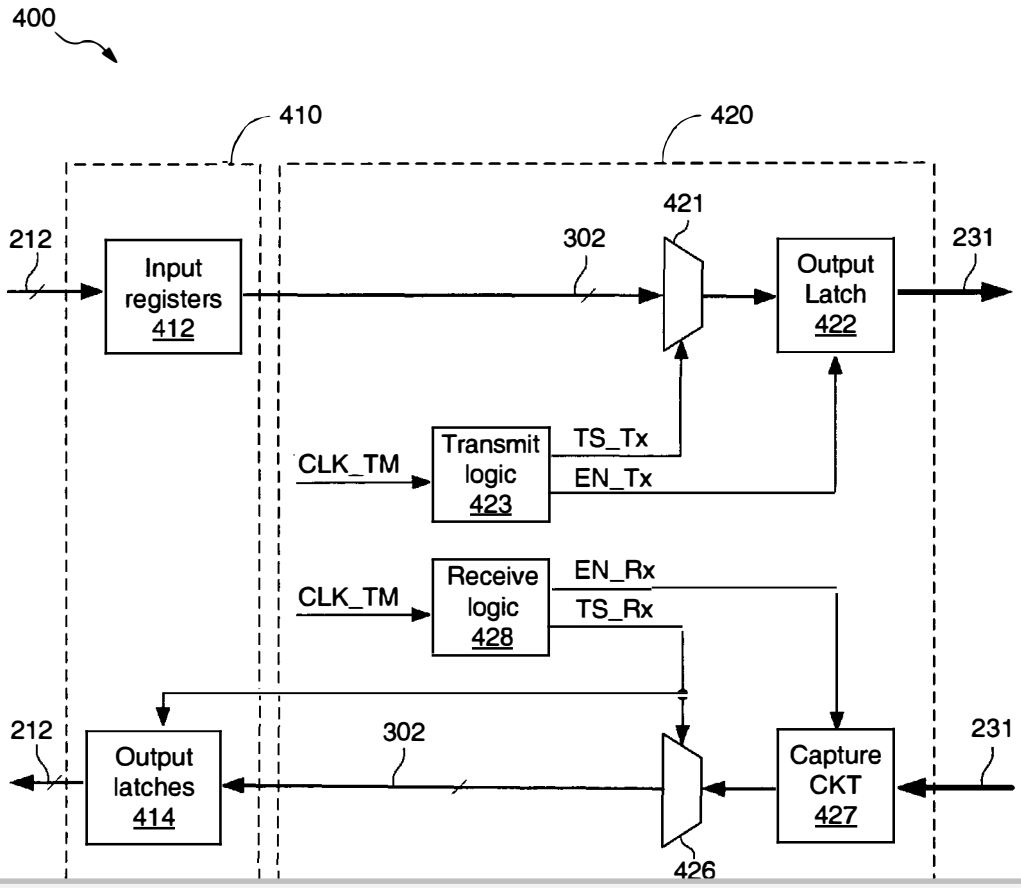
(57) **ABSTRACT**

A programmable logic device (PLD) includes a plurality of configurable resources, a programmable interconnect having a plurality of signal lines for providing a number of dedicated signal paths between any of the configurable resources, and a subway routing system having a shared subway bus coupled to the signal lines of the programmable interconnect at a plurality of connection points by a plurality of corresponding subway ports. The subway routing system, which provides alternate routing resources for the programmable interconnect, may be used to route different signals between different configurable resources at different times.

19 Claims, 7 Drawing Sheets



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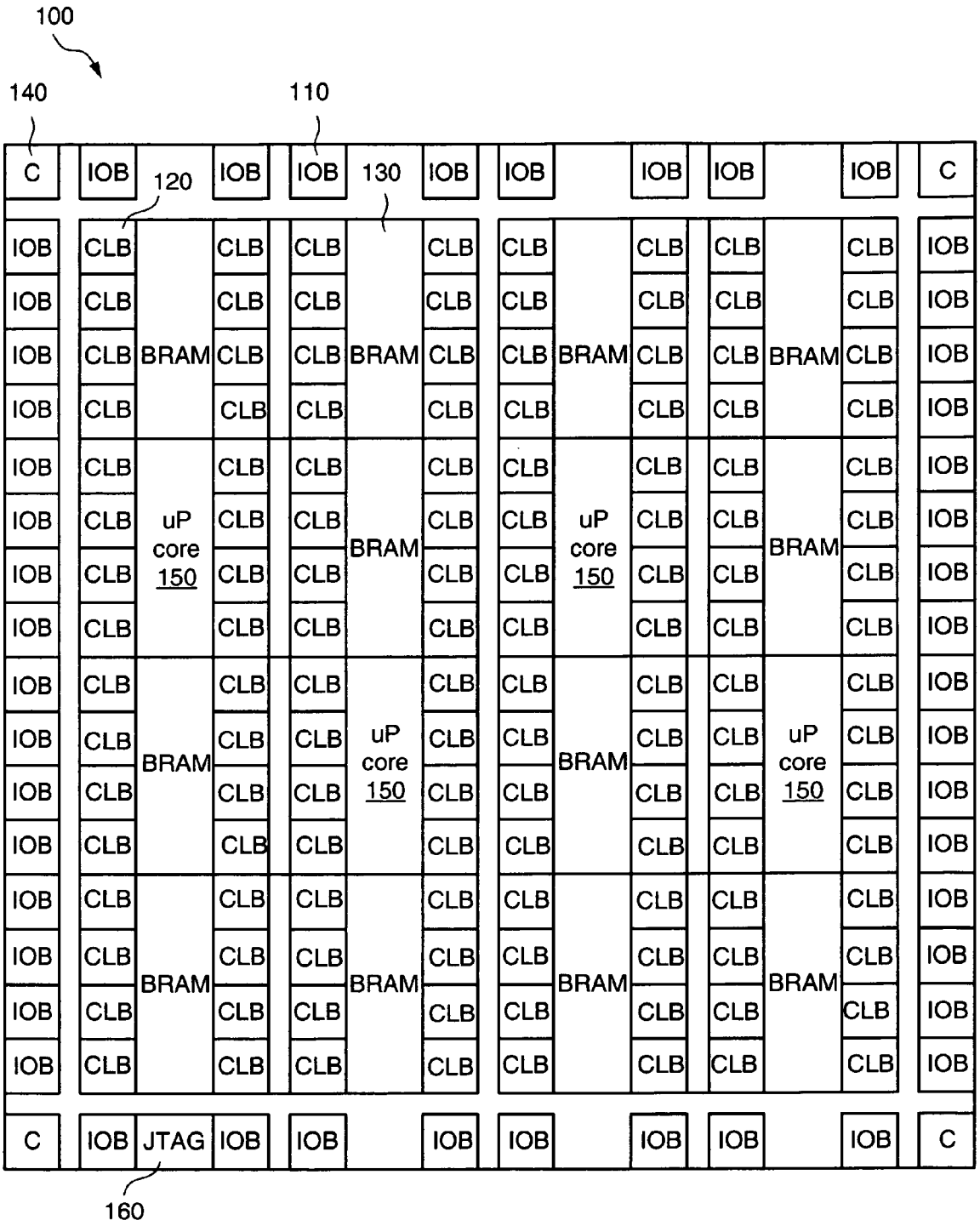

FIG.1

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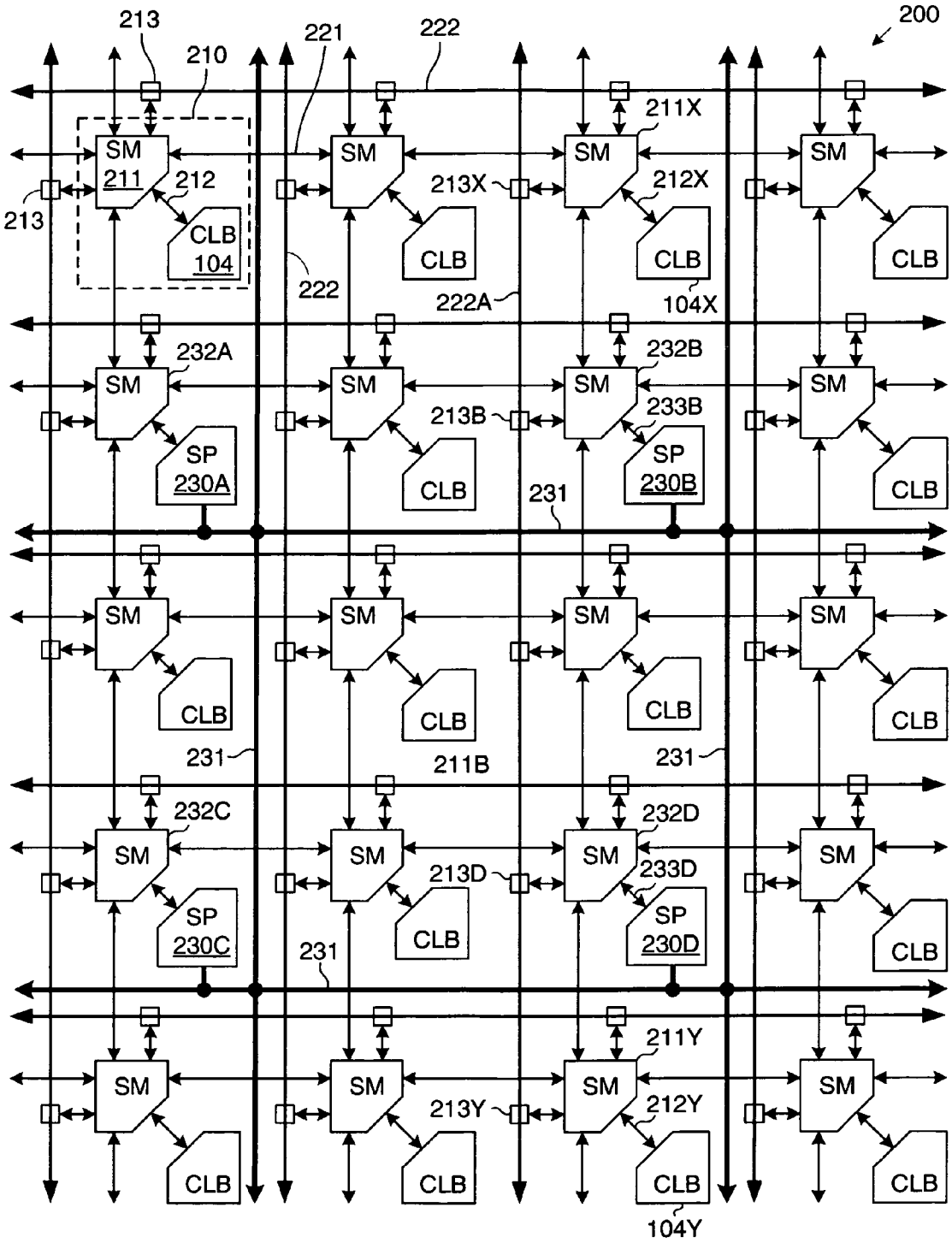

FIG. 2

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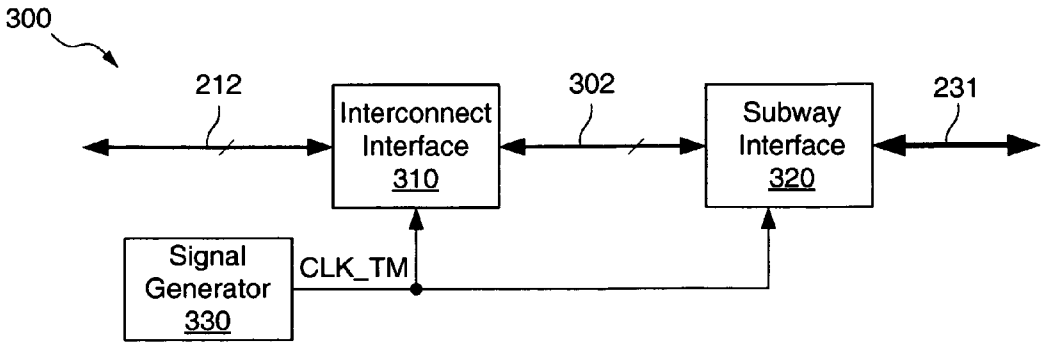

FIG. 3

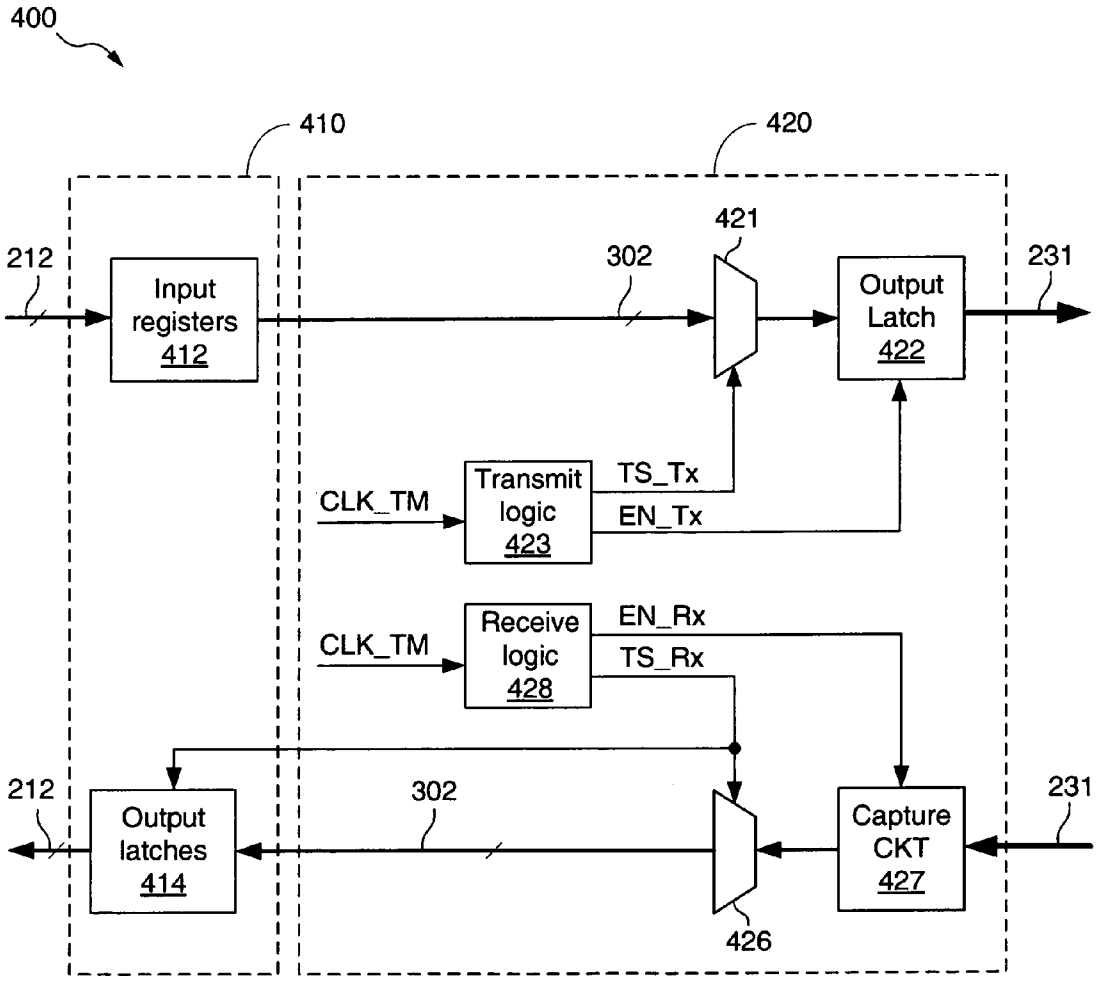

FIG. 4

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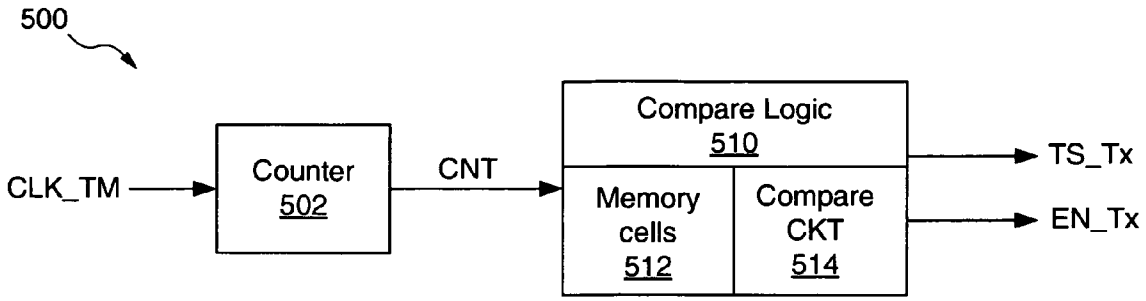

FIG. 5A

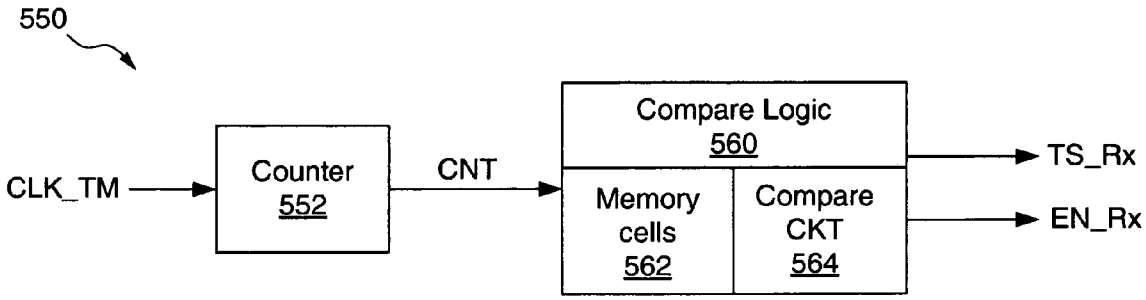

FIG. 5B

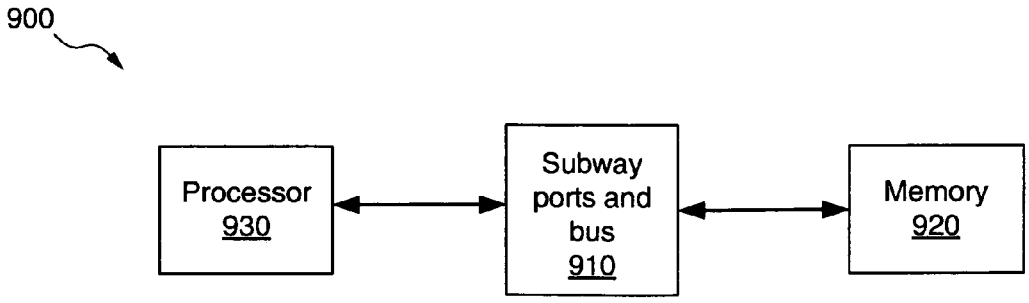

FIG. 9

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