UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC., and QUALCOMM, INC.,
Petitioners

v.

DAEDALUS PRIME LLC.
Patent Owner.

# DECLARATION OF TREVOR MUDGE IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,049,080

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1. Independent Claim 1 ..... 36

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a. Element 1[pre]: A multi-core processor comprising: ....36

b. Element 1[a][i]: a first plurality of cores and a second plurality of cores that support a same instruction set,....37

c. Element 1[a][ii]: wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and....46

d. Element 1[b][i]: power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,....47

e. Element 1[b][ii]: wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand....58

2. Dependent Claim 2: The multi-core processor of claim 1, wherein the second plurality of cores comprise logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores. ....61

3. Dependent Claim 3: The multi-core processor of claim 1, wherein the second plurality of cores comprise logic gates that consume less power than corresponding logic gates of the first plurality of cores....63

4. Dependent Claim 4: The multi-core processor of claim 1, wherein the second plurality of cores each have a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores. ....64

5. Dependent Claim 7: The multi-core processor of claim 1, wherein the first plurality of cores are at a maximum operating frequency in the state. ....65

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6. Dependent Claim 8: The multi-core processor of claim 1, wherein ..... 66
   a. Element 8[a]: the power management hardware is to enable all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores, ..... 66
   b. Element 8[b]: wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand. ..... 71
7. Independent Claims 9 and 17: ..... 71
   a. Element 9[preamble]: A method comprising: ..... 71
   b. Element 17[preamble]: A non-transitory machine readable medium containing program code that when processed by a machine causes a method to be performed, the method comprising: ..... 71
   c. Elements 9[a][i] and 17[a][i]: operating a multi-core processor such that a first plurality of cores and a second plurality of cores execute a same instruction set, ..... 72
   d. Elements 9[a][ii] and 17[a][ii]: wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and ..... 72
   e. Elements 9[b][i] and 17[b][i]: disabling with power management hardware, from a state where the first plurality of cores and the second plurality of cores are enabled, all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, ..... 72
   f. Element 9[b][ii] and 17[b][ii]: wherein an operating system executing on the multi-core processor monitors a demand for the multi-core processor and controls the power management hardware based on the demand. ..... 72

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8. Dependent Claims 10 and 18: The [method of claim 9/non-transitory machine readable medium of claim 17], wherein the operating of the second plurality of cores comprises driving logic gates that have narrower logic gate driver transistors than corresponding logic gates of the first plurality of cores. ....73

9. Dependent Claims 11 and 19: The [method of claim 9/non-transitory machine readable medium of claim 17], wherein the operating of the second plurality of cores comprises driving logic gates that consume less power than corresponding logic gates of the first plurality of cores. ....73

10. Dependent Claims 12 and 20: The [method of claim 9/non-transitory machine readable medium of claim 17], wherein the operating comprises operating the second plurality of cores at a maximum operating frequency that is less than a maximum operating frequency of the first plurality of cores. ....73

11. Dependent Claims 15 and 23: The [method of claim 9/non-transitory machine readable medium of claim 17], wherein the operating comprises operating the first plurality of cores at a maximum operating frequency in the state....73

12. Dependent Claims 16 and 24: The [method of claim 9/non-transitory machine readable medium of claim 17], further comprising....74

a. Elements 16[a] and 24[a]: enabling, with the power management hardware, all of the first plurality of cores for an increase in demand above the threshold without disabling any of the second plurality of cores,....74

b. Elements 16[b] and 24[b]: wherein an operating system is to monitor a demand for the multi-core processor and control the power management hardware based on the demand....74

B. Ground 2: Claims 5-6, 13-14, and 21-22 are rendered obvious by Sutardja in view of Rychlik....74

1. Dependent Claims 5, 13, and 21:....74

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