



(12) **United States Patent**
George et al.

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(54) **ASYMMETRIC PERFORMANCE
MULTICORE ARCHITECTURE WITH SAME
INSTRUCTION SET ARCHITECTURE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 13/335,257, filed on Dec. 22, 2011, now Pat. No. 9,569,278.

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(51) **Int. Cl.**
G06F 15/80 (2006.01)
G06F 13/40 (2006.01)
G06F 1/32 (2006.01)

(57) **ABSTRACT**

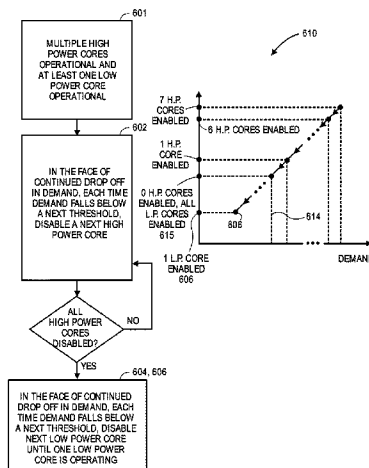
(52) **U.S. Cl.**
CPC **G06F 15/80** (2013.01); **G06F 1/3206** (2013.01); **G06F 1/3293** (2013.01); **G06F 1/3296** (2013.01); **G06F 13/4022** (2013.01)

A method is described that entails operating enabled cores of a multi-core processor such that both cores support respective software routines with a same instruction set, a first core being higher performance and consuming more power than a second core under a same set of applied supply voltage and operating frequency.

(58) **Field of Classification Search**

None
See application file for complete search history.

24 Claims, 8 Drawing Sheets



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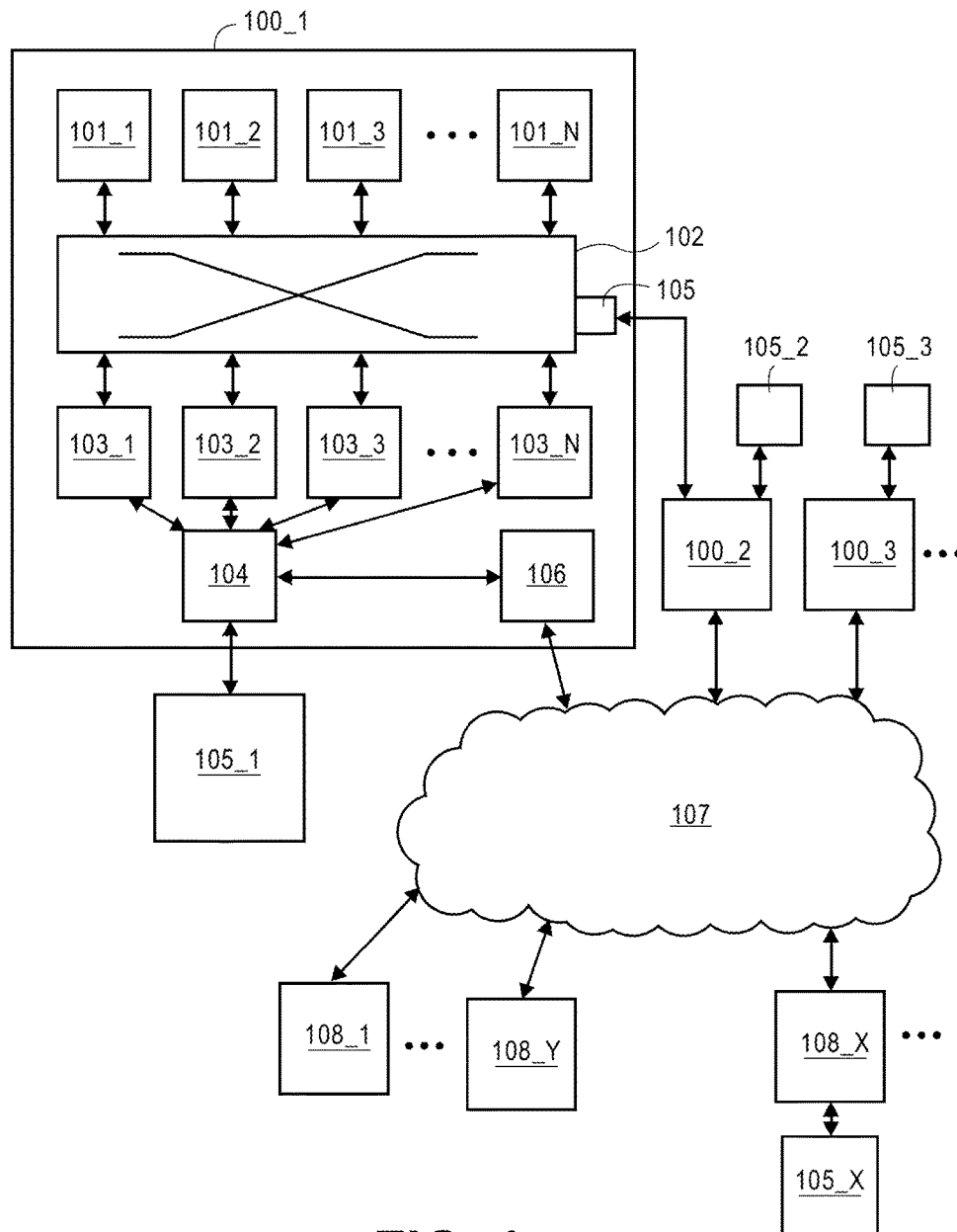


FIG. 1

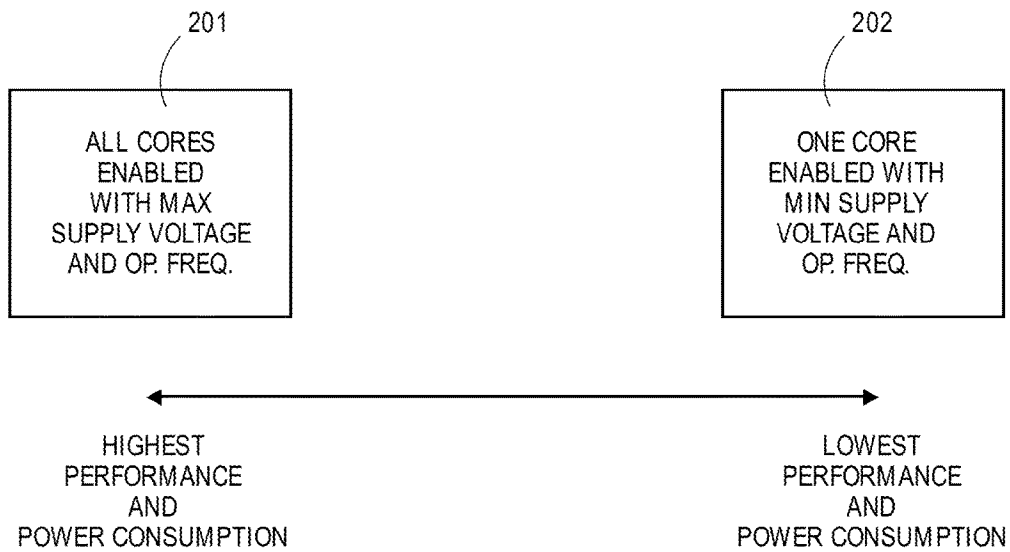


FIG. 2

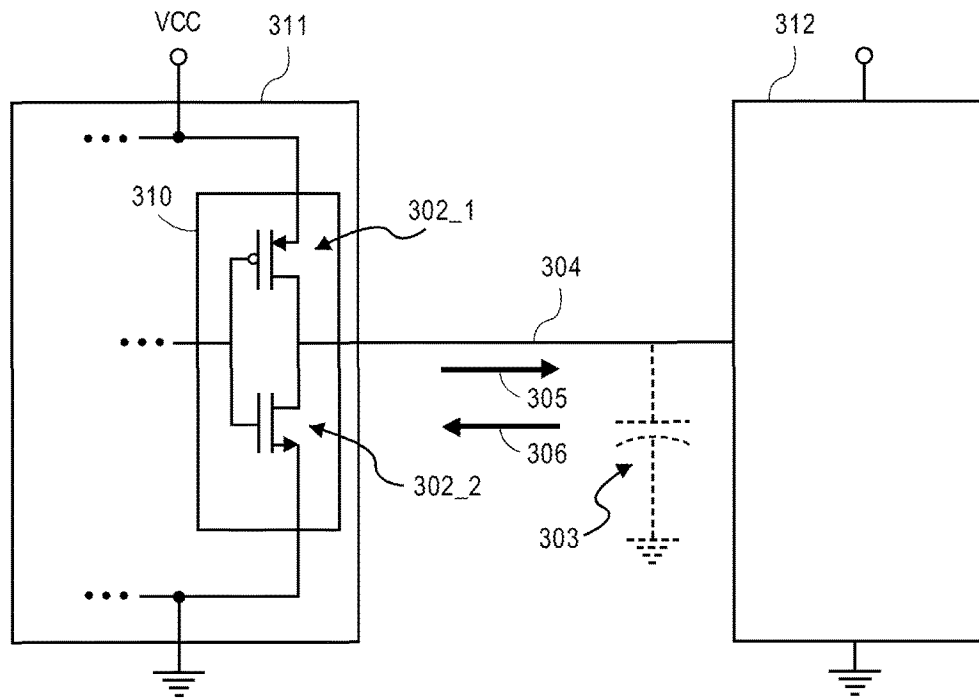


FIG. 3

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