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Thomson et al.

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(54) **SYSTEM AND APPARATUS FOR CONSOLIDATED DYNAMIC FREQUENCY/VOLTAGE CONTROL**

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(51) **Int. Cl.**

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G06F 1/26	(2006.01)
G06F 15/16	(2006.01)
H04L 29/08	(2006.01)
G06F 9/38	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 1/3296*** (2013.01); ***G06F 1/324*** (2013.01); ***G06F 1/3228*** (2013.01); *G06F 1/3206* (2013.01); *G06F 9/3885* (2013.01); *H04L 67/10* (2013.01); *Y02B 60/1217* (2013.01); *Y02B 60/1285* (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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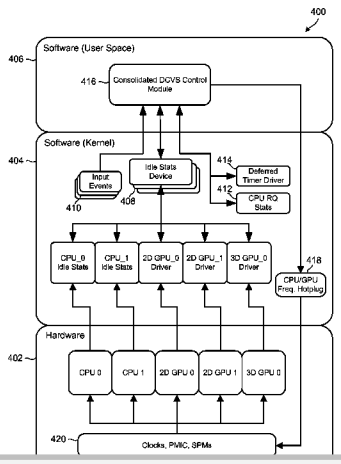
(57) **ABSTRACT**

Methods and apparatus for accomplishing dynamic frequency/voltage control between at least two processor cores in a multi-processor device or system include receiving busy, idle and wait, time and/or frequency information from a first processor core and receiving busy, idle, wait, time and/or frequency information from a second processor core. The received busy, idle, wait, time and/or frequency information may be correlated to identify patterns of interdependence. The correlated information may be used to determine dynamic frequency/voltage control settings for the first and second processor cores to provide a performance level that accommodates interdependent processes, threads and processor cores. The correlation of received busy, idle, wait, time and/or frequency information may involve generating a consolidated busy/idle pulse train that can then be used to set the frequency or voltage of each processor core independently.

40 Claims, 11 Drawing Sheets



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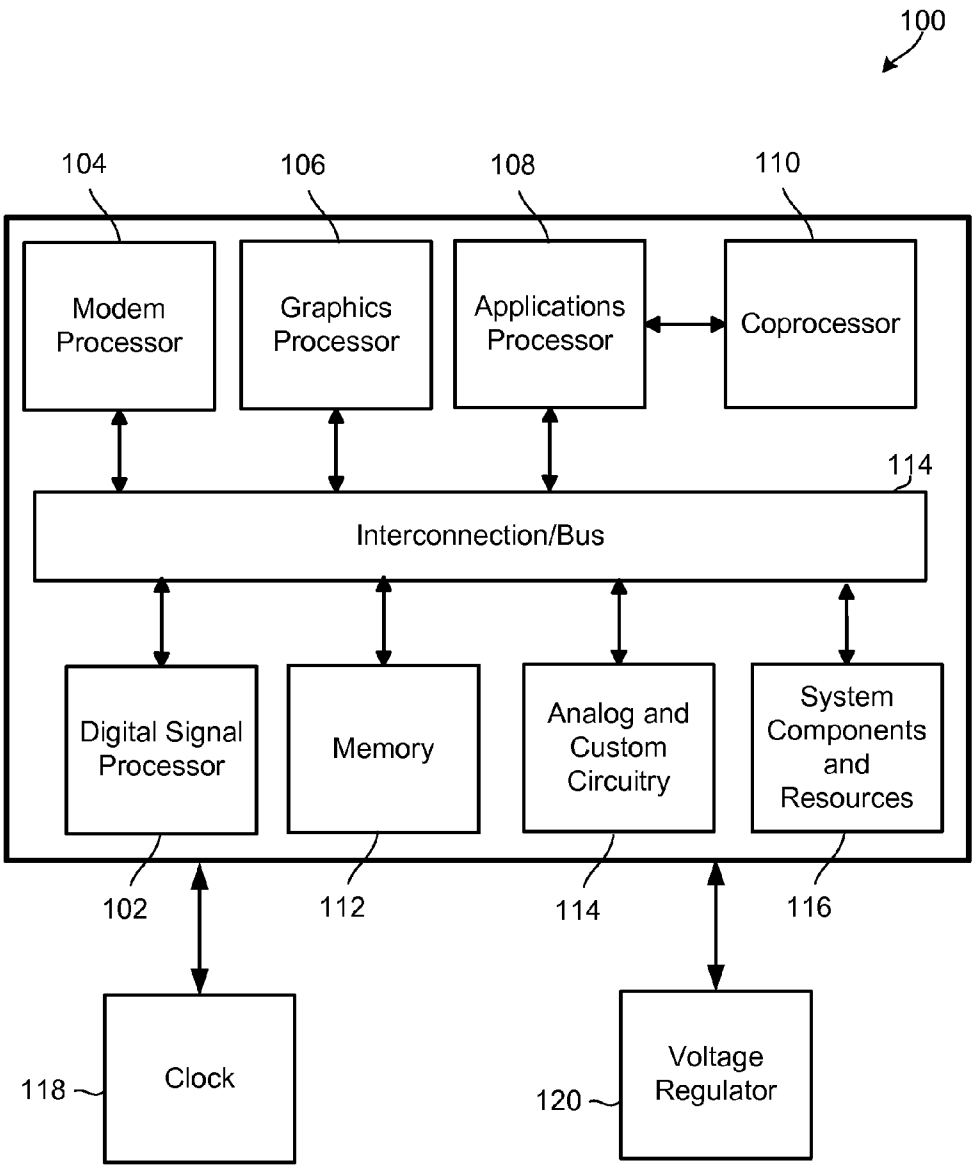

FIG. 1

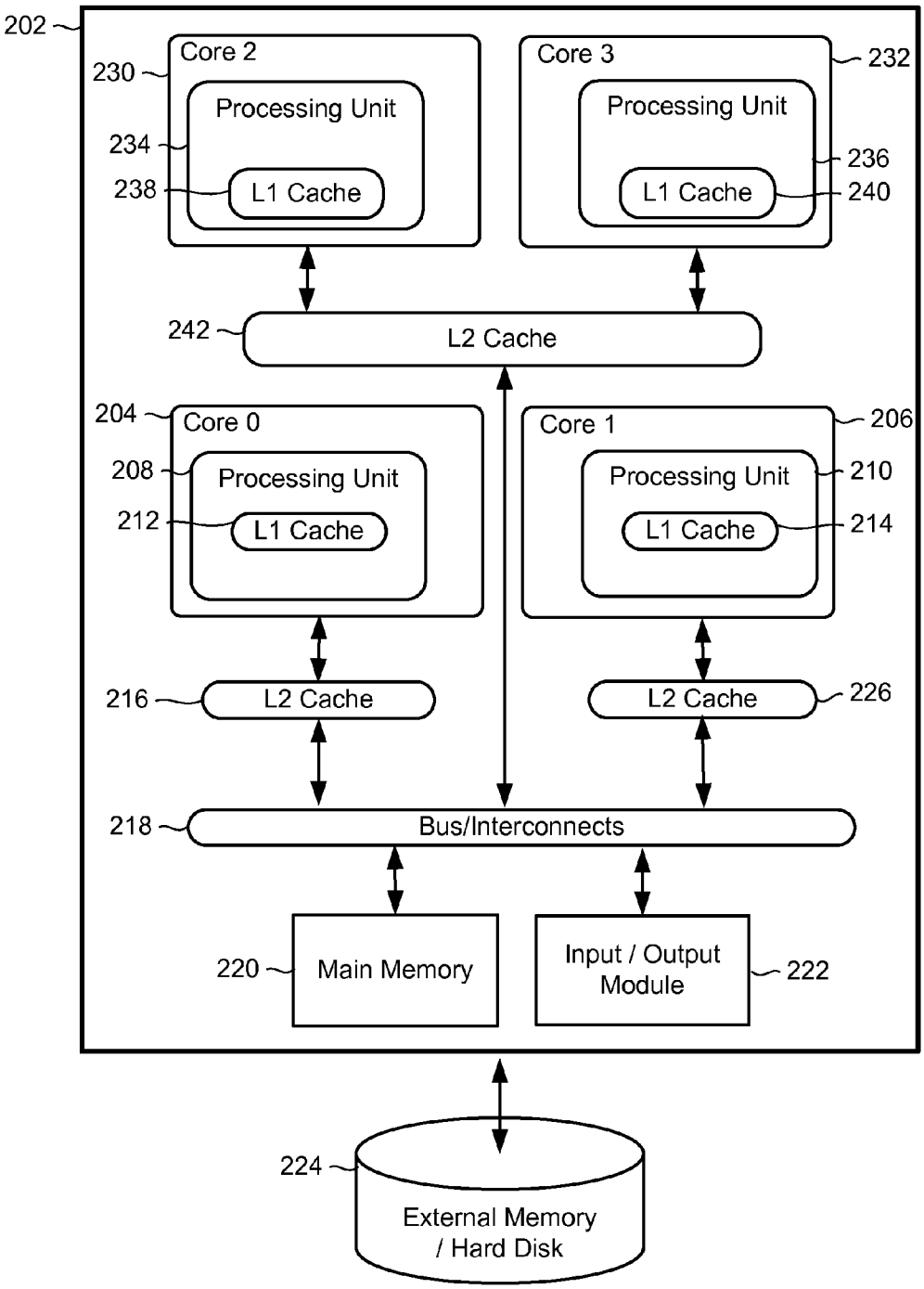

FIG. 2

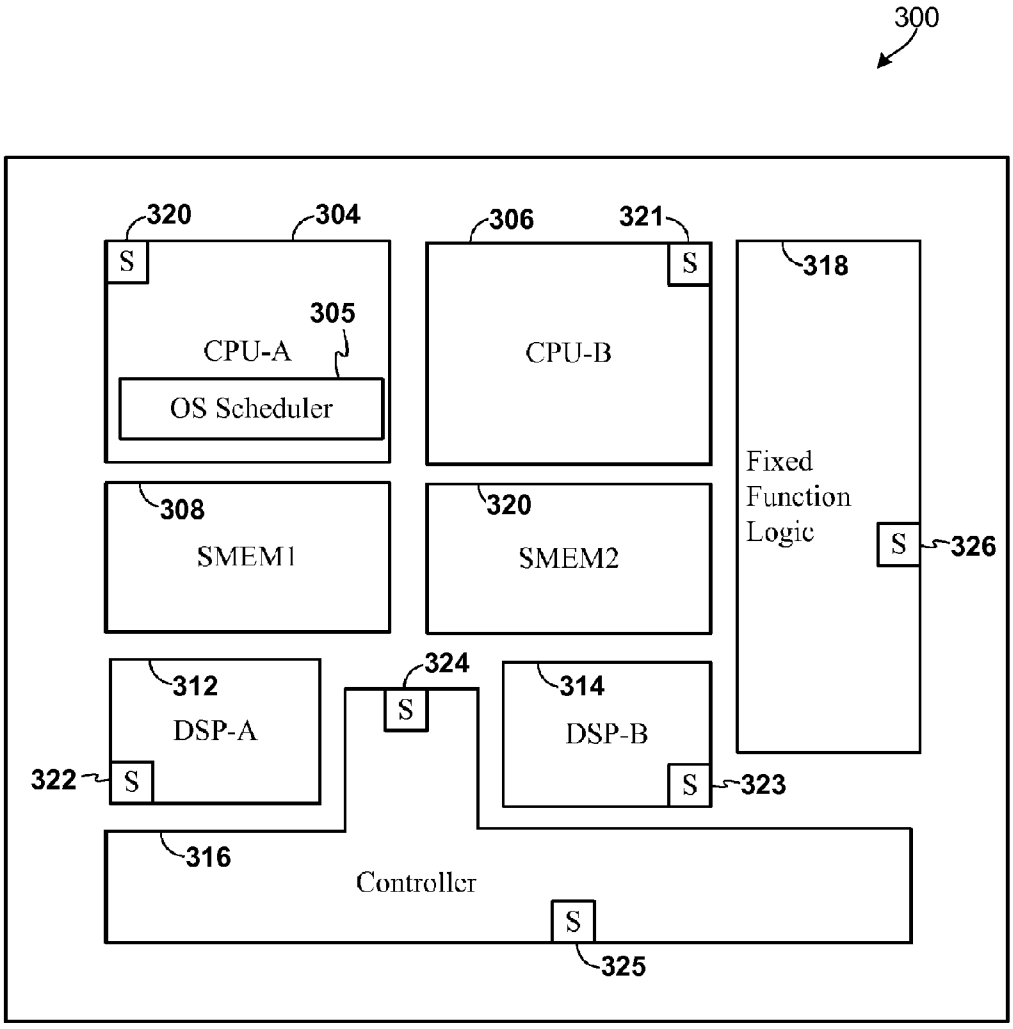

FIG. 3

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