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Vajda

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(54) **METHOD FOR EXECUTING SEQUENTIAL CODE ON THE SCALABLE PROCESSOR AT INCREASED FREQUENCY WHILE SWITCHING OFF THE NON-SCALABLE PROCESSOR CORE OF A MULTICORE CHIP**

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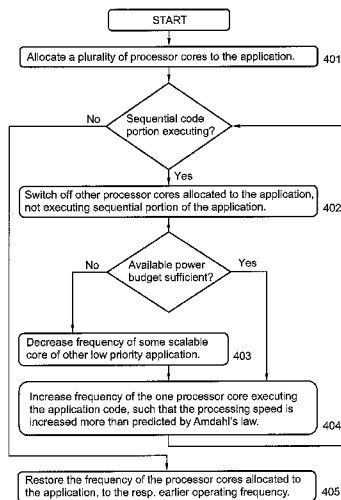
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CPC **G06F 9/4893** (2013.01); **G06F 1/3203** (2013.01); **G06F 1/3287** (2013.01); Y02B 60/144 (2013.01); Y02B 60/1217 (2013.01)
USPC **718/104**; 713/320; 713/323; 713/324

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See application file for complete search history.

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(57) **ABSTRACT**

Method and scheduler in an operating system, for scheduling processing resources on a multi-core chip. The multi-core chip comprises a plurality of processor cores. The operating system is configured to schedule processing resources to an application to be executed on the multi-core chip. The method comprises allocating a plurality of processor cores to the application. Also, the method comprises switching off another processor core allocated to the application, not executing the sequential portion of the application, when a sequential portion of the application is executing on only one processor core. In addition, the method comprises increasing the frequency of the one processor core executing the application to the second frequency, such that the processing speed is increased more than predicted by Amdahl's law.

12 Claims, 6 Drawing Sheets

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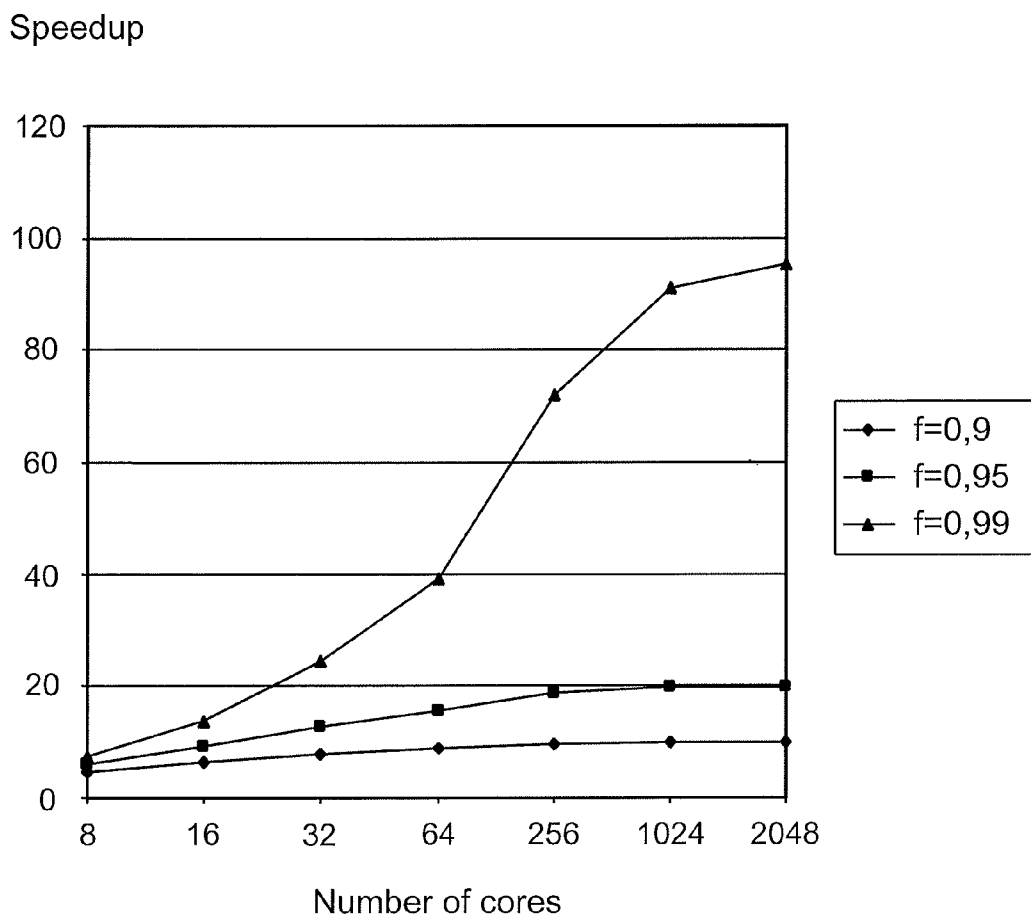
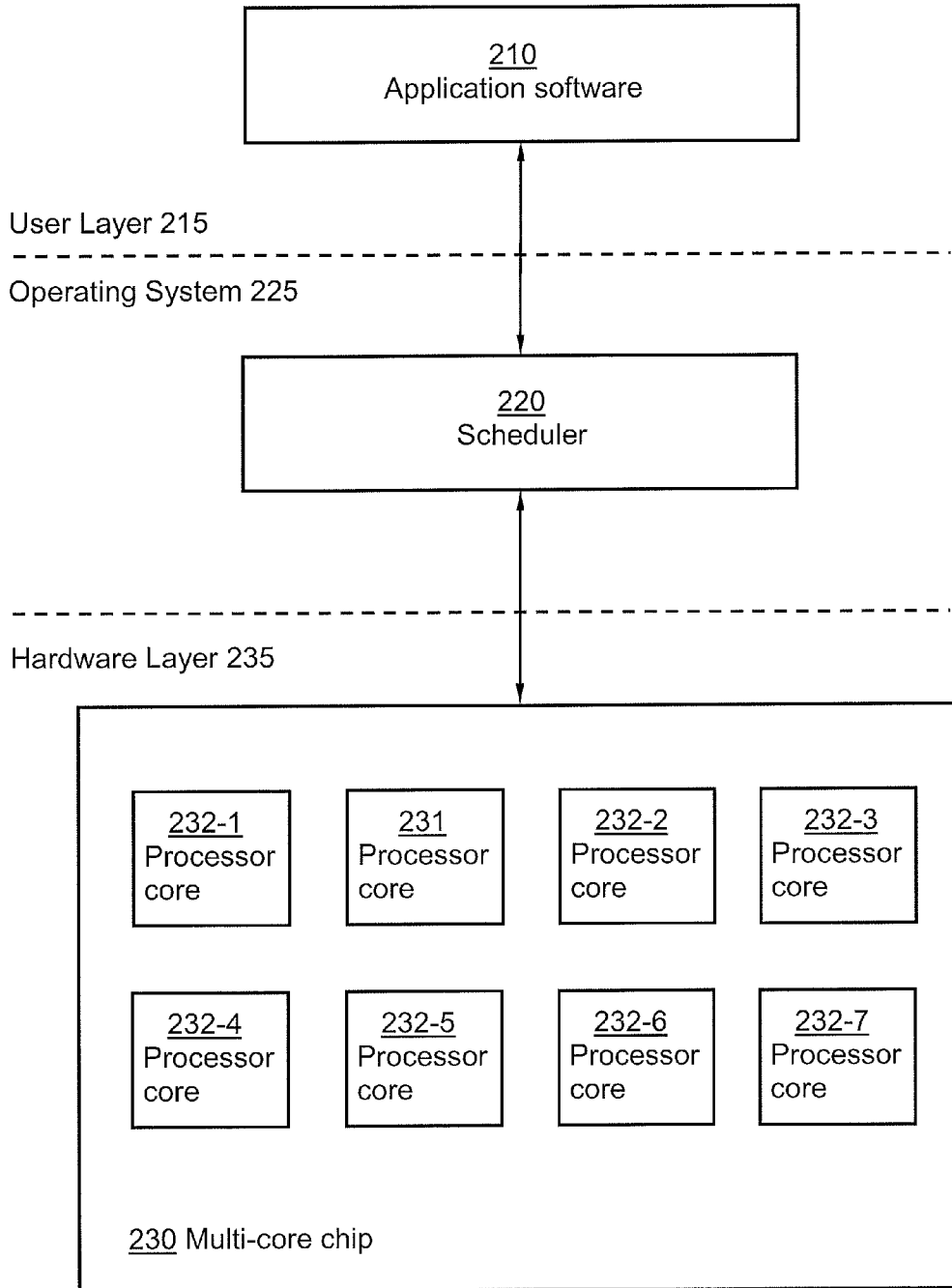* cited by examiner
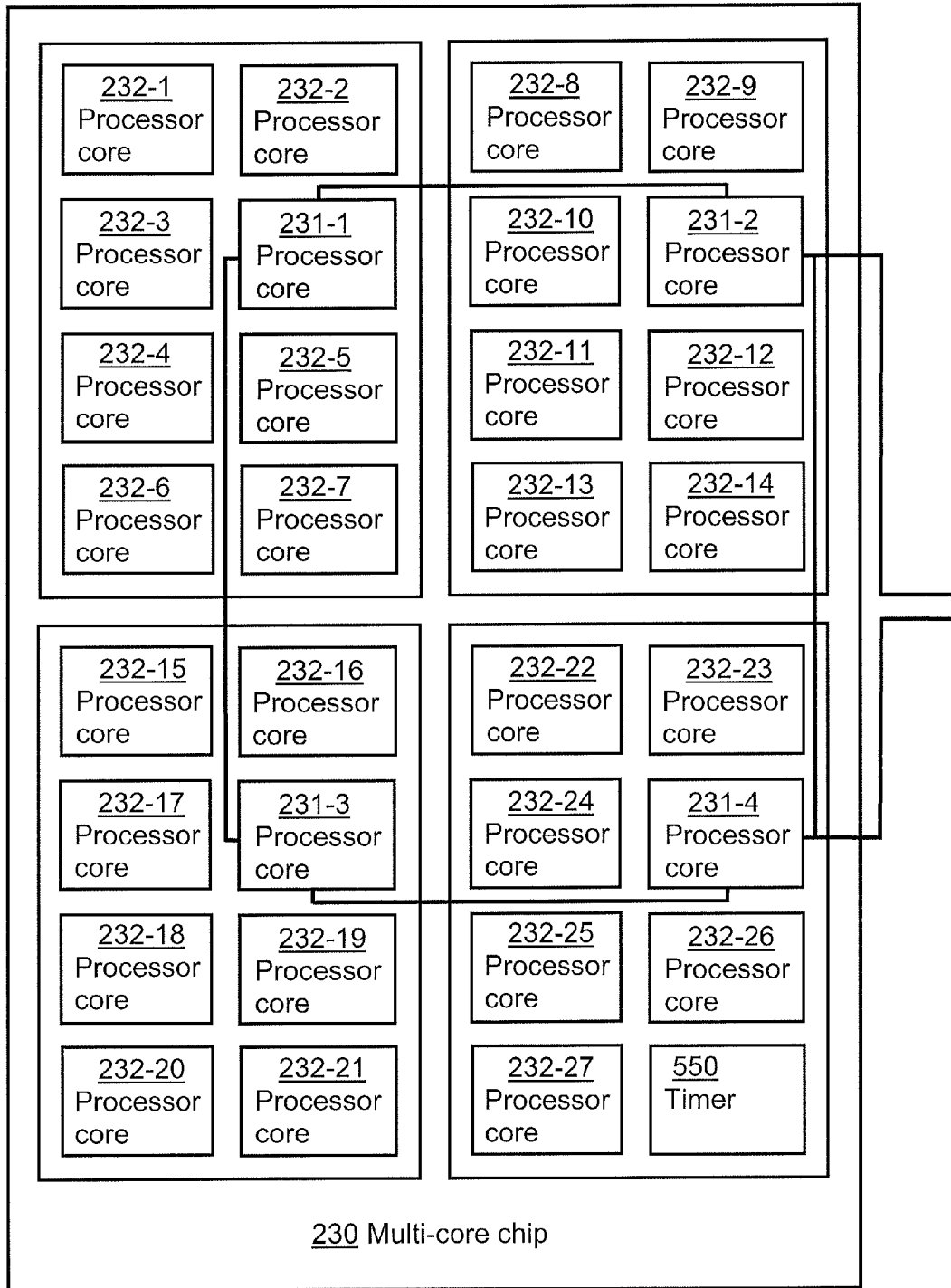
Speed-up according to Amdahl's law

Fig. 1

Fig. 2

232-1 Processor core	232-2 Processor core		232-8 Processor core	232-9 Processor core
232-3 Processor core	231-1 Processor core		232-10 Processor core	231-2 Processor core
232-4 Processor core	232-5 Processor core		232-11 Processor core	232-12 Processor core
232-6 Processor core	232-7 Processor core		232-13 Processor core	232-14 Processor core

232-15 Processor core	232-16 Processor core		232-22 Processor core	232-23 Processor core
232-17 Processor core	231-3 Processor core		232-24 Processor core	231-4 Processor core
232-18 Processor core	232-19 Processor core		232-25 Processor core	232-26 Processor core
232-20 Processor core	232-21 Processor core		232-27 Processor core	550 Timer

230 Multi-core chip

Fig. 3

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