JEDEC STANDARD

CONFIGURATIONS FOR SOLID STATE MEMORIES

JEDEC Standard No. 21–C
Release 7

January 1997

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT

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JESD 21–C, Release 7 Insertion Instructions
Instructions for adding Release 7 to JEDEC Standard 21–C.
Inclosed with this instruction sheet are new and replacement pages for JEDEC Standard 21–C. Those pages which contain new material are labeled "Release 7" at the bottom of the page. In some cases, there will be old material on the back of the sheet containing a Release 7 page. This old material will be labeled Release 1, Release 2, Release 3, Release 4, Release 5, or Release 6 as there are no changes from the original release. All new text is marked by a "Revision Bar" in the outside margin in addition to the "Release 7" label in the inside footer of the page.

In this release, I have introduced a new feature in the Release #. In the past when an older sheet was replaced with a new one, either to make a correction, or to revise the original sheet, the new release number simply replaced the old number, thus loosing the information of the original release number. In this release, the old number will be retained followed by the letter "c" for correction, or "r" for revised, this followed by the new release number (e.f 4c7 or 6r7)

The following is a series of sheet by sheet instructions to be used to print the pages for this release. The instruction numbers correspond directly the instructions intended for the holders of the Standard. These are also included with the new originals for R–6. These instructions should be included as the first pages in Release 6. In the printing instructions, the Release # s are refered to as R#.

In the following 75 instructions, the material is arranged in 3 columns. The first column tells which sheet to remove from the 21–C binder. The second column tells which sheet to add to the binder. The third column gives an explanation of the reason for the change or addition.

REMOVE	ADD	REASON
1. Remove Cover Page	Add replacement Cover Page	Contains new Release level and date.
2. Remove Title Page;	Add replacement Title Page:	Contains revision Log for Standard.
3. Remove TOC, 8 sheets;	Add replacement TOC, 9 sheets;	Revised Table of Contents
4. Remove PP 2–3/4	Add replacement PP 2–3/4	New definitions added
5. Remove PP 2–5/6	Add replacement PP 2–5/6	
6. Remove PP 2–7/8	Add replacement PP 2–7/8	New material added.
7. Remove PP 2–9/10	Add replacement PP 2–9/10	New material added.
8. Remove P 3.5.1–3	Add replacement PP 3.5.1–3/4	New standards added
9.	Add new PP 3.5.1–33/34	New standard added
10. Remove P 3.5.2–3	Add replacement P 3.5.2–3	New standards added
11. Remove P 3.5.2–9	Add replacement PP 3.5.2–9/10	New devices added to existing standard.
12.	Add new P 3.5.2–11	New standard
13. Remove P 3.5.3–1	Add replacement P 3.5.3–1/2	Section re–orgainzed
14. Remove P 3.5.3–3/4	Add replacement PP 3.5.3–3/4	New standards added.
15. Remove P 3.5.3–5/6	Add replacement PP 3.5.3–5/6	New standard added
16. Remove P 3.5.3–7/8	Add replacement P 3.5.3–7/8	New standards added
17.	Add new P 3.5.3–9/10	New standards added
18.	Add new P 3.5.3–11/12	New standards added
19.	Add new P 3.5.3–13/14	New standards added
20.	Add new P 3.5.3–15	New standards added
21. Remove P 3.7.5–1/2	Add replacement PP 3.7.5–1/2	New standards added.
22. Remove P 3.7.5–3/4	Add replacement PP 3.7.5–3/4	New standards added.
23. Remove P 3.7.5–25/26	Add replacement PP 3.7.5–25/26	Errors corrected
24. Remove P 3.7.7–15/16	Add replacement PP 3.7.7–15/16	Errors corrected
25. Remove P 3.7.8–3	Add replacement P 3.7.8–3	Existing standard modified.

26.	Remove PP 3.7.8–9/10	Add replacement PP 3.7.8–9/10	New device added.
27.		Add new P 3.7.8–11	New standards added
28.	Remove P 3.9.1–15/16	Add replacement PP 3.9.1–15/16	New standards added.
29.	Remove P 3.9.2–3/4	Add replacement PP 3.9.2–3/4	New standards added.
30.	Remove PP 3.9.2–15/16	Add replacement PP 3.9.2–15/16	Modified drawing of existing standard.
31.	Remove PP 3.9.2–17/18	Add replacement PP 3.9.2–17/18	Modified drawing of existing standard
32.		Add new PP 3.9.2–19	New standard.
33.	Remove P 3.9.3–11/12	Add replacement P 3.9.3–11/12	Standard modified.
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36.			
37.	Remove P 3.9.5–3	Add replacement P 3.9.5–3	New standards added.
38.	Remove P 3.9.5–15/16	Add replacement PP 3.9.5–15/16	New standard added.
39.	Remove P 3.10.3–1/2	Add replacement PP 3.10.3–1/2	New standards added.
40.	Remove P 3.10.3–5/6	Add replacement PP 3.10.3–5/6	Correct error.
41.		Add new PP 3.10.3–9	New standards added.
42.	Remove PP 3.10.4–3/4	Add replacement PP 3.10.4–3/4	New standards added
43.	Remove PP 3.10.4–17/18	Add replacement PP 3.10.4–17/18	New standards added
44.	Remove PP 3.10.4–19/20	Add replacement PP 3.10.4–19/20	New standards added
45.		Add new PP 3.10.4–21	New standards added
46.	Remove P 3.11.2–1	Add replacement P 3.11.2–1	New standard added.
47.	Remove P 3.11.2–3/4	Add replacement PP 3.11.2–3/4	Existing standard modified.
48.		Add new PP 3.11.2–5	New standards added
49.	Remove P 3.11.3–1	Add replacement P 3.11.3–1	New standard added.
50.	Remove P 3.11.3–3/4	Add replacement PP 3.11.3–3/4	Existing standard modified, new standard added.
51.		Add new PP 3.11.3–5	New standards added
52.	Remove P 3.11.4–1	Add replacement P 3.11.4–1/2	Standards revised.
53.	Remove P 3.11.4–3/4	Add replacement PP 3.11.4–3/4	Standards revised.
54.	Remove P 3.11.4–5/6	Add replacement PP 3.11.4–5/6	Standards revised.
55.	Remove P 3.11.4–7/8	Add replacement PP 3.11.4–7/8	Standards revised, correct error.
56.		Add new PP 3.11.4–9	New standards added.
57.	Remove PP 3.11.5–7/8	Add replacement PP 3.11.5–7/8	Correct error.
58.	Remove PP 3.11.5–9/10	Add replacement PP 3.11.5–9/10	Terminology corrections.

Section 4 on Modules has been completely re–organized. Remove and discard all of the old pages from Section 4 and replace them with the new ones supplied. No sub–dividers are supplied, but it will enhance the usability of the section by adding your own dividers. The individual sheets are not listed here as they are supplied in correct order for insertion.

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CONFIGURATIONS FOR SOLID STATE MEMORIES

Formulated under the cognizance of Committees JC–42.1, PLD devices, JC–42.3, volatile memories, JC–42.4, non–volatile memories, and JC–42.5, memory modules and cards, and approved by the JEDEC Council.

Standard 21–C Revision Log.

Release 1, August 1990

Release 2, September 1991

Release 3, November 1992

Release 4, November 1993

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Release 7, January 1997

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2.1.17 – DC, DIAGNOSTIC CLOCK

The input that, on some devices, invokes and controls any built–in diagnostic test features.

2.1.18 – DQ(n)(x), DATA INPUT/OUTPUT

The pins that serve as data output(s) when in the read mode and as data input(s) when in the write mode. When the device is not selected or enabled, the output(s) are in a floating state. On a devices having both serial and parallel access ports, these pins provide access to the parallel RAM port data channels. The suffix (n) is a numeric value indicating the number assignment of a particular pin with numbering starting at 0. In some situations the letters U or L are used to indicate that the pins are assigned to the upper or lower byte of a 2 byte data interface. In devices where the standard supports an optional 9th bit that may be used as a parity bit, the suffix P may be used in lieu of a numeric value. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.19 – DQM, INPUT/OUPUT DATA MASK

A control signal used primarily on SDRAMs that acts as as mask for reading and writing functions. In some instances, the DQM term will includes a prefix "U" or "L" indicating upper or lower byte control. In devices where more than two data bit groupings have a data mask applied, a "x" is applied where "x" takes the values of a, b, c, etc.

2.1.20 – E, CHIP ENABLE

The input that, when true, permits active operation including the input and/or output of data, and when false, prevents active operation and causes the memory to be in a reduced power standby mode with the outputs floating.

2.1.21 – F, REFRESH

An input that, when true, causes the device to enter a data refresh mode.

2.1.22 – G(n), OE(n), OUTPUT ENABLE

The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.23 – GS, SYNCHRONOUS OUTPUT ENABLE

An output enable input that must be set in by a synchronizing clock signal, K (q.v.).

2.1.24 – $\overline{\mathrm{I}}$, INITIALIZE INPUT

A control input that provides a preassigned Manufacturer or User defined code to be set into the data register. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.25 – ID(n), IDENTIFICATION

A group of output terminals, nominally used to convey information about the configuration or other attributes of the device when plugged into a system. The function of these outputs are similar to those of the PD(n) terminals but they often have different electrical interface chatacteristics.

2.1.26 – I/O, INPUT/OUTPUT

A generic term for otherwise undefined signal pins which can have either an input and/or an output function. This term is not used as a specific pin name, only as a generic indicatior of the nature of the function of the pin.

2.1.27 – $\overline{\mathrm{IS}}$, INITIALIZE INPUT (SYNCHRONOUS)

A control input that provides a preassigned Manufacturer or User defined code to be presented to the data register for subsequent setting by a clock input. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.28 – K, INPUT CLOCK

The input that, on devices that contain input buffer registers, causes the address on the A(n), the data on the D(n) pins and/or certain control inputs to be set into the register.

2.1.29 – L, LATCH ENABLE or LOWER BYTE

An input that, on devices containing a latch register, causes the data to be latched into the register. When L is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. $\overline{\mathrm{LW}}$).

2.1.30 – LB, LOWER BYTE ENABLE

An input, on wordwide devices, that, when true, enables the lower byte data input/outputs, pins DQ0 through DQ7.

2.1.31 – LW, LOWER BYTE WRITE ENABLE

An input, on wordwide devices, that when true causes the data present on the lower byte input/output, terminals DQ0 through DQ7, to be written into the addressed cells of the device.

2.1.32 – M(n), M, MODE SELECT, MASK

Input signals that when true select an alternative mode of operation for the device. The alternative modes available must be defined in the applicable device standard. When M is used in conjuction with other symbols to create a new pin name, it signifies that the pin function is either MASK or MODE related.

2.1.33 – MA, MATCH

An output signal that when true indicates that there has been a match (logic compare equal) between data stored in the memory and data presented on a set of input pins as defined in the individual device standard.

2.1.34 – MCH, MUST CONNECT HIGH

A pin which must be connected to a voltage that is interpreted as logic high or "true" signal.

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2.1.35 – MCL, MUST CONNECT LOW
A pin which must be connected to a voltage that is interpreted as logic low or "false" signal.

2.1.36 – NC, NO CONNECTION
A pin to which no internal electrical connection is present or allowed.

2.1.37 – NE, NON–VOLATILE ENABLE
The input, on a NVRAM, that enables the non–volatile functions ST & RC as determined by the states of S,E,G, and W.

2.1.38 – NF, NO FUNCTION
An input that is electrically connected to the device but for which the signal has no function in the device operation.

2.1.39 – NP, NO PIN
A pin position on a package where the pin has been purposely been left blank or removed after assembly. No physical pin is allowed in this position.

2.1.40 – NU, NOT USABLE
A device pin to which there may or may not be an internal connection but to which no external connections are allowed.

2.1.41 – OE,(n), G(n) OUTPUT ENABLE
The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.42 – OP, OPTIONAL
The designation for pins on which the manufacturer has the freedom to supply a specialized function not previously defined in the standard, and still have his part meet the requirements of the standard.

2.1.43 – P, PROGRAM or PROGRAM ENABLE, PARITY
The input on a non–volatile memory device that, when true, causes the data present on the D or DQ pins to be written into the addressed cell(s) of the device. The letter P may also be used as a suffix for data pins where an optional 9th bit, that may be used for parity, is allowed by the standard (e.g. DQP)

2.1.44 – PD(n), PRESENCE DETECT
A group of output pins, normally used on modules or cards, whose state is used to convey information about the capacity, speed, configuration, or other attributes of the device when plugged into a system.

2.1.45 – PR, PAGE RESET
The input on a page select memory that, when true, unconditionally causes the page select address register to be reset to zero and the corresponding page to be selected.

2.1.46 – PS, PAGE SELECT
The input on a page select memory that, when true, causes one of the pages of memory to be selected as identified by the inputs on the DQ pins (as defined in the appropriate function table) and for this page address to be stored in an internal register.

2.1.47 – Q(n)(x), DATA OUTPUT
The outputs whose state represents the data read from the selected cells. When the device is not selected or enabled, the outputs are usually in a floating (Z, high impedance) state. When the numbering of the data outputs is significant for device operation, the data outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.48 – RA, ROW ADDRESS INPUT
In an address multiplexed DRAM, the address field that is captured by the ROW ENABLE signal, RAS\. When the numbering of the row address numbering is significant for device operation, the RA are numbered beginning with 0

2.1.49 – RAS, (RE) ROW ENABLE INPUT
A chip enable signal that, on certain dynamic RAMs, actuates only row address oriented internal circuitry. In modules that have multiple RAS\s, the RAS\s are numbered beginning with 0.

2.1.50 – RC, RECALL
The input on a NVRAM, that transfers the non–volatile data into the RAM array.

2.1.51 – RFU, RESERVED FOR FUTURE USE
A terminal whose function is not currently defined, but which is intended to be defined in some future enhancement of this Standard. This terminal should not be used (either internally or externally) until it has been further defined.

2.1.52 – RSVD, RESERVED
In a family of standards where some devices in the family are subsets of others, terminals that are defined in some devices but not used in others. To allow for upgradeability, the unused terminals are "RESERVED" to prevent their being used. NC has often been used in similar situations.

2.1.53 – RY, READY
The output that, on some devices, signifies that no internal asynchronous operations are still in process, and that the device is available for normal functions. This signal is normally implemented so that multiple devices can be OR–tied. This signal is the inverse of BY ($RY=\overline{BY}$)

2.1.54 – S(n)(x), CHIP SELECT
The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption. When deselected, the outputs go to the inactive state (floating (Z) for MOS and TTL devices and low (L)

for ECL devices), and the device becomes insensitive to a write command. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.55 – ST, STORE

The input, on a NVRAM, that initiates the non–volatile data storage of the entire RAM array.

2.1.56 – Sxx, SYNCHRONOUS FUNCTION

On a synchronous memory device, any input terms that are synchronous with a clock should start with the letter S. For example: $\overline{SG}$ = Synchronous Output Enable, $\overline{SW}$ = Synchronous Write Enable.

2.1.57 – $\overline{TF}$, TEST FUNCTION

The input, on a MEMORY that, when true, causes built in on–chip test logic to be actuated and for the part to go into its test mode of operation.

2.1.58 – U, UPPER BYTE

When U is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. UW).

2.1.59 – UB, UPPER BYTE ENABLE

An input that, on wordwide devices, when true, enables the upper byte data input/outputs, pins DQ8 through DQ15.

2.1.60 – UW, UPPER BYTE WRITE ENABLE

An input, on wordwide devices, that, when true, causes the data present on the upper byte input/output, terminals DQ8 through DQ15, to be written into the addressed cells of the device.

2.1.61 – WE, W, WRITE ENABLE

The input that, when true, causes the data present on the D or the DQ pin(s) to be written into the address cell(s) of the device. In devices that have a WE per byte, the WEs are designated LWE & UWE for 2 byte devices. In devices that have a WE per byte and more that two bytes, the WE are numbered beginning with 0. In modules that have multiple WEs, the WEs are numbered beginning with 0.

2.2 MULTIPORT DRAM PIN NAMES

The following pin names apply primarily to specialized function pins for MPDRAM. In some situations, the names may also be applicable to other types of memories such as Graphics DRAMs.

2.2.1 – DSF, SPECIAL FUNCTION ENABLE INPUT

The input on a device, that when true, actuates certain special operational functions. In devices and modules that have multiple DSFs, the DSFs are numbered beginning with 0.

2.2.2 – DT/$\overline{OE}$(n), $\overline{TRG}$(n), DATA TRANSFER/OUTPUT ENABLE INPUT

The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

2.2.3 – QSF, QSY, TRANSFER ACKNOWLEDGE OUTPUT

The output on a device having both serial and parallel access ports which signifies that a transfer of data from the parallel to the serial port, in certain special transfer cycles, has been completed. In devices and modules that have multiple QSFs, the QSFs are numbered beginning with 0.

2.2.4 – SC, SERIAL CLOCK

An input, on devices having a serial data access port, that actuates the serial transfer of data, either in or out.

2.2.5 – SDQ(n)(x), SERIAL DATA INPUT/OUTPUT

The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode and as serial data inputs(s) when in the write mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data input/outputs is significant for device operation, the serial data input/outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.2.6 – SE, SERIAL PORT ENABLE

The input that, when true, actuates the device's serial access circuitry.

2.2.7 – SG, SERIAL PORT OUTPUT ENABLE

The input that, when true, actuates the device's serial data output circuitry.

2.2.8 – SQ(n), SERIAL DATA OUTPUT

The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode, When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data outputs is significant for device operation, the serial data outputs are numbered beginning with 0.

2.2.9 – $\overline{TRG}$(n), DT/$\overline{OE}$(n) DATA TRANSFER/OUTPUT ENABLE INPUT

The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

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2.3 POWER PIN NAMES

The following symbols are used to designate the power pins in a memory device. When only a single pin is provided for a given supply, the pin name is used without suffix. When multiple pins are used, a suffix may be used to designate specific pins. A numeric suffix is used to indicate the preferred order of implementation when optional redundant pins are allowed. An alphabetic suffix is used to indicate pins which have a specific power circuit or loop connection. The use of a common suffix for different supplies indicates that those pins connect to a common power loop.

2.3.1 – VBB, SUBSTRATE POWER VOLTAGE

A bias voltage that maintains the substrate at a potential which is negative with respect to GND or VSS in an NMOS or CMOS part.

2.3.2 – VCC, LOGIC POWER VOLTAGE

The most positive potential of the two logic power supply pins. This is used for the memory device power voltage when the supply voltage is nominally 5 V. VCC is also commonly used to designate the ground reference power supply voltage for ECL interface devices.

2.3.3 – VCCQ, OUTPUT STAGE LOGIC POWER VOLTAGE

See VDDQ for definition. VCCQ is restricted to 5 V applications only

2.3.4 – VDD, DRAIN POWER VOLTAGE

The primary power voltage on MOS devices that require a potential that is different from the normal system logic voltage. This is used interchangeably with VCC on devices that use 5 V.

2.3.5 – VDDQ, OUTPUT STAGE DRAIN POWER VOLTAGE

The power pin that is intended to feed power to the output transistors of the device to supply the potential and energy to drive the load applied to the data output (Q) pins or data input/output (DQ) pins. Other, non–data, output pin transistors may also be designated to be fed by this power pin. VDDQ/VCCQ may be specified to have the same or a different potential from that feeding the primary device power pins (VDD/VCC) but is DC isolated on the chip from these and any other chip power pins.

2.3.6 – VEE, EMITTER POWER VOLTAGE

For ECL interface devices, the primary and most negative power supply terminal.

2.3.7 – VHH, SPECIAL FUNCTION ENABLE VOLTAGE

A special high voltage logic level (super voltage) that enables special on–chip functions.

2.3.8 – VPP, PROGRAMMING POWER VOLTAGE

A special high voltage supply that supplies the potential and energy for altering the state of certain non–volatile memory arrays. On some devices the presence of VPP also acts as a PROGRAM ENABLE signal (see P).

2.3.9 – VREF, REFERENCE POWER SUPPLY

A power supply that acts as a reference for determining internal threshold voltages but does not supply any substantial power to the device.

2.3.10 – VSS, (GND), GROUND REFERENCE or SOURCE POWER VOLTAGE

The ground reference voltage for NMOS, CMOS, and TTL devices, commonly the reference pin for all other device pins. VSS is normally the system ground and the symbol is often used interchangeably with GND.

2.3.11 – VSSQ, (GNDQ), OUTPUT STAGE SOURCE POWER VOLTAGE or OUTPUT STAGE GROUND REFERENCE

The ground reference voltage for the data output (Q) or input/output (DQ) pins. Other, non–data, output pin transistors may also be designated to be referenced to this ground pin. Internal to the device, this pin shall be DC isolated from the primary ground reference (VSS) pin and any other ground reference pin. External to the device it must be DC common with the primary ground reference.

2.4 DEVICE TYPE NAMES

2.4.1 – ASIC, Programmable Application Specific Device

A complex array of logic elements whocs interconnection pattern can be field programmed to fill the needs of specific applications.

2.4.2 – BDRAM, Burst DRAM

A DRAM that has BURST mode data capability.

2.4.3 – Bxxx,

Device names that have the prefix "B" are devices that have a "Burst" data capability.

2.4.4 – DPM, Dual Port Memory

Any memory that has two essentially identical data ports.

2.4.5 – DPSRAM, Dual Port Static RAM

A static RAM that contains two sets of identical random access address and data ports.

2.4.6 – DRAM, Dynamic Random Access Memory

These devices are made using Dynamic RAM circuit configurations that have data storage that must be refreshed periodically.

2.4.7 – FEEPROM, Flash EEPROM

An EEPROM in which clearing can be performed only on blocks or the entire array.

Note: there are no restrictions on the block archetecture in the fefinition of FEEPROM. the blocks within a device may be of various capacities ranging from a single address to the entire memory array.

2.4.8 – EEPROM, Electrically Erasable Programmable Read Only Memory

A reprogammable ROM in which cells may be erased electrically and in which each cell may be reprogrammed electrically.

2.4.9 – EPROM, Erasable Programmable Read Only Memory

A reprogrammable ROM in which all cells may be simultaneously erased using ultraviolet light and in which each cell may be reprogrammed electrically.

2.4.10 – GRAM, Gaphics DRAM

A DRAM that contains special graphics features, similar to those contained in a MPDRAM. When the term has a prefix "S", it becomes synchronous GRAM.

2.4.11 – LPROM, Latched PROM

A PROM that contains a latch register for the output data.

2.4.12 – MPDRAM, Multiport DRAM

A dynamic RAM that contains in addition to the conventional random access data and address port, a serial access port that allows serial access to a portion of the stored data in a way which is independent of the normal RAM data terminals and in which simultaneous serial and random operations may be executed. This type of memory has been referred to as "Video RAM" because of its primary field of application.

2.4.13 – MPM, Multiport Memory

Any memory array that has two or more data ports which do not have the same architecture. The most common form of MPM is one in which there is a random access port and a serial access port.

2.4.14 – MPRAM, Multiport RAM

A RAM that has more than one port for data, address, and control, that are not identical in nature. Normally at least one port provides parallel access while one other provides serial access. When the term has a prefix "S", it becomes s synchronous MPDRAM.

2.4.15 – NVRAM, Non–Volatile Random–Access Memory

An SRAM in which provisions exist on chip for the state of the cells to be saved when power is removed.

2.4.16 – PLD, Programmable Logic Array

An array of logic elements in which the interconnection pattern can be programmed (either mask or user programmed) to perform specific logic functions.

2.4.17 – PROM, Programmable Read–Only Memory

A field programmable ROM which can have the data content of each cell altered only once.

2.4.18 – PSRAM, Pseudo Static Random–Access Memory

A combinational form of dynamic RAM that incorporates various refresh and control circuits on–chip (e.g. refresh address counter and multiplexer, interval timer, and/or arbiter). These circuits allow the PSRAM operating characteristics to closely resemble those of a SRAM.

2.4.19 – RAM, Random–Access Memory

A memory in which access to all storage data can be achieved in essentially the same time, independent of the location. In a multiport memory, this term refers to that portion of the array which contains the memory cell array and its drivers, sense amplifiers, and control circuitry and the circuitry associated with the normal random access data port.

2.4.20 – ROM, Read–Only Memory

A memory in which the contents are not intended to be altered during operation.

2.4.21 – RPROM, Registered PROM

A PROM that contains a "D" type FF register for the output data.

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2.4.21 – Sxxx

The prefix "S" on a device term can mean either "Static" as in SRAM, "Serial" as in SAM, or "Synchronous" as in SDRAM and SGRAM.

2.4.22 – SAM, Serial Access Memory

A memory (or serial port in a multiport memory) in which data is accessed sequentially and the time for access depends on the location of the data desired. In a multiport memory, this term refers to that portion of the device which is related to the serial access port and its associated functions.

2.4.23 – SDRAM, Synchronous DRAM

A DRAM that has a clocked synchronous interface.

2.4.24 – SGRAM, Synchronous Graphics DRAM

A GRAM that has a synchronous interface.

2.4.25 – SMPDRAM, SVRAM, Synchronous MPDRAM (VRAM)

An MPDRAM that has a synchronous interface on all ports.

2.4.26 – SRAM, Static Random Access Memory

A read/write memory in which the data is retained in the absence of control signals generated inside or outside the integrated circuit.

2.4.27 – SSRAM, Synchronous Static RAM

An SRAM that has input and/or output buffers (either register or latch), that are controlled by an externally supplied clock (or clocks).

2.4.28 – VRAM, Video Ram

A term commonly used in the Industry to describe the device class referred to in this standard as MPDRAM. It is a multi–ported DRAM that has features keyed to the video buffer application

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2.5 MISCELLANEOUS DEVICE RELATED TERMS

2.5.1 – Bit Plane
In a semiconductor memory device having a data interface that is wider than 1 bit, those storage cells and associated circuitry which are associated with a given bit in the data interface.

2.5.2 – Bit Wide
A class of memory devices that have only a single–bit data interface.

2.5.3 – Byte Wide
A class of memory devices that have a parallel 8–bit or occasionally 9–bit data interface.

2.5.4 – K
When describing the storage capacity of a memory device the quantity K=1024 is used.

2.5.5 – M
When describing the storage capacity of a memory device, the quantity M=2 exp 20 or 1024 K is used.

2.5.6 – MX, Multiplexed
A term describing a device that has pins used for different purposes at different times as a function of one or more of its control inputs. The signal groups that are multiplexed onto a common pin set are given together as in: AA MX signifying ADDRESS, ADDRESS multiplex, OR ADQ MX signifying ADDRESS, DATA IN, DATA OUT multiplex.

2.5.7 – Nibble Wide
A class of memory devices that have a parallel 4–bit data interface. This term should not be confused with “nibble mode” (see 3.1.3.2), which refers to a serial data access mode in memories.

2.5.8 – Word Wide
A class of memory devices that have a parallel 16–bit or longer data interface.

2.6 Special Operational Cycles for MPDRAM

The following terms describe a series of special operational cycles for MPDRAM. They are presented in the order of their logical relationships rather than alphabetically.

2.6.1 LOGIC SETUP, (LS)

A special non-memory cycle in which the logic state of the device is set up to actuate the desired mode of operation for future memory cycles. The selected mode is normally persistent until canceled by some subsequent special control cycle.

2.6.2 INTERNAL REFRESH, (CBR)

Defined in 3.9.2.3.

2.6.3 WRITE TRANSFER, (WT)

An operation in which the data to be written is introduced through the serial port and is then transferred internally to the memory array data bus for writing into the cells. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial register into which data is entered. Data is entered serially from this point with wrap around when the end of the register is reached. The contents of the full serial register are transferred in parallel. In addition to the normal write transfer, there are numerous other types of special write transfers defined in the following paragraphs.

2.6.4 PSEUDO WRITE TRANSFER, (PWT)

This is a non-memory cycle in which the operational mode of the serial port is changed from output to input. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial data register into which data is entered. Data is entered serially from this point with wrap around when the end is reached.

2.6.5 MASKED WRITE TRANSFER, (MWT)

A write transfer in which the transfer of new data from the serial register into the memory array is controlled by a "Write Mask" that is supplied on the DQ(n) terminals. This mask allows the selective writing of new data into one or more of the data bit planes of the storage array corresponding to the data bits of the parallel array. In a normal implementation, a high M value enables the writing of new data while a low M inhibits the writing and leaves the existing data unchanged. A new mask value must be supplied for each masked write cycle.

2.6.6 FLASH WRITE WITH MASK, (FWM)

A write cycle in which the contents of an entire row of the memory array can be selectively set to a stated value. The "mask" value determines which bit planes are to be altered while the "color register" (qv) contains the data value to be written. The color register is loaded in a previous "Load Color Register" cycle with a persistent value. The mask value is supplied during the cycle on the DQ(n) terminals. A new mask value must be supplied for each cycle performed. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.7 SPECIAL WRITE TRANSFER

A write transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal SAM to RAM data transfers. These variations are defined in the following paragraphs.

2.6.8 SPLIT WRITE TRANSFER, (SWT)

A write transfer in which the SAM data register is split into two halves and the data is transferred to the RAM data bus separately after each half of the SAM register is filled.

2.6.9 AUTO-LOAD WRITE TRANSFER, (AWT)

A split SAM data register transfer in which the transfer from each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is filled.

2.6.10 READ TRANSFER, (RT)

A read operation in which the contents of one row of the memory array is transferred into the SAM data register in parallel.

2.6.11 SPECIAL READ TRANSFER

A read transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal RAM to SAM data transfers. These variations are defined in the following paragraphs.

2.6.12 SPLIT READ TRANSFER, (SRT)

A read transfer in which the SAM data register is split into two halves and the data is transferred from the RAM data bus separately into each half of the SAM register as it is needed for transfer to the SDQn terminals.

2.6.13 AUTO-LOAD READ TRANSFER, (ART)

A split SAM data register transfer in which the transfer into each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is emptied.

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3.5.1.10 - 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
PACKAGE--32 LEAD TSOP-1, 8 mm X 18.4 mm
PIN ASSIGNMENT--Fig. 3.5.1-10

3.5.1.11 - EXTENDED FEATURE SET FOR 256K BIT EEPROM

This standard specifies features beyond the existing pinout standards that need to be standardized for 32K X 8 EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.1..

3.5.1.11.1 - REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 32K Byte EEPROMs and must be implemented to be in compliance with this standard:

-Operate with a primary power supply of 5.0 V nominal
-Operate in conformance with the standard truth table
-Have read and write timing cycles which are consistent with the standard timing diagrams
-Contain Data & Address Latches for Write cycles
-Operate with self timed write cycles
-Operate with input levels between 0 and 5 Volts.

3.5.1.11.2 - OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:

-Page Write Mode with standard write cycle timings
-Minimum page size of 16 Byte in page write mode
-DATA\ Polling
-Software Data Protect Option
-Hardware Mass Erase (All 1's)
-Software Mass Erase (All 1's)

3.5.1.12 - OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM

This Standard provides an optional command set for DUAL-SUPPLY EEPROM devices (commonly known as FLASH EEPROM). This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.2-4

3.5.1.13 - 512K BY 8 DUAL-SUPPLY EEPROM IN RCC

CAPACITY--512K WORDS OF 8 BITS,
PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
PIN ASSIGNMENT--Fig. 3.5.1-12

3.5.1.14 - 128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP-1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
THESE DEVICES ARE APPROVED IN THREE PACKAGES:
DIP PACKAGE--32 LEAD DIP, 15.24 mm (0.6") WIDE WITH 2.54 mm (0.1") PP
PIN ASSIGNMENT--Fig. 3.5.1-13
RCC PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
PIN ASSIGNMENT--Fig. 3.5.1-14
TSOP-1 PACKAGE--32 LEAD TSOP-1, 8 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT--Fig. 3.5.1-15

3.5.1.15 – 256K, 512K, & 1M BY 8 DUAL–SUPPLY EEPROM IN TSOP–1

CAPACITY—256K, 512K, 1M WORDS OF 8 BITS,
PACKAGE—40 LEAD TSOP–1, 10 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT—256K, 512K, Fig. 3.5.1–18
PIN ASSIGNMENT—1M, Fig. 3.5.1–16

The 256K & 512K devices have a different pin assignment pattern from the 1M device, therefor are not backward compatible with the 1M device.

3.5.1.16 – 1M TO 8M BY 8 SINGLE–SUPPLY EEPROM FAMILY IN TSOP–1

CAPACITY—1M, 2M, 4M, & 8M WORDS OF 8 BITS,
PACKAGE—48 LEAD TSOP1, 12 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–17

3.5.1.17 – 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP–2

CAPACITY—8K WORDS OF 256 OR 264 BYTES, SERIALLY ACCESSED
PACKAGE—44/40 LEAD TSOP2, 10.16 mm WIDE WITH 0.8 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–19 A
CONTROL & LOGIC TABLES—Figs. 3.5.1–19 B & C

3.5.1.18 – 1M & 2M BY 8 SINGLE OR DUAL SUPPLY EEPROM FAMILY IN PSOP

CAPACITY—1M & 2M WORDS OF 8 BITS,
PACKAGE—44 LEAD PSOP 16 mm wide WITH 1.27 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–20

N.3

Logic Table

Function	CL	AL	$\overline{E}$	$\overline{W}$	$\overline{R}$	$\overline{WP}$
Command Input	H	L	L	⎺↓⎽⎽⎽⎺	H	·
Data Input	L	L	L	⎺↓⎽⎽⎽⎺	H	·
Address Input	L	H	L	⎺↓⎽⎽⎽⎺	H	·
Address Output	L	H	L	H	⎺↓⎽⎽⎽⎺	·
Serial Read & Output	L	L	L	H	⎺↓⎽⎽⎽⎺	·
During Auto Program	·	·	·	·	·	H
During Auto Erase	·	·	·	·	·	H
During Busy State	·	·	·	·	·	H
Program/Erase Protect	·	·	·	·	·	L

Serial Address Input

	ADQ0	ADQ1	ADQ2	ADQ3	ADQ4	ADQ5	ADQ6	ADQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	A15
3rd Cycle	A16	A17	A18	A19	A20	RFU	RFU	RFU

A0 ⇒ A7 : Column Address
A8 ⇒ A11 : NAND Address
A12 ⇒ A20 : Block Address

PIN DEFINITIONS

The following pin terms are used in this device, but some may not appear in Sec. 2 on terminology of this Standard,

CL:	Command Latch Enable	AL:	Address Latch Enable
$\overline{E}$:	Chip Enable	$\overline{W}$:	Write Enable
$\overline{R}$:	Read Enable	$\overline{WP}$:	Write Protect
RY:	Ready	ADQn:	Address/Data/Command Multiplex

FIGURE 3.5.1-19 C
8K BY 256B or 8K BY 264B SERIAL ACCESS EEPROM LOGIC TABLE

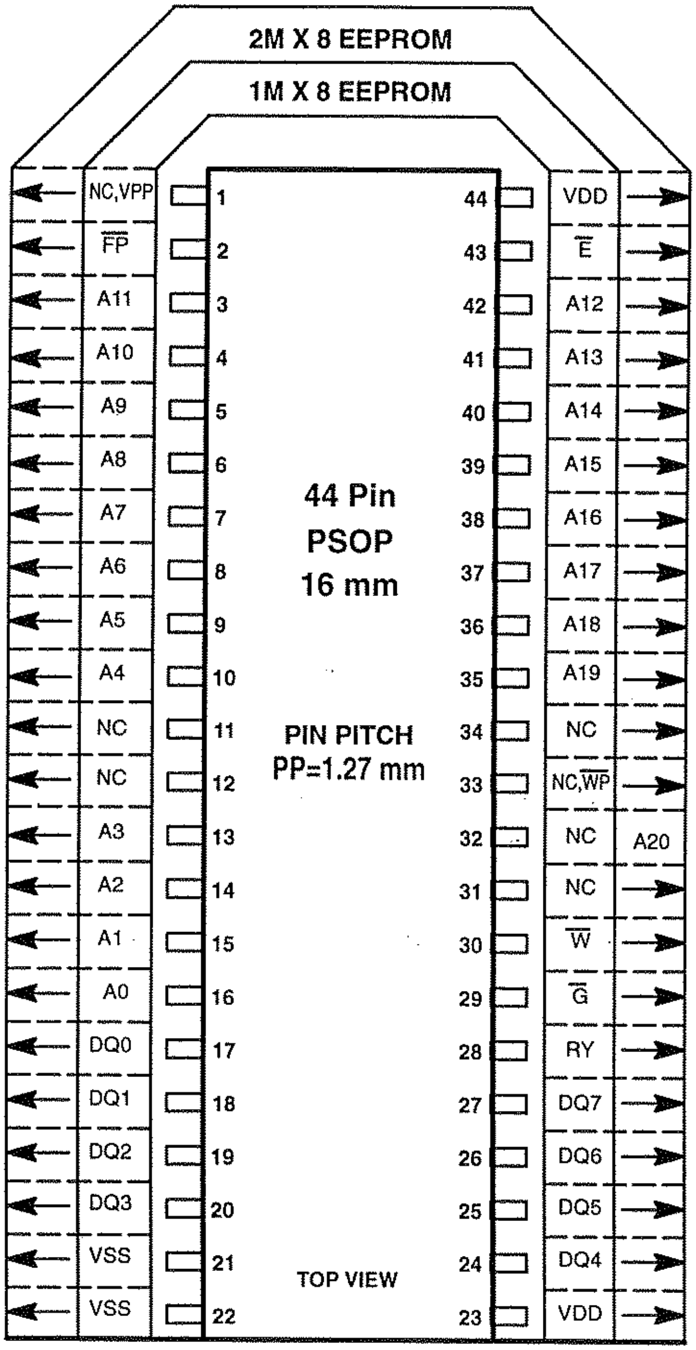


FIGURE FIGURE 3.5.1-20
1M & 2M BY 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP

3.5.2.1 – 4K TO 32K BY 16 EEPROM IN DIP

CAPACITY—4K TO 32K WORDS OF 16 BITS,
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.5.2-1

3.5.2.2 – 4K TO 256K BY 16 EEPROM IN SCC

CAPACITY—4K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.5.2-2

3.5.2.3 – 256K TO 128M BY 16 EEPROM IN DIP AND SOP

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, 64M, and 128M WORDS OF 16 BITS
PACKAGE—44, 48 or 52 PIN DIP and SOP, 0.600" WIDE
PIN ASSIGNMENTS—256K TO 2M, Fig. 3.5.2-4
PIN ASSIGNMENTS—4M TO 128M, Fig. 3.5.2-3

3.5.2.4 – 1M TO 4M BY 16 DUAL SUPPLY EEPROM IN SSOP

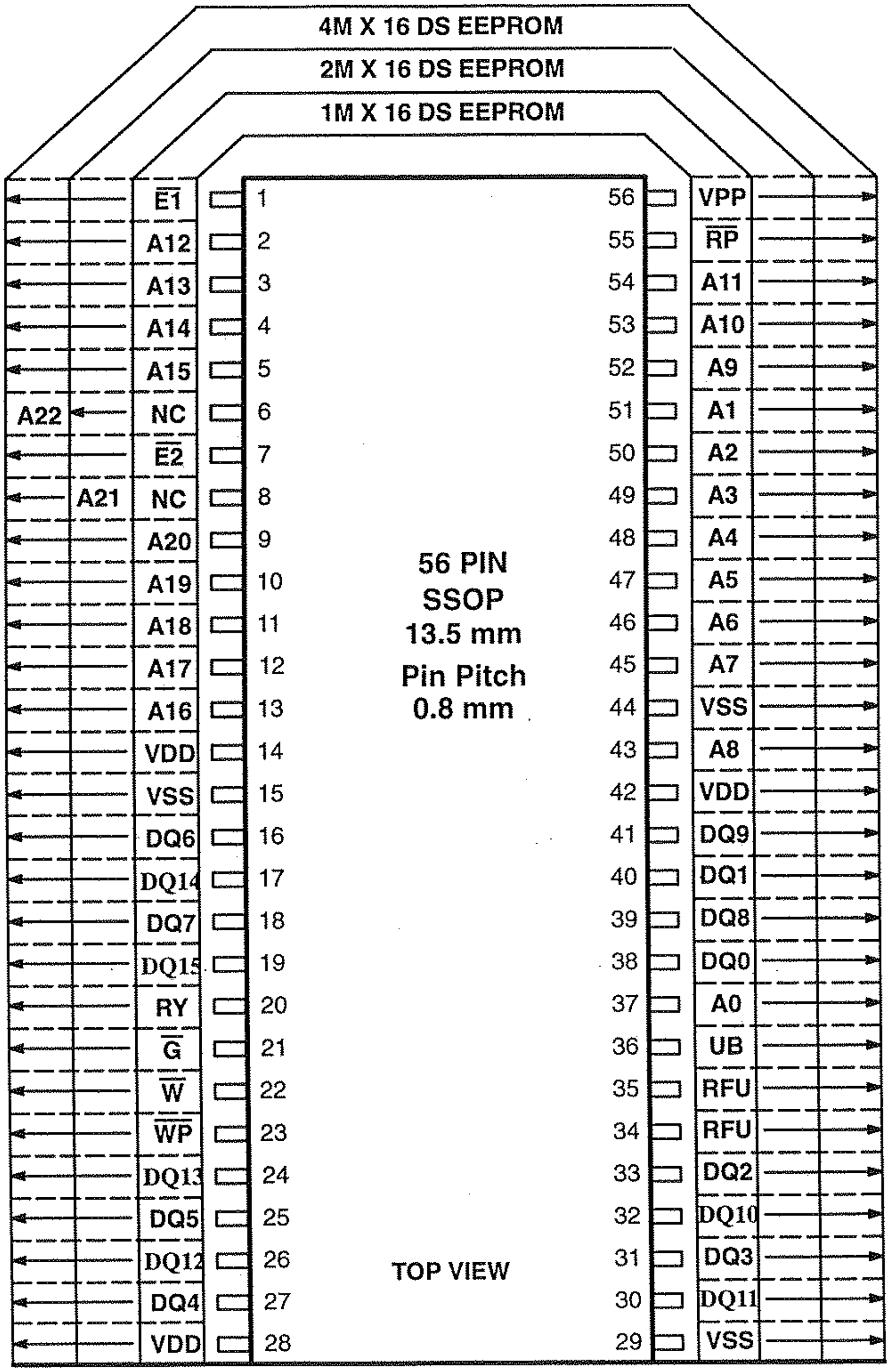
CAPACITY—1M, 2M, 4M WORDS OF 16 BITS,
PACKAGE—56PIN SSOP, 13.5 mm WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENTS—Fig. 3.5.2-5

3.5.2.5 – 1M, 2M, & 4M DENSITY, BY 8 & 16 FEEPROM IN PSOP

CAPACITY—1M, 2M, & 4M, BITS WITH x8 OR x16 DATA INTERFACE.
—128K, 256K, OR 512K WORDS OF 8 BITS
—64K, 128, OR 256K WORDS OF 16 BITS
PACKAGE—44 PIN PSOP, 16 mm WIDE
PIN ASSIGNMENTS—Fig. 3.5.2-6
POWER SUPPLIES—SINGLE OR DUAL SUPPLY DESIGN

3.5.2.6 – 1M TO 32M DENSITY, BY 8 & 16 FEEPROM IN TSOP1

CAPACITY—1M, 2M, 4M, 8M, 16M, & 32M BITS WITH x8 OR x16 DATA INTERFACE.
—128K, 256K, 512K, 1M, 2M, OR 4M WORDS OF 8 BITS
—64K, 128, 256K, 512K, 1M, OR 2M WORDS OF 16 BITS
PACKAGE—44 PIN TSOP1, 20 mm X 16 mm with 0.5 mm PP.
PIN ASSIGNMENTS—Fig. 3.5.2-7
POWER SUPPLIES—SINGLE OR DUAL SUPPLY DESIGN



	UB	A0	DQ0 ⇒DQ7	DQ8⇒DQ15
Word Access	VIH	X	Even Byte	Odd Byte
Odd Byte Access	VIL	VIH	Odd Byte	High Z
Even Byte Access	VIL	VIL	Even Byte	High Z

FIGURE 3.5.2–5
1M TO 4M BY 16 DUAL SUPPLY EEPROM IN SOP

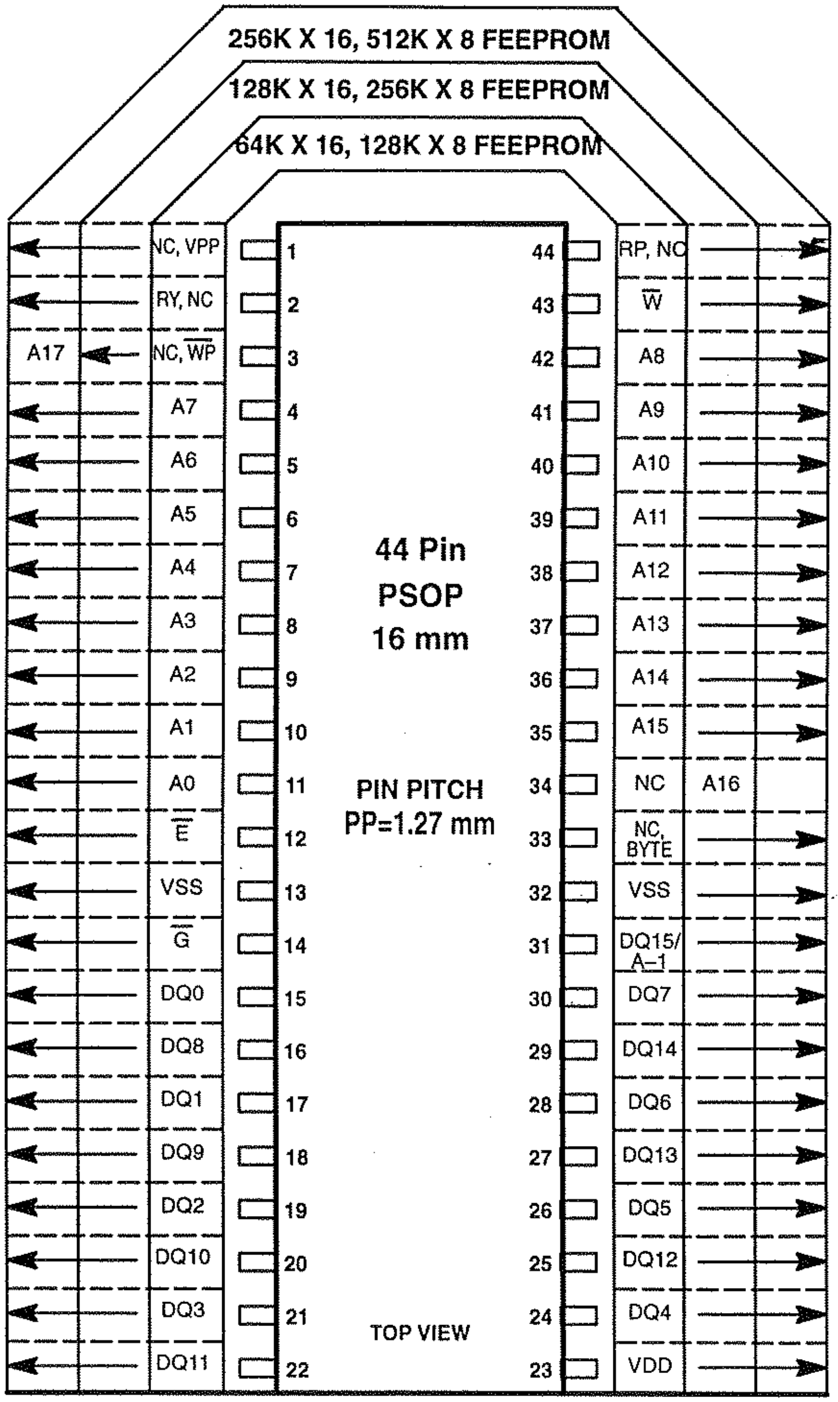
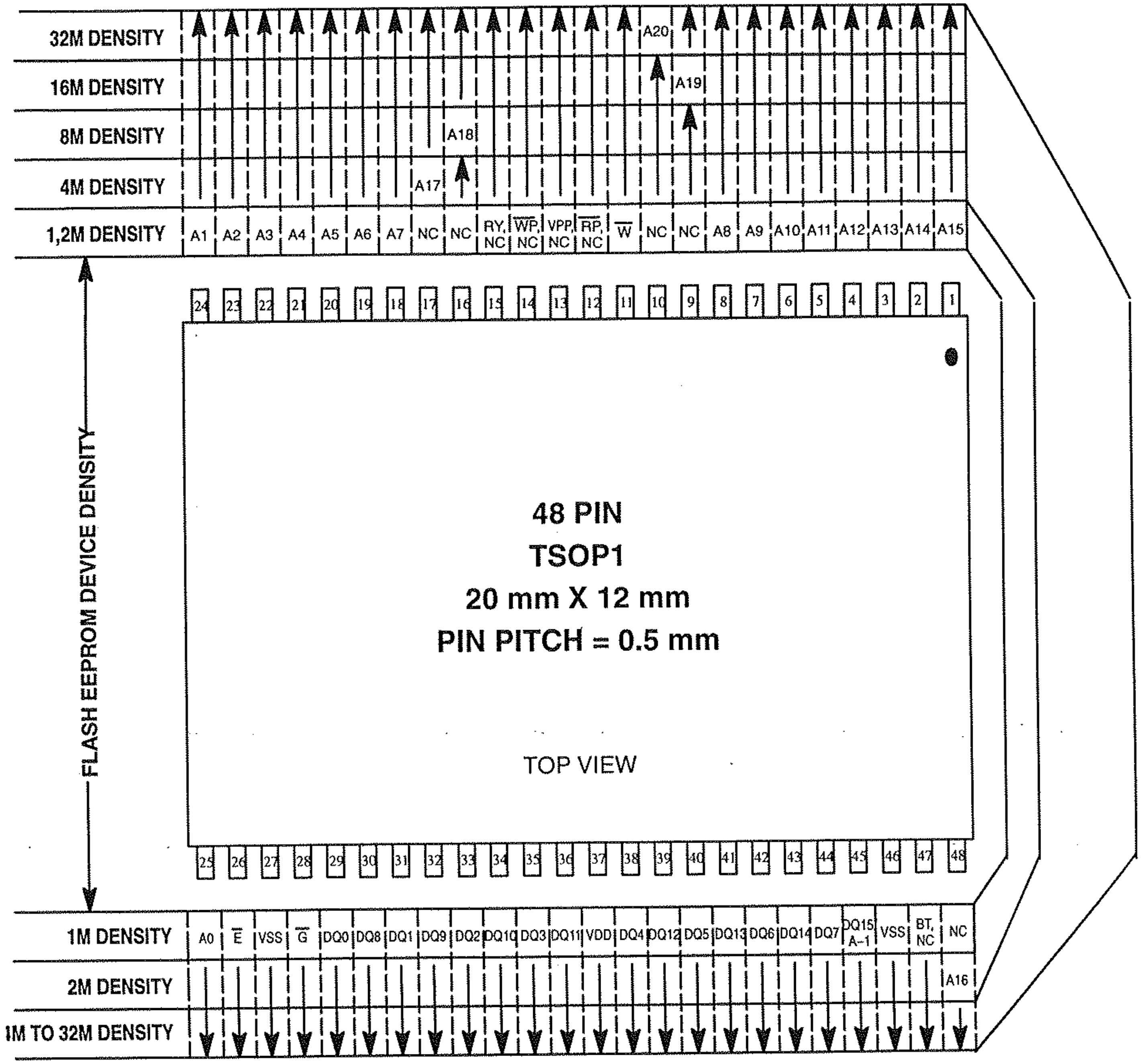


FIGURE 3.5.2-6
1M, 2M, & 4M DENSITY BY 8 & 16 SINGLE OR DUAL SUPPLY FEEPROM IN PSOP, 128K TO 512K BY 8 OR 64K TO 256K BY 16



ORGANIZATION VS. DENSITY TABLE

DENSITY	X16	X8
1Mb	64K X 16,	128K X 8
2Mb	128K X 16	256K X 8
4Mb	256K X 16	512K X 8
8Mb	512K X 16	1M X 8
16Mb	1M X 16	2M X 8
32Mb	2M X 16	4M X 8

FIGURE 3.5.2-7
1M TO 32M DENSITY BY 8 & 16 SINGLE OR DUAL SUPPLY FEEPROM IN TSOP1, 64K TO 2M BY 16 OR 128K TO 4M BY 8

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3.5.3 EEPROM EXTENDED FEATURES

There are a number of extended feature standards for EEPROMS that depend on the capacity and number of power supplies used in the design. The various standards and their location are listed as follows:

- 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARDS. PP 3.5.1–15 to 22
- DUAL POWER SUPPLY EEPROM COMMAND SET. Fig. 3.5.3.2, P 3.5.3–13
- EXTENDED FEATURE SET FOR EEPROM (256Kb and larger) . Sec. 3.5.3.1 following
- SINGLE POWER SUPPLY EEPROM COMMAND CODES. SEC. 3.5.3.3
- EEPROM TOGGLE BIT FEATURE (larger than 256 Kb) . Sec. 3.5.3.4

3.5.3.1 – EXTENDED FEATURE SET FOR EEPROM (256Kb and larger)

This standard specifies features beyond the existing pinout standards that need to be standardized for EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.3.2

3.5.3.1.1 – REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 256Kb and larger EEPROMs and must be implemented to be in compliance with this standard:
–Operate with a primary power supply of 5.0 V and lower nominal
–Operate in conformance with the defines standard command set
–Operate in conformance with the standard truth table
–Have read and write timing cycles which are consistent with the standard timing diagrams
–Contain Data & Address Latches for Write cycles
–Operate with self timed write cycles
–Operate with input levels between 0 and 5 Volts.
–DATA\ Polling

3.5.3.1.2 – OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:
–Page Write Mode with standard write cycle timings
–Minimum page size of 16 Byte in page write mode
–Software Data Protect Option
–Hardware Mass Erase (All 1's)
–Software Mass Erase (All 1's)

3.5.3.2 – OPTIONAL COMMAND SET FOR DUAL–SUPPLY EEPROM

This Standard provides an optional command set for DUAL–SUPPLY EEPROM devices. This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.1–11

3.5.3.3 – SINGLE POWER SUPPLY EEPROM COMMAND CODES

These tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

3.5.3.4 – EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies. The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

EEPROM EXTENDED FEATURE STANDARD (256Kb and greater)

The mandatory features, which are the minimum set necessary to achieve functional compability for 256Kb and larger EEPROMs, must be implemented to be in compliance with this standard. Any, all, or none of the optional features may be implemented at the manufacturers discretion. However, if an optional feature defined in this standard is implemented, it must operate as specified in this standard to be in compliance with the standard.

Other features not described in the standard may be incorporated and the device still be in compliance as long as they are compatible with the required and optional features in this standard.

BYTEWIDE EEPROM REQUIRED STANDARD FEATURES (256Kb and larger)

1. VDD SUPPLY IS 5 V OR LESS NOMINAL
2. STANDARD LOGIC TRUTH TABLE (FIG. A1–1)
3. STANDARD COMMAND SET (Fig. A1–2)
4. STANDARD READ CYCLE TIMING (FIG. A1–3)
5. STANDARD BYTE WRITE CYCLE FEATURES
   –TIMING (FIG. A1–4)
   –DATA AND ADDRESS LATCHES
   –SELF–TIMED WRITE CYCLES
   –ALL INPUT LEVELS IN RANGE BETWEEN 0 V AND 5 V.
6. DATA POLLING (FIG. A1–5)
   MUST MEET NORMAL READ CYCLE AND WRITE CYCLE TIMING

OPTIONAL FEATURES

1. PAGE WRITE MODE (FIG. A1–6)
   –STANDARD PAGE WRITE CYCLE TIMING
   –16 BYTE MINIMUM PAGE SIZE (A0 – A3)
2. SOFTWARE DATA PROTECT OPTION (FIGS. A1–7 & A1–8)
3. HARDWARE MASS ERASE (ALL 1'S) (FIG. A1–9)
4. SOFTWARE MASS ERASE (ALL 1'S) (FIG. A1–10)

EEPROM TRUTH TABLE					
$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
L	L	H	READ	Q	ACTIVE
L	H	L	WRITE	D	ACTIVE
H	X	X	STANDBY AND WRITE INHIBIT	HIGH Z	STANDBY
L	L	L	WRITE INHIBIT	HIGH Z	ACTIVE
L	H	H	WRITE INHIBIT	HIGH Z	ACTIVE

~NOTE: $\overline{G}$ functions as both an output control and a write Inhibit control in this EEPROM Standard.

FIGURE A1–1

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SINGLE–SUPPLY EEPROM COMMAND SET

Bus Command Table

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	FOH										
Reart/Reset	4	5555H	AAH	2AAAH	55H	5555H	FOH	RA	RD				
Autoselect	4	5555H	AAH	2AMH	55H	5555H	90H						
Fyte Program	4	5555H	AAH	2AMH	55H	5555H	AOH	PA	Data				
Chip Erase	6	5555H	AAH	2AMH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	1OH
Sector Erase	6	5555H	AAH	2AMH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don~t rare), Data (BOH)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don~t care), Data (30H)											

Note: A0 is always LSB regardless of data width.

FIGURE A1–2

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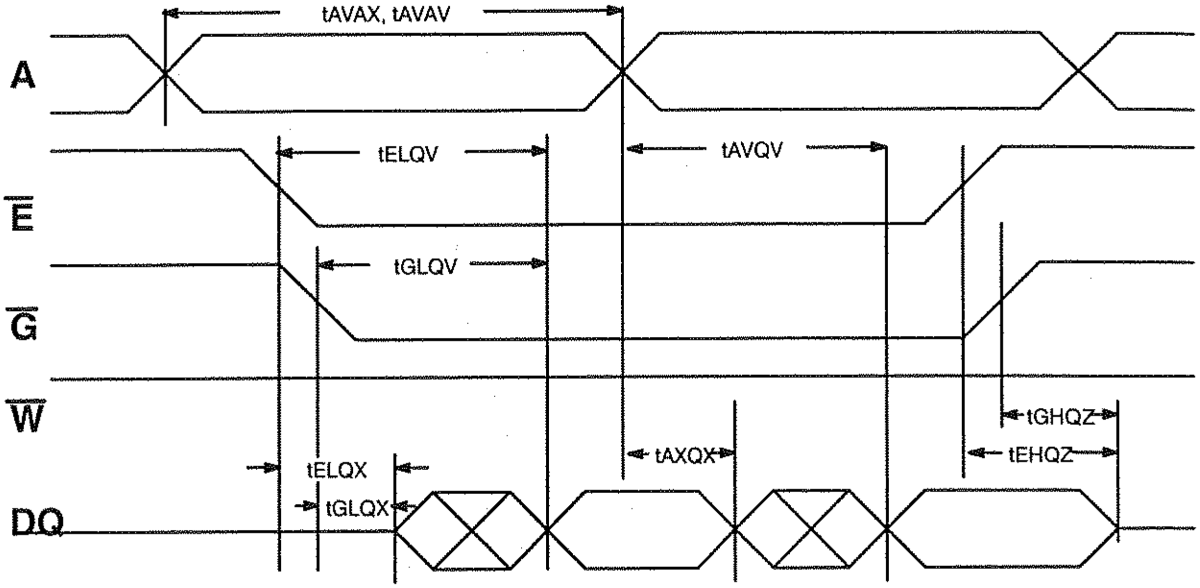
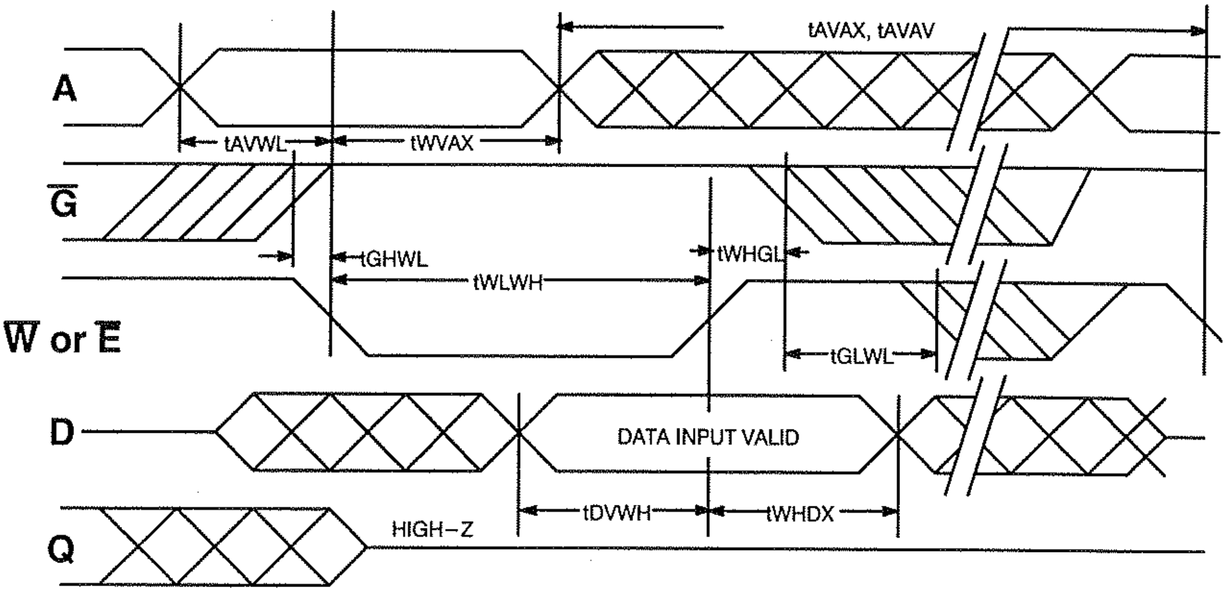
SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL	DESCRIPTION
tAVAX, tAVAV	ADDRESS VALID TO ADDRESS CHANGE (READ CYCLE TIME)
tELQV	E LOW TO OUTPUT VALID (CHIP ENABLE ACCESS TIME)
tAVQV	ADDRESS VALID TO OUTPUT VALID (ADDRESS ACCESS TIME) tGLQV
tELQX	E LOW TO ACTIVE OUTPUT
tGLQX	G LOW TO ACTIVE OUTPUT
tEHQZ	E HIGH TO HIGH-Z OUTPUT
tGHQZ	G HIGH TO HIGH-Z OUTPUT
tAXQX	ADDRESS INVALID TO DATA OUT INVALID

FIGURE A1-3

SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL (NOTE 1)	DESCRIPTION
tWLWL, tELEL	W̅ OR E̅ LOW TO W̅ OR E̅ LOW CYCLE TIME (WRIITE CYCLE TIME)
tAVWL, tAVEL	ADDRESS VALID TO W̅ OR E̅ LOW TIME (ADDRESS SETUP TIME)
tWLAX, tELAX	W̅ OR E̅ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	G̅ HIGH TO W̅ OR E̅ LOW TIME
tWHGL, tEHGL	G̅ HIGH HOLD TIME FROM W̅ OR E̅ HIGH
tWLWH, tELEH	W̅ OR E̅ LOW TO W̅ OR E̅ HIGH (WRITE PULSE DURATION)
tGLWL, tGLEL	G̅ LOW TO W̅ OR E̅ LOW (G̅ LOW WRITE INHIBIT SETUP TIME)
tDVWH, tDVEH	DATA INPUT VALID TO W̅ OR E̅ HIGH (DATA SET-UP TIME)
tWHDX, tEHDX	W̅ OR E̅ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1-4

SINGLE SUPPLY EEPROM DATA BAR POLLING AND AUTOMATIC WRITE OPERATION STATUS

IN PROGRESS	AUTO PROGRAMMING	DQ7	TOGGLE	0	0	0	RFU
	PROGRAMMING IN AUTO–ERASE	0	TOGGLE	0	0	1	
	ERASING IN AUTO–ERASE	0	TOGGLE	0	1	1	
EXCEEDED TIME LIMITS	AUTO PROGRAMMING	DQ7	TOGGLE	1	0	0	RFU
	PROGRAMMING IN AUTO–ERASE	0	TOGGLE	1	0	1	
	ERASING IN AUTO–ERASE	0	TOGGLE	1	1	1	

FIGURE A1–5

Definition of Automatic Algorithm

Automated Write
Data Command = 10h/ Byte Address and Data (1st/2nd bus cycle)

Write the automated program set–up command (10h) and program command (Byte address and program data). The device automatically times the program pulse width, provides the program verify to guarantee adequate data retention, and counts the number of pulses required for complete programming.

A data polling status bit (output pin DQ7) and a toggle bit status (output pin DQ6) provide feedback to the system as to the status of the programming operation. Either DQ7 or DQ6 can be used.

Data Polling– DQ7

While the automated algorithms are in operation, an attempt to read the device (address = don't care) will produce the compliment of the intended valid program or erase data on DQ7. Upon completion of the automated algorithm, an attempt to read the device will produce the valid data expected from DQ7.

The data polling feature is valid after the rising edge of the second W pulse of the two write pulse sequence.

Toggle Bit– DQ6

While the automated algorithms are in progress, successive attempts to read data (address = don't care) from the device will result in DQ6 toggling between the logic levels "1" and "O". Once the automated operation is complete, DQ6 will stop toggling and valid data will be read.

The toggle bit is valid after the rising edge of the first W pulse of the two write pulse sequence, unlike data polling which is valid after the rising edge of the second W pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

Exceeded Timing Limits – DQ5

DQ5 will indicate if the program or erase pulse counts have exceeded the specified limits. Under this condition, DQ5 will provide a logic "1 " output.

Hardware Sequence Flash – DQ4

If the device has exceeded the specified erase or program time and DQ5 is at logic level "1", then DQ4 will indicate which step in the algorithm the device exceeded limits. A logic level "O" in DQ4 indicates that the programming limits were exceeded. A logic level "1" indicates erase limits were exceeded.

Sector Erase Timer– DQ3

After the compietion of the initial sector erase command sequence, the sector erase time–out of 100µs will begin. If another sector erase command is written within the 100µs time–out window, the timer is reset.

If Data Polling or the Toggle bit (DQ6) indicates that the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is at logic level "1" the internally controlled erase cycle has begun. Any further attempts to write subsequent commands to the device will be ignored untilthe erase operation is completed which is indicated by Data Polling or the Toggle bit. If DQ3 is at logic level "0", the device will accept additional sector erase
commands.

DQ0–DQ2 are reserved for future use.

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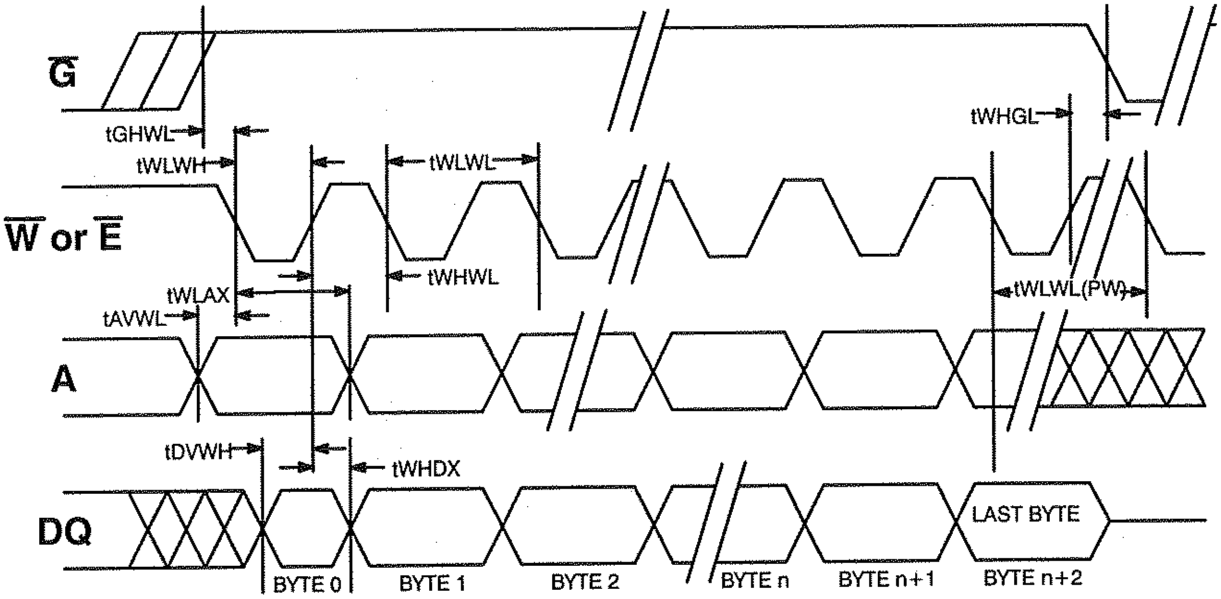
SINGLE SUPPLY EEPROM PAGE MODE WRITE CYCLE TIMING



SYMBOL (NOTE 1)	DESCRIPTION
tWLWL(PW)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW CYCLE TIME (PAGE WRIITE CYCLE TIME)
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SETUP TIME)
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	$\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME
tWHGL, tEHGL	$\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)
tWLWL, tELEL	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW (BYTE LOAD CYCLE TIME)

FIGURE A1–6

SINGLE SUPPLY EEPROM OPTIONAL SOFTWARE DATA PROTECTION

–SOFTWARE DATA PROTECTION IS A DIFFERENT METHOD OF PREVENTING INADVERTANT WRITE OPERATIONS IN A NONVOLATILE MEMORY COMPARED TO THE "HARDWAREU METHODS, SUCH AS: E, G, AND W LOGIC COMBINATIONS, VCC LEVEL DETECTORS, AND POWER UP TIMERS.

–A SPECIFIC DATA AND ADDRESS SOFTWARE SEQUENCE MUST BE ISSUED TO ENABLE A SINGLE PAGE OR BYTE WRITE.

–DATA INPUT FORMAT: D7/D6/D5/D4/D3/D2/D1/D0

–ADDRESS FORMAT: A14/A13/A12/A11/A10/A9/A8/A7/A6/A5/A4/A3/A2/A1/A0

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS WRITE"	5555H	AAH
2	"ACCESS WRITE"	2AAAH	55H
3	"ACCESS WRITE"	5555H	A0H
4	"PAGE WRITE"	Address	Data

–ALL WRITES MUST CONFORM TO THE PAGE MODE TIMING REQUIREMENTS FOR THE PART.

–SINCE THE PAGE ADDRESS IS CHANGED (A VIOLATION OF THE NORMAL PAGE MODE WRITE CYCLE), THE FIRST THREE "ACCESS" WRITES (STEPS 1–3) ARE USED ONLY FOR SOFTWARE ACCESS, NO DATA IS ACTUALLY WRITTEN TO THE EEPROM.

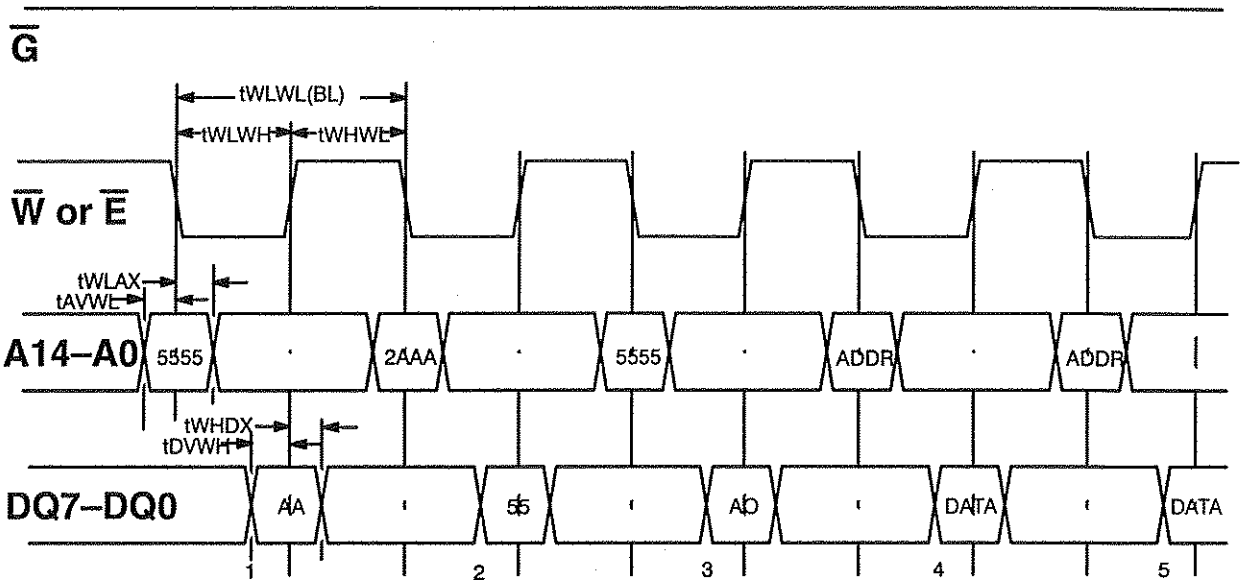
–THE FIRST TIME THIS SEQUENCE IS APPLIED TO THE PART A NON–VOLATILE BIT IS SET, WHICH RECONFIGURES THE PART FROM HARDWARE PROTECTED ONLY TO HARDWARE AND SOFTWARE SEQUENCE PROTECTED. ONCE THIS BIT IS SET, THE SOFTWARE SEQUENCE MUST BE USED TO WRITE TO THE PART.

–THE SOFTWARE PROTECTION CAN BE DISABLED AND THE PART RECONFIGURED TO HARDWARE–ONLY PROTECTION, BY APPLYING THE SIX STEP SOFTWARE SEQUENCE BELOW:

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	20H

FIGURE A1–7

SINGLE SUPPLY EEPROM SOFTWARE DATA PROTECTION TIMING



NOTE 5: Software Data Protection Timings are referenced to $\overline{W}$ or $\overline{E}$ Inputs, whichever is last going LOW, and the $\overline{W}$ or $\overline{E}$ Inputs, whichever is first going HIGH.

SYMBOL (NOTE 5)	DESCRIPTION
tWLWL(BL), tELEL(BL)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW BYTE LOW CYCLE TIME
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tWHWL, tEHEL	$\overline{W}$ OR $\overline{E}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME (WRITE HIGH RECOVERY)
tAVWL tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SET–UP TIME)
tWLAX, ELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID TIME (ADDRESS HOLD TIME)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX. tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1–8

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SINGLE SUPPLY EEPROM OPTIONAL HARDWARE MASS ERASE (ALL 1'S) FEATURE

– IF A HARDWARE MASS ERASE MODE IS IMPLEMENTED ON THE 256K EEPROM, THE FOLLOWING CONVENTIONS MUST BE FOLLOWED:

– $\overline{E}$ = LOW LOGIC LEVEL

– $\overline{W}$ = LOW LOGIC LEVEL

– $\overline{G}$ = SUPER VOLTAGE (WAVEFORM, LEVEL AND TIMING TO BE DETERMINED BY THE MANUFACTURER).

– DQ0 – DQ7 = ALL HIGH LOGIC LEVEL (FFH)

– A0 – A14 = DON'T CARE (EITHER HIGH OR LOW LOGIC LEVELS)

FIGURE A1–9

SINGLE SUPPLY BIT EEPROM OPTIONAL SOFTWARE MASS ERASE (ALL 1'S) FEATURE

IF A SOFTWARE MASS ERASE FEATURE IS IMPLEMENTED IN THE SINGLE SUPPLY EEPROM, IT MUST OPERATE BY APPLYING THE FOLLOWING SIX DATA/ADDRESS SEQUENCE TO THE PART.

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	10H

–ALL ACCESS WRITES MUST FOLLOW THE STANDARD PAGE MODE WRITE CYCLE TIMING SPECIFIED FOR THE PART,

–NO DATA IS ACTUALLY WRITTEN TO THE EEPROM DURING THE "ACCESS" WRITES. ONCE THE 6 STEP SEQUENCE IS COMPLETED, THE PART AUTOMATICALLY COMPLETES A MASS ERASE CYCLE INTERNALLY.

FIGURE A1–10

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3.5.3.2 – DUAL POWER SUPPLY EEPROM COMAND SET

The following command set is applicable to dual power supply EEPROMs of any capacity.

COMAND CODES		
1st CYCLE	2nd CYCLE	OPERATION DESCRIPTION
00		RESERVED
10		Automated Write
20	20	Automated Block Erase
20	D0	Automated Block Erase
30	30	Automated Chip Erase
40		Algorithmic Write
50		Reserved
60	60	Algorithmic Block Erase
70		Reserved
80		Reserved
90		Read ID
A0		Algorithmic Erase Verify
B0		Reserved
C0		Algorithmic Write Verify
D0		Reserved
E0		Reserved
F0		

NOTE: All operands are in HEX.

This Standard provides an optional command set for use with the dual supply voltage EEPROM devices. This command set comprehends algorithmic commands and adds a set of automatic codes. A device may respond to either or both operating modes.

The Standard is applicable to devices with all data interface widths..

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3.5.3.3 – SINGLE POWER SUPPLY EEPROM COMMAND CODES

The following tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

Three cycle Command Codes

Command	1st Cycle		2nd Cycle		3rd Cycle	
	Address	Data	Address	Data	Address	Data
SDP Write Disable	5555	AA	2AAA	55	5555	A0
Product Identification Entry	5555	AA	2AAA	55	5555	90
Reset/Product Identification Exit	5555	AA	2AAA	55	5555	F0
Note: All operands are in HEX.						

Six Cycle Command Codes

	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
Command	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
SDP Write Disable	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	20
Chip Clear (Erase)	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Note: All operands are in HEX												

All timings are per the EEPROM Software Data Protect Timing shown in Fig. A1-7

The address space required is encompassed by A0-A14; other address lines, e.g., A15, A16, can be at any level between VSS minimum and VCC maximum. The data space required is encompassed by DQ0-DQ7; other I/O lines, DQ8, DQ9, can be at any level between VSS minimum and VCC maximum.

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3.5.3.4 – EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies.

–The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

–Whenever the part is read during a nonvolatile write cycle, the data on DQ6 will toggle, i.e., alternate between high and low, on alternate read cycles. Any address can be used when reading to get the Toggle Bit output. Typically, the first toggle out is high (logic "1").

–When the nonvolatile write cycle automatically times out, normal valid data is read at the outputs for any provided address.

–A software routine uses this feature to determine when the nonvolatile write cycle is complete.

–The normal read cycle timing specified for the part must be used for Toggle Bit read cycles.

–An additional parameter, tWHGL (tEHGL), must also be specified for the toggle bit cycle. tWHGL (tEHWL) is the minimum time the system must wait from the last rising edge of $\overline{\text{W}}$ ($\overline{\text{WE}}$) or $\overline{\text{E}}$ until the Toggle Bit read cycle is initiated by the falling edge of $\overline{\text{G}}$ ($\overline{\text{OE}}$).

–The actual completion of the nonvolatile write cycle is asynchronous with the system; therefore, a Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system will possibly get an erroneous result, i.e., valid data may appear to conflict with DQ6. In order to prevent spurious rejections, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the reject is valid.

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3.7.5.10 – 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ

CAPACITY—32K, & 128K WORDS OF 8 BIT
LOGIC FEATURES—SEPARATE DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE
PACKAGE—40 PIN DIP, 0.6" wide
—40 PIN SOJ, UNDEFINED
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–10

3.7.5.11 – 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC

CAPACITY—2K, 8K, 32K WORDS OF 9 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—68 PAD (PIN) SCC, 0.950" X 0.950"
PIN ASSIGNMENT—Fig. 3.7.5–11

This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.12 – 32K BY 9 CACHE SRAM IN 44 SCC

CAPACITY—32K WORDS OF 9 BITS,
LOGIC FEATURES—Internal CACHE data compare logic
PACKAGE—44 TERMINAL SCC, 0.500" X 0.500"
PIN ASSIGNMENT—Fig. 3.7.5–12

This part contains specialized logic functions which allow it to be used to implement the CACHE memory function conveniently.

3.7.5.13 – 128K BY 8 SRAM IN TSOP1

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN TSOP1, 20 mm X 8 mm, 0.5 mm PIN PITCH
PIN ASSIGNMENTS—Fig. 3.7.5–13

3.7.5.14 – 128K BY 8 & 9 SSRAM IN SOJ

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN SOJ, 0.400"
PIN ASSIGNMENTS—Fig. 3.7.5–14

3.7.5.15 – 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP

CAPACITY—1K, 2K WORDS OF 8 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—48 PIN DIP, 0.600"
PIN ASSIGNMENT—Fig. 3.7.5–15

This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.16 – 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO–N

CAPACITY—128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN LEADLESS CERAMIC SO, 0.400"
PIN ASSIGNMENT—Fig. 3.7.5–16

This family of parts is based on the evolutionary SRAM pinout family described in Sec. 3.7.5.7

3.7.5.17 – 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP, TSOP2, AND SOJ

CAPACITY—128K & 512K WORDS OF 8 OR 9 BITS,
LOGIC FEATURES—Both Synchronous and Asynchronous versions of the 128K part
PACKAGE—36 PIN DIP, TSOP2, or SOJ, 0.400" or 0.600",
— See Fig. 3.7.5–17 for specific package approvals and dimensions.
PIN ASSIGNMENT—Fig. 3.7.5–17

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3.7.5.18 – 128K TO 2M BY 8/9 BURST SRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5-18
These parts contain BURST addressing capability.

3.7.5.19 – 128K TO 2M BY 8/9 SSRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5-19
Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.5-20

3.7.5.20 – 32K BY 8 SRAM IN TSOP1

CAPACITY—32K WORDS OF 8 BITS
PACKAGE—32 PIN TSOP1, 8 mm X 11.8 mm, 0.55 mm PP
PIN ASSIGNMENTS—Fig. 3.7.5-21

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3.7.5 Byte Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

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3.7.5.1 – 64 BY 9 TTL SRAM IN SCC

CAPACITY—64 WORDS OF 9 BITS
PACKAGE—28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENTS—Fig. 3.7.5–1
This standard was developed by Committee 42.1.

3.7.5.2 – 1K & 2K BY 8 TTL SRAM IN DIP

CAPACITY—1K, 2K WORDS OF 8 BITS
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–2

3.7.5.3 – 2K & 4K BY 8 TTL SRAM IN RCC

CAPACITY—2K, 4K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–3
These parts are CC equivalents of 24 Pin DIP devices.

3.7.5.4 – 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,

CAPACITY—2K, 4K, 8K, 16K, & 32K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
—28 PIN DIP, 0.3" WIDE OPTIONAL FOR 8K & 32K DEVICES
PIN ASSIGNMENT—Fig. 3.7.5–4

3.7.5.5 – .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

CAPACITY—.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–5

3.7.5.6 – 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP–2,

CAPACITY—32K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—28 OR 32 PIN SOJ, 0.3", 0.4" WIDE OR NOT DEFINED
—32 PIN TSOP–2 (see Fig. 3.7.5–6 for package approvals)
PIN ASSIGNMENT—Fig. 3.7.5–6

3.7.5.7 – 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,

CAPACITY—64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–7

3.7.5.8 – 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
—OPTIONAL 32 PIN DIP & SOJ, 0.3" WIDE FOR 32K DEVICE
PIN ASSIGNMENT—Fig. 3.7.5–8

3.7.5.9 – 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—32K, 128K, 512K, 2M WORDS OF 8 BIT AND 512K, 2M WORDS OF 9 BITS
LOGIC FEATURES—COMMON DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–9

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SSRAM Boundry Scan Order					
X9 Part					
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2, NC	5R	22	NC, SA¯	3B
2	SA	6T	23	NC, SE2 SA#	2B
3	SA	4P	24	SA	3A
4	SA	4T	25	SA	3C
5	SA	6R	26	SA	2C
6	SA	5T	27	SA	2A
7	NC, ZZ	7T			
			28	DQ	2G
8	DQ	6L			
			29	DQ	1H
9	DQ	7K			
			30	ZQ, NC	4D
10	$\overline{K}$, NC	4L	31	$\overline{SS}$	4E
11	K	4K	32	$\overline{C}$, NC	4G
12	$\overline{G}$	4F	33	C, NC	4H
			34	$\overline{SW}$	4M
13	DQ	6H			
14	DQ	7G	35	DQ	2K
			36	DQ	1L
15	DQ, NC	7E			
16	SA	6A			
17	SA	6C	37	SA	3T
18	SA	5C	38	SA	2R
18	SA	5A	39	SA	4N
20	NC, $\overline{SE2}$ SA◇	6B	40	SA	2T
21	NC, SA*	5B	41	M1, NC	3R

FIGURE 3.7.5-20
128K TO 2M BY 8/9 SSRAM IN BGA BOUNDRY SCAN ORDER

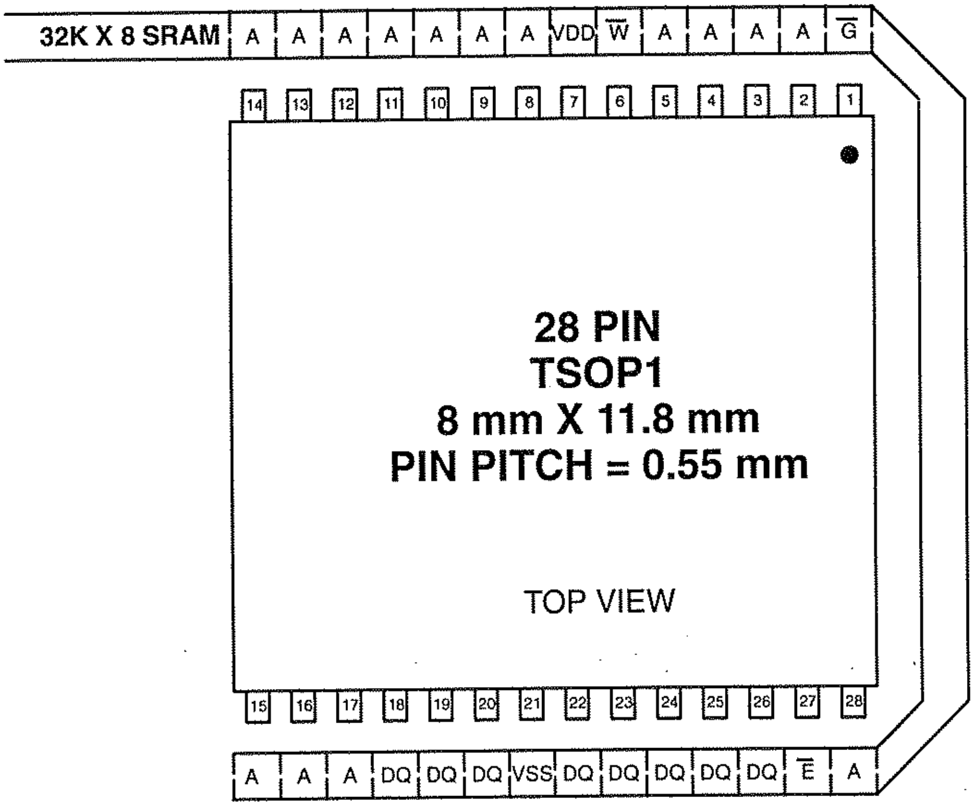

FIGURE 3.7.5–21
32K BY 8 SRAM IN TSOP–1

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Synchronous SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View

X18	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA~	NC	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	VSS	NC, ZQ	VSS	DQa, NC	NC
E	NC	DQb	VSS	$\overline{SS}$, $\overline{SE}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{G}$, $\overline{SG}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{SBb}$	NC, $\overline{C}$	VSS	NC	DQa
H	DQb	NC	VSS	NC, C	VSS	DQa	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQb	VSS	CK, K	VSS	NC	DQa
L	DQb	NC	VSS	$\overline{CK}$, $\overline{K}$, NC	$\overline{SBa}$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{SW}$	VSS	NC	VDDQ
N	DQb	NC	VSS	SA	VSS	DQa	NC
P	NC	DQb, NC	VSS	SA	VSS	NC	DQa
R	NC	SA	M1, NC	VDD	M2, NC	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table

Density	Address Assignment	Nominal Exterior Package Dimension
1M (64K X 18)	Basic SA	14 mm X 22 mm
2M (128K X 18)	~	14 mm X 22 mm
4M (256K X 18)	~, *	14 mm X 22 mm
8M (512K X 18)	~, *, ◇	TBD
16 M (1M X 18)	~, *. ◇, #	TBD

Mode Truth Table	M1	M2
Single Clock, Register Flow Through	VSS	VSS
Single Clock, Register–Register	VSS	VDD
Single Clock, Register–Latch	VDD	VSS
Dual Clock	VDD	VDD

FIGURE 3.7.7–10
64K TO 1M BY 16 & 18 SSRAM IN BGA

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SSRAM Boundry Scan Order

X18 Part

Exit Order	Signal	Bump #		Exit Order	Signal	Bump #
1	M2, NC	5R		26	NC, SA~	3B
2	SA			27	NC, SE2 SA#	2B
3	SA	6T		28	SA	3A
		4P		29	SA	3C
4	SA	6R		30	SA	2C
5	SA	5T		31	SA	2A
6	NC, ZZ	7T				
				32	DQB	1D
7	DQa	7P		33	DQb	2E
8	DQa	6N				
				34	DQb	2G
9	DQa	6L				
				35	DQb	1H
10	DQa	7K		36	$\overline{\text{SBb}}$	3G
11	$\overline{\text{SBa}}$	5L		37	ZQ, NC	4D
12	$\overline{\text{K}}$, NC	4L		38	$\overline{\text{SS}}$	4E
13	K	4K		39	$\overline{\text{C}}$, NC	4G
14	G	4F		40	C, NC	4H
				41	$\overline{\text{SW}}$	4M
15	DQa	6H				
16	DQa	7G		42	DQb	2K
				43	DQb	1L
17	DQa	6F				
18	DQa	7E		44	DQb	2M
				45	DQb	1N
19	DQa, NC	6D				
20	SA	6A		46	DQb, NC	2P
21	SA	6C		47	SA	3T
22	SA	5C		48	SA	2R
23	SA	5A		49	SA	4N
24	NC, $\overline{\text{SE2}}$ SA◇	6B		50	SA	2T
25	NC, SA*	5B		51	M1, NC	3R

FIGURE 3.7.7–11
64K TO 1M BY 16 & 18 SSRAM IN BGA BOUNDRY SCAN ORDER

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3.7.8.1 – 32K TO 128K BY 32 & 36 BURST SSRAM IN TQFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
PACKAGE—100 PIN TQFP, 20 mm X 14 mm WITH 0.65 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–1
These parts combine the features of Synchronous SRAM with BURST addressing capability. This standard modifies the one published previously in Release 5 ab adding new functions and deleting some that were not used.

3.7.8.2 – 32K TO 128K BY 32 & 36 SRAM AND SSRAM FAMILIES IN 100 TQFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
LOGIC FEATURES —There are two version of this part available:
—SYNCHRONOUS WITH ADDRESS LATCH OR ASYNCHRONOUS
—UPPER BYTE AND LOWER BYTE SELECTABLE
—COMMON DATA I/O
PACKAGE—100 PIN TQFP, 20 mm X 14 mm 0.65 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–2

3.7.8.3 – 32K TO 512K BY 32 & 36 BURST SRAM IN BGA

CAPACITY—32K, 64K,128K, 256K, OR 512K WORDS OF 32 OR 36 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–3
These parts contain BURST addressing capability.

3.7.8.4 – 32K TO 512K BY 16 & 18 SSRAM IN BGA

CAPACITY—32K, 64K, 128K, 256K, OR 512K WORDS OF 32 OR 36 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–4
.Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.8–5

3.7.8.5 – 16K TO 64K BY 64 & 72 BURST SSRAM IN QFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
PACKAGE—120 PIN TQFP, 20 mm X 14 mm WITH 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–6
These parts combine the features of Synchronous SRAM with BURST addressing capability.

3.7.8.6 – 16K TO 256K BY 64 & 72 BURST SSRAM IN BGA

CAPACITY—16K, 32K, 64K, 128K, OR 256K WORDS OF 64 OR 72 BITS,
PACKAGE—11 X 19 BALL BGA 20 mm X 25 mm OR UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–7
These parts combine the features of Synchronous SRAM with BURST addressing capability.

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SSRAM Boundry Scan Order						
X36 Part						
Exit Order	Signal	Bump #		Exit Order	Signal	Bump #
1	M2, NC	5R		36	NC, SA¯	3B
				37	NC, SE2 SA#	2B
2	SA	4P		38	SA	3A
3	SA	4T		39	SA	3C
4	SA	6R		40	SA	2C
5	SA	5T		41	SA	2A
6	NC, ZZ	7T		42	DQc,NC	2D
7	DQa, NC	6P		43	DQc	1D
8	DQa	7P		44	DQc	2E
9	DQa	6N		45	DQc	1E
10	DQa	7N		46	DQc	2F
11	DQa	6M		47	DQc	2G
12	DQa	6L		48	DQc	1G
13	DQa	7L		49	DQc	2H
14	DQa	6K		50	DQc	1H
15	DQa	7K		51	$\overline{\text{SBc}}$	3G
16	$\overline{\text{SBa}}$	5L		52	ZQ, NC	4D
17	$\overline{\text{K}}$, NC	4L		53	$\overline{\text{SS}}$	4E
18	K	4K		54	$\overline{\text{C}}$, NC	4G
19	$\overline{\text{G}}$	4F		55	C, NC	4H
20	$\overline{\text{SBb}}$	5G		56	$\overline{\text{SW}}$	4M
21	DQb	7H		57	$\overline{\text{SBd}}$	3L
22	DQb	6H		58	DQd	1K
23	DQb	7G		59	DQd	2K
24	DQb	6G		60	DQd	1L
25	DQb	6F		61	DQd	2L
26	DQb	7E		62	DQd	2M
27	DQb	6E		63	DQd	1N
28	DQb	7D		64	DQd	2N
29	DQb, NC	6D		65	DQd	1P
30	SA	6A		66	DQd, NC	2P
31	SA	6C		67	SA	3T
32	SA	5C		68	SA	2R
33	SA	5A		69	SA	4N
34	NC, $\overline{\text{SE2}}$ SA◇	6B				
35	NC, SA*	5B		70	M1, NC	3R

FIGURE 3.7.8-5

32K TO 512K BY 32 & 36 SSRAM IN BGA BOUNDRY SCAN ORDER

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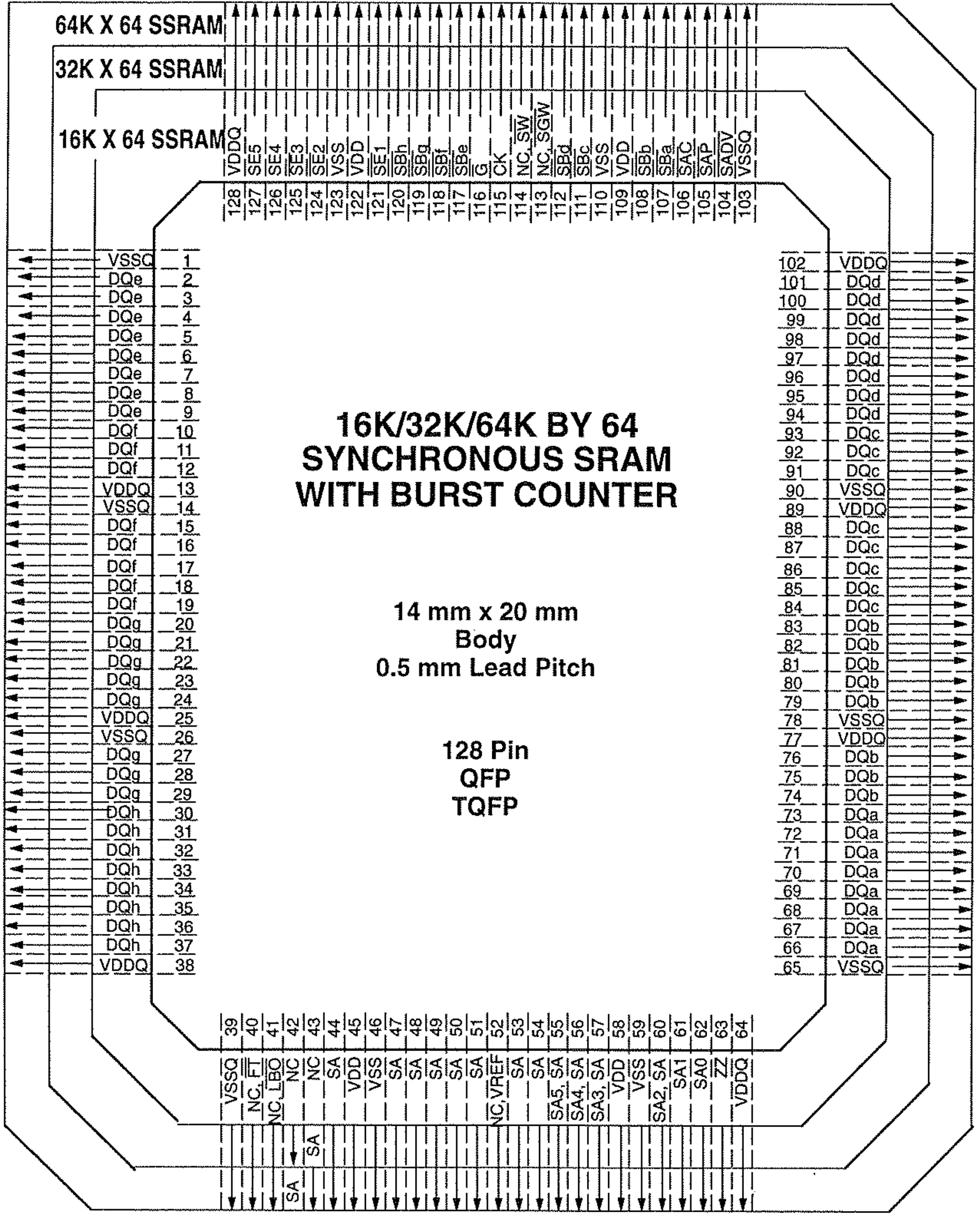

Notes: (1) This standard accommodates synchronous burst address fields ranging from 2 to 6 address b

(2) An 8-word (3 address bits) interleaved burst sequence is currently specified in commercial data sheets

FIGURE 3.7.8-6
16K/32K/64K BY 64 SYNCHRONOUS SRAM WITH BURST COUNTER

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Burst SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View

X72	1	2	3	4	5	6	7	8	9	10	11
A	DQe	DQe	NC, SA#	SA	SA	$\overline{\text{SS}}$, $\overline{\text{SE1}}$	SA	SA	NC, SA$	DQd	DQd
B	DQe	DQe	NC, SA~	SA	SA	$\overline{\text{G}}$	SA	SA	NC, SA◇	DQd	DQd
C	DQe	DQe	NC, SE2	VDD, VDDQ	VDD, VDDQ	ND, $\overline{\text{SGW}}$	VDD, VDDQ	VDD, VDDQ	NC, $\overline{\text{SE3}}$	DQd	DQd
D	DQe	DQe	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{\text{ADV}}$	VSS, VSSQ	VDD	VDD, VDDQ	DQd	DQD
E	DQe, NC	DQf, NC	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{\text{SAC}}$	VSS, VSSQ	VDD	VDD, VDDQ	DQc, NC	DQd, NC
F	DQf	DQf	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{\text{SAP}}$	VSS, VSSQ	VDD	VDD, VDDQ	DQc	DQc
G	DQf	DQf	VDD, VDDQ	VDD	VSS, VSSQ	VSS, VSSQ	VSS, VSSQ	VDD	VDD, VDDQ	DQc	DQc
H	DQf	DQf	VDD, VDDQ	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	VDD, VDDQ	DQc	DQc
J	DQf	DQf	$\overline{\text{SWe}}$, $\overline{\text{SBe}}$	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	$\overline{\text{SWd}}$, $\overline{\text{SBd}}$	DQc	DQc
K	$\overline{\text{SWf}}$, $\overline{\text{SBf}}$	$\overline{\text{SWg}}$, $\overline{\text{SBg}}$	NC, VREF	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	NC, VREF	$\overline{\text{SWb}}$, $\overline{\text{SBb}}$	$\overline{\text{SWc}}$, $\overline{\text{SBc}}$
L	DQg	DQg	$\overline{\text{SWh}}$, $\overline{\text{SBh}}$	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	$\overline{\text{SWa}}$, $\overline{\text{SBa}}$	DQb	DQb
M	DQg	DQg	VDD, VDDQ	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	VDD, VDDQ	DQb	DQb
N	DQg	DQg	VDD, VDDQ	VDD	VSS, VSSQ	VSS, VSSQ	VSS, VSSQ	VDD	VDD, VDDQ	DQb	DQb
P	DQg	DQg	VDD, VDDQ	VDD	VSS, VSSQ	NC, $\overline{\text{CK}}$, $\overline{\text{K}}$	VSS, VSSQ	VDD	VDD, VDDQ	DQb	DQb
R	DQg, NC	DQh, NC	VDD, VDDQ	VDD	VSS, VSSQ	CK, K	VSS, VSSQ	VDD	VDD, VDDQ	DQa, NC	DQb, NC
T	DQh	DQh	VDD, VDDQ	VDD	VSS, VSSQ	NC, $\overline{\text{SW}}$	VSS. VSSQ	VDD	VDD, VDDQ	DQa	DQa
U	DQh	DQh	$\overline{\text{LBO}}$, NC	VDD, VDDQ	VDD, VDDQ	SA1	VSS, VSSQ	VDD, VDDQ	NC, $\overline{\text{FT}}$	DQa	DQa
V	DQh	DQh	NC	SA	SA	SA0	SA	SA	NC	DQa	DQa
W	DQh	DQh	NC, ZQ	NC, TMS	NC, TDI	NC, TCK	NC, TDO	NC, TRST	NC, ZZ	DQa	DQa

Address Assignment and Package Dimension Table

Density	Address Assignment	Nominal Exterior Package Dimension
1M (16K X 64, 72)	Basic SA	21 mm X 25 mm
2M (32K X 64, 74)	~	21 mm X 25 mm
4M (64K X 64, 72)	~, *	21 mm X 25 mm
8M (128K X 64, 72)	~, *, ◇	TBD
16 M (256K X 64, 72)	~, *. ◇, #	TBD

FIGURE 3.7.8–7
16K TO 256K BY 64 & 72 BURST SRAM IN BGA

65
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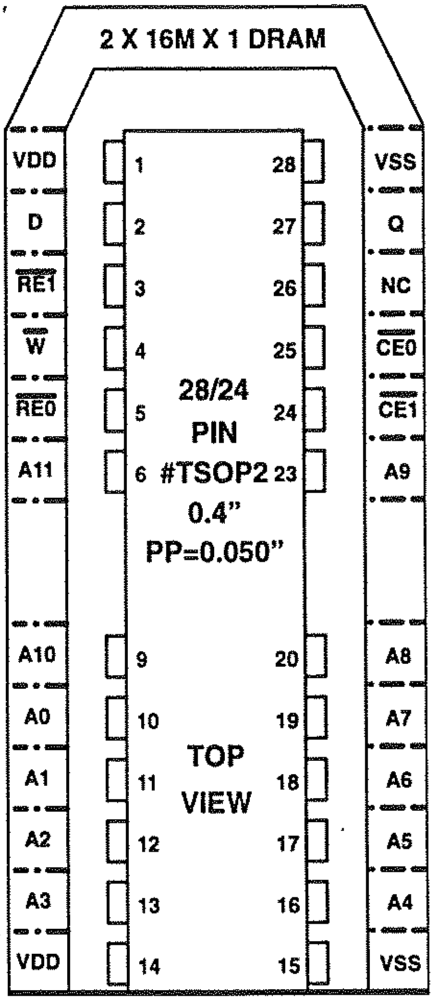
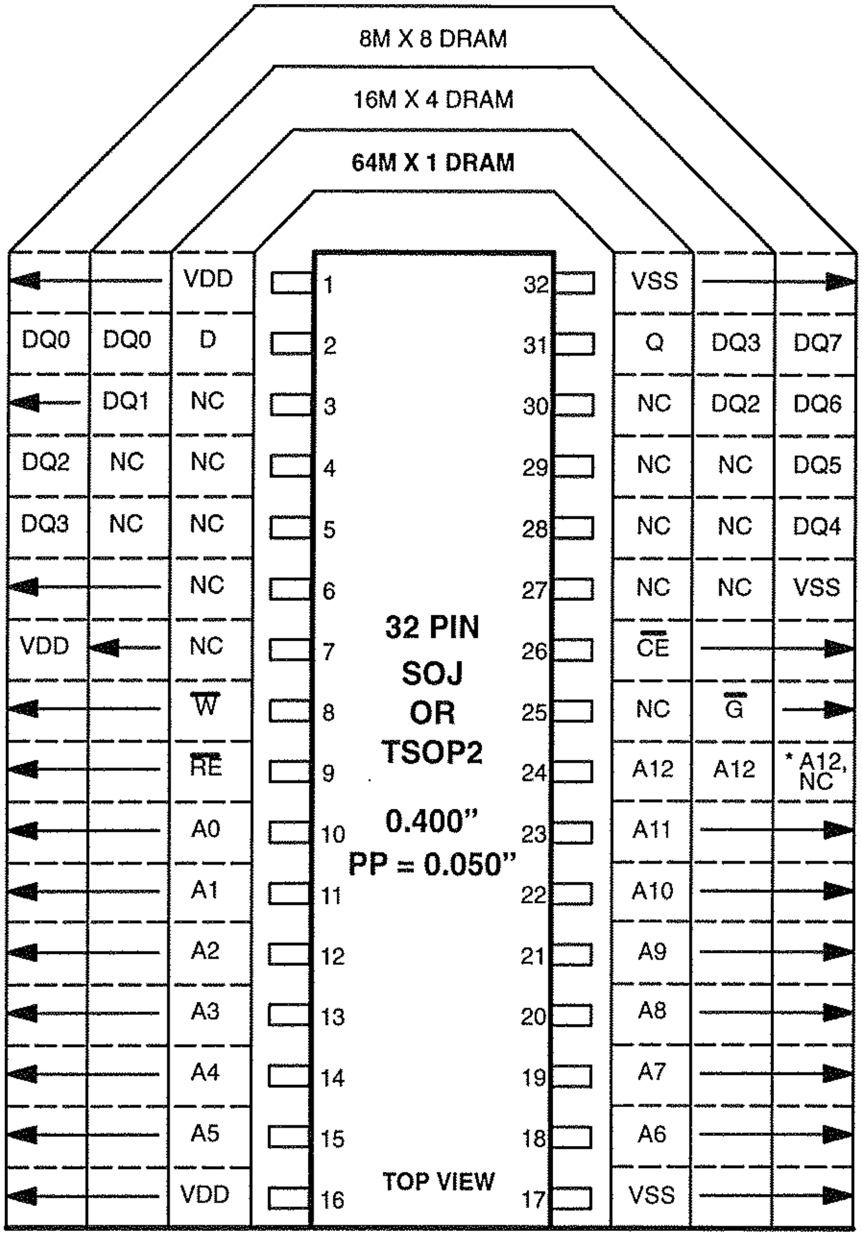


The JEDEC approved term for this package is PDSO–G

ROW, REFRESH, & COLUMN ADDRESS CONFIGURATION

DEVICE CONFIGURATION	2 X 16M X 1	2 X 16M X 1
REFRESH COUNT	2048 Refresh	4096 Refresh
ROW ADDRESS	A0 → A11	A0 → A11
REFRESH ADDRESS	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A11	A0 → A11

FIGURE 3.9.1–11
2 X 16M BY 1 DRAM IN TSOP2



* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4	16M X 4	8M X 8	8M X 8
ROW COUNT		4K Rows	8K Rows	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.1–12
64M BY 1 DRAM IN SOJ & TSOP2

3.9.2.1 – 16K & 64K BY 4 DRAM IN DIP

CAPACITY—16K, 64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—18 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2–1

3.9.2.2 – 16K BY 4 DRAM IN DIP

CAPACITY—16K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Separate DATA I/O
PACKAGE—20 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2–1
NOTE: At the time that this document was published, this standard was in the process of being rescinded by the Committee.

3.9.2.3 – 64K BY 4 DRAM IN RCC

CAPACITY—64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with Common DATA I/O
PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT—Fig. 3.9.2–2

3.9.2.4 – 256K & 1M BY 4 DRAM FAMILY IN DIP

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN DIP, Width: 0.3" for 256K & 1M,
PIN ASSIGNMENT—Fig. 3.9.2–3

3.9.2.5 – 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 256K
—26/20 PIN SOJ or TSOP2: 0.3" or 0.35" by 0.675" for 1M
—26/24 PIN SOJ OR TSOP–2: 0.3" for 4M
—28/24 PIN SOJ: 0.4" by 0.725 for 4M
PIN ASSIGNMENT—Fig. 3.9.2–4

3.9.2.6 – 64K TO 4M BY 4 DRAM IN ZIP

CAPACITY—64K, 256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN ZIP, 0.400" WIDE FOR 64K, 256K, & 1M PARTS
—24 PIN ZIP, 0.475" WIDE FOR 4M PART
PIN ASSIGNMENT—Fig. 3.9.2–5

3.9.2.7 – 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with 4 CE clocks controlling the 4 data bits
PACKAGE—26/24 PIN SOJ, Width: 0.3"
—26/24 PIN TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–6

3.9.2.8 – 256K BY 4 DRAM IN TSOP1

CAPACITY—256K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—24/20 PIN TSOP1, 14.4 mm x 6.0 mm, 0.5 mm LEAD PITCH
PIN ASSIGNMENT—Fig. 3.9.2–7

3.9.2.9 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT or 4M WORDS OF 4 BITS
LOGIC FEATURES—Configurable as a X1 or a X4 part
—The data access mode can be chosen by logic control
PACKAGE—28 PIN SOJ
PIN ASSIGNMENT—Fig. 3.9.2–8

3.9.2.10 – 256K TO 4M BY 4 NON–MUX DRAM FAMILY IN SOJ

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Non–Multiplexed Address
PACKAGE—28, 32, OR 34 PIN SOJ, WIDTH Not yet defined
PIN ASSIGNMENT—Fig. 3.9.2–9

3.9.2.11 – 4M BY 4 DRAM WITH 1 $\overline{\text{CE}}$ AND 4 $\overline{\text{CE}}$ IN TSOP2

CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
—There are two versions of this part, one with 1 $\overline{\text{CE}}$ and one with 4 $\overline{\text{CE}}$ controlling each of the data bits
PACKAGE—28/24 PIN TSOP2, 0.4" WIDE FOR THE 1 $\overline{\text{CE}}$ PART
— 28 PIN TSOP2, 0.4" WIDE FOR THE 4 $\overline{\text{CE}}$ PART
PIN ASSIGNMENT—Fig. 3.9.2–10

3.9.2.12 – 16M BY 4 DRAM IN SOJ & TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address

This part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.

PACKAGE—34 PIN SOJ, WIDTH: 0.5"
—34PIN TSOP2, WIDTH: 0.5", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–11
PACKAGE—32 PIN SOJ, 0.400" Wide
—32 PIN TSOP2, 0.400" WIDE, 0.050" PP.
PIN ASSIGNMENT—Fig. 3.9.1–12

3.9.2.13 – 1M, 2M, & 4M BY 2 DRAM IN SOJ & TSOP2

CAPACITY—1M, 2M, & 4M WORDS OF 2 BITS
LOGIC FEATURES—Multiplexed Address and a separate $\overline{\text{CE}}$ control for each data bit.
PACKAGE—26/20, 26/24, & 28/24 PIN SOJ or TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–12

3.9.2.14 – 16M BY 4 DRAM WITH 4 $\overline{\text{CE}}$ IN SOJ OR TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
—The part, has 4 $\overline{\text{CE}}$, one controlling each of the data bits.
PACKAGE— 34 PIN TSOP2, 12.7 mm WIDE, PP = 1.27 mm
— 34 PIN SOJ, 12.7 mm WIDE, PP = 1.27 mm
PIN ASSIGNMENT—Fig. 3.9.2–14
PACKAGE—32 PIN SOJ, 10.16 mm Wide
—32 PIN TSOP2, 10.16 mm Wide, 1.27 mm PP
PIN ASSIGNMENT—Fig. 3.9.2–14

3.9.2.15 – 64M X 4 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 64M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.2–15

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

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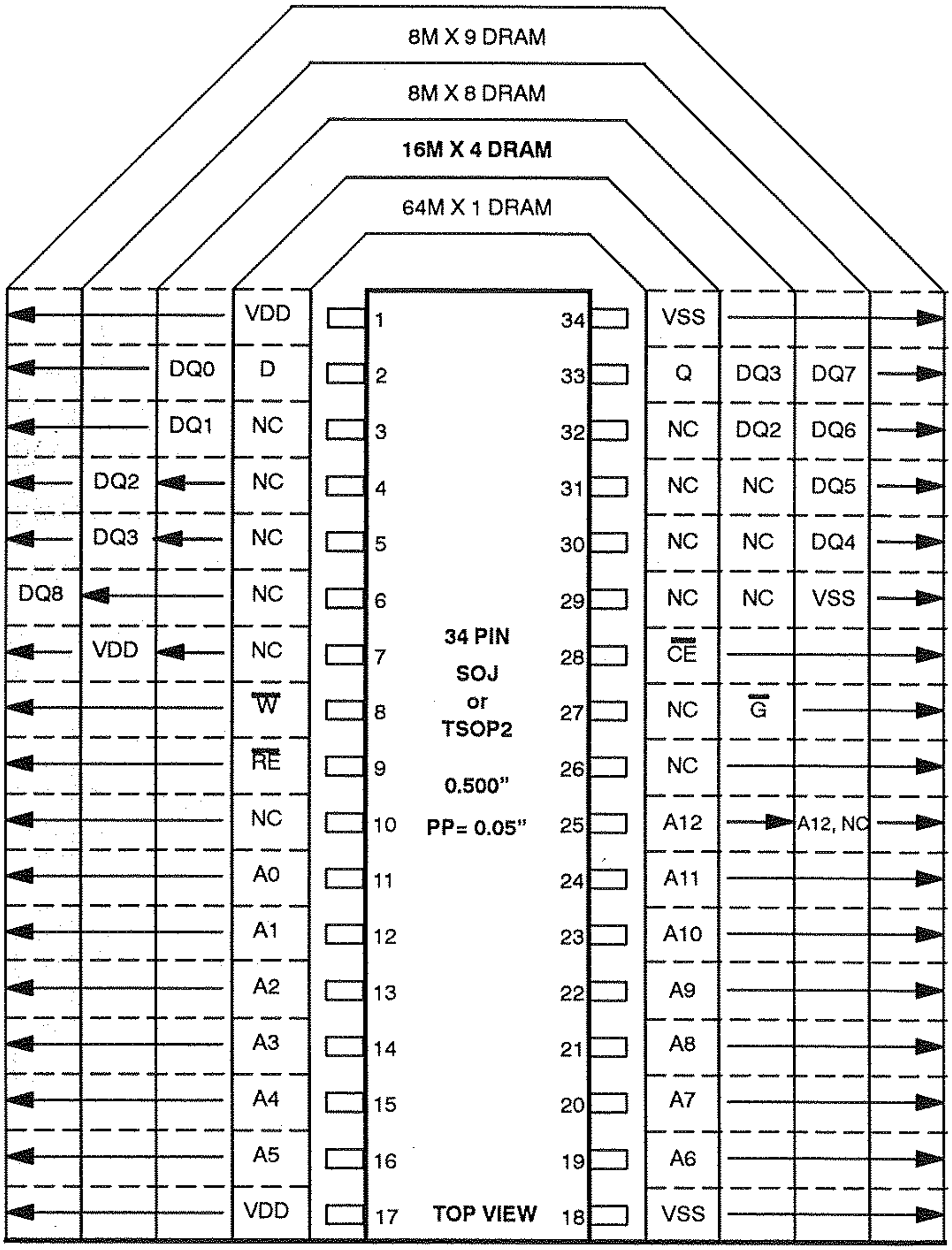


ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

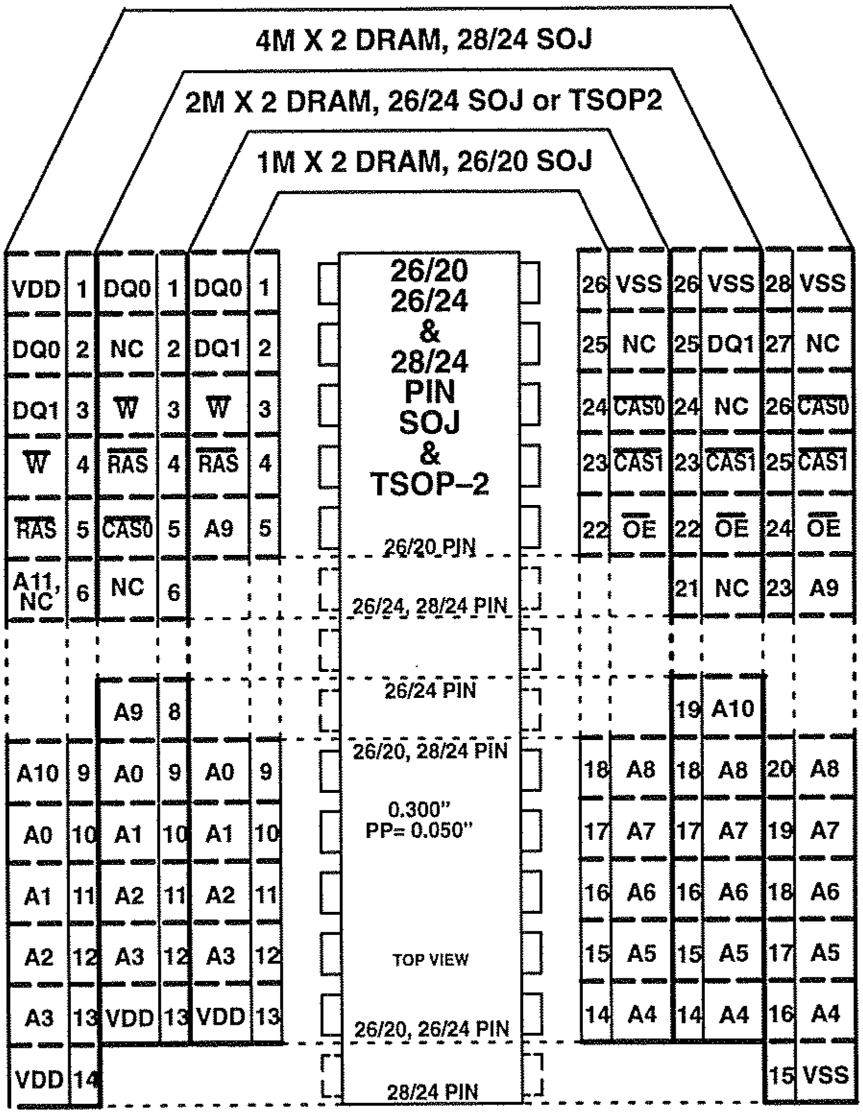
DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.2-11

16M BY 4 DRAM IN SOJ & TSOP2

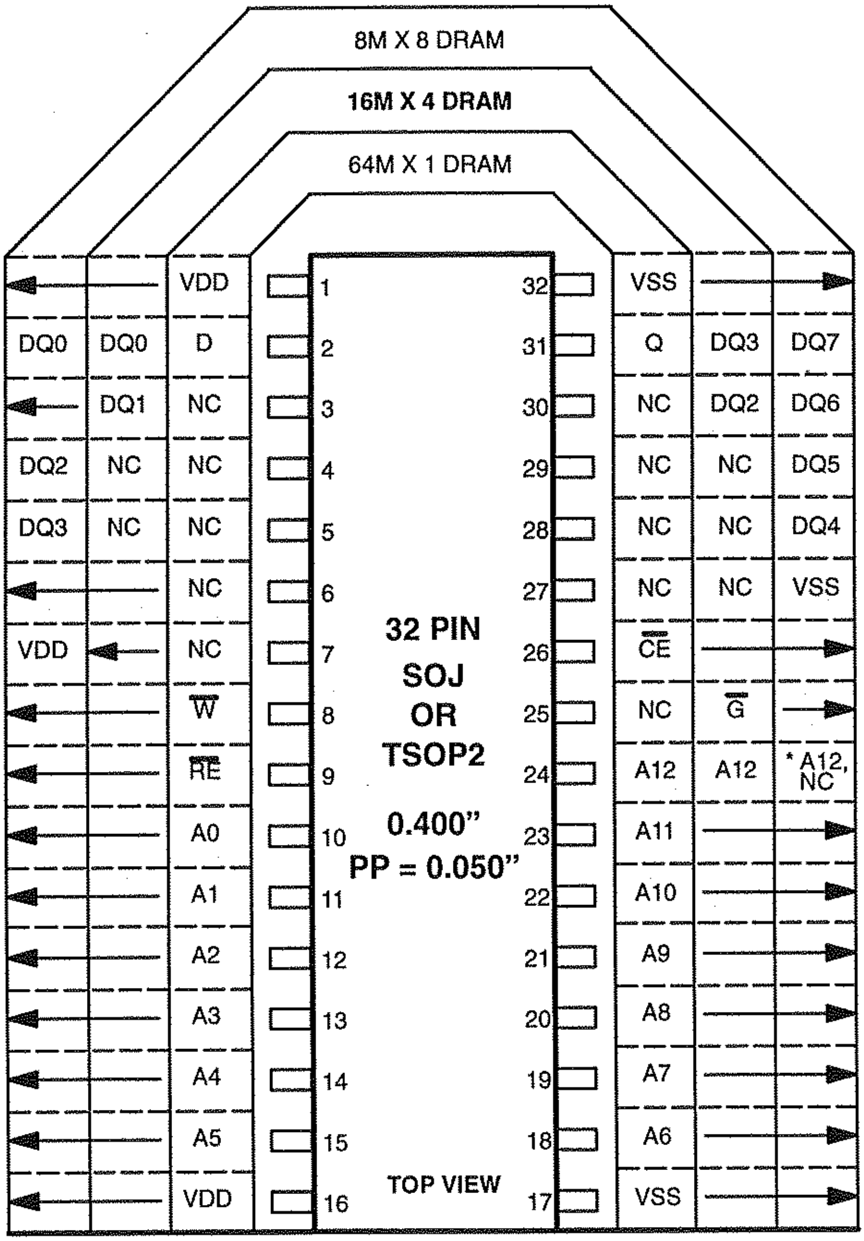
7C



ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	1M X 2	2M X 2	4M X 2	4M X 2
ROW COUNT	1K Rows	1K Rows	2K Rows	4K Rows
ROW ADDRESSES	A0 → A9	A0 → A10	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A9	AO → A9	A0 → A10	A0 → A9

FIGURE 3.9.2-12
1M TO 4M BY 2 DRAM WITH 2 CAS IN SOJ & TSOP2

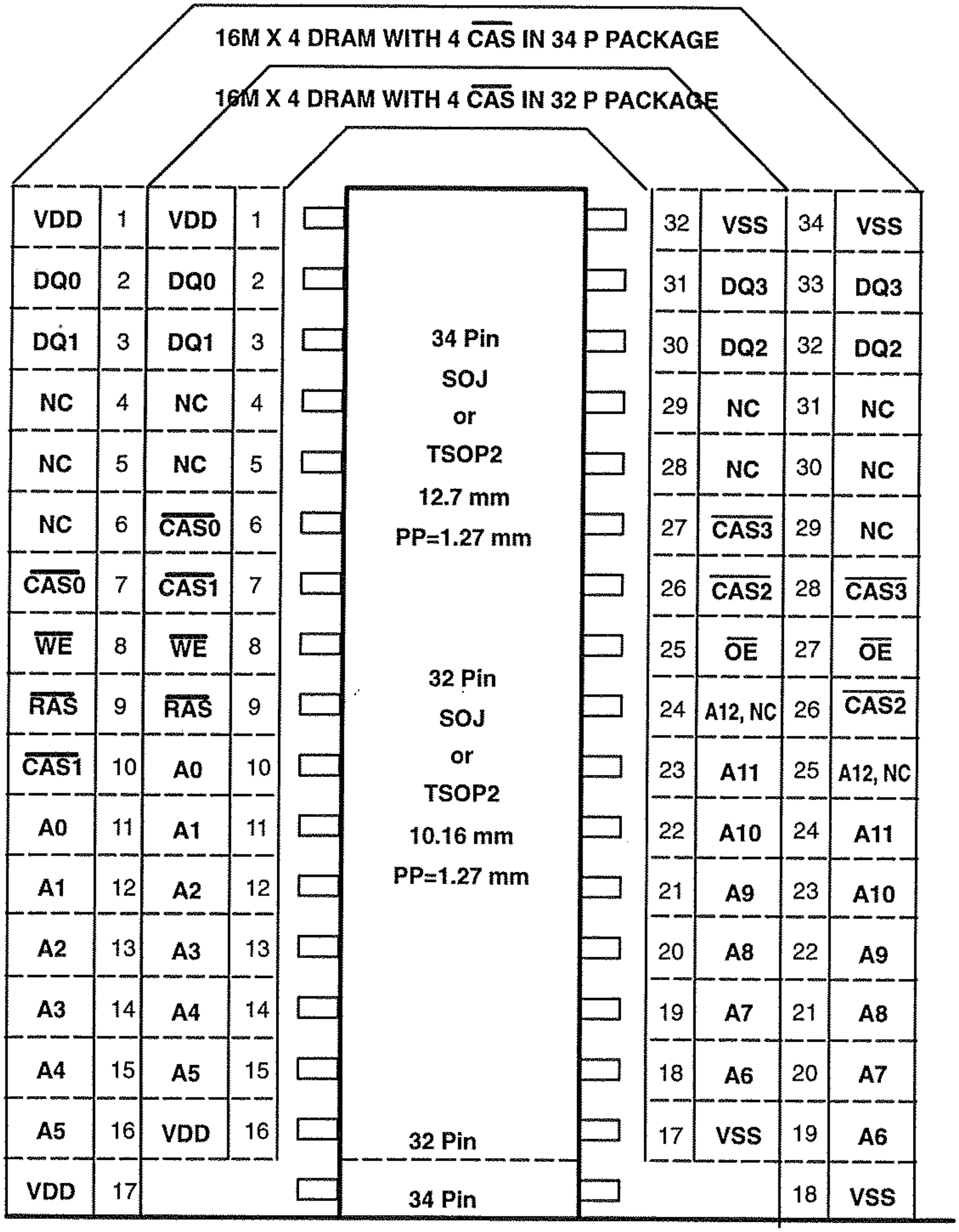


* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION ROW COUNT	64M X 1	16M X 4 4K Rows	16M X 4 8K Rows	8M X 8 4K Rows	8M X 8 8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.2–13
16M BY 4 DRAM IN SOJ & TSOP2



34 P	Pin	32 P	Pin	Pin	32 P	Pin	34 P
VDD	1	VDD	1	32	VSS	34	VSS
DQ0	2	DQ0	2	31	DQ3	33	DQ3
DQ1	3	DQ1	3	30	DQ2	32	DQ2
NC	4	NC	4	29	NC	31	NC
NC	5	NC	5	28	NC	30	NC
NC	6	$\overline{\text{CAS0}}$	6	27	$\overline{\text{CAS3}}$	29	NC
$\overline{\text{CAS0}}$	7	$\overline{\text{CAS1}}$	7	26	$\overline{\text{CAS2}}$	28	$\overline{\text{CAS3}}$
$\overline{\text{WE}}$	8	$\overline{\text{WE}}$	8	25	$\overline{\text{OE}}$	27	$\overline{\text{OE}}$
$\overline{\text{RAS}}$	9	$\overline{\text{RAS}}$	9	24	A12, NC	26	$\overline{\text{CAS2}}$
$\overline{\text{CAS1}}$	10	A0	10	23	A11	25	A12, NC
A0	11	A1	11	22	A10	24	A11
A1	12	A2	12	21	A9	23	A10
A2	13	A3	13	20	A8	22	A9
A3	14	A4	14	19	A7	21	A8
A4	15	A5	15	18	A6	20	A7
A5	16	VDD	16	17	VSS	19	A6
VDD	17					18	VSS

ADDRESS CONFIGURATIONS		
ROW COUNT	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A11	A0 ⇒ 12
COLUMN ADDRESSES	A0 ⇒ A11	A0 ⇒ 10

*NOTE: The JESD30 approved term for the TSOP2 package is PDSO-G, for the SOJ is PDSO-J

FIGURE 3.9.2-14
16M BY 4 DRAM WITH 4 $\overline{\text{CAS}}$ IN SOJ & TSOP2

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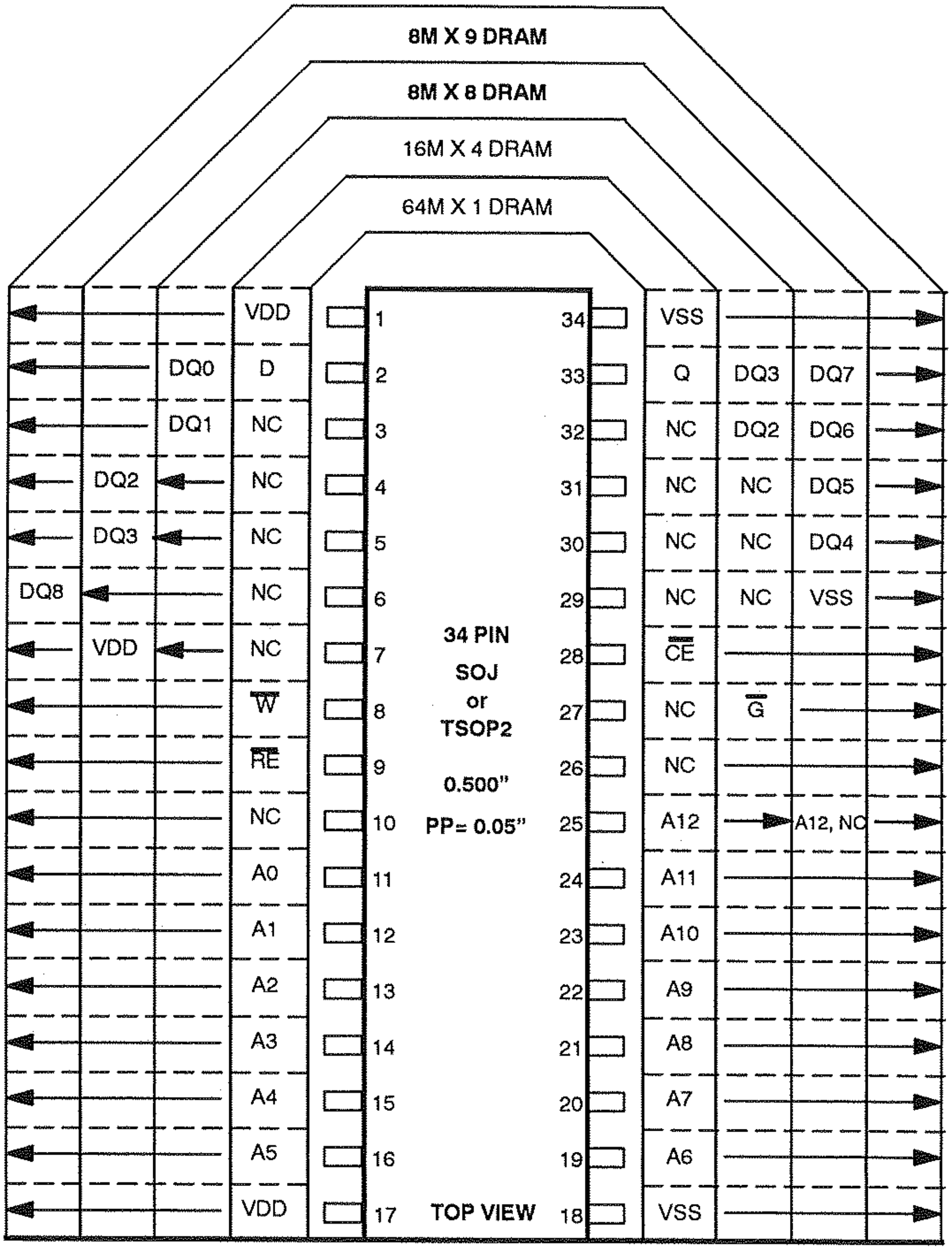


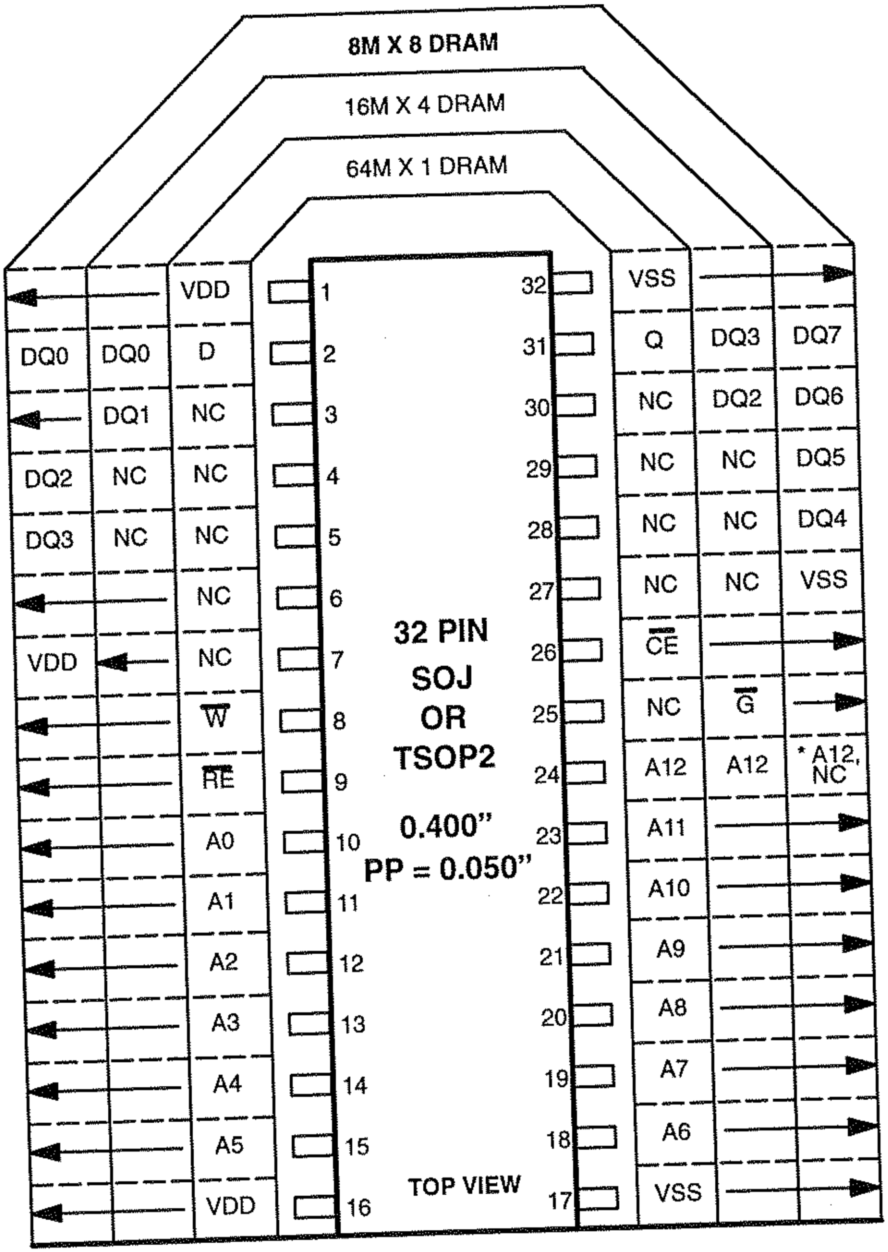
ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.3-7

8M BY 8 & 9 DRAM IN SOJ & TSOP2



* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION ROW COUNT	64M X 1	16M X 4 4K Rows	16M X 4 8K Rows	8M X 8 4K Rows	8M X 8 8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.3-8
8M BY 8 DRAM IN SOJ & TSOP2

3.9.4.1 – 64K BY 16 DRAM WITH 2 $\overline{\text{W}}$ IN SOJ & TSOP2

CAPACITY—64K WORDS OF 16 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—40 PIN SOJ, 0.400" WIDE
—44/40 PIN TSOP2, 0.400" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–1 (SOJ)
—Fig. 3.9.4–6 (TSOP2)

3.9.4.2 – 256K & 1M BY 16 & 18 WITH 2 $\overline{\text{CE}}$ OR 2 $\overline{\text{W}}$ DRAM IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 16 & 18 BITS,
The standard for the 2 $\overline{\text{W}}$ versions of the 1M part has been rescinded and removed from Figs. 3.9.4–4 & 3.9.4–5 in Release 5.
LOGIC FEATURES—MULTIPLEXED ADDRESS
—There are two versions of these parts, one with 2 $\overline{\text{W}}$ and the other with 2 $\overline{\text{CE}}$.
—The two clocks control the LOWER BYTE and UPPER BYTE data bits.
—The 1M part allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—256K in 40 PIN SOJ, 0.400" WIDE
—256K in 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
—1M IN 42 PIN SOJ, 0.400" WIDE
—1M in 50/44 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–2 (256K SOJ)
—Fig. 3.9.4–3 (256K TSOP2)
—Fig. 3.9.4–4 (1M SOJ)
—Fig. 3.9.4–5 (1M TSOP2)

3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—This part contains multiple logic functions that are similar to those used in MPDRAMS and that are keyed for VIDEO memory applications. All devices meeting this standard must contain all functions which must be implemented as defined in the TRUTH TABLE.
PACKAGE—40 PIN DIP, 0.400" WIDE, 0.100" PIN PITCH
—40 PIN SOJ, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–7A
FUNCTION TRUTH TABLE—Fig. 3.9.4–7B

3.9.4.4 – 2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP2

CAPACITY—2M & 4M WORDS OF 16 or 4M WORDS OF18 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts utilizes 4K or 8K refresh cycles
PACKAGE—50 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH, X16 parts only
PACKAGE—54 PIN TSOP2, 0.500" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–8

3.9.4.5 – 128K & 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, OR ZIP

CAPACITY—128K OR 256K WORDS OF 16 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts have BURST data out capability
PACKAGE—40 PIN SOJ, 10.16 mm WIDE, 1.27 mm PIN PITCH
PACKAGE—44/40 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PIN PITCH
PACKAGE—40 PIN ZIP, 1.27 mm PIN PITCH (256K only)
PIN ASSIGNMENT—SOJ, Fig. 3.9.4–9
PIN ASSIGNMENT—TSOP2, Fig. 3.9.4–10
PIN ASSIGNMENT—ZIP, Fig. 3.9.4–11, (256K ONLY)

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3.9.4.6 – 16M X 16 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 16M WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.4–12

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.7 – 128K AND 256K BY 32 DRAM WITH 4 $\overline{CE}$ IN SSOP

CAPACITY—128K OR 256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—The part, has 4 $\overline{CE}$, one controlling each group of 8 data bits.
PACKAGE— 64 PIN SSOP, 0.525" WIDE, PP = 0.8 mm
PIN ASSIGNMENT—Fig. 3.9.4–13

3.9.4.8 – 512K & 2M BY 32 & 36 DRAM WITH 4 $\overline{CE}$ IN SOJ & TSOP2

CAPACITY—512K, 2M WORDS OF 32 & 36 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—The part, has 4 $\overline{CE}$, one controlling each group of 8 or 9 data bits.
—The standard allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—70 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PP
—70 PIN TSOP2, 10.16 mm WIDE, 0.65 mm PP, 512K only.
—70 PIN SOJ, 10.16 mm WIDE, 0.8 mm PP
PIN ASSIGNMENT—Fig. 3.9.4–14

3.9.4.9 – 8M X 32 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 8M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.4–15

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.10 – 2M X 32 DRAM IN TSOP2

CAPACITY— 8M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—86 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.9.4–16

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MANDATORY TRUTH TABLE FOR 256K BY 16 DRAM with EXTENDED FUNCTIONS

Mnem.	Function	Valid at RE					Valid at CE
		CE	G	W	DSF(1)	*DSF2	DSF(1)
RW	READ/WRITE	1	1	1	0	0	0
BW	BLOCK WRITE	1	1	1	0	0	1
LMR	LOAD MASK REGISTER	1	1	1	1	0	0
LCR	LOAD COLOR REGISTER	1	1	1	1	0	1
RWM	WRITE, MASKED	1	1	0	0	0	0
BWM	BLOCK WRITE, MASKED	1	1	0	0	0	1
CBR	CBR REFRESH (1)	0	X	1	0	0	X
CBRN	CBR REFRESH (2)	0	X	1	1	0	X
FWT	FLASH WRITE	1	1	0	1	0	X

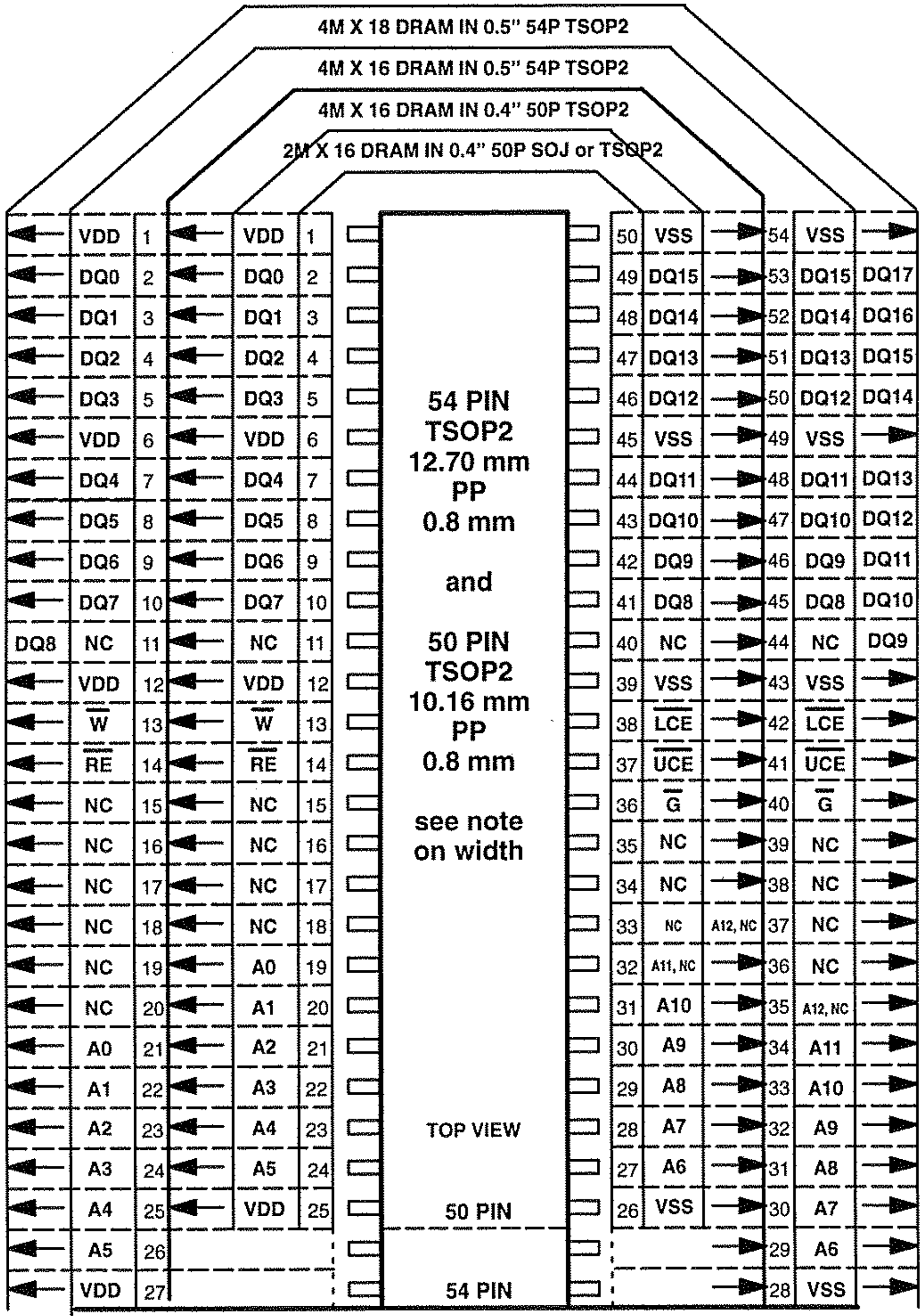
* IF DSF2 IS PRESENT

CBR(1) – All optional modes reset

CBR(2) – Any optional modes remain active

FIGURE 3.9.4–7 B

256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE



	VDD	1	VDD	1	50	VSS		54	VSS	
	DQ0	2	DQ0	2	49	DQ15		53	DQ15	DQ17
	DQ1	3	DQ1	3	48	DQ14		52	DQ14	DQ16
	DQ2	4	DQ2	4	47	DQ13		51	DQ13	DQ15
	DQ3	5	DQ3	5	46	DQ12		50	DQ12	DQ14
	VDD	6	VDD	6	45	VSS		49	VSS	
	DQ4	7	DQ4	7	44	DQ11		48	DQ11	DQ13
	DQ5	8	DQ5	8	43	DQ10		47	DQ10	DQ12
	DQ6	9	DQ6	9	42	DQ9		46	DQ9	DQ11
	DQ7	10	DQ7	10	41	DQ8		45	DQ8	DQ10
DQ8	NC	11	NC	11	40	NC		44	NC	DQ9
	VDD	12	VDD	12	39	VSS		43	VSS	
	$\overline{W}$	13	$\overline{W}$	13	38	$\overline{LCE}$		42	$\overline{LCE}$	
	$\overline{RE}$	14	$\overline{RE}$	14	37	$\overline{UCE}$		41	$\overline{UCE}$	
	NC	15	NC	15	36	$\overline{G}$		40	$\overline{G}$	
	NC	16	NC	16	35	NC		39	NC	
	NC	17	NC	17	34	NC		38	NC	
	NC	18	NC	18	33	NC	A12, NC	37	NC	
	NC	19	A0	19	32	A11, NC		36	NC	
	NC	20	A1	20	31	A10		35	A12, NC	
	A0	21	A2	21	30	A9		34	A11	
	A1	22	A3	22	29	A8		33	A10	
	A2	23	A4	23	28	A7		32	A9	
	A3	24	A5	24	27	A6		31	A8	
	A4	25	VDD	25	26	VSS		30	A7	
	A5	26						29	A6	
	VDD	27						28	VSS	

* NOTES:
For 54P parts, Pin 35 is A12 for 8K rows and NC for 4K rows.

For 50P 4M parts, Pin 33 is A12 for 8K rows and NC for 4K rows. Pin 32 is NC for devices with 11 row & 11 columns and A11 for other Refresh/Address options..

For 50P 2M parts, Pin 32 is A11 for devices with 4K rows and NC for devices with 2K rows.

The use of CBR for Refresh is strongly recommended for these devices.

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

This standard recognizes that some early deliveries of the 54P parts may have to be in a 0.6"wide package

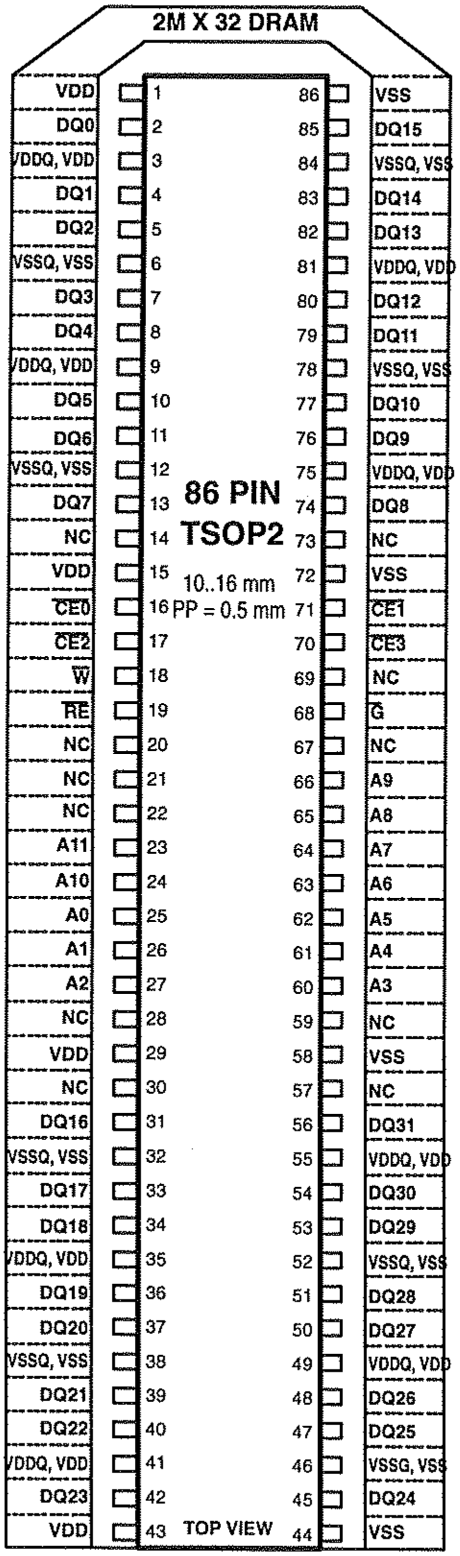
54 P ADDRESS CONFIGURATION

4M X 16/18	4K ROWS	8K ROWS
ROW ADDRESSES	A0 → A11	A0 → A12
COLUMN ADDRESSES	A0 → A9	A0 → A8

50 P ADDRESS CONFIGURATION

2M X 16	2K ROWS	4K ROWS	8K ROWS
ROW ADDRESS	A0 ⇒ A10	A0 ⇒ A11	
COLUMN ADDRESS	A0 ⇒ A9	A0 ⇒ A8	
4M X 16	2K ROWS	4K ROWS	8K ROWS
ROW ADDRESS	A0 ⇒ A10	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESS	A0 ⇒ A10	A0 ⇒ A9	A0 ⇒ A8

FIGURE 3.9.4–8
2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP–2



NOTES
1. The standard refresh period is 64 ms.
2. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally DC isolated from the VDD power supply pins.
3. The VSSQ designator is used when the ground reference pins

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

Configuration	**2M X 32**
ROW COUNT	4K Rows
ROW ADDRESS	A0 ⇒ A11
COLUMN ADDRESS	A0 ⇒ A8

FIGURE 3.9.4-16
2M BY 32 DRAM IN TSOP2

3.9.5.1 – OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM

The definitions for serial data access, bit write, and refresh control included in Release 1 of this standard have been replaced by the more general definitions of Optional Operational Modes and Cycles beginning on page 3.9.5–11

3.9.5.2 – 1M DRAM BUILT IN TEST FUNCTION

An approved option for 1M DRAM (1M X 1 or 256K X 4) is the inclusion of a built in manufacturer defined "Test Mode". This mode is enabled using a dedicated pin which is optional NC or TF. When the optional mode is implemented, the manufacturer should include notes on his data sheet as follows:

(A) Normal operation requires the "TF" pin be connected to a VSS or logic low level or left unconnected.

(B) When the "TF" pin is connected to the manufacturer defined positive voltage, the internal test mode will be actuated. Contact the manufacturer for specific operational details of the Test Mode.

3.9.5.3 – ON–CHIP REFRESH CONTROL FOR X8 DRAM

This standard describes an optional feature that is applicable to the non–address multiplexed byte wide dynamic RAMs described in this publication. The standard establishes the clock timing sequence needed to invoke an on–chip refresh feature.

3.9.5.4 – $\overline{G}$ BEFORE $\overline{E}$ REFRESH

If G is low when E falls, a refresh cycle is executed. During this type of refresh cycle, an internal counter/register provides the refresh address and the external address is ignored

3.9.5.5 – DRAM SPECIAL TEST AND OPERATIONAL MODES

This standard defines a scheme for controlling a series of special operational modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control and exit from the special modes. In addition, it defines a basic test mode plus a series of other special test and operational modes. The details of this standard are given on pages 3.9.5–7 through 3.9.5–10.

3.9.5.6 – NON–MULTIPLEXED DRAM OPERATION

This standard defines multiple aspects of the address and clock relationships for DRAMs that have a non–multiplexed address architecture. It also defines the relationships between the address bits of multiplexed and non–multiplexed devices. The details of the standard are given on page 3.9.5–13

3.9.5.7 – DRAM EXTENDED DATA OUT

This standard defines the output characteristics of Extended Data Out (EDO) feature for DRAMs. Any part encorporating "EDO" must satisfy all of the following criteria to conform to the Standard. The details of the EDO standard are given on P 3.9.5–14

3.9.5.8 – 256M DRAM TEST MODE DATA AND ADDRESS COMPRESSION

This standard defines the algorithms for data and address compression when 256M DRAMs are operated in the built in special test mode. The detaild of the Compression standard are given on P 3.9.5–15

3.9.5.9 – PIPELINED NIBBLE MODE DEFINITION

This standard defines the output characteristics of the Pipelined Nibble Mode feature for DRAMs. Any part encorporating Pipelined Nibble Mode must satisfy all of the following criteria to conform to the Standard. The details of the standard are given on P 3.9.5–16

Pipelined Nibble Mode Definition

Devices that operate in the Pipelined Nibble Mode are required to meet the following criteria to conform to this Standard.

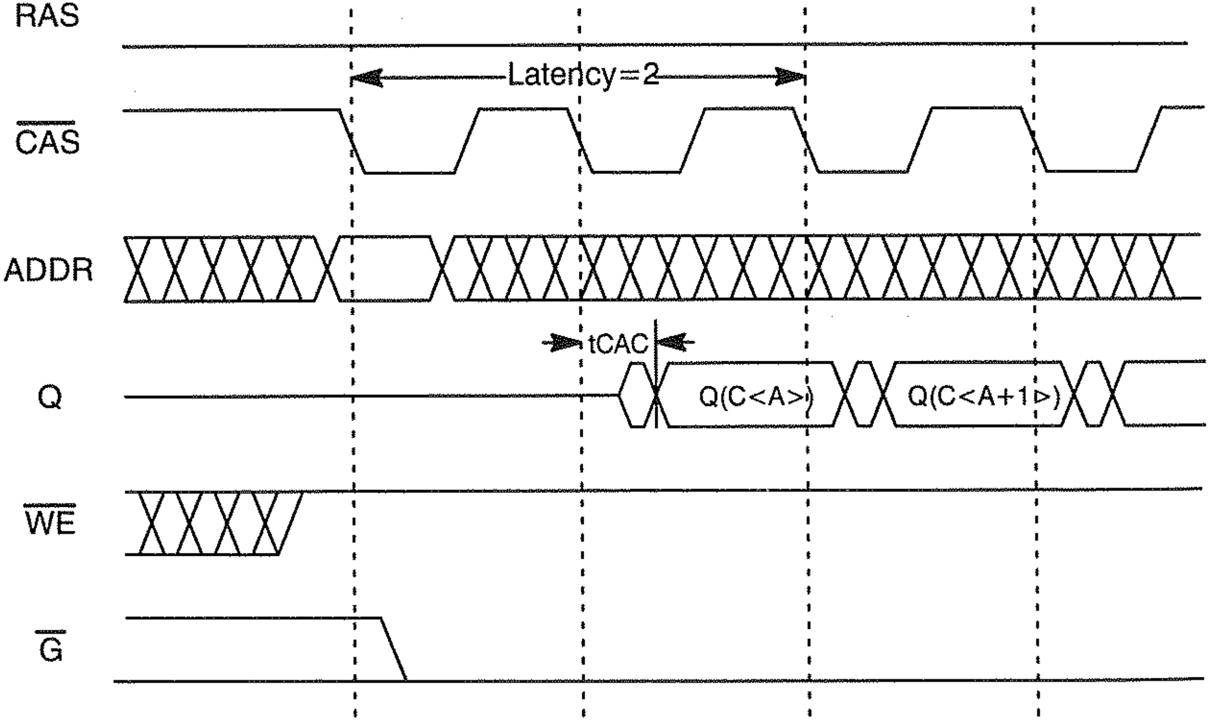
1. Burst Length shall be 4
2. Read Latency shall be 2 (refer to attached timing diagram for clarification)
3. Write Latency shall be 0
4. A WCBR, with the address keys shown below, is used to program the burst sequence. It is persistant until it is reprogrammed.

Address Sequence	A0	A1	A2	A3	A4	A5	A6	A7
Linear	0	0	0	0	0	1	0	0
Interleaved	1	0	0	0	0	1	0	0

5. $\overline{\text{WE}}$ transition during $\overline{\text{CAS}}$ precharge time causes burst to terminate
6. $\overline{\text{WE}}$ transition during $\overline{\text{CAS}}$ low, which remains through the $\overline{\text{CAS}}$ rising edge, causes burst to terminate.
7. $\overline{\text{WE}}$ pulse which is fully enclosed by a $\overline{\text{CAS}}$ low will be ignored and not cause a burst terminate.
8. Same output enable function as in EDO definition.
9. Read–modify–write cycle within $\overline{\text{CAS}}$ active cycle is not supported.
10. A Pipelined Nibble Mode device may not be reconfigured by the user to operate in the standard EDO (non–burst) mode.

FOR REFERENCE ONLY

Pipelined Nibble Mode Read Latency Timing



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256M DRAM Address Compression for Test–Mode

Devices		16K Refresh cycles (RA0–RA13)			8K Refresh cycles (RA0–RA12)		
		Normal Mode Input Addr.	Test Mode		Normal Mode Input Addr.	Test Mode	
			Input Address	Compress. Address		Input Address	Compress. Address
256M	64M X 4	RA0–RA13 CA0–CA11	RA0–RA13 CA0–CA7	CA8–11	RA0–RA12 CA0–CA12	RA0–RA12 CA0–CA8	CA9–12
	32M X 8	RA0–RA13 CA0–CA11	RA0–RA13 CA0–CA7	CA8–10	RA0–RA12 CA0–CA11	RA0–RA12 CA0–CA8	CA9–11
	16M X 16	RA0–RA13 CA0–CA9	RA0–RA13 CA0–CA7	CA8–9	RA0–RA12 CA0–CA10	RA0–RA12 CA0–CA8	CA9–10
	8M X 32	RA0–RA13 CA0–CA8	RA0–RA13 CA0–CA7	CA8	RA0–RA12 CA0–CA9	RA0–RA12 CA0–CA8	CA9

256M DRAM Data Space Compression for Test–Mode

When the memory device is operating in the compression mode, the data space is compressed with four DQn circuits supplying test data and receiving test results as defined in the following table.

Devices		Normal Mode Data Interface	Test Mode Data Interface	
			Active Data Bits	Data Bits Served
256M	64M X 4	DQ0–DQ3	DQ0	DQ0
			DQ1	DQ1
			DQ2	DQ2
			DQ3	DQ3
	32M X 8	DQ0–DQ7	DQ0	DQ0, DQ1
			DQ3	DQ2, DQ3
			DQ5	DQ4, DQ5
			DQ6	DQ6, DQ7
	16M X 16	DQ0–DQ15	DQ0	DQ0⇒DQ3
			DQ7	DQ4⇒DQ7
			DQ11	DQ8⇒DQ11
			DQ12	DQ12⇒DQ15
	8M X 32	DQ0–DQ31	DQ0	DQ0⇒DQ7
			DQ15	DQ8⇒DQ15
			DQ23	DQ16⇒DQ23
			DQ24	DQ24⇒DQ31

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3.10.3 Word Wide MPDRAM & GRAM

3.10.3.1 – 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—SERIAL and RAM data ports
There are two versions of these parts: One with 2 $\overline{W}$ and the other with 2 $\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with 2 W, 256K with 2 CE. .
PACKAGE—64 PIN SOG, 12 mm wide, 0.8 mm pin pitch
PIN ASSIGNMENTS—FIG. 3.10.3–1

3.10.3.2 – 128K & 256K BY 16 MPDRAM IN TSOP–2 WITH MULTIPLE CLOCKS

CAPACITY—128K AND 256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—SERIAL and RAM data ports
There are two versions of these parts: One with 2 $\overline{W}$ and the other with 2 $\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with 2 $\overline{W}$, 128K & 256K with 2 $\overline{CE}$. .
PACKAGE—70 PIN TSOP–2 10.16 mm wide (0.400"), 23.49 mm long. 0.65 mm pin pitch
NOTE: These parts have essentially the same pin rotation as the parts defined in Par. 3.10.3.1 with the exception of the addition of NC pins in the middle.
PIN ASSIGNMENTS—FIG. 3.10.3–2

3.10.3.3 – 256K BY 16 SGRAM IN TSOP–2

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—50 PIN TSOP–2, 10.16 mm wide (0.400"), 0.8 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–3
NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4–1 with the exception of the DSF function on P 33.

3.10.3.4 – 256K BY 32 SGRAM IN QFP or TQFP

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–4
NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4–4 with the exception of the DSF function on P 33.

3.10.3.5 – 256K BY 32 SGRAM IN TSOP2

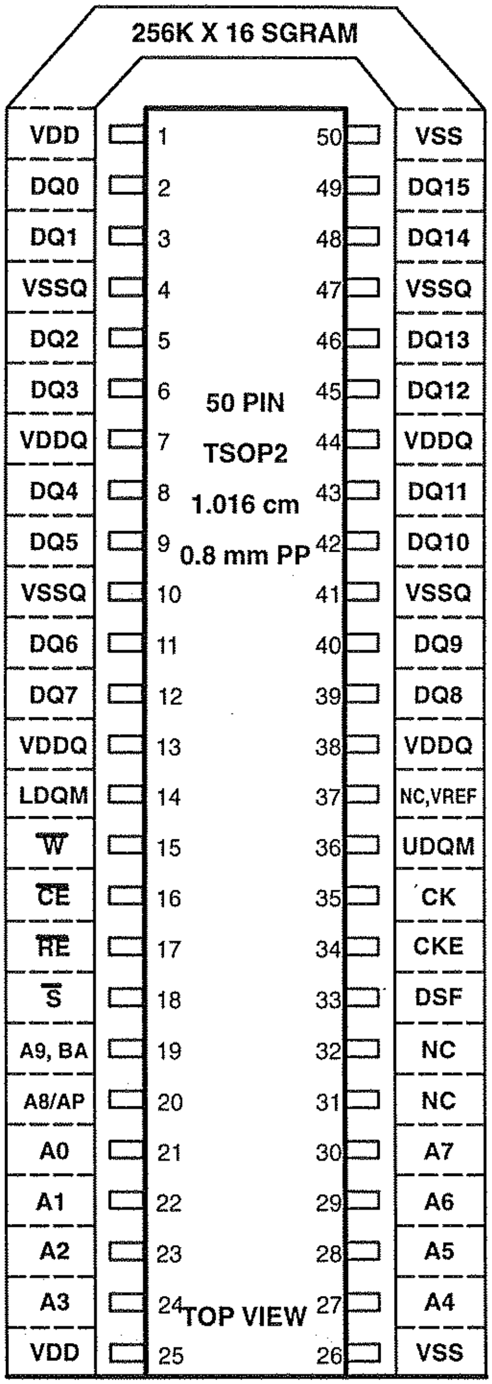
CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—80 PIN TSOP2, 10.16 mm wide (0.400"), 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–5

3.10.3.6 – 256K BY 32 SYNCHRONOUS MPDAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A multiple data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—120 PIN QFP or TQFP, 20 mm X 14 mm, 0.5 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–5

3.10.3.7 – 256K BY 32 SYNCHRONOUS MPDAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A multiple data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–6



This pinout is the same as the one for the 256K X 16 SDRAM shown in Fig. 3.11.4-1 except for the DSF function on pin 33.

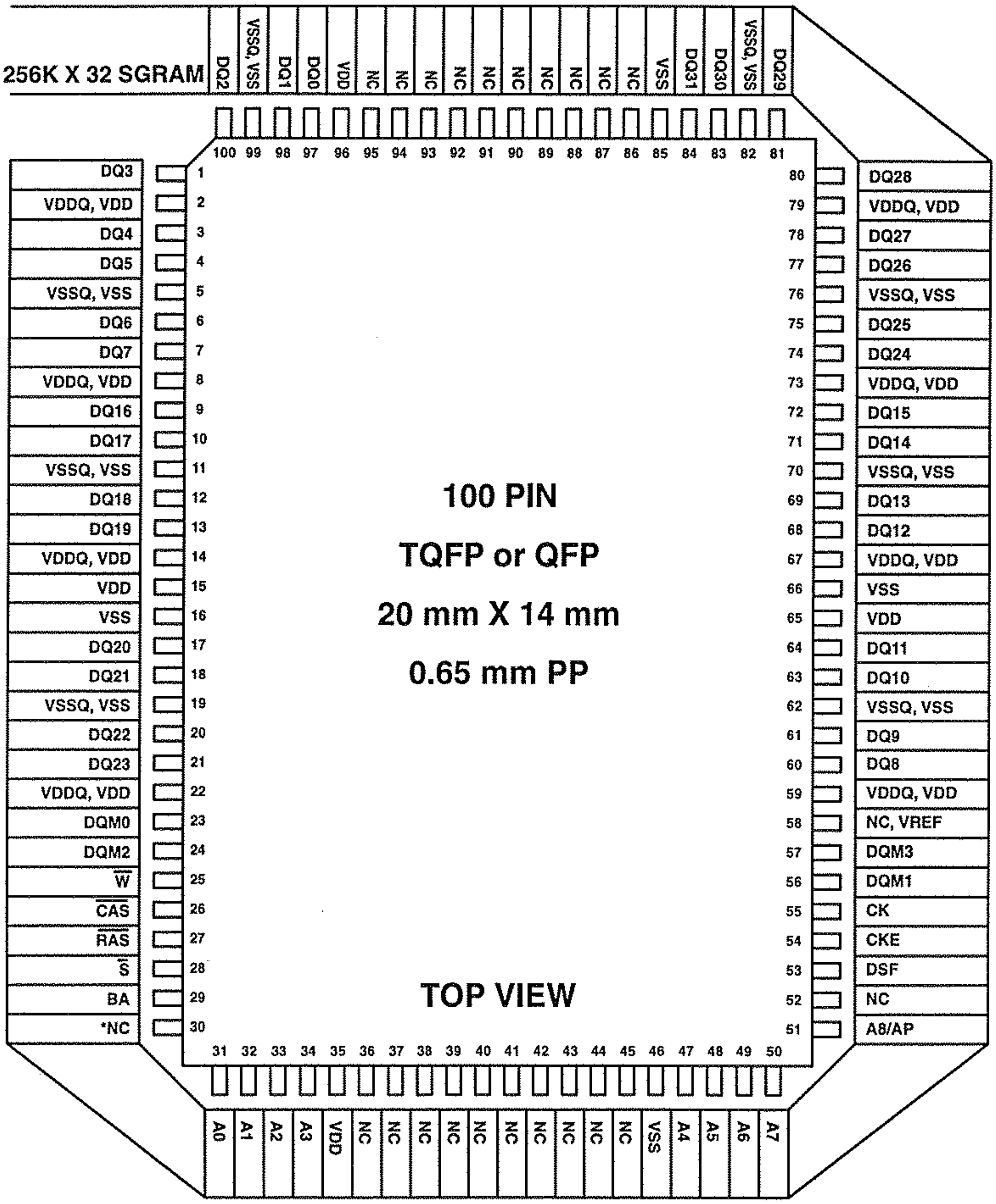
The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

* NOTE—All VDDQ and VSSQ pins may be VDD and VSS at the option of the supplier.

ADDRESS STRUCTURE

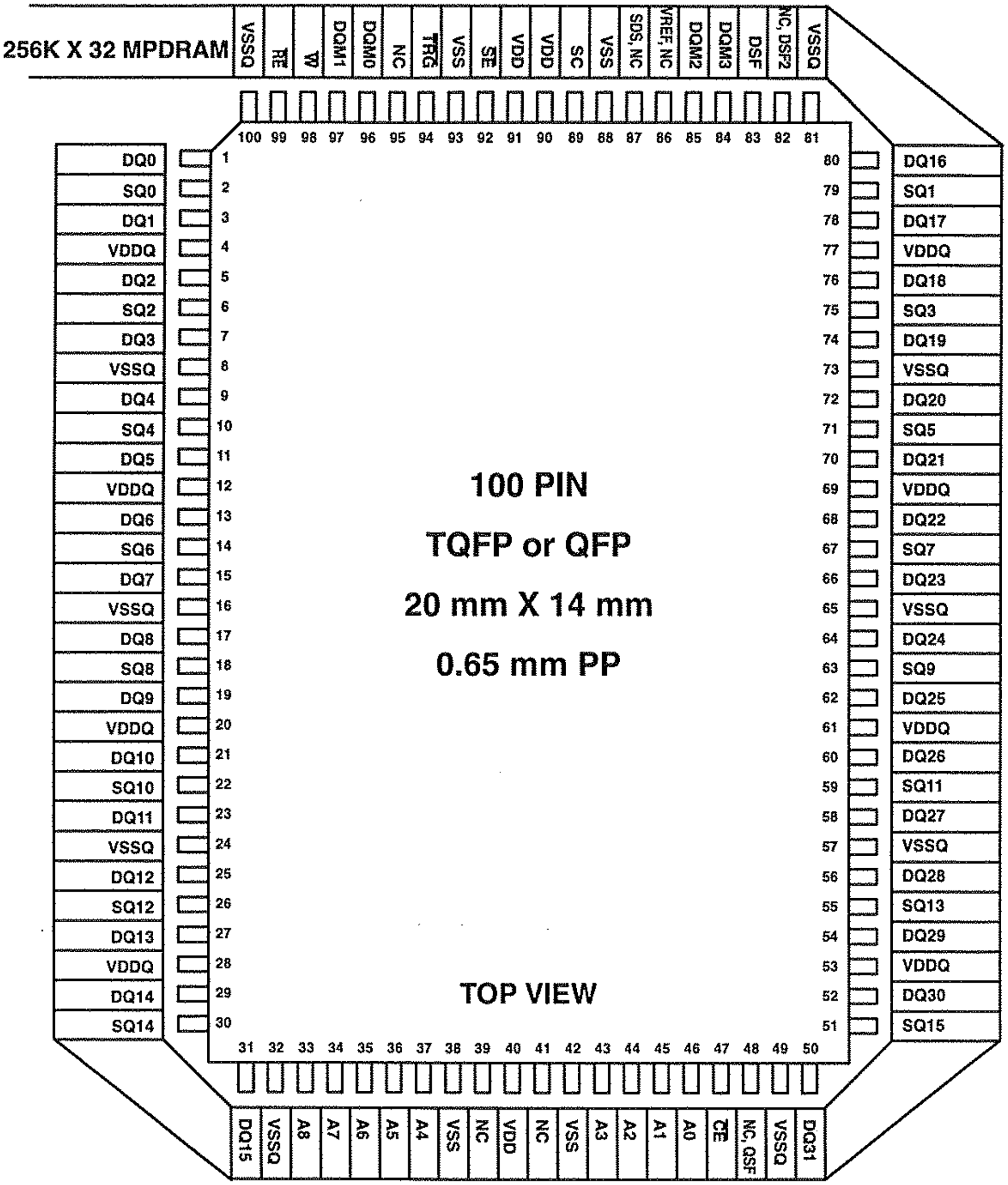
RA	A0 ⇒ A8
CA	A0 ⇒ A7

FIGURE 3.10.3-3
256K BY 16 SGRAM IN TSOP2



* In Release 6, Pin 30 had an optional VREF. This was deleted by action of the Committee in Release 7.

FIGURE 3.10.3-4
256K BY 32 SGRAM IN QFP



Configuration
DRAM = 256K X 32
SAM = 512 X 16
ROW ADDRESS A0⇒A8
COLUMN ADDRESS A0⇒A8

FIGURE 3.10.3–7
256K BY 32 MPDRAM IN QFP

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3.10.4.1 – 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4-1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.2 – 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard, in addition to the minimum feature set defined in Table 3.10.4-1, may contain any of the features described in the Table, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.3 – MPDRAM BIT WRITE OPTIONAL FEATURE

This feature allows individual data bits of a memory array with a multi bit data interface to be selectively modified during a write cycle while other bits remain unchanged. The timing sequence used to control the feature is shown in figure 3.10.4-1 and operates as follows:

1–If W\ is low at the time that RE\ goes low, the state of the individual DQ pins determines if that data bit is to be written.

2–If DQ is HIGH write is ENABLED for that bit and the data present on DQ at the time that CE\ goes low is written.

3–If DQ is LOW, write is DISABLED for that bit and no subsequent writing can occur during that RE\ cycle.

4–If W\ is high at the time that RE\ goes low but goes low later in the cycle, a normal write cycle will be performed and all data bits will be written.

3.10.4.4 – 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 128K BY 8 MPDRAM described in this standard must contain, as a minimum, the feature set described in Table 3.10.4-2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.5 – 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 128K X 8 MPDRAM described in this Standard may, in addition to the minimum feature set defined, contain any of the other features described in Table 3.10.4-2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.6 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 2Mb & 4Mb density MPDRAMs described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4-3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.7 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE INCLUDING REQUIRED MINIMUM OPTIONAL FEATURE SET

The 2Mb & 4Mb density MPDRAMs described in this Standard must, in addition to the minimum basic feature set defined in Par. 3.10.4.6, contain all of the minimum defined set of optional features if any of them are included. In addition, any of the other features described may be included. The basic and optional features are shown in Table 3.10.4-3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. These logic features must operate exactly as defined in the table to conform to the Standard. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM

This standard describes an option internal architectural feature which is applicable to the SERIAL PORT in MPSRAMs. The details are shown in Figure 3.10.4-2.

3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM

This standard describes an option internal architectural feature which is applicable to the SERIAL PORT in MPSRAMs. The details are shown in Figure 3.10.4–2.

3.10.4.9 – PIPELINED FAST PAGE MODE FOR MPDRAM

This standard describes the operational characteristics of an optional serial access data mode for the RAM PORT of MPDRAMs. The details and timing diagrams are given in Figures 3.10.4–3A and 3.10.4–3B.

3.10.4.10 – EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM

The EXTENDED DATA OUT FAST PAGE MODE defined in Sec. 3.9.5, DRAM OPTIONAL Features, on Page 3.9.5–11, Par. 1.4 is also applicable to MPDRAM as is needed. The mode is further defined with timing diagrams in Fig. 3.10.4–4.

3.10.4.11 – SAM OPTIONS FOR 4Mb MPDRAM

For 4 Mb MPDRAMs organized as 256K x 16, there are two options for the length of the SAM (Serial Access Memory). It may be either (1), 256 (Half SAM) or (2), 512 bits (Full SAM) for a 512 Column Page Depth. The details of these two options are described in Figs. 3.10.4–5A and 3.10.4–5B.

3.10.4.12 – Synchronous GRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Graphics DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–6 on Page 3.10.4–15.

3.10.4.13 – Synchronous MPDRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Multiport DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–7 on Page 3.10.4–16.

3.10.4.14 – Synchronous GRAM OPERATIONAL FUNCTION TABLES

This standard gives a set of functional truth tables for Synchronous Graphics DRAM. Three truth tables are given that define all standard operational functions. They are given in Tables 3.10.4–4A⇒C on Pages 3.10.4–17⇒19.

3.10.4.15 – 8Mb MPDRAM FEATURE SET FUNCTION TABLE

The 8Mb MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–15 on Page 3.10.4–8. This standard applies to devices with any interface data word length.

3.10.4.16 – Extended Functions for SGRAM and MPDRAM.

These standards define two special write function operations for SGRAM and MPDRAM. The functions defined are:

Write–Per–Bit
Block Write

These logic features must operate exactly as defined in the table to conform to the Standard. Details of the standards are given on Page 3.10.4–6.

SGRAM FUNCTION TABLE

CURRENT STATE	$\overline{S}$	$\overline{TR}$	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	X	H	L	X	BA, CA	ILLEGAL[2]
	L	L	X	H	L	H	CA	Latch Tap Address[7]
	L	H	L	L	H	H	BA, RA	Row (&Bank) active; Latch Row Address; No Mask
	L	H	H	L	H	H	BA, RA	Row (&Bank) active; Latch Row Address; Use Mask
	L	L	L	L	H	H	BA, RA	Read Transfer; Latch Row Address ⇒ Precharge
	L	L	H	L	H	H	BA, RA	Split Read Transfer; Latch Row Address ⇒ Precharge
	L	H	L	L	H	L	BA, AP	NOP[4]
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	H	L	L	L	H	X	Auto–Refresh[6]
	L	H	H	L	L	H	X	ILLEGAL
	L	L	X	L	L	H	X	ILLEGAL
	L	H	L	L	L	L	Op–code	Mode Register Access[6]
	L	H	H	L	L	L	Op–code	Special Register Access[5]
	L	L	X	L	L	L	X	ILLEGAL
ROW ACTIVE	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	L	H	L	H	BA, CA, AP	Begin Read; Latch CA; Determine AP
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Begin Write; Latch CA; Determine AP
	L	H	H	H	L	L	BA, CA, AP	Block Write; Latch CA; Determine AP
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Precharge
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	X	X	L	L	H	X	ILLEGAL
	L	H	L	L	L	L	Op–code	ILLEGAL
	L	H	H	L	L	L	Op–code	Special Register Access[5]
	L	L	X	L	L	L	X	ILLEGAL

TABLE 3.10.4–4 A
SGRAM FUNCTION TABLE

SGRAM FUNCTION TABLE (continued)

CURRENT STATE	$\overline{S}$	TR	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
READ	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Row Active)
	L	X	X	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	L	H	H	L	X	RESERVED (Term. Burst);⇒Row Active
	L	H	H	H	H	L	X	ILLEGAL
	L	L	X	H	H	L	X	ILLEGAL
	L	H	L	H	L	H	BA, CA, AP	Term Burst, New Read, Determine AP[3]
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Term Burst, Start Write, Determine AP[3]
	L	H	H	H	L	L	BA, CA, AP	Term Burst, Start Write, Determine AP[3]
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Term Burst, Precharge Timing for Reads
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	X	X	L	L	X	X	ILLEGAL
WRITE	H	X	X	X	X	X	X	NOP(Continue Burst to End;⇒Row Active)
	L	X	X	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	L	H	H	L	X	RESERVED (Term Burst);⇒Row Active
	L	H	H	H	H	L	X	ILLEGAL
	L	L	X	H	H	L	X	ILLEGAL
	L	H	L	H	L	H	BA, CA, AP	Term Burst, Start Read, Determine AP[3]
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Term Burst, New Write, Determine AP[3]
	L	H	H	H	L	L	BA, CA, AP	Term Burst, Block Write, Determine AP[3]
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Term Burst, Precharge[3]
	L	X	X	L	L	X	X	ILLEGAL
READ with AUTO Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	H	BA, CA, AP	ILLEGAL[2]
	L	X	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	X	BA, RA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL
WRITE with AUTO Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	H	BA, CA, AP	ILLEGAL[2]
	L	X	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	X	BA, RA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL

TABLE 3.10.4–4 B
SGRAM FUNCTION TABLE (Continued)

SGRAM FUNCTION TABLE (continued)

CURRENT STATE	$\overline{S}$	TR	$\overline{DSF}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H	X	X	X	X	X	X	NOP⇒idle after tRP
	L	X	X	H	H	H	X	NOP⇒idle after tRP
	L	X	X	H	H	L	X	ILLEGAL^2
	L	H	X	H	L	X	BA, CA, AP	ILLEGAL^2
	L	L	X	H	L	H	CA	Latch Tap Address^7
	L	X	X	L	H	H	BA, RA	ILLEGAL^2
	L	X	X	L	H	L	BA, AP	NOP^4
	L	X	X	L	L	X	X	ILLEGAL
ROW Activating	H	X	X	X	X	X	X	NOP⇒Row Active after tRCD
	L	X	X	H	H	H	X	NOP⇒Row Active after tRCD
	L	X	X	H	H	H	X	ILLEGAL^2
	L	X	X	H	L	X	BA, CA, AP	ILLEGAL^2
	L	X	X	L	H	H	BA, RA	ILLEGAL^2
	L	X	X	L	H	L	BA, AP	ILLEGAL^2
	L	X	X	L	L	X	X	ILLEGAL
WRITE Recovering	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL^2
	L	X	X	H	L	X	BA, CA, AP	ILLEGAL^2
	L	X	X	L	H	H	BA, RA	ILLEGAL^2
	L	X	X	L	H	L	BA, AP	ILLEGAL^2
	L	X	X	L	L	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	X	NOP⇒idle after tRP
	L	X	X	H	H	X	X	NOP⇒idle after tRP
	L	X	X	H	L	X	X	ILLEGAL
	L	X	X	L	H	X	X	ILLEGAL
	L	X	X	L	L	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL
	L	X	X	H	L	X	X	ILLEGAL
	L	X	X	L	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address
CA = Column Address
BA = Bank Address
AP = Auto Precharge
Term = Terminate
NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n–rule", bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and AP).
5. Legal only if all banks are in idle or row active state.
6. Illegal if any bank is not idle.
7. Illegal if any bank is not idle or precharging.

ILLEGAL = Device operation and/or data–integrity are not guaranteed

TABLE 3.10.4–4 C
SGRAM FUNCTION TABLE (Continued)

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8M BURST MPDRAM FUNCTION TABLE

8 Mb BURST MPDRAM FUNCTION TRUTH TABLE													
CYCLE	$\overline{RE}$ Fall					$\overline{CE}$		A(n)		DQ(n)			
CODE	$\overline{CE}$	TRG	$\overline{W}$	DSF1	DSF2	DSF1	DSF2	$\overline{RE}$	$\overline{CE}$.	$\overline{RE}$	$\overline{CE}$	DQM	FUNCTION
OPTION	0	0	0	0	0	—	0	MODE	—	X	—	X	OPTIONAL
CBRR	0	X	1	0	0	—	0	X	—	X	—	X	CBR REFRESH (OPTION RESET)
CBRS	0	X	0	1	0	—	0	STOP Addr	—	X	—	X	CBR REFRESH STOP POINT SET
CBRSD	0	X	0	1	1	—	0	X	—	X	—	X	CBR REFRESH SDS MODE SET
CBRN	0	X	1	1	0	—	0	X	—	X	—	X	CBR REFRESH NO RESET
RT	1	0	1	0	0	0	0	ROW	TAP	X	X	X	READ TRANSFER CYCLE
SRT	1	0	1	1	0	0	0	ROW	TAP	X	X	X	SPLIT READ TRANSFER CYCLE
RWM	1	1	0	0	0	0	0	ROW	COL	WPBM	DATA IN	DQM	READ MASKED WRITE CYCLE
BRWM	1	1	0	0	1	0	0	ROW	COL	WPBM	DATA IN	DQM	BURST READ MASKED WRITE CYCLE
BWM	1	1	0	0	0	1	0	ROW	CA3–CA8 CA0=CR	WPBM	COL ADDR MASK	DQM	MASKED BLOCK WRITE CYCLE
RW	1	1	1	0	0	0	0	ROW	COL	X	DATA IN	DQM	READ WRITE CYCLE (NO MASK)
BRW	1	1	1	0	1	0	0	ROW	COL	X	DATA IN	DQM	BURST READ WRITE CYCLE (NO MASK)
BI	—	—	—	—	—	0	1	ROW	COL	X	X	X	BURST INTERRUPT
BW	1	1	1	0	0	1	0	ROW	CA3–CA8 CA0 = CR	X	COL ADDR. MASK	DQM	BLOCK WRITE
LCR	1	1	1	1	0	1	0	ROW	CA0 = CR	X	COLOR	DQM	LOAD COLOR REGISTER
LMR	1	1	1	1	0	0	0	ROW	X	X	WPBM	DQM	LOAD MASK REGISTER

X = Don't care 0 or 1 — = NOT APPLICABLE

NOTES: CR = 0 selects Color Register 0 CR = 1 selects Color Register 1
All states not defined are illegal. If used, device operation and/or data integrity are not guaranteed.

BYTE ENABLE TRUTH TABLE		
		$\overline{CE}$ FALLING
DQM0–DQM3		
DQM0	0	Byte Write Enable (DQ0–DQ7)
	1	Byte Write Disable (DQ0–DQ7)
DQM1	0	Byte Write Enable (DQ8–DQ15)
	1	Byte Write Disable (DQ8–DQ15)
DQM2	0	Byte Write Enable (DQ16–DQ23)
	1	Byte Write Disable (DQ16–DQ23)
DQM3	0	Byte Write Enable (DQ24–DQ31)
	1	Byte Write Disable (DQ24–DQ31)

8MB BURST MPDRAM FUNCTION TABLE
TABLE 3.10.4–5

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Extended Functions for SGRAM and SVRAM

WRITE–PER–BIT WPB, for Synchronous Video RAMs (SVRAM), and Synchronous Graphics RAMs (SGRAM) is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when enabled.

1) A Bank Active Command with DSF = 1 (high) enables Write–per–bit for the associated bank. A bank active command with DSF = O (low) disables Write–Per–BIt for the associated bank.

2) The mask used for Write per–bit operations is stored in the Mask Register accessed by Special Register Access command. When a mask bit = 1 (high), the associated data bit is written when a Write Command is executed and Write–per–bit has been enabled for the bank being written. When a mask bit = O (low) the associated data bit is unaltered when a Write Command is executed and Write–per–bit has been enabled for the bank being written.

3) No additional, timing conditions are required for Write per–bit operations. Write–per–bit writes can be either single writes, burst writes, or block writes.

4) DQM masking is the same for WPB and non–WPB writes.

BLOCK WRITE for Synchronous Multi–port DRAMs (SMPRAM), and Synchronous Graphics RAMs (SGRAM). A feature allowing the simultaneous writing of consecutive columns of data within RAM device during a single access cycle. During block write the data to be written comes from an internal "color" register and the DQ I/O pins are used for independent column selection. The block of columns to be written is aligned on 8 column boundaries and is defined by the column address with the 3 LSB's ignored.

1) A Write Command with DSF = 1 (high) enables Block Write for the associated bank. A Write Command with DSF = O (low) disables Block Write for the associated bank.

2) The block size is 8 columns. Where column = "n" bits for by "n" part.

3) The Color Register is the same width as the data port of the part. It is written via a special register access where data present on the DQ pins is copied into the internal color register. The color register provides the data to be copied to the 8 column locations during a block write cycle as masked by the DQ column select, WPB mask (if enabled), and DQM byte mask.

4) Column data masking is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per byte basis (i.e. DQ[0:7] provides the column mask for data byte [0;7], DQ[8.15] provides the column mask for data byte [8:15] and so on). A DQ column mask of 1 (high) enables the particular column to be written while a value of 0 (low) disables writing of the data. The relationship between DQ bits and column within the block is logically equivalent within each byte (i.e. DQ[0] masks column [0] for data bits [0:7] DQ[8] masks column [0] for data bits [8:15], DQ[1] masks column [1] for data bits [0:7], DQ[9] masks column [1] for data bits 18:15], etc.).

5) Block Writes are always non–burst, independent of the burst length that has been programmed into the Mode Register. Back–to–back Block Writes are allowed provided that the specified Block Write cycle time is satisfied.

6) If Write–per–bit was enabled to the bank by executing a Bank Active Command with DSF=1 (high), then write–per–bit masking of the Color Register data is enabled. If Write–per–bit was disabled to the bank by executing a Bank Active Command with DSF=O (Low), then write–per–bit masking of the color Register data is disabled.

7) DQM masking provides independent data byte masking during block write exactly the same as It does during normal write operations, except that the control is extended to the 8 consecutive columns of the block write.

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3.11.2 NIBBLE WIDE SDRAM

3.11.2.1 – 4M BY 4 SDRAM IN TSOP2

CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—44 Pin TSOP2, 7.62 mm or 10.16 mm WIDE, 0.8mm PIN PITCH
—44 Pin SOJ 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.2–1

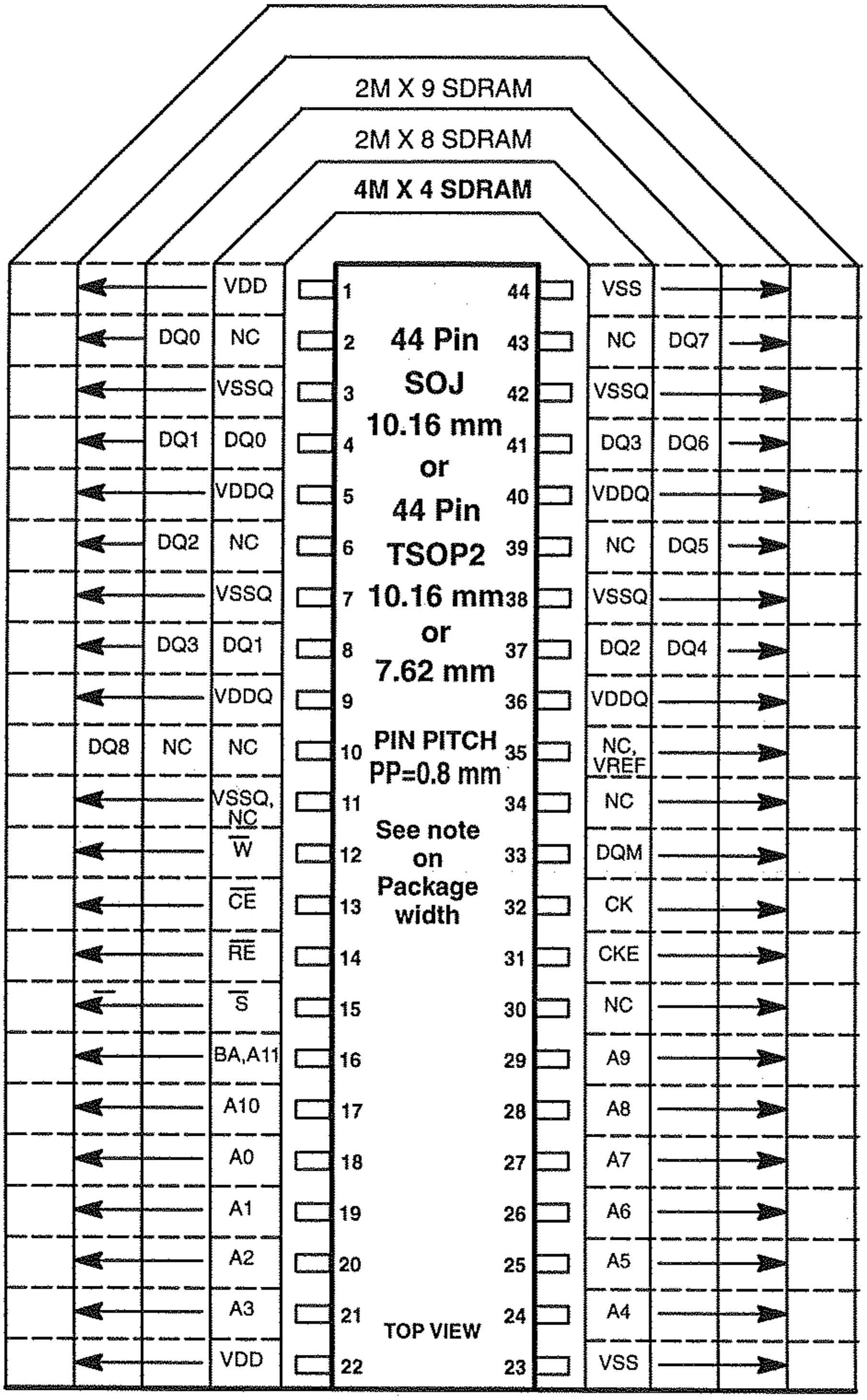
3.11.2.2 – 16M BY 4 SDRAM IN TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.2–1

3.11.2.3 – 64M BY 4 SDRAM PIN ROTATION

CAPACITY—64M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.2–5

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

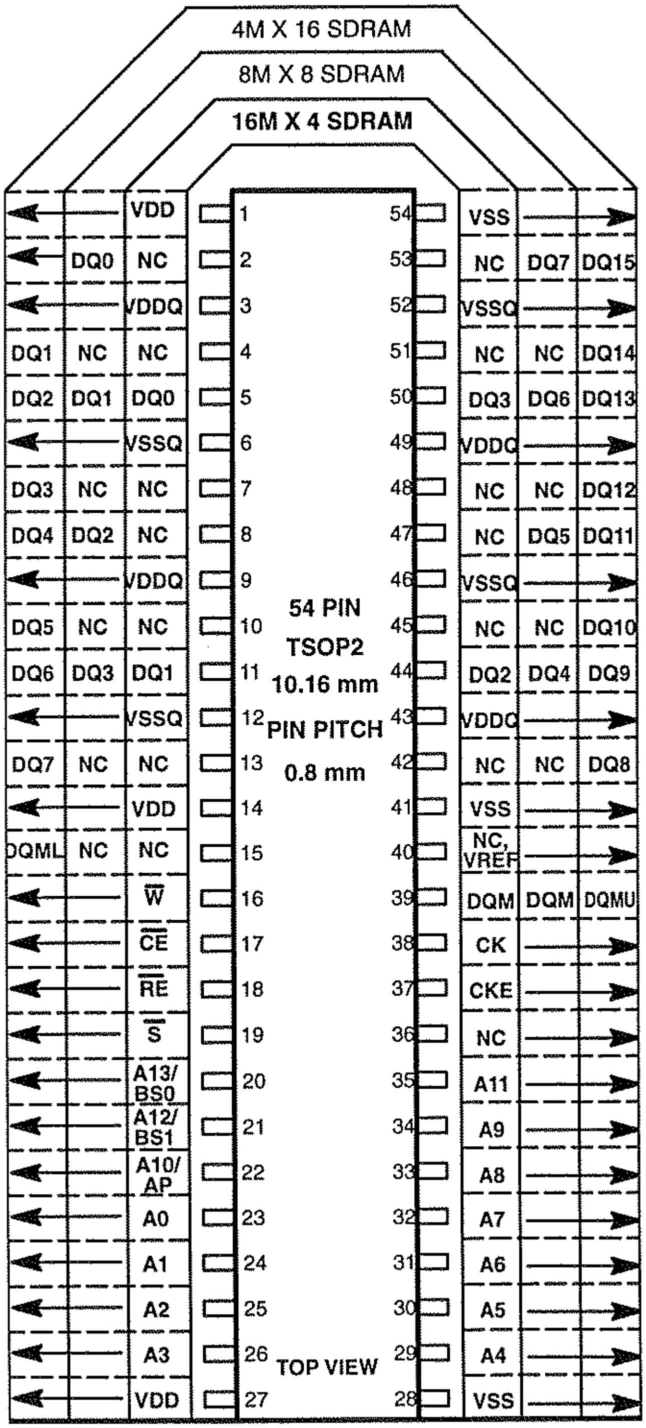


CONFIGURATION	4M X 4	2M X 8/9
ROW ADDRESS	A0 TO A11	A0 TO A11
COLUMN ADDRESS	A0 TO A9 & A11	A0 TO A8 & A11

Notes:
1) The VREF option on P35 was added when the 0.3" package was approved.

2) The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G
The 4M X 4 and 2M X 8 parts are also approved for delivery in a 7.62 mm package.

FIGURE 3.11.2–1
4M X 4 SDRAM IN TSOP2



	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16	A0⇒A13	A0⇒A7

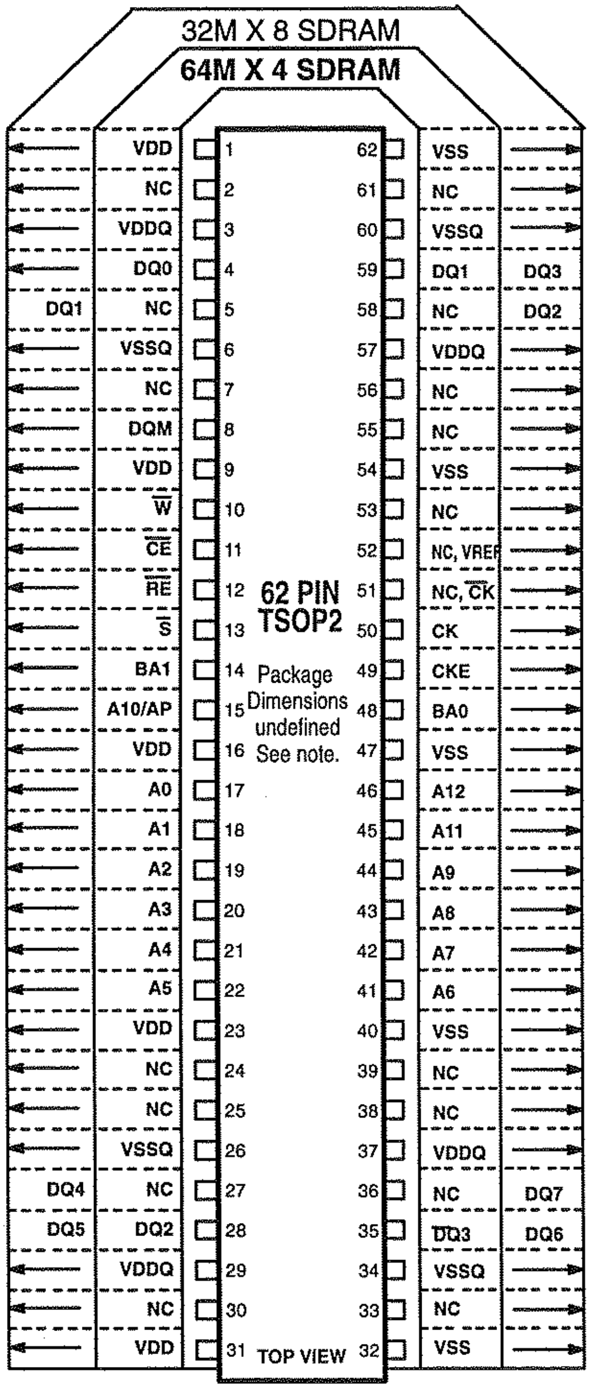
A10	AUTO PRECHARGE

BANKS	BANK SELECT ADDRESS
4	A13/A12
2	A13

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.2–2
16M BY 4 SDRAM IN TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non-synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS).

7. BA0 is the Least Significant Bank Addr.

8. BA1 is the Most Significant Bank Addr.

9. A10/AP is row addr. A10, autoprecharge and precharge all banks input.

* NOTE: The JEDEC Std. 0 term for the TSOP-2 package is PDSO-G.

Configuration	**64M X 4**	**32M X 8**
ROW ADDRESS	A0⇒A12	A0⇒A12
COLUMN ADDRESS	A0⇒A9,A11	A0⇒A9

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.2-3
64M BY 4 SDRAM PIN ROTATION IN TSOP2

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3.11.3 BYTE WIDE SDRAM

3.11.3.1 – 2M BY 8 or 9 SDRAM IN TSOP2

CAPACITY—2M WORDS OF 8 or 9 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LVTTL
PACKAGE—44 Pin TSOP2, 7.62 mm WIDE, 0.8mm PIN PITCH (2M X 8 part only)
PACKAGE—44 Pin TSOP2, 10.16 WIDE, 0.8mm PIN PITCH
PACKAGE—44 Pin SOJ, 10.16 WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.3–1

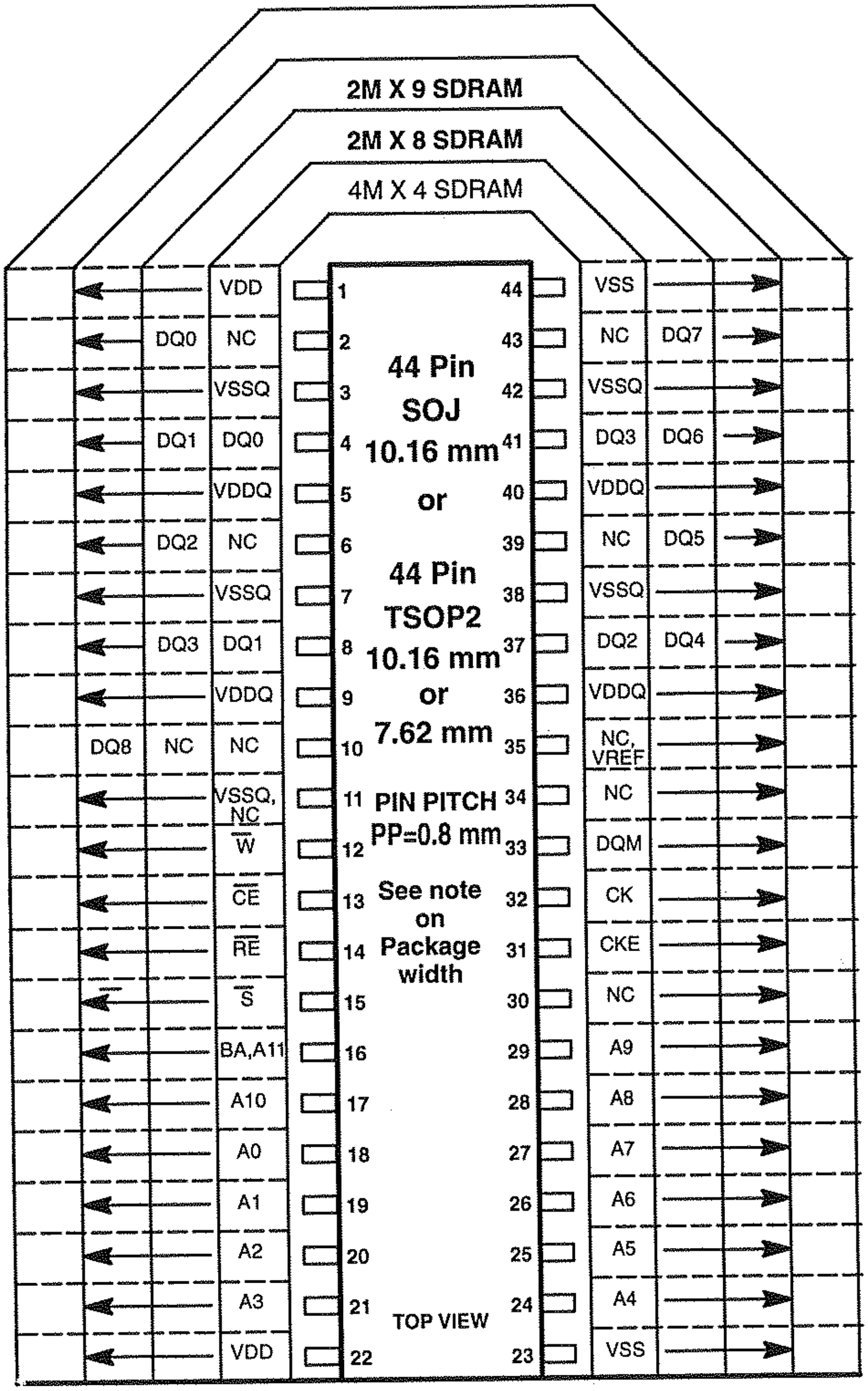
3.11.3.2 – 8M BY 8 SDRAM IN TSOP2

CAPACITY—8M WORDS OF 8 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.3–2

3.11.3.3 – 32M BY 8 SDRAM PIN ROTATION

CAPACITY—32M WORDS OF 8 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.3–5

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.



CONFIGURATION	4M X 4	2M X 8/9
ROW ADDRESS	A0 TO A11	A0 TO A11
COLUMN ADDRESS	A0 TO A9 & A11	A0 TO A8 & A11

Notes:
1) The VREF option on P35 was added when the 0.3" package was approved.

2) The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G
The 4M X 4 and 2M X 8 parts are also approved for delivery in a 7.62 mm package.

FIGURE 3.11.3–1
2M BY 8 OR 9 SDRAM IN TSOP2

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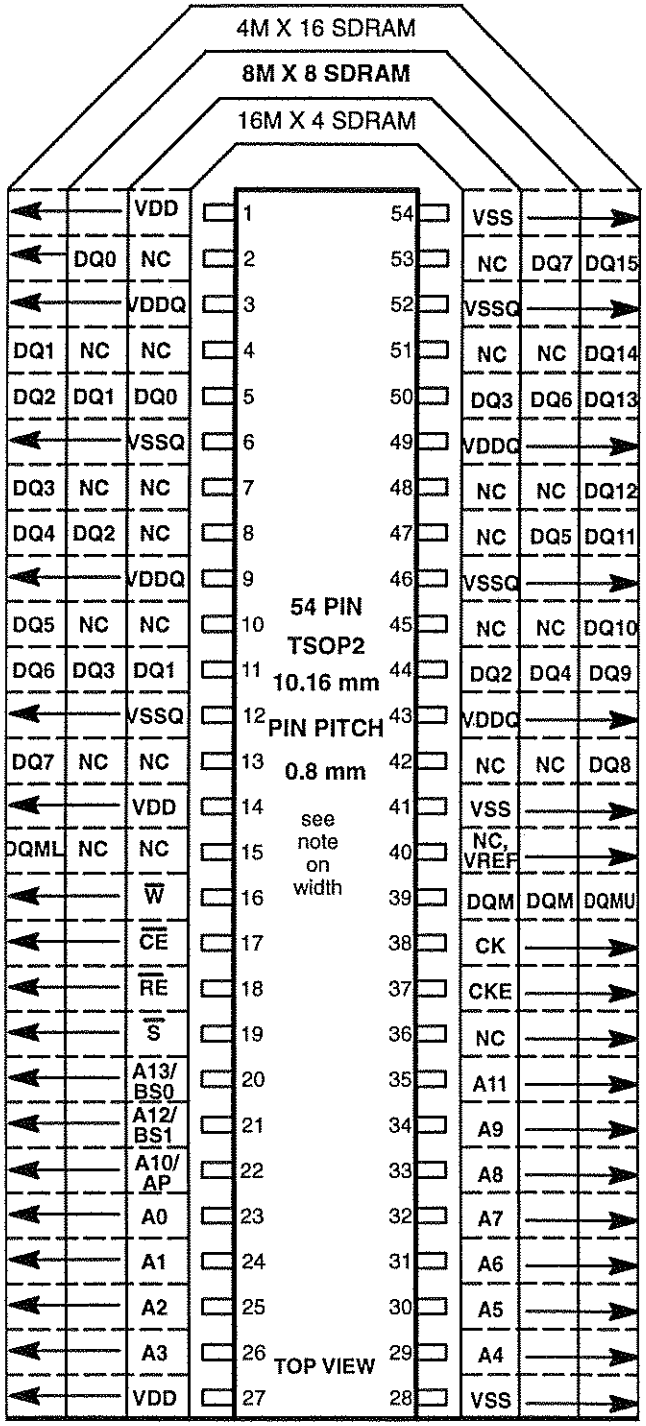


	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16	A0⇒A13	A0⇒A7

A10	AUTO PRECHARGE

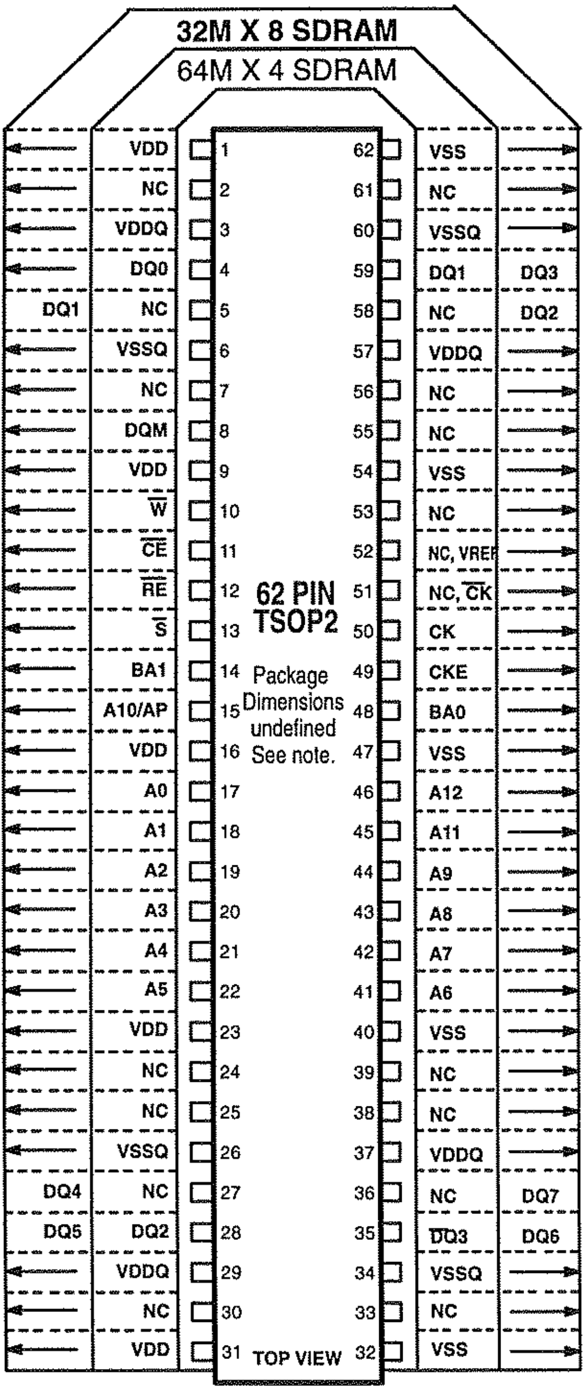
BANKS	BANK SELECT ADDRESS
4	A13/A12
2	A13

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.3–2
8M BY 8 SDRAM IN TSOP2

jCS



Configuration	64M X 4	32M X 8
ROW ADDRESS	A0⇒A12	A0⇒A12
COLUMN ADDRESS	A0⇒A9,A11	A0⇒A9

NOTES

1. **Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.**
2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 μs per row with 8K rows, 3.9 μs with 16K rows.
4. (NC, VREF) is VREF on devices that require an external voltage reference.
5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.
6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS).
7. BA0 is the Least Significant Bank Addr.
8. BA1 is the Most Significant Bank Addr.
9. A10/AP is row addr. A10, autoprecharge and precharge all banks input.

* NOTE: The JEDEC Std. 0 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.3–3
32M BY 8 SDRAM PIN ROTATION IN TSOP2

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3.11.4 WORD WIDE SDRAM

3.11.4.1 – 256K BY 16 AND 1M BY 16 & 18 SDRAM IN TSOP2

CAPACITY—256K WORDS OF 16 BITS AND 1M WORDS OF 16 OR 18
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LOWER LEVEL INTERFACE CONSISTENT WITH THE VALUE OF VDD CHOSEN.
PACKAGE—50 Pin SOJ, 10.16 mm WIDE, 0.8mm PIN PITCH
PACKAGE—50 Pin TSOP2, 0.400" WIDE (10.16 mm), 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.4–1

NOTE: The 256K part has the same pinout as the SGRAM part shown in Fig. 3.10.3–3 with the exception of the DSF function on P 33.

3.11.4.2 – 2M & 4M BY 16 SDRAM IN TSOP2

CAPACITY—2M or 4M WORDS OF 16 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.4–2

3.11.4.3 – 16M BY 16 SDRAM IN TSOP2 PIN ROTATION

CAPACITY—16M WORDS OF 16 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.4–3

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.11.4.4 – 256K BY 32 SDRAM IN QFP or TQFP

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.11.4–4

NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.10.3–4 with the exception of the DSF function on P 33.

3.11.4.5 – 2M BY 32 SDRAM IN TSOP2

CAUTION: See note in Fig. 3.11.4–5 regarding the use of this device.
CAPACITY—2M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—Synchronous address & control interface.
PACKAGE—84 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP
PIN ASSIGNMENTS—FIG. 3.11.4–5

3.11.4.6 – 8M BY 32 SDRAM IN TSOP2 PIN ROTATION

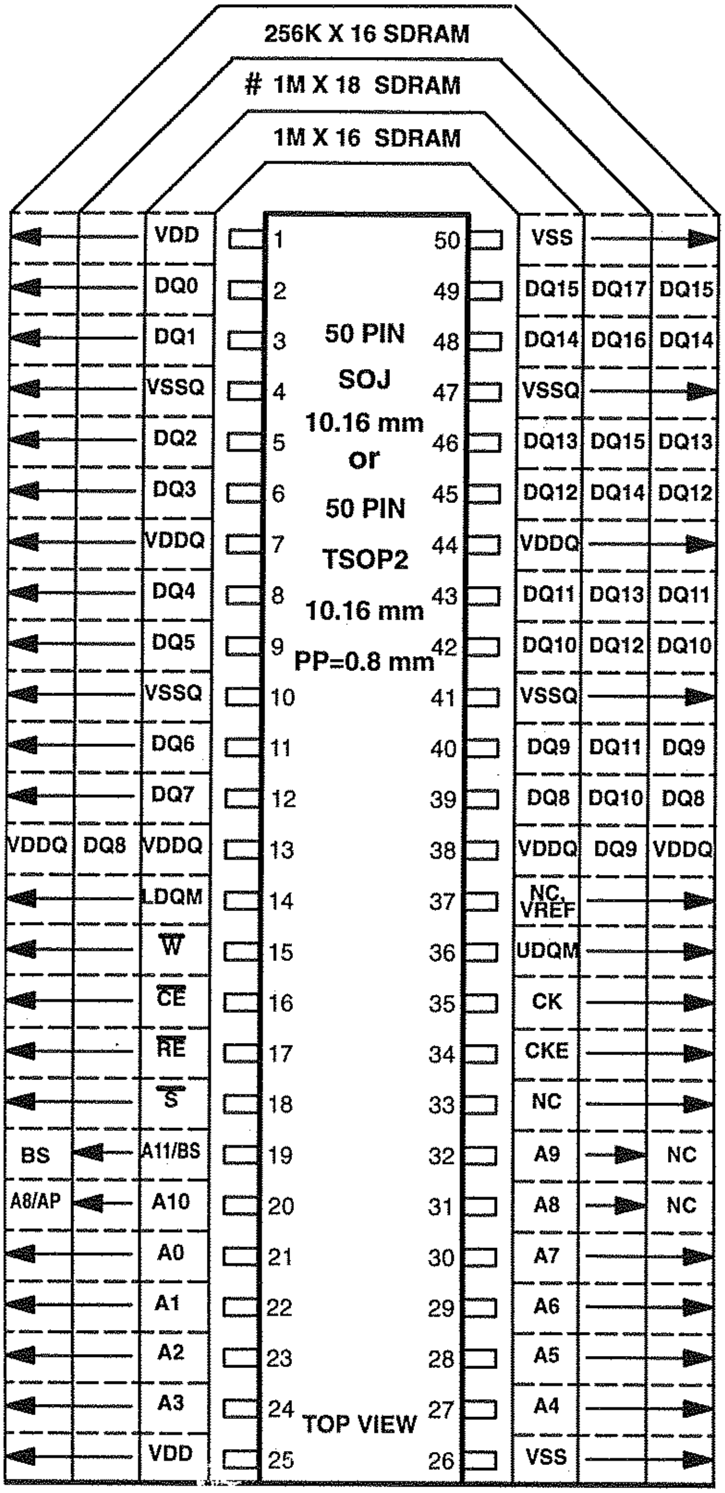
CAPACITY—8M WORDS OF 32 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.4–6

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

1Ch1

3.11.4.7 – 2M BY 32 & 36 SDRAM IN TSOP2

CAPACITY—8M WORDS OF 32 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—86 PIN TSOP2, 10.16 mm Wide, 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.11.4–7



	256K	1M 1K RFSH	1M 4K RFSH
ROW/REFRESH ADDRESSES	A0 ⇒ A8	A0 ⇒ A9	A0 ⇒ A11
COLUMN ADDRESSES	A0 ⇒ A7	A0 ⇒ A9	A0 ⇒ A7

FIGURE 3.11.4–1
256K X 16 & 1M X 16/18 SDRAM IN SOJ & TSOP–2

* Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

1) Pin 20 (A10) id the auto–precharge input during read and write commands.

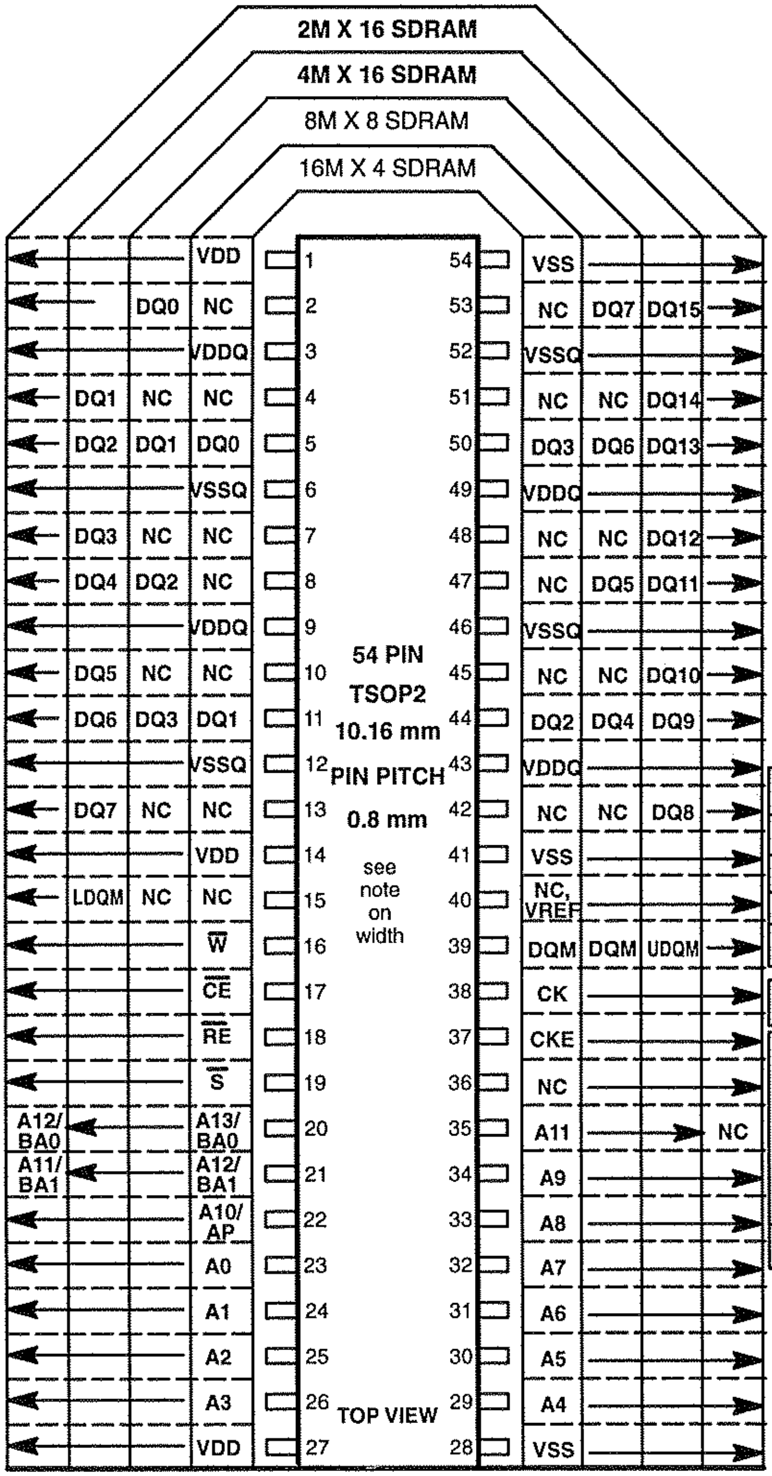
2) Pin 37 (NC, VREF) is VREF on devices that need an external voltage reference. On other devices, it is a NC.

3) All VDDQ and VSSQ pins may be VDD and VSS at the option of the supplier

4) BS is the Bank Select Address

5) The 256K device has the same pinout as the 256K X 16 SGRAM shown in Fig 3.10.3–3 except for the lack of a DSF function on pin 33.

\# The 1M X 18 device is approved for use in the TSOP2 package only.



Device	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16, 4M	A0⇒A13	A0⇒A7
X16, 2M	A0⇒A12	A0⇒A7

A10	AUTO PRECHARGE

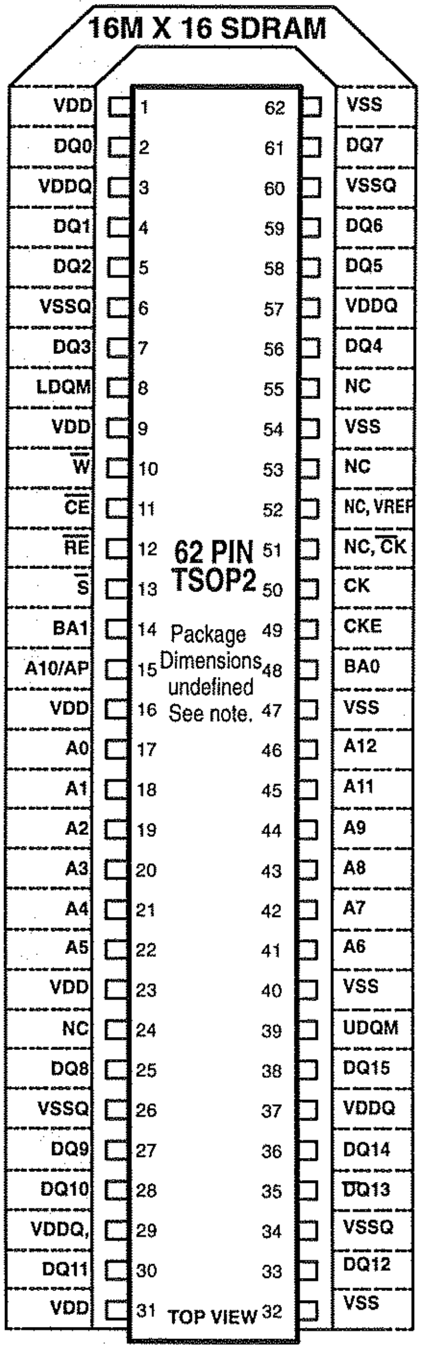
BANKS	BANK SELECT ADDRESS
4	A13/A12
4 #	A12/A11
2	A13
2 #	A12

2M X 16

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.4–2
2M & 4M BY 16 SDRAM IN TSOP2



Configuration	**16M X 16**
ROW ADDRESS	A0–A12
COLUMN ADDRESS	A0–A8

NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. The standard refresh interval (tREF) for 256Mb SDRAMs is 64ms.

3. (NC, VREF) is VREF on devices that require an external voltage reference.

4. BA0 is the least significant bank address

5. BA1 is the most significant bank address

6. A10/AP is row address A10, autoprecharge and precharge all banks.

7. (NC, C̅K̅) is NC for devices using a single ended clock. C̅K̅ is used for devices using a differential clock.

8. (NC, VREF) is VREF on devices that require an external voltage reference.

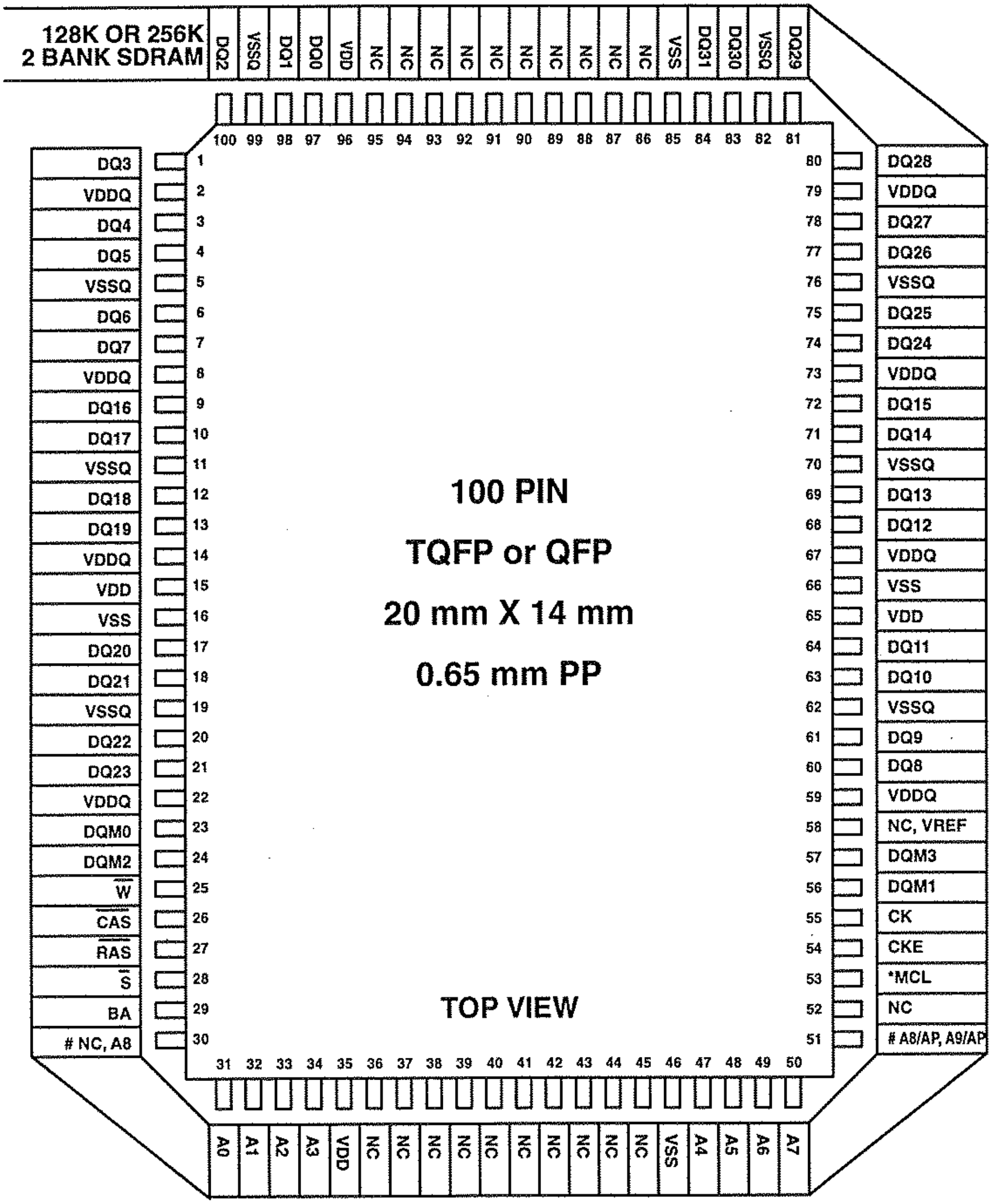
9. This standard is for a 4 Bank version only.

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4–3

16M BY 16 SDRAM PIN ROTATION IN TSOP2



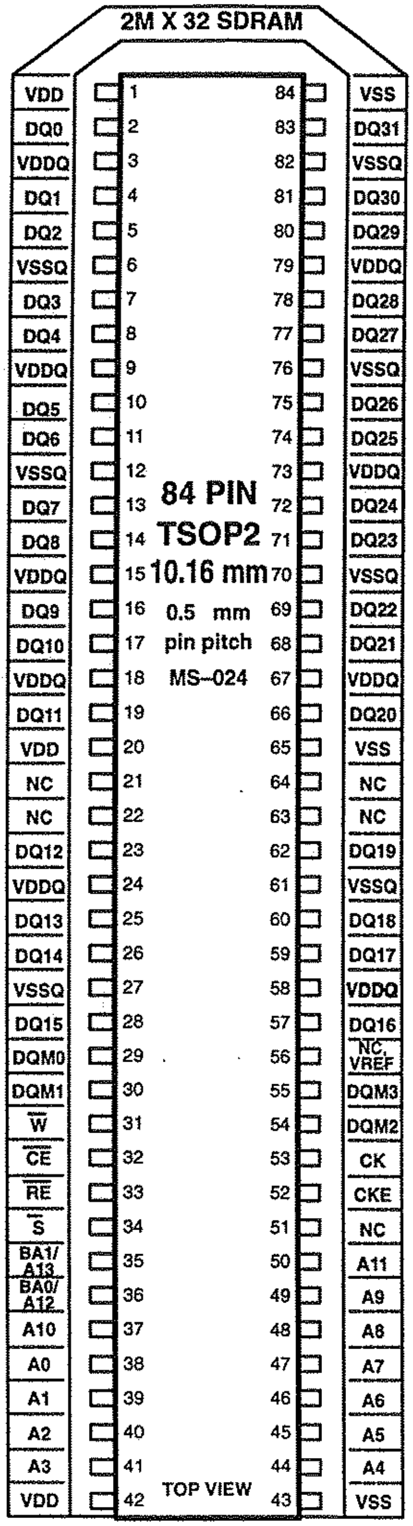
Note: This pinout is for both 128K and 256K parts. The Pin assignments are as follows

Configuration	P30	P51
128K x 2 Bank	NC	A8/AP;
256K X 2 Bank	A8	A9/AP

* Note: This part is a subset of the SGRAM shown in Fig. 3.10.3-4. P53 is DSF for the SGRAM version and MCL for the SDRAM.
MCL = Must Connect to Logic Low

Configuration	**128K X 2**	**256K X 2**
ROW ADDRESS	A0⇒A8,BA	A0⇒A9,BA
COLUMN ADDRESS	A0⇒A7	A0⇒A7
BANK SELECT		A9
REFRESH PERIOD	16 ms	32 ms
# ROWS REFRESH	1024	2048

FIGURE 3.11.4-4
128K & 256K BY 32, 2 BANK SDRAM IN QFP



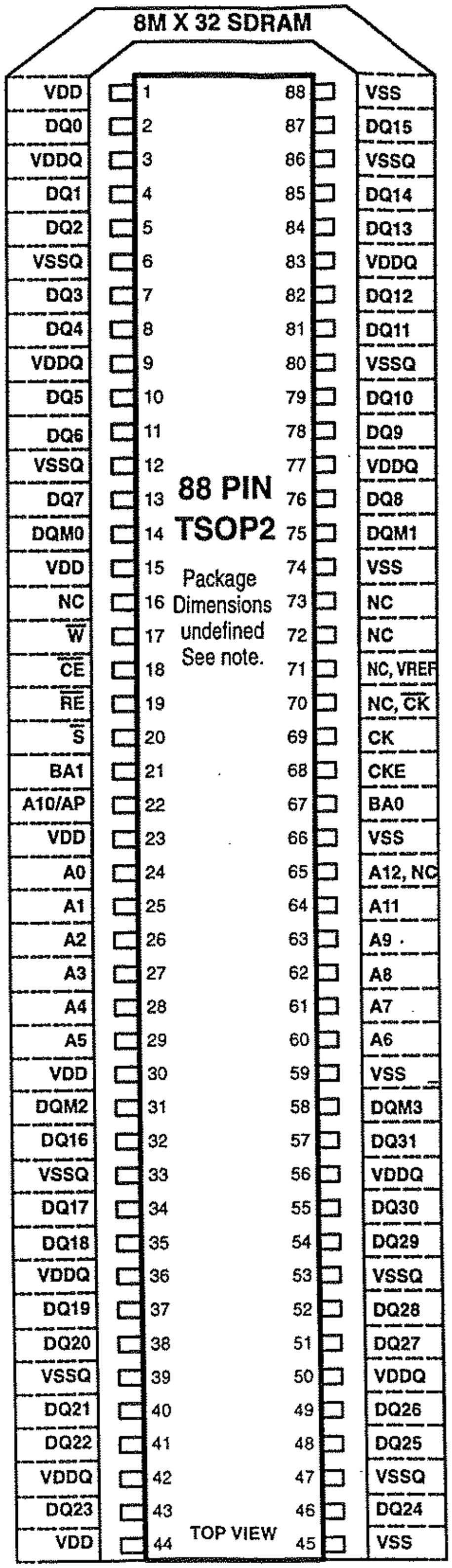
NOTE:
In addition to this pinout for a 2M X 32 SDRAM, there is another one that has the DQ pins at the outer ends of the package and the control pins in the center and superceeds this one. The other device should be used for all new designs. It is found in figure 3.11.4-7.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

ADDRESS ORGANIZATION

NUMBER BANKS	2	4
ROW ADDR.	A0⇒A13	A0⇒A13
COL. ADDR.	A0⇒A6	A0⇒A6
AUTO-PRECHARGE	A10	A10
BANK ADDRESS	A13	A12, A13

FIGURE 3.11.4-5
2M BY 32 SDRAM IN TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. The standard refresh interval (tREF) for 256Mb SDRAMs is 64ms.

3. (NC, VREF) is VREF on devices that require an external voltage reference.

4. BA0 is the least significant bank address

5. BA1 is the most significant bank address

6. A10/AP is row address A10, autoprecharge and precharge all banks.

7. (NC, $\overline{CK}$) is NC for devices using a single ended clock. $\overline{CK}$ is used for devices using a differential clock.

8. (NC, VREF) is VREF on devices that require an external voltage reference.

9. This standard is for a 4 Bank version only.

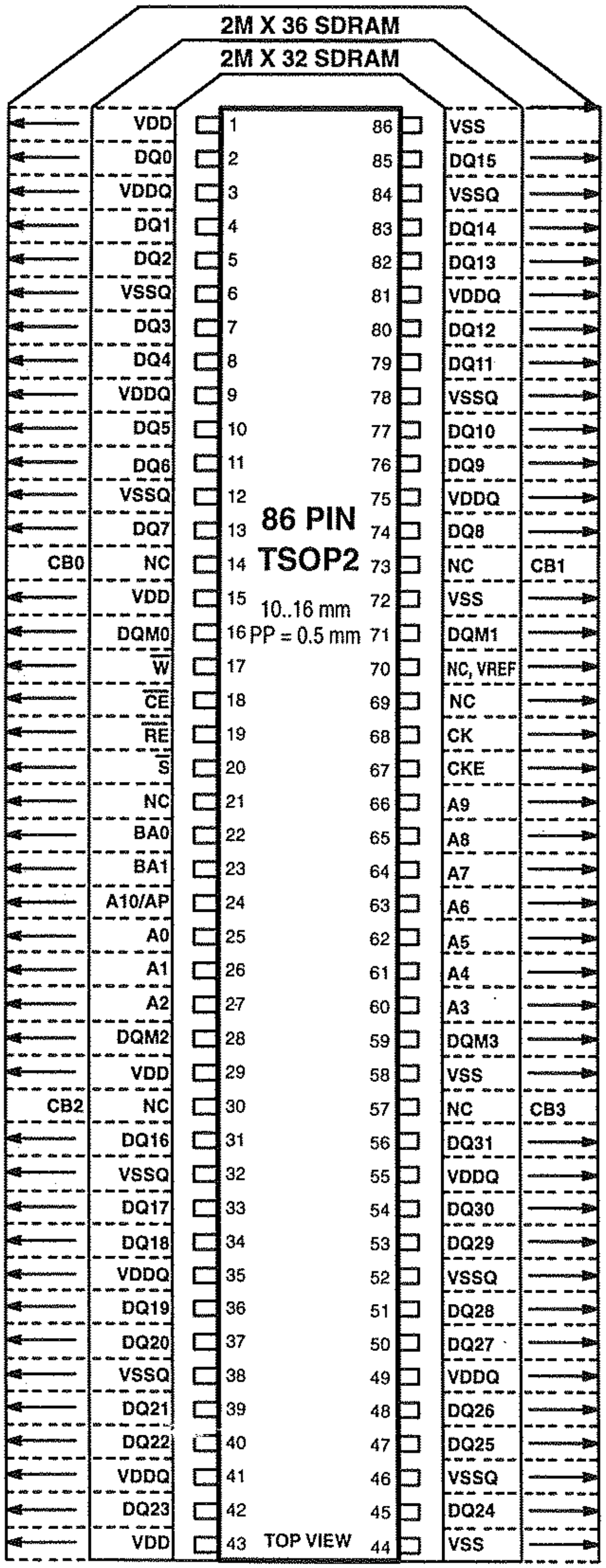
The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	**8M X 32**	8M X 32
Number RA	13	12
ROW ADDRESS	A0⇒A12	A0⇒A11
COLUMN ADDRESS	A0⇒A7	A0⇒A8

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4–6
8M BY 32 SDRAM PIN ROTATION IN TSOP2

Release 6c7



NOTES

1. A10/AP Is Row Address A10, Autopre
charge And Precharge All Banks Input.

2. (NC,VREF) is VREF on devices that require an external voltage reference.

3. The VDDQ designator is used when t
power supply pins for the DQ I/O drivers
are internally DC isolated from the VDD
power supply pins.

4. The VSSQ designator is used when t
ground reference pins for the DQ I/O
drivers are internally DC isolated from t
primary ground reference (VSS) power
supply pins.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

Configuration	**2M X 32**
REFRESH ADDR.	A0 ⇒ A11
ROW ADDRESS	A0 ⇒ A11
COLUMN ADDRESS	A0 ⇒ A8

FIGURE 3.11.4-7
2M BY 32 & 36 SDRAM IN TSOP2

SDRAM FUNCTION TRUTH TABLE for CKE

CURRENT STATE	CKE_{n-1}	CKE_n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Self–refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	H	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self–Refresh)
Power–Down	H	X *	X	X	X	X	X	INVALID
	L	H *	H	X*	X*	X*	X	EXIT Power Down⇒ABI
	L	H *	L	H	H	H	X	EXIT Power Down⇒ABI
	L	H *	L	H	H*	L*	X	ILLEGAL
	L	H *	L	H*	L*	X*	X	ILLEGAL
	L	H*	L	L	X*	X*	X	ILLEGAL
	L	L	X	X*	X*	X	X	NOP(Maintain Low–Power Mode)
All Banks Idle[7]	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power–Down
	H	L	L	H	H	H	X	Enter Power–Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self–Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8]
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS

ABI = All Banks Idle

NOTES:

6. CKE Low–to–High transition will re–enable CK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power–Down and Self–Refresh can be entered only from the All Banks Idle State.
8. Must be legal command.

* Elements of the table that were in error in the first printing of Release 4

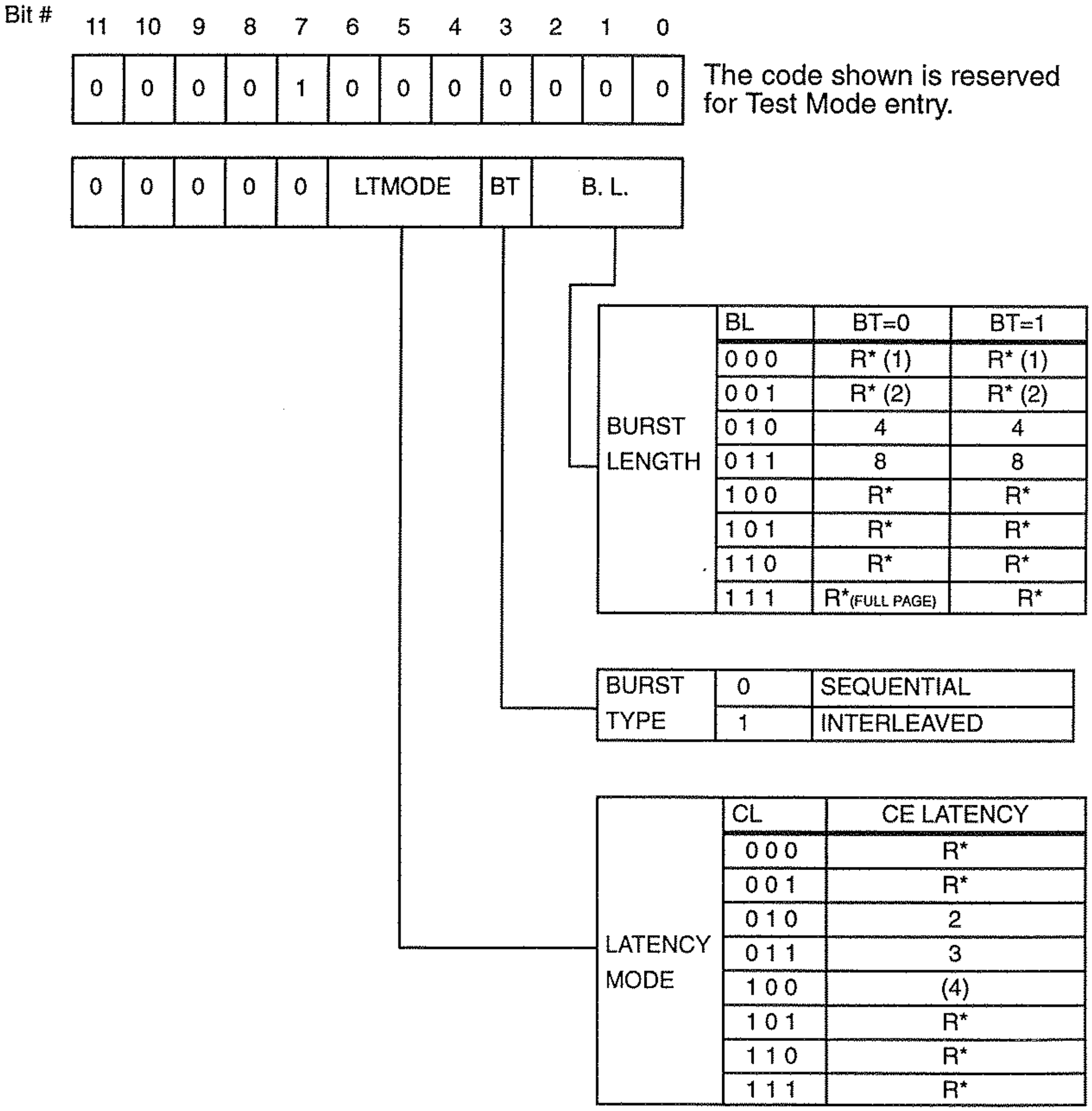
TABLE1 3.11.5–2

SDRAM FUNCTION TRUTH TABLE for CKE

SDRAM Mode Register

This Mode Register is located on the Synchronous DRAM (SDRAM) chip. Its purpose is to store the mode–of–operation data. This data is written after power–on and before normal operation. The data contains the Burst Length, the Burst Type, the $\overline{CE}$ Latency, and whether it is to be operating in Test Mode, or Normal operating mode. During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode–Register–Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in Interleaved address mode.

SDRAM Mode Register architecture:



Bit #	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	1	0	0	0	0	0	0	0
	0	0	0	0	0	LTMODE			BT	B. L.		

The code shown is reserved for Test Mode entry.

	BL	BT=0	BT=1
BURST LENGTH	0 0 0	R* (1)	R* (1)
	0 0 1	R* (2)	R* (2)
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R*	R*
	1 0 1	R*	R*
	1 1 0	R*	R*
	1 1 1	R*(FULL PAGE)	R*

BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED

	CL	CE LATENCY
LATENCY MODE	0 0 0	R*
	0 0 1	R*
	0 1 0	2
	0 1 1	3
	1 0 0	(4)
	1 0 1	R*
	1 1 0	R*
	1 1 1	R*

NOTE: All items in parentheses are optional

FIGURE 3.11.5–1
SDRAM MODE REGISTER ARCHITECTURE

3.11.5.4–Power On Sequence (Recommended)

The synchronous nature of the inputs and outputs of the SDRAM device create the possibility that a SDRAM device could power up in a state with data being driven out of the part, and in a multipart system, such a condition may cause data contention and possibly device damage in the long term. In an attempt to reduce the possibility of data contention, both system and device designers should strive toward ensuring a High–Z output state during the initial power up sequence. The following recommended power on sequence is offered for both system and device designers as a means to help the device power up with the outputs in a High–Z state.

The default power on value for the mode register is supplier specific and may be undefined.

The default power on value for the device is supplier specific and may be undefined.

The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μS.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more autorefresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.

3.11.5.5–Auto Precharge

The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle. The following table defines the options available from AP during the column address portion of any cycle.

AP	Option
0	Do not auto precharge, leave bank active at end of burst.
1	Auto precharge bank specified by BA at end of burst.

The user must wait until the precharge is completed before issuing another command to the device. Timing for auto precharge is required to be the same as or less than the minimum requirement of external precharge.

3.11.5.6–Precharge All Banks

The user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks. BA is used to specify the bank to be precharge, and AP is used to indicate the precharge option. The following table defines the options available from AP during the precharge cycle.

PA	Option
0	Precharge bank specified by BA
1	Precharge All banks

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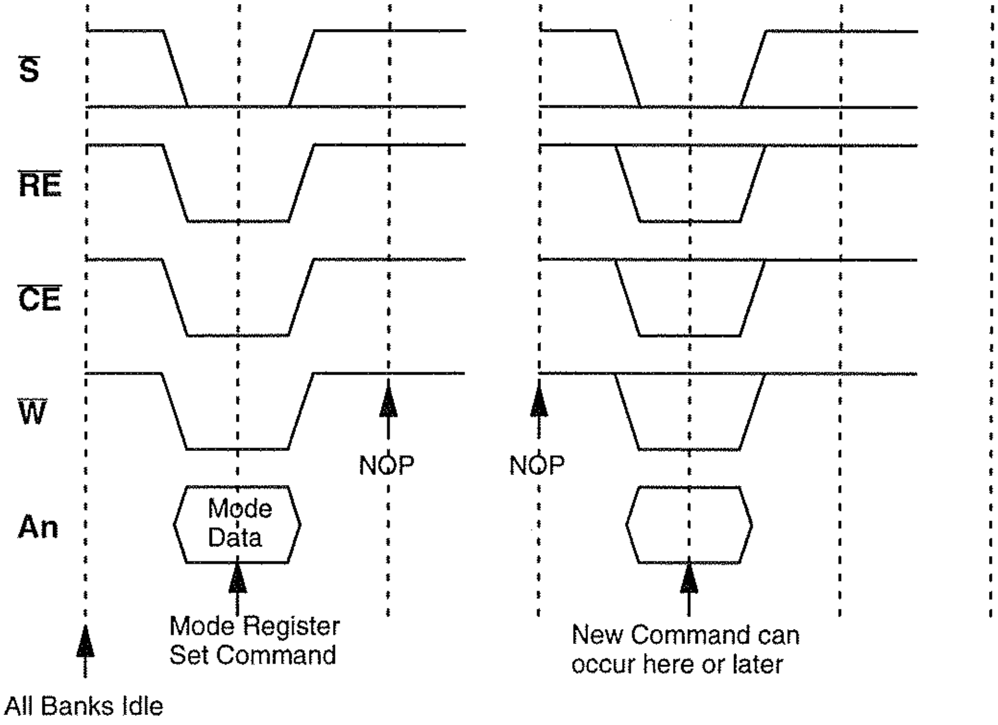
3.11.5.7–Mode Register Write Timing

The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.



Note: Clock Low–to–high transitions occur at the dotted lines.

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4 MEMORY MODULES AND CARDS

The following standards for MODULES and CARDS were developed by Committee JC–42.5. In earlier releases of JESD 21–C, the individual standards were intermixed and appeared in one section, 4, in the order in which they were approved with no regard for the module structure or organization. In Release 7, the section has been reorganized and the individual standards grouped in sub–sections by the data word length. A separate section is included (4.1) for those standards that describe features that are generic in nature and independent of the module organization.

The standards establish pin assignments for a series of multi–chip modules. The package configurations and dimensions are as defined in JEDEC Publication 95. The modules will normally be made using surface mount devices described in section 3 of this standard. The initial standards were for DRAM modules, but the since the publication of Std. 21–B, a standard for a families of SRAM and non–volatile modules have been approved. In addition to the device standards, there is a standard that addresses special nomenclature related to the modules.

The sub–sections are as follows:

4.1 Module & Card Features
4.2 One Byte Modules
4.3 Two Byte Modules and Cards
4.4 Four Byte Modules and Cards
4.5 Eight Byte Modules
4.6 Sixteen Byte Modules

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4.1 Module Features & Properties

The following standards are applicable to modules and cards without regard to the data word length except as where specifically indicated.

4.1.1 Memory Module Nomenclature

4.1.2 Memory Module Serial Presence Detect (SPD) General Standard

4.1.2.1 SPD Appendix A

4.1.2.2 SPD Appendix B

4.1.2.3 SPD Appendix C

4.1.2.4 SPD Appendix D

4.1.2.5 SPD Appendix E

4.1.2.6 SPD Appendix F

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4.1.1 Memory Module Nomenclature

4.1.1.1 – Purpose

The purpose of this standard is to establish a format for a number system which defines the format of a number which is an architectural description of multi–chip memory modules. It is intended to be used with but not restricted to modules made with DRAM devices.

4.1.1.2 – Number Format

The description number designation shall consist of 8 fields with the form nnSccbbDttIpp where :
nn = the number of longitudinal positions on the module: 4, 5, 8, 9.
S = the number of sides on the module stated as "single or double" : S, D
cc = the capacity of the memory chip stated in terms of the log(2) of the capacity (i.e.–the number of address bits needed for the chip): 16, 18, 20, 22
bb = the number of data bits in the interface: 1, 2, 4, 5, 8, 9, 10, 17
D = the data interface configuration, common, separate, or mixed: C, S, M
tt = total number of words stated as log(2) of the capacity: 16—26
I = mechanical interface: P = pins, E = edge card connector
pp = number of pins or pads

4.1.1.3 – Number Example

A module with the following attributes:
9 chips long
Double sided
18 bit data interface
Separate I/O for parity bits, common I/O for other bits
1M X 1 memory chips
Pin interface
Architectural number: 9D2018M20P40

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4.1.2 – SERIAL PRESENCE DETECT STANDARD, General Standard

Introduction: New memory technologies are continually being introduced to the industry. As these new technologies are considered, the need for expansion modules becomes evident; consequently, new memory technologies are being incorporated onto existing module form factors. Unfortunately, upon a module's first implementation, the module designer is often unable to predict all of the (as yet unreleased) memory technologies which would eventually be used on the module form factor; hence the parallel Presence Detect method did not allow for these newer technologies. Given that memory modules do not regularly change form factor when a new memory technology is implemented, a Serial Presence Detect (SPD) method should be available and predefined so that it can be considered for new memory modules when needed.

1 **Scope:** This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect (SPD) standard is intended for use on any memory module independent of memory technology or module form factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology.

When a specific memory technology is being depicted (e.g. Fast Page Mode DRAM), an appendix to this standard will be added describing the characteristics, features, and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each appendix.

When a new module form factor implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:

- SPD Interface protocol (see section 2 herein)
- Acceptable module configurations,
- Legitimate architectures: depth, width, #banks, addressing
- Acceptable error checking schemes (ECC, Parity...)
- SPD Wiring diagram and pinout to module.

2 **Interface Protocol.** Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Examples of SPD interface protocol include IIC, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.

3 **Data Order and PD Size:** This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required and optional data; when a fundamental memory technologies' PD bits are defined, then the entire address map for those SPDs must also be defined.

4 **SPD Data Types:** SPD data is stored in a non–volatile serial memory device. The different types of data include, but are not limited to:

- Look Up Table entries
- Binary data
- Optional data (Binary, ASCII, etc. data)
- Checksums

4.1 **Look Up Table (LUT) Entries:** Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g. fast page mode DRAM will have specific tables for tRAC, tCAC, # of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a look–up– table specified within an appendix within this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its appendices.

4.2 **Optional Data:** The current Jedec Standard allows for manufacturers to insert some of their own specific data into the SPD ROM. This data includes manufacturer ID, manufacturers' module serial numbers, and other ASCII, Binary Coded Decimal, or binary data.

4.3 **Checksums:** In various cases, checksums are required. Checksum calculation method is currently being proposed at time of publication of this standard.

5 **SPD Content:** The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the following must be addressed in any SPD implementation:

Description	Data Type	Address Map Byte #
SPD size	LUT Entry	0
Total SPD memory size	LUT Entry	1
Fundamental memory type	LUT Entry, Appendix A	2
Definition of features specific to the fundamental memory	See pertinent appendix	3–31
(Optional) Superset memory type	See appendix B	32
(Optional) definition of features specific to the superset memory	See pertinent appendix	33–61
SPD Revision designator	LUT	62
Checksum for bytes 0–62	Checksum	63
Manufacturers Jedec ID code per JEP–106	LUT	64–71
Manufacturing location	Supplier Unique	72
Manufacturer's Part Number	Supplier Unique	73–90
Revision Code	Supplier Unique	91–92
Manufacturing date	BCD	93–94
Assembly Serial Number	Supplier Unique	95–98
Manufacturer Specific Data	Supplier Unique	99–125
Reserved	N/A	126–127
Open free–form area	Application Specific	128–255

Detailed descriptions follow in paragraphs 5.x

5.1 **Byte 0,** Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data:

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

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5.2 **Byte 1, Total SPD Memory Size:** This field describes the total size of the serial memory (often an EEPROM) used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

5.3 **Byte 2,** Fundamental Memory Type: This field will identify the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in **appendix A** herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre–existing technology, then it should be considered a Superset technology and so described as detailed (in paragraph 5.5) within this standard.

5.4 **Bytes 3–31:** Descriptions of Module Specific Features: Appendices to this standard detail the tables for the features specific to each of the fundamental memory types as described above. For example, see appendix C for details of SPD features for Fast Page Mode and Extended Data Out DRAM Modules.

5.5 **Byte 32:** Superset Memory Type: When a new technology is developed which is completely backward compatible to an already specified (fundamental) technology, then it may be considered a $Superset' technology. The benefits of specifying a technology as a superset are obvious; if a system is capable of operating in a $fundamental' mode only and a superset module is inserted, then the system can still use the module. The memory superset type or technology is specified in appendix B to this standard. Appendix B provides the decode of specific superset technologies. It references other appendices where the specific superset PDs are further detailed. As new supersets are created, appendices must also be added. Presence Detects for a superset technology are specified just as for any given fundamental technology except that any and all backward compatible fundamental technologies must be referenced.

5.6 **Bytes 33–63:** Superset Features: Appendices to this standard detail the tables for the features specific to each of the superset memory types as described above. A new appendix must be added to this standard detailing the PDs for that superset technology detailed in appendix B and represented in byte 32. Appendix B would identify the superset technology type and would also reference the appropriate appendix where the superset is detailed.

5.9.0 **Bytes 64–127:** Module manufacturers may include information which is pertinent to their particular modules. This information is detailed below in paragraph 5.9.X:

5.9.1 **Bytes 64–71**: Manufacturers Jedec ID code per JEP106. Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FF indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes would be FFh.

5.9.2 **Byte 72:** Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

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5.9.3 Bytes 73–90: Manufacturer's Part Number: Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.9.4 Bytes 91–92: Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.9.5 Bytes 93–94: Date of Module Manufacture: The module manufacturer may include a date code for the module. If this is done, then specifically, byte 93 must contain the year in Binary and byte 94 must contain the week in Binary.

5.9.6 Bytes 95–98: Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.9.7 Bytes 99–125: Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.

5.9.8 Bytes 126–127: Reserved. These bytes are reserved and cannot be later allocated.

5.10 Bytes 128–255: System Integrators specific information: The system integrator may choose to use the SPD ROM for various items. If so, then bytes 128–255 may be used.

4.1.2.1 – Appendix A: Table of Fundamental Memory Types:

This table is modified/appended whenever a new fundamental memory technology is to be added to the Serial Presence Detect (SPD) standard. When a new memory type is added to this standard, a new appendix must also be added which details the specific features pertinent to the new fundamental type. The following table details the fundamental memory types.

Byte 2, Fundamental Memory Type: This field identifies the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in this Appendix herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre–existing technology, then it should be considered a Superset technology and so described as detailed (in paragraph 5.5 of the General Standard) within this standard.

The fundamental memory types are identified as follows:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	See Appndx
Reserved	0	0	0	0	0	0	0	0	N/A
Standard FPM DRAM	0	0	0	0	0	0	0	1	C
EDO	0	0	0	0	0	0	1	0	C
PNEDO									
	0	0	0	0	0	0	1	1	TBD
Sync Dram	0	0	0	0	0	1	0	0	E
Multiplexed ROM	0	0	0	0	0	1	0	1	F
TBD	0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	0	1	TBD
TBD	1	1	1	1	1	1	1	0	TBD
TBD									
	1	1	1	1	1	1	1	1	TBD

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4.1.2.2 – Appendix B: Table(s) of Superset Memory Types:

This table is modified/appended whenever a new Superset memory technology is to be added to the Serial Presence Detect (SPD) standard. When a new superset memory type is added to this standard, a new appendix must also be added which details the specific features pertinent to the new superset type. The following table identifies the Superset memory types and their pertinent fundamental technologies.

The Superset memory types are identified as follows:

Superset Mem. Type Appndx	Fundamental memory type. (note 1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	See
Reserved		0	0	0	0	0	0	0	0	N/A
TBD		0	0	0	0	0	0	0	1	TBD
TBD		0	0	0	0	0	0	1	0	TBD
TBD		0	0	0	0	0	0	1	1	TBD
TBD		0	0	0	0	0	1	0	0	TBD
TBD		0	0	0	0	0	1	0	1	TBD
TBD		0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
TBD		1	1	1	1	1	1	0	1	TBD
TBD		1	1	1	1	1	1	1	0	TBD
TBD		1	1	1	1	1	1	1	1	TBD

Note 1: The fully backward compatible Fundamental memory type must be referenced when a superset is specified.

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4.1.2.3 – Appendix C: Specific PD's for Fast Page Mode or Extended Data Out DRAM.

1 **Introduction:** This appendix describes the Presence Detects for Fast Page Mode DRAM and Extended Data Out (EDO) DRAM Modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 **Address map:** The following is the SPD address map for FPM and EDO. It describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# DRAM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	RAS# access time of this assembly	4
10	CAS# access time of this assembly	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	DRAM width, Primary DRAM	
14	Error Checking DRAM data width	
15–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106	6
72	Manufacturing location	6
73–90	Manufacturer's Part Number	6
91–92	Revision Code	6
93–94	Manufacturing date	6
95–98	Assembly Serial Number	6
99–125	Manufacturer Specific Data	6
126–127	Reserved	
128–255	Open User Free–Form area$not defined	

notes:

1) This will be 128 bytes for FPM and EDO DRAM

2) This will be 256 bytes, represented as 08h. See below.

3) High order bit defines is assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)

4) From data sheet.

5) High order bit (MSB) is Self Refresh $flag'. If bit seven is "1", assembly supports self refresh.

6) Per the JEDEC spec, these are optional.

2 **Bytes 0–2,** For Reference: Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in **appendix A** to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE 0,** From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte 1,** From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 **Byte 2,** From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3 **Data Type(s):** Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4 The following PD bytes are those specific to modules implementing Fast Page Mode and EDO DRAM technology. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

4.1 **Byte #3, Number of ROW Addresses:** This first field describes the number of Row Addresses in the DRAM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit7: "0" indicates normal addressing; "1" indicates redundant addressing

4.2 **Byte #4, Number of COLUMNs Addresses:** This field describes the number of COLUMN addresses in the module's DRAM array:

Number of COLUMN Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte #5, Number of Banks:** This field describes the number of banks on the DRAM Module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4 **Bytes 6 & 7,** Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
576	0000 0010	0100 0000

Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.1 **Byte 7, Module Data Width Continued:** This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 **Byte 8, Module Interface Levels:** This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6 **Byte 9, RAS Access Time (tRAC):** This field describes the module's RAS access time:

RAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
50ns	0	0	1	1	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
60ns	0	0	1	1	1	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
70ns	0	1	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80ns	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

4.7 **Byte 10, CAS Access Time (tCAC):** This field describes the module's CAS access time:

CAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
10ns	0	0	0	0	1	0	1	0
11ns	0	0	0	0	1	0	1	1
12ns	0	0	0	0	1	1	0	0
13ns	0	0	0	0	1	1	0	1
14ns	0	0	0	0	1	1	1	0
15ns	0	0	0	0	1	1	1	1
16ns	0	0	0	1	0	0	0	0
17ns	0	0	0	1	0	0	0	1
18ns	0	0	0	1	0	0	1	0
19ns	0	0	0	1	0	0	1	1
20ns	0	0	0	1	0	1	0	0
21ns	0	0	0	1	0	1	0	1
22ns	0	0	0	1	0	1	1	0
23ns	0	0	0	1	0	1	1	1
24ns	0	0	0	1	1	0	0	0
25ns	0	0	0	1	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

4.8 Byte 11, Module Configuration type: This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.9 Byte 12, Refresh Rate/Type: This field describes the module's refresh rate and type:

Refresh Period	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

4.10 Byte 13, DRAM width, Primary DRAM: This field describes the width of the primary DRAMs used on the module. The primary DRAM is that which is used for data; examples of primary (data) DRAM widths are x4, x8, x16, x32. Note that if the module is made with DRAMs which provide extra bits for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples using x72 modules include:

Module width	Primary Data DRAM Width	Error Checking DRAM Width	Qty Primary Data DRAMs	Byte 13 (Binary)
x72	x9	—	8	0000 1001
x72	x8	x8	9	0000 1000
x72	x16	x1	4	0001 0000

DRAM Width, Primary DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.11 Byte 14, Error Checking DRAM data width: If the module incorporates error checking and if the primary data DRAM does not include these bits; i.e. there are separate error checking DRAMs, then the error checking DRAM's width is expressed in this byte. Examples of error checking DRAM widths include x1, x4, x8. For Example:

Module width	Primary DRAM Width	Error Checking DRAM Width	Qty of Error Checking DRAMs	Byte 14 (Binary)
x72	x9	—	—	0000 0000
x72	x8	x8	1	0000 1000
x72	x16	x1	8	0000 0001

DRAM Width Error Checking DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

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4.12 **Bytes 15–31:** Open. There are no defined PD settings for these bytes.

4.13 **Bytes 32 through 62, Superset information:** If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in bytes 32 through 62.

4.14 **Byte 63, Checksum for bytes 0–62:** At time of the publish of this standard, the checksum method is currently in ballot and is not yet incorporated, suggested method is modulo 256.

5 **From the general SPD standard:** The descriptions of bytes 64–127 are repeated here For Reference ONLY. Manufacturers MAY include information which is pertinent to their particular modules, place and date of manufacture, etc. If a module manufacturer decides to write data into bytes 64–127, they must follow the format and order presented below. If a module manufacturer chooses not to include the data outlined below, they must leave bytes 64–127 unprogrammed; blank state of these bytes may be 00h or FFh. Detailed implementation of bytes 64–127 is detailed below in paragraphs 5.X:

5.1 **Bytes 64–71:** Manufacturers ID code per EIA/JEP106. Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FFh indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes should be FFh.

5.2 **Byte 72:** Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.3 **Bytes 73–90:** Manufacturer's Part Number: Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.4: **Bytes 91–92:** Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.5 **Bytes 93–94:** Date of Module Manufacture: The module manufacturer may include a date code for the module. Specifically, byte 93 may contain the year in Binary and byte 94 may contain the week in Binary.

5.6 **Bytes 95–98:** Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.7 **Bytes 99–125:** Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.

5.8 **Bytes 126–127:** Reserved. These bytes are reserved and cannot be later allocated.

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4.1.2.4 – Appendix D: Table not yet defined

Table D is not yet defined. It will be placed in this location when it is published.

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4.1.2.5 – Appendix E: Specific PD's for Synchronous DRAM (SDRAM).

Date of last update: 11/25/96

1. **Introduction:** This appendix describes the Presence Detects for Synchronous DRAM Modules. These PD's are those referenced in the SPD standard document for "Specific Features". The following PD fields will occur, in the order presented, in table 1.1. Further descriptions of bytes 0 and 1 are found in the SPD standard. Further description of byte 2 is found in appendix A of the SPD standard.

1.1 **Address map:** The following is the SPD address map for SDRAM. It describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# Module Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	SDRAM Cycle time at Max. Supported CAS Latency (CL), CL=X	4
10	SDRAM Access from Clock	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	SDRAM width, Primary DRAM	
14	Error Checking SDRAM data width	
15	Minimum Clock Delay, Back to Back Random Column Addresses	
16	Burst Lengths Supported	
17	# Banks on Each SDRAM device	4
18	CAS# Latencies Supported	4
19	CS# Latency	4
20	Write Latency	4
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	
23–31	TBD	
32–62	Superset information	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106E	6
72	Manufacturing location	6
73–90	Manufacturer's Part Number	6
91–92	Revision Code	6
93–94	Manufacturing date	6
95–98	Assembly Serial Number	6
99–125	Manufacturer Specific Data	
126–127	Reserved	
128–255	Open for Customer use.	7

notes:

1) This will be programmed as 128 bytes for the 168 pin DIMM Module.
2) This must be programmed as 256 bytes, 256 byte EEPROM's will be used for SPD on 168 pin SDRAM DIMMs.
3) High order bit defines if assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)
4) From data sheet.
5) High order bit (MSB) is Self Refresh $flag'. If bit seven is "1", assembly supports self refresh.
6) The JEDEC spec specifies that these bytes are optional.
7) Module suppliers will need to assure that these bytes are open for reads/writes by Customer.

2 **For Reference, Bytes 1–3:** Descriptions of bytes 1 and 2 can be found in the main body of the SPD standard, and byte 3 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE 0:** From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte 1:** From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 Byte 2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
SDRAM	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3. Data Type(s): Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4. The following PD bytes are those specific to modules implementing Synchronous DRAM technology. Note that these full descriptions start at byte 3 below and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology

4.1 Byte 3: Number of ROW Addresses: This first field describes the number of row Addresses in the SDRAM array. This does not include the Bank Select pin. For example, the number of Row Addresses used on a 2MX64 SDRAM DIMM is

Decimal	Binary	Addresses
11	0000 1011	(for RA0 through RA10):

No. of Row Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
14(redundant)	1	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit7: "0" indicates normal addressing; "1" indicates redundant addressing

4.2 **Byte 4: Number of COLUMN Addresses:** This field describes the number of COLUMN Addresses in the module's SDRAM array:

Number of Columns	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte 5: Number of Banks on module:** This field describes the number of physical banks on the SDRAM Module. This is not to be confused with the number of logical banks on a given SDRAM device :

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4 Bytes 6 & 7, Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.2 Byte 7. Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 Byte 8, Module Interface Levels: This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	1

4.6 **Byte 9, SDRAM Cycle time (tCYC):** This byte defines the minimum cycle time for the SDRAM Module at the highest CAS Latency, CAS Latency=X, defined in byte 18. If other CAS latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate cycletimes at lower CAS Latencies. Byte 9, Cycle time for CAS Latency = X, is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are		and bits 3:0 are		then the cycle time is
1010		0101		
(10ns)	+	(0.5ns)	=	10.5ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Cycle Time Subfield A:								
Units of nanoseconds (bits 4 through 7)					SEE Subfield Table B			
Undefined	0	0	0	0				
1ns/16ns	0	0	0	1				
2ns	0	0	1	0				
3ns	0	0	1	1				
4ns	0	1	0	0				
5ns	0	1	0	1				
6ns	0	1	1	0				
7ns	0	1	1	1				
8ns	1	0	0	0				
9ns	1	0	0	1				
10ns	1	0	1	0				
11ns	1	0	1	1				
12ns	1	1	0	0				
13ns	1	1	0	1				
14ns	1	1	1	0				
15ns	1	1	1	1				
SDRAM Cycle Time Subfield B:								
Tenths of ns (bits 0 through 3).	SEE Subfield table A							
+0ns					0	0	0	0
+0.1ns					0	0	0	1
+0.2ns					0	0	1	0
+0.3ns					0	0	1	1
+0.4ns					0	1	0	0
+0.5ns 1						0	1	0
+0.6ns					0	1	1	0
+0.7ns					0	1	1	1
+0.8ns					1	0	0	0
+0.9ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.7 **Byte 10, SDRAM Access time from Clock (tAC):** This byte defines the maximum clock to data out for the module. This is the Clock to data out specification at the highest given CAS Latency specified/depicted in byte 18 of this SPD specification/ standard. If other CAS latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate tAC's at lower CAS Latencies. The byte is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are		and bits 3:0 are		then the cycle time is
1001		0000		
(9ns)	+	(0.0ns)	=	9.0ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Access time from Clock:								
Subfield A: Units of nanoseconds (bits 4 through 7)								
Undefined	0	0	0	0	SEE Subfield Table B			
1ns	0	0	0	1				
2ns	0	0	1	0				
3ns	0	0	1	1				
4ns	0	1	0	0				
5ns	0	1	0	1				
6ns	0	1	1	0				
7ns	0	1	1	1				
8ns	1	0	0	0				
9ns	1	0	0	1				
10ns	1	0	1	0				
11ns	1	0	1	1				
12ns	1	1	0	0				
13ns	1	1	0	1				
14ns	1	1	1	0				
15ns	1	1	1	1				
SDRAM Access time from CLK								
Subfield B: Tenths of ns (bits 0 through 3)								
+0ns	SEE Subfield Table A				0	0	0	0
+0.1ns					0	0	0	1
+0.2ns					0	0	1	0
+0.3ns					0	0	1	1
+0.4ns					0	1	0	0
+0.5ns					0	1	0	1
+0.6ns					0	1	1	0
+0.7ns					0	1	1	1
+0.8ns					1	0	0	0
+0.9ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.8 **Byte 11, Module Configuration type:** This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.9 **Byte 12, Refresh Rate/Type:** This field describes the module's refresh rate and type:

Refresh Period Bit 0	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

4.10 **Byte 13, SDRAM width, Primary SDRAM:** This field describes the width of the primary SDRAMs used on the module. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, x32. Note that if the module is made with SDRAMs which provide for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples using (1 bank) x72 modules include:

Module width	Primary Data SDRAM Width	Error Checking SDRAM Width	Qty Primary Data SDRAMs	Byte 13 (Binary)
x72	x9	—	8	0000 1001
x72	x8	x8	9	0000 1000
x72	x16	x4	4	0001 0000

SDRAM Width, Primary SDRAM Bit 0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.11 Byte 14, Error Checking SDRAM data width: If the module incorporates error checking and if the primary data SDRAM does not include these bits; i.e. there are separate error checking SDRAMs, then the error checking SDRAM's width is expressed in this byte. Examples of error checking SDRAM widths include x4, x8, x16. For Example:

Module width	Primary SDRAM Width	Error Checking SDRAM Width	Qty of Error Checking SDRAMs	Byte 14 (Binary)
x72	x9	—	—	0000 0000
x72	x8	x8	1	0000 1000
x72	x16	x4	8	0000 0100

SDRAM Width Error Checking DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.12 Byte 15, as determined by the limiting part on the assembly, SDRAM Device Attributes: Minimum Clock Delay, Back to Back Random Column Accesses. Note that SDRAM architecture can be gained with this parameter. A latency of 1 for random writes denotes Pipelined SDRAM and a latency of 2 for random writes denotes Prefetch SDRAMs:

Number of Clocks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
.	.					.		
255	1	1	1	1	1	1	1	1

4.13 Byte 16, SDRAM Device Attributes, Burst Lengths Supported: This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is "1", then that Burst Length is supported on the module; If the bit is "0", then that burst length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1
1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

4.14 Byte 17, SDRAM Device Attributes, Number of Banks on the discrete SDRAM Device: This byte details how many banks are on each discrete SDRAM installed onto the module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
.	.					.		
255	1	1	1	1	1	1	1	1

4.15 Byte 18, SDRAM Device Attributes, CAS# Latency: This byte describes which of the programmable CAS# Latencies are supported by the Module. If the bit is "1", then that CAS# Latency is supported on the module; If the bit is "0", then that CAS# Latency is not supported by the module. Bytes 9,10,23–26 all relate CAS Latency dependent timings.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CAS# Latency = 7	CAS# Latency = 6	CAS# Latency = 5	CAS# Latency = 4	CAS# Latency = 3	CAS# Latency = 2	CAS# Latency = 1
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.16 Byte 19, SDRAM Device Attributes, CS# Latency: This byte describes which of the programmable CS# Latencies are acceptable for the Module. If the bit is "1", then that CS# Latency is supported on the module; If the bit is "0", then that CS# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CS# Latency = 6	CS# Latency = 5	CS# Latency = 4	CS# Latency = 3	CS# Latency = 2	CS# Latency = 1	CS# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.17 Byte 20, SDRAM Device Attributes, WE# Latency: This byte describes which of the programmable WE# Latencies are acceptable for the Module. If the bit is "1", then that WE# Latency is supported on the module; If the bit is "0", then that WE# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	WE# Latency = 6	WE# Latency = 5	WE# Latency = 4	WE# Latency = 3	WE# Latency = 2	WE# Latency = 1	WE# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.18 Byte 21, SDRAM Module Attributes: This byte depicts various aspects of the module. It details various unrelated but critical elements pertinent to the module. A given module characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, then the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	Differential Clock Input	Registered DQMB Inputs	Buffered DQMB Inputs	On–Card PLL (Clock)	*Registered Address/Control Inputs	*Buffered Address/Control Inputs
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

* Address, RAS, CAS, WE, CKE, CS

4.19 Byte 22, SDRAM Device Attributes, General: This byte depicts various aspects of the SDRAMs on the module. It details various unrelated but critical elements pertinent to the SDRAMs. A given SDRAM characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, then the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	Supports Write1/Read Burst	Supports Precharge All	Supports Auto–Precharge	Supports Early RAS# Precharge
0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

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4.1.2.6 – Appendix F: Specific PD's for Address Multiplexed ROMs (MXROM).

1.0 Introduction: This appendix describes the Presence Detects for Multiplexed ROM modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 Address map: The following is the SPD address map for Multiplexed ROM. It describes where the individual LUT–Entries/ bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	
4	# Column Addresses on this assembly	
5	# ROM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	Address Access Time of this assembly$	3
10	$Address Access Time continuation	3
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Reserved	
13	Page Mode Access Time of this assembly	3
14	Output Enable Access Time of this assembly	3
15	Chip Enable Access Time of this assembly$	3
16	$Chip Enable Access Time continuation	3
17	Burst Length of this assembly	
18–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106	4
72	Manufacturing location	4
73–90	Manufacturer's Part Number	4
91–92	Revision Code	4
93–94	Manufacturing date	4
95–98	Assembly Serial Number	4
99–125	Manufacturer Specific Data	4
126–127	Reserved	
128–255	Open User Free–Form area$not defined	

notes:

1) This will be 128 bytes for Multiplexed ROM assemblies.
2) This will be 256 bytes, represented as 08h. See below.
3) From data sheet.
4) Per the JEDEC spec, these are optional.

2 **Bytes #0–2, For Reference:** Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE #0, From General SPD Standard, Number of Bytes used by Module Manufacturer:** This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte #1, From General SPD Standard, Total SPD Memory Size:** This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 Byte #2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
Multiplexed ROM	0	0	0	0	0	1	0	1

3 Data Type(s): Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4 The following PD bytes are those specific to modules implementing ROM devices with a multiplexed address interface. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

4.1 Byte #3, Number of ROW Addresses: This first field describes the number of Row Addresses in the ROM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.2 **Byte #4, Number of COLUMN Addresses:** This field describes the number of COLUMN addresses in the module's ROM array:

Number of COLUMN Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte #5, Number of Banks:** This field describes the number of banks on the ROM Module.

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4 Bytes 6 & 7, Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.2 Byte #7, Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 Byte #8, Module Interface Levels: This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6 **Bytes #9 & #10, Address Access Time (t_{AA}):** Bytes 9 and 10 are used to designate the address access time of the module. This access time is presented as a 16 bit word; bit 0 of byte 9 becomes the LSB of the 16 bit access time identifier and bit 7 of byte 10 becomes the MSB. Consequently, if the module has an address access time of less than 256ns, byte 10 will have a value of 00h. If the address access time is 256ns or greater, byte 10 is used in conjunction with byte 9 to designate the total access time.

4.6.1 **Byte 9:**

Address Access Time (LSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 (+x0A) ns	0	0	0	0	0	0	0	1
2 (+x0A) ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
254 (+x0A) ns	1	1	1	1	1	1	0	1
255 (+x0A) ns	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6.2 **Byte #10, Address Access Time Continued:** This byte will be left at 00h if the address access time of the module is less than 256 nanoseconds. If the address access time of the module is 256 nanoseconds or greater, byte 10 is used in conjunction with byte 9 to determine the access time of the assembly.

Address Access Time (MSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (+x09) ns	0	0	0	0	0	0	0	0
256 (+x09) ns	0	0	0	0	0	0	0	1
512 (+x09) ns	0	0	0	0	0	0	1	0
1024 (+x09) ns	0	0	0	0	0	0	1	1
2048 (+x09) ns	0	0	0	0	0	1	0	0
4096 (+x09) ns	0	0	0	0	0	1	0	1
8192 (+x09) ns	0	0	0	0	0	1	1	0
16384 (+x09) ns	0	0	0	0	0	1	1	1
–	–	–	–	–	–	–	–	–

4.7 **Byte #11, Module Configuration type:** This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.8 **Byte #12, Reserved:** This byte is reserved for future offerings.

4.9 Byte #13, Page Mode Access Time (t_{PA}): Byte 13 represents the page mode access time from chip enable of the device (t_{PA}) in nanoseconds.

Page Mode Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 ns	0	0	0	0	0	0	0	1
2 ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
253 ns	1	1	1	1	1	1	0	1
254 ns	1	1	1	1	1	1	1	0
New Table	1	1	1	1	1	1	1	1

4.10 Byte #14, Output Enable Access Time (t_{OE}): Byte x14 represents the access time from output enable of the device (t_{OE}) in nanoseconds.

Output Enable Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 ns	0	0	0	0	0	0	0	1
2 ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
253 ns	1	1	1	1	1	1	0	1
254 ns	1	1	1	1	1	1	1	0
New Table	1	1	1	1	1	1	1	1

4.11 Bytes #15 & #16, Chip Enable Access Time (t_{OE}): Bytes 15 and 16 are used to designate the access time from chip enable of the module. This access time is presented as a 16 bit word; bit 0 of byte 15 becomes the LSB of the 16 bit access time identifier and bit 7 of byte 16 becomes the MSB. Consequently, if the module has a chip enable access time of less than 256ns, byte 16 will have a value of 00h. If the chip enable access time is 256ns or greater, byte 16 is used in conjunction with byte 15 to designate the total chip enable access time.

4.11.1 Byte #15:

Chip Enable Access Time (LSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 (+x0F) ns	0	0	0	0	0	0	0	1
2 (+x0F) ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
254 (+x0F) ns	1	1	1	1	1	1	0	1
255 (+x0F) ns	1	1	1	1	1	1	1	1

4.11.2 Byte #16, Chip Enable Access Time Continued: This byte will be left at 00h if the chip enable access time of the module is less than 256 nanoseconds. If the chip enable access time of the module is 256 nanoseconds or greater, byte 16 is used in conjunction with byte 15 to determine the chip enable access time of the assembly.

Chip Enable Access Time (MSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (+x0F) ns	0	0	0	0	0	0	0	0
256 (+x0F) ns	0	0	0	0	0	0	0	1
512 (+x0F) ns	0	0	0	0	0	0	1	0
1024 (+x0F) ns	0	0	0	0	0	0	1	1
2048 (+x0F) ns	0	0	0	0	0	1	0	0
4096 (+x0F) ns	0	0	0	0	0	1	0	1
8192 (+x0F) ns	0	0	0	0	0	1	1	0
16384 (+x0F) ns	0	0	0	0	0	1	1	1
–	–	–	–	–	–	–	–	–

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4.12 **Byte #17, Burst Length:** Byte 17 is an 8 bit mask which indicates all burst lengths supported by the device. If a bit in byte 17 is "1" then the associated burst length is supported by the module. If the bit is "0", then that burst length is not supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length 8	Burst Length 4	Burst Length 2	Burst Length 1
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.13 **Bytes 18–31:** Open. There are no defined PD settings for these bytes.

4.14 **Bytes 32 through 62, Superset information:** If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in bytes 32 through 62.

4.15 **Byte 63, Checksum for bytes 0–62:** At time of the publish of this standard, the checksum method is currently in ballot and is not yet incorporated, suggested method is modulo 256.

5 **From the general SPD standard:** The descriptions of bytes 64–127 are repeated here For Reference ONLY. Manufacturers MAY include information which is pertinent to their particular modules, place and date of manufacture, etc. If a module manufacturer decides to write data into bytes 64–127, they must follow the format and order presented below. If a module manufacturer chooses not to include the data outlined below, they must leave bytes 64–127 unprogrammed; blank state of these bytes may be 00h or FFh. Detailed implementation of bytes 64–127 is detailed below in paragraphs 5.X:

5.1 **Bytes 64–71, Manufacturers ID code per EIA/JEP106.** Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FFh indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes should be FFh.

5.2 **Byte 72, Manufacturing Location.** Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.3 **Bytes 73–90, Manufacturer's Part Number:** Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.4 **Bytes 91–92, Revision Code:** This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.5 **Bytes 93–94, Date of Module Manufacture:** The module manufacturer may include a date code for the module. Specifically, byte 93 may contain the year in Binary and byte 94 may contain the week in Binary.

5.6 **Bytes 95–98, Module Serial Number:** The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.7 **Bytes 99–125, Manufacturers specific data, open area:** The module manufacturer may add any additional information desired into the module within these locations.

5.8 **Bytes 126–127, Reserved:** These bytes are reserved and cannot be later allocated.

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4.2 One Byte Memory Modules

4.2.1 – 22 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K WORDS OF 4 BITS
CONFIGURATION—SINGLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—22 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 24 PIN SIP/SIMM DRAM MODULE

CAPACITY—128K, 512K WORDS OF 4 BITS
CONFIGURATION—DOUBLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—24 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 30 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K, 1M, 4M WORDS OF 8 OR 9 BITS, & 16M WORDS OF 8 BITS
CONFIGURATION—SINGLE SIDED MODULE
—USING 64K, 256K, 1M, 4M, OR 16M MEMORY DEVICES
LOGIC FEATURES—Some of the modules contain a "presence detect" feature which conists of outputs that supply an encoded value which defines the storage capacity of the module.
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

4.2.2 – 30 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 8M WORDS OF 4 OR 5 BITS
—128K TO 16M WORDS OF 2 BITS
—256K TO 32M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENT Fig. 4.2–2

4.2.3 – 23/25/26/28 PIN ZIP/SIMM DRAM MODULE FAMILY

CAPACITY —256K TO 16M WORDS OF 4 BIT
—1M TO 64M WORDS OF 1 BIT
CONFIGURATION—DOUBLE SIDED, USING 1M, 4M, 16M, OR 64M DEVICES
PACKAGE—THE X4 MODULES, 26 PIN ZIP/SIP MODULE
THE X1 MODULES, 23 PIN ZIP/SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–3
NOTE: At the highest density using 64M memory devices, the modules must be expanded to 25 or 28 pins to provide the needed addresses. These modules will be defined in more detail when the packages for the 64M memory devices have been defined.

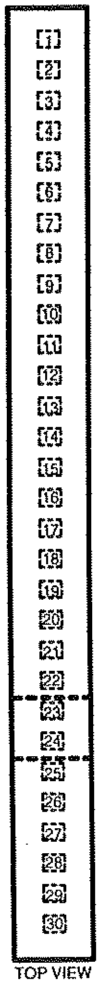
4.2.4 – 60 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 4 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 8, 128K, 512K, OR 2M BY 4
PACKAGE—60 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–4

– 70 PIN ZIP/SIMM SRAM MODULE

CAPACITY—64K, 256K, 1M WORDS OF 9 BITS
CONFIGURATION—SINGLE BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 9
LOGIC FEATURE—SEPARATELY CONTROLLABLE BIT FOR USE AS PARITY BIT
PACKAGE—70 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–5

1.54



PHYSICAL CONFIGURATION	4 DEVICES LONG				8 OR 9 DEVICES LONG			
	SINGLE BANK		DOUBLE BANK		SINGLE BANK			DOUBLE BANK
VERSION	N X 4	@ 4N X 1	2N X 4	N X 8	* N X 8(9)	* N X 8(9)	16M X 8	* 2N X 8(9)
1	$ A8	VSS	** NC	% NC	VDD	VDD	VDD	VDD
2	VDD	VDD	A8	A8	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
3	D0	$\overline{RE0}$	VDD	VDD	DQ0	DQ0	DQ0	DQ0
4	Q0	Q	D0	DQ0	A0	A0	A0	A0
5	$\overline{CE}$	A3	Q0	DQ1	A1	A1	A1	A1
6	A7	A6	$\overline{CE}$	$\overline{CE}$	DQ1	DQ1	DQ1	DQ1
7	A5	D	A7	A7	A2	A2	A2	A2
8	A4	$\overline{W}$	A5	A5	A3	A3	A3	A3
9	D1	$\overline{RE1}$	A4	A4	VSS	VSS	VSS	VSS
10	Q1	A0	D1	DQ2	DQ2	DQ2	DQ2	DQ2
11	$\overline{W}$	A7	Q1	DQ3	A4	A4	A4	A4
12	A1	A8	$\overline{W}$	$\overline{W}$	A5	A5	A5	A5
13	A3	$\overline{CE}$	A1	A1	DQ3	DQ3	DQ3	DQ3
14	A6	$\overline{RE2}$	A3	A3	A6	A6	A6	A6
15	Q2	A2	A6	A6	A7	A7	A7	A7
16	D3	A1	Q2	DQ4	DQ4	DQ4	DQ4	DQ4
17	A2	@ A9	D2	DQ5	A8	A8	A8	A8
18	A0	A4	A2	A2	* A9	* A9	A9	* A9
19	$\overline{RE}$	$\overline{RE3}$	A0	A0	* A10	NC	A10	$\overline{RE2}$
20	D3	A5	RE1	$\overline{RE}$	DQ5	DQ5	DQ5	DQ5
21	Q0	VDD	D3	DQ6	$\overline{W}$	$\overline{W}$	$\overline{W}$	$\overline{W}$
22	VSS	VSS	Q3	DQ7	VSS	VSS	VSS	VSS
23			VSS	VSS	DQ6	DQ6	DQ6	DQ6
24			*** $\overline{RE2}$	NC	# NC	PD1	A11	PD1
25					DQ7	DQ7	DQ7	DQ7
26					Q8	PD2	NC	PD2
27					$\overline{RE}$	$\overline{RE}$	$\overline{RE}$	$\overline{RE1}$
28					$\overline{CE8}$	NC	NC	NC
29					D8	DQ8	NC	DQ8
30					VDD	VDD	VDD	VDD

* ON THE 30 PIN MODULE, 1M & 4M DEVICES MAY BE USED. PINS 18 & 19 ARE USED TO PROVIDE ADDRESS EXPANSION. THE OTHER MODULES WILL ACCOMIDATE 64K & 256K DEVICES ONLY.

** OPTIONAL VSS

*** NC FOR SINGLE BANK VERSION

$ OPTIONAL VSS WHEN A8 NOT NEEDED

\# OPTIONAL REFRESH (F) FUNCTION

@ ON THE 22 PIN 4N X 1 MODULE, 1 MB & 4 MB DEVICES MAY BE USED. PIN 17 IS USED FOR ADDRESS EXPANSION

% POTENTIAL VSS

PRESENCE DETECT TRUTH TABLE

SIZE	256K	512K	1M
PIN			
PD1	L	H	L
PD2	H	L	L

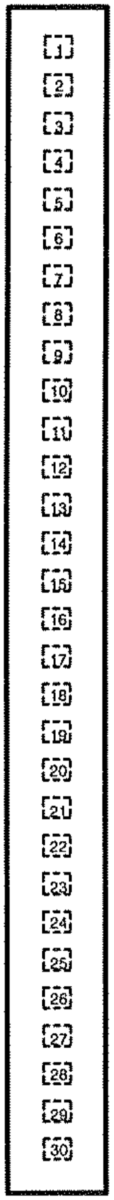
CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED.

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

FIGURE 4.2-1

22, 24,& 30 PIN DRAM MODULES

PHYSICAL CONFIGURATION	4 OR 5 DEVICES LONG SINGLE SIDED			4 OR 5 DEVICES LONG DOUBLE SIDED		
VERSION	N X 4(5)	2N X 2	4N X 1	2N X 4(5)	4N X 2	8N X 1
1	VDD	→	→	→	→	→
2	D4	NC	NC	D4	NC	NC
3	Q4	NC	NC	Q4	NC	NC
4	A8	→	→	→	→	→
5	A9	→	→	→	→	→
6	*A10	→	→	→	→	→
7	D3	D1	NC	D3	D1	NC
8	Q3	Q1	NC	Q3	Q1	NC
9	VSS	→	→	→	→	→
10	A6	→	→	→	→	→
11	A7	→	→	→	→	→
12	A2	→	→	→	→	→
13	A1	→	→	→	→	→
14	D2	NC	D	D2	NC	D
15	Q2	NC	Q	Q2	NC	Q
16	A4	→	→	→	→	→
17	A5	→	→	→	→	→
18	A3	→	→	→	→	→
19	A0	→	→	→	→	→
20	D1	D0	NC	D1	D0	NC
21	Q1	Q0	NC	Q1	Q0	NC
22	VSS	→	→	→	→	→
23	$\overline{W}$	→	→	→	→	→
24	$\overline{CE}$	$\overline{CE1}$	→	→	→	→
25	NC	$\overline{CE2}$	→	→	→	→
26	$\overline{RE}$	→	→	$\overline{RE1}$	→	→
27	NC	NC	NC	$\overline{RE2}$	→	→
28	D0	NC	$\overline{CE3}$	D0	NC	$\overline{CE3}$
29	Q0	NC	$\overline{CE4}$	Q0	NC	$\overline{CE4}$
30	VDD	→	→	→	→	→



30 PIN
SIP MODULE
TOP VIEW

* PIN 6 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEFICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED

MEMORY DEVICES WITH A CAPACITY OF UP TO 4Mb BY 1 CAN BE ACCOMIDATED ON THE MODULES DEFINED IN THIS STANDARD

FIGURE 4.2–2

30 PIN DRAM MODULE FAMILY

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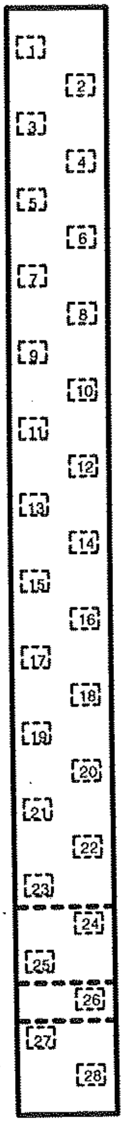
VERSION	@ N X 1	# N X 1	& N X 4	% N X 4
1	VSS	VSS	VSS	VSS
2	$\overline{RE0}$	$\overline{RE0}$	Q0	Q0
3	$\overline{RE1}$	$\overline{RE1}$	D0	D0
4	* A10	A10	Q0	Q0
5	* A9	A9	D1	D1
6	A0	A0	* A10	A10
7	A1	A1	* A9	A9
8	A2	A2	A0	A0
9	A3	A3	A1	A1
10	VCC	VCC	A2	A2
11	D	D	A3	A3
12	Q	Q	VCC	VCC
13	$\overline{W}$	$\overline{W}$	$\overline{RE}$	$\overline{RE}$
14	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
15	VCC	VCC	$\overline{W}$	$\overline{W}$
16	A4	A4	VCC	VCC
17	A5	A5	A4	A4
18	A6	A6	A4	A4
19	A7	A7	A6	A6
20	A8	A8	A7	A7
21	$\overline{RE2}$	A11	A8	A8
22	$\overline{RE3}$	NC	D2	A11
23	VSS	$\overline{RE2}$	Q2	NC
24		$\overline{RE3}$	D3	D2
25		VSS	Q3	Q2
26			VSS	D3
27				Q3
28				VSS



**23, 25, 26, OR 28
PIN ZIP SIMM
TOP VIEW**

N = THE ADDRESS CAPACITY OF THE MEMORY DEVICE USED

@ THIS CONFIGURATION IS APPLICABLE TO 1M, 4M, & 16M X 1 DEVICES.

THIS CONFIGURATION IS APPLICABLE TO A 64M X 1 DEVICE

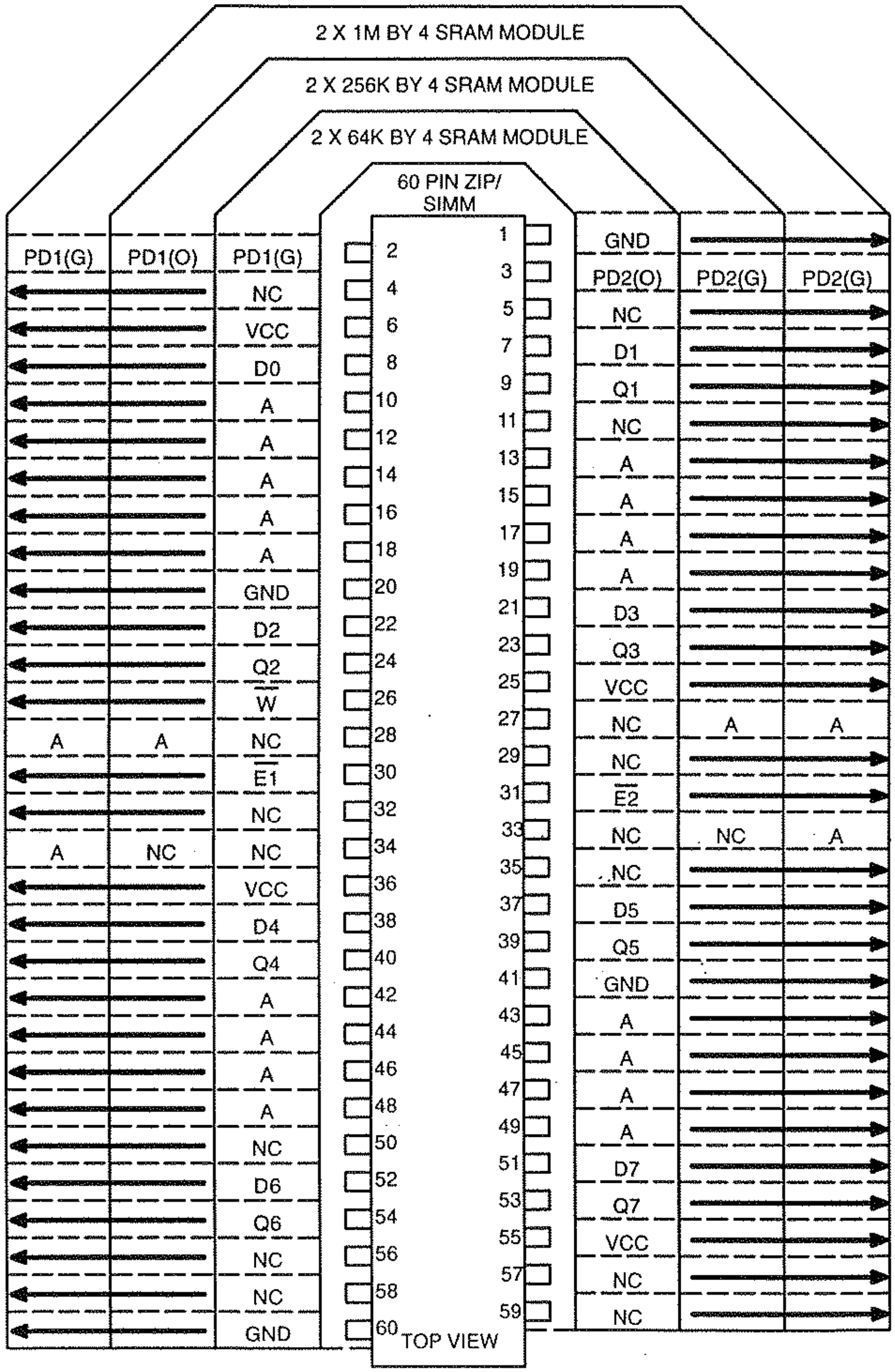
& THIS CONFIGURATION IS APPLICABLE TO 256K, 1M, & 4M X 4 DEVICES.

% THIS CONFIGURATION IS APPLICABLE TO A 16M X 4 DEVICE

* THESE ADDRESS PINS ARE NC WHEN NOT NEEDED FOR THE MEMORY DEVICE USED.

FIGURE 4.2–3

23/25/26/28 PIN DRAM MODULE FAMILY



2 X 1M BY 4 SRAM MODULE	2 X 256K BY 4 SRAM MODULE	2 X 64K BY 4 SRAM MODULE	60 PIN ZIP/ SIMM
PD1(G)	PD1(O)	PD1(G)	2
←	←	NC	4
←	←	VCC	6
←	←	D0	8
←	←	A	10
←	←	A	12
←	←	A	14
←	←	A	16
←	←	A	18
←	←	GND	20
←	←	D2	22
←	←	Q2	24
←	←	$\overline{W}$	26
A	A	NC	28
←	←	$\overline{E1}$	30
←	←	NC	32
A	NC	NC	34
←	←	VCC	36
←	←	D4	38
←	←	Q4	40
←	←	A	42
←	←	A	44
←	←	A	46
←	←	A	48
←	←	NC	50
←	←	D6	52
←	←	Q6	54
←	←	NC	56
←	←	NC	58
←	←	GND	60

60 PIN ZIP/ SIMM	2 X 64K BY 4 SRAM MODULE	2 X 256K BY 4 SRAM MODULE	2 X 1M BY 4 SRAM MODULE
1	GND	→	→
3	PD2(O)	PD2(G)	PD2(G)
5	NC	→	→
7	D1	→	→
9	Q1	→	→
11	NC	→	→
13	A	→	→
15	A	→	→
17	A	→	→
19	A	→	→
21	D3	→	→
23	Q3	→	→
25	VCC	→	→
27	NC	A	A
29	NC	→	→
31	$\overline{E2}$	→	→
33	NC	NC	A
35	NC	→	→
37	D5	→	→
39	Q5	→	→
41	GND	→	→
43	A	→	→
45	A	→	→
47	A	→	→
49	A	→	→
51	D7	→	→
53	Q7	→	→
55	VCC	→	→
57	NC	→	→
59	NC	→	→

The PD(n) pins are connected to GND (G) or left optn (O).

E1 ENABLES Q0, Q2, Q4, & Q6
E2 ENABLES Q1, Q3, Q5, & Q7

FIGURE 4.2–4
2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY

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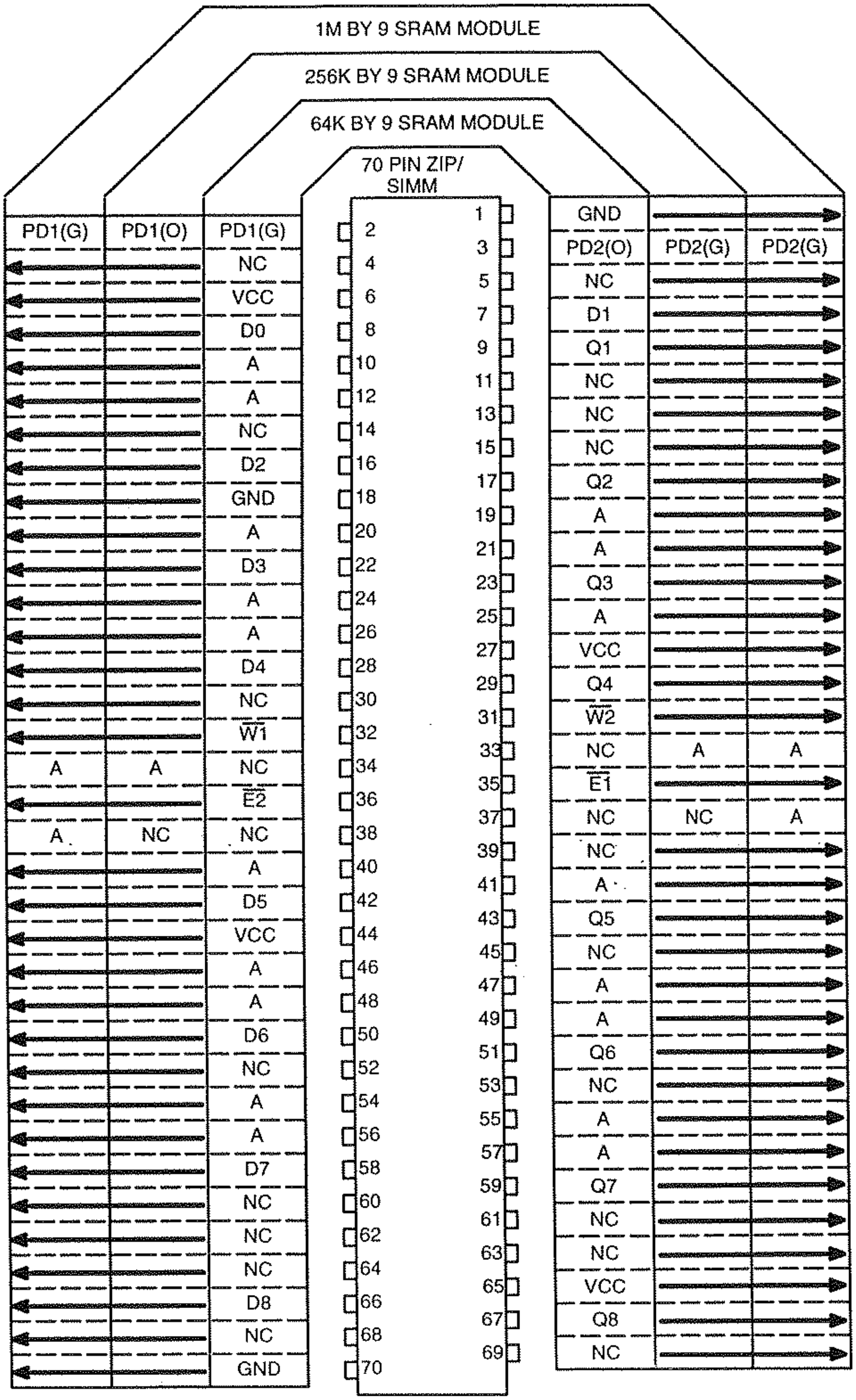

1M BY 9 SRAM MODULE	256K BY 9 SRAM MODULE	64K BY 9 SRAM MODULE	70 PIN ZIP/ SIMM	70 PIN ZIP/ SIMM	64K BY 9 SRAM MODULE	256K BY 9 SRAM MODULE	1M BY 9 SRAM MODULE
PD1(G)	PD1(O)	PD1(G)	2	1	GND	→	→
←	←	NC	4	3	PD2(O)	PD2(G)	PD2(G)
←	←	VCC	6	5	NC	→	→
←	←	D0	8	7	D1	→	→
←	←	A	10	9	Q1	→	→
←	←	A	12	11	NC	→	→
←	←	NC	14	13	NC	→	→
←	←	D2	16	15	NC	→	→
←	←	GND	18	17	Q2	→	→
←	←	A	20	19	A	→	→
←	←	D3	22	21	A	→	→
←	←	A	24	23	Q3	→	→
←	←	A	26	25	A	→	→
←	←	D4	28	27	VCC	→	→
←	←	NC	30	29	Q4	→	→
←	←	$\overline{W1}$	32	31	$\overline{W2}$	→	→
A	A	NC	34	33	NC	A	A
←	←	$\overline{E2}$	36	35	$\overline{E1}$	→	→
A	NC	NC	38	37	NC	NC	A
←	←	A	40	39	NC	→	→
←	←	D5	42	41	A	→	→
←	←	VCC	44	43	Q5	→	→
←	←	A	46	45	NC	→	→
←	←	A	48	47	A	→	→
←	←	D6	50	49	A	→	→
←	←	NC	52	51	Q6	→	→
←	←	A	54	53	NC	→	→
←	←	A	56	55	A	→	→
←	←	D7	58	57	A	→	→
←	←	NC	60	59	Q7	→	→
←	←	NC	62	61	NC	→	→
←	←	NC	64	63	NC	→	→
←	←	D8	66	65	VCC	→	→
←	←	NC	68	67	Q8	→	→
←	←	GND	70	69	NC	→	→

The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q1, Q2, Q3, Q5, Q6, Q7, Q8
E2 & W2 CONTROL Q4

FIGURE 4.2-5

64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY

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4.3 Two Byte Modules & Cards

4.3.1 – 76 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 9 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 18
128K, 512K, OR 2M BY 9
LOGIC FEATURE—2 SEPARATELY CONTROLLABLE BITS FOR USE AS PARITY BITS
PACKAGE—76 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.3–1

4.3.2 – 40 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 4M WORDS OF 16 OR 18 BITS
—64K TO 8M WORDS OF 8 OR 9 BITS
—128K TO 16M WORDS OF 4 BITS
—256K TO 32M WORDS OF 2 BITS
—512K TO 64M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
PACKAGE—40 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.3–2

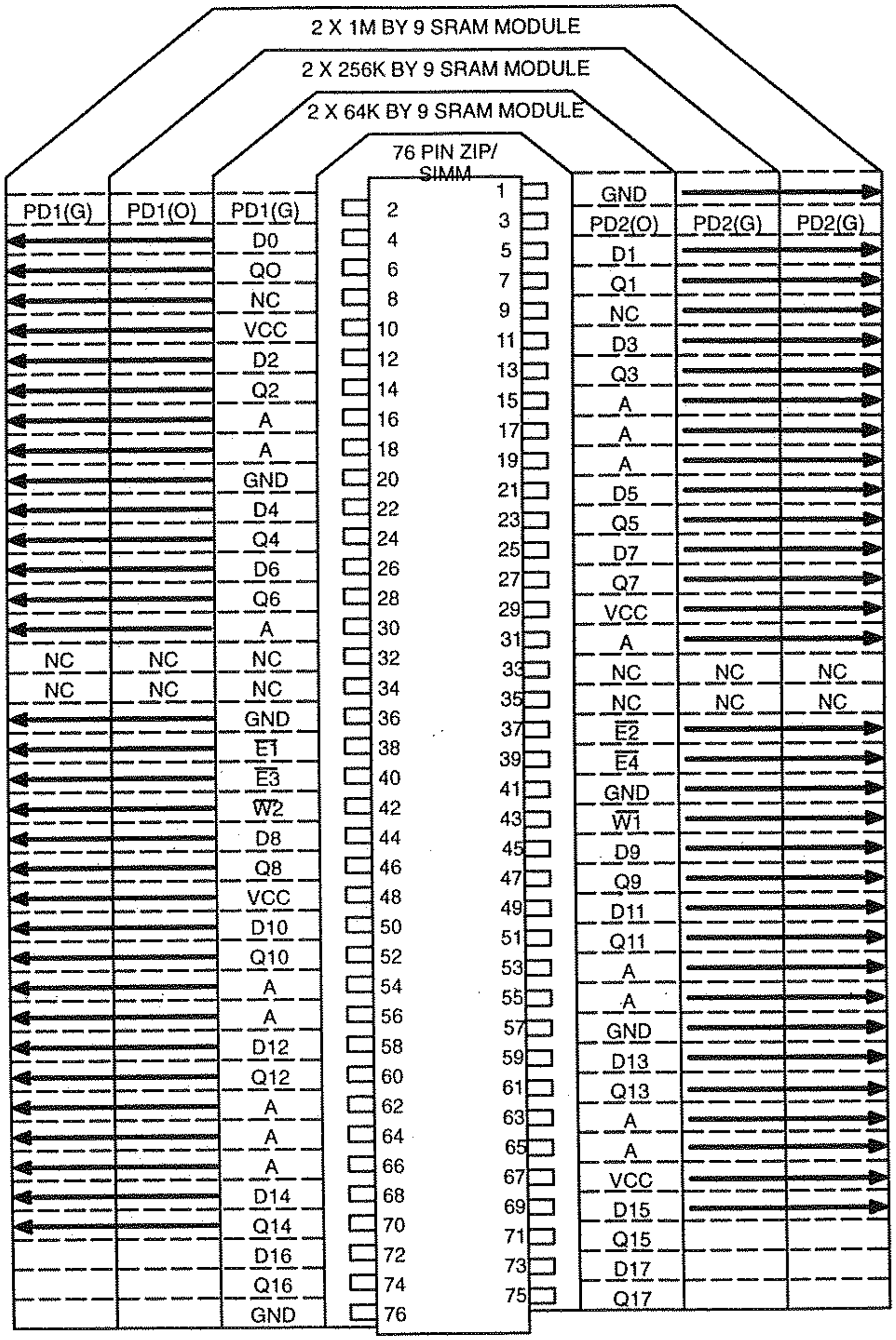
4.3.3 – 60 PIN DRAM CARD FAMILY

CAPACITY—512K, 1M, 2M, 4M, & 8M WORDS OF 16 OR 18 BITS
CONFIGURATION—SEVEN DIFFERENT CONFIGURATIONS
—USING 1Mb & 4Mb DEVICES AND WITH 1, 2, OR 4 RE CLOCKS.
LOGIC FEATURES, The cards contain a “PRESENCE DETECT” feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—60 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3–3A
CONFIGURATION BLOCK DIAGRAMS—Fig. 4.3–3B

4.3.4 – 68 PIN MULTIPLE TECHNOLOGY MEMORY CARD FAMILY

CAPACITY—UP TO 32M WORDS OF 16 BITS
CONFIGURATION—ONE BASIC CONFIGURATION that allows the use of SRAM, EEPROM, EPROM, or ROM memory devices with software or firmware control to accomidate the device characteristic differences.
LOGIC FEATURES,
—The card contains an internal MEMORY called the “ATTRIBUTE MEMORY”; the contents describe the hardware and software characteristics, and use of the card.
— The card contains a “PRESENCE DETECT” feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—68 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3–4A
MEMORY CARD OPERATION TRUTH TABLE— Page 4.3–4B
MEMORY CARD SPECIFIC TERMINOLOGY— Sec. 2.8, Page 2–13

1,60



PD1(G)	PD1(O)	PD1(G)	2
←	←	D0	4
←	←	QO	6
←	←	NC	8
←	←	VCC	10
←	←	D2	12
←	←	Q2	14
←	←	A	16
←	←	A	18
←	←	GND	20
←	←	D4	22
←	←	Q4	24
←	←	D6	26
←	←	Q6	28
←	←	A	30
NC	NC	NC	32
NC	NC	NC	34
←	←	GND	36
←	←	$\overline{E1}$	38
←	←	$\overline{E3}$	40
←	←	$\overline{W2}$	42
←	←	D8	44
←	←	Q8	46
←	←	VCC	48
←	←	D10	50
←	←	Q10	52
←	←	A	54
←	←	A	56
←	←	D12	58
←	←	Q12	60
←	←	A	62
←	←	A	64
←	←	A	66
←	←	D14	68
←	←	Q14	70
		D16	72
		Q16	74
		GND	76

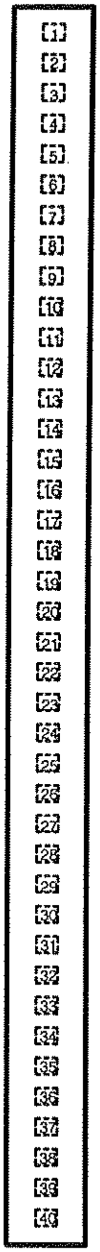
1	GND	→	→
3	PD2(O)	PD2(G)	PD2(G)
5	D1	→	→
7	Q1	→	→
9	NC	→	→
11	D3	→	→
13	Q3	→	→
15	A	→	→
17	A	→	→
19	A	→	→
21	D5	→	→
23	Q5	→	→
25	D7	→	→
27	Q7	→	→
29	VCC	→	→
31	A	→	→
33	NC	NC	NC
35	NC	NC	NC
37	$\overline{E2}$	→	→
39	$\overline{E4}$	→	→
41	GND	→	→
43	$\overline{W1}$	→	→
45	D9	→	→
47	Q9	→	→
49	D11	→	→
51	Q11	→	→
53	A	→	→
55	A	→	→
57	GND	→	→
59	D13	→	→
61	Q13	→	→
63	A	→	→
65	A	→	→
67	VCC	→	→
69	D15	→	→
71	Q15		
73	D17		
75	Q17		

The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q2, Q4, Q6, Q10, Q12, Q14, Q16
E2 & W1 CONTROL Q1, Q3, Q5, Q7, Q11, Q13, Q15, Q17
E3 & W2 CONTROL Q8
E4 & W2 CONTROL Q9

FIGURE 4.3-1

2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY



40 PIN
SIP MODULE
TOP VIEW

PHYSICAL CONFIGURATION	8 OR 9 DEVICES LONG, SINGLE SIDED				8 OR 9 DEVICES LONG, DOUBLE SIDED			
VERSION	N X 8(9)	2N X 4	4N X 2	8N X 1	4N X 4	8N X 2	16N X 1	@ N X 18
1	VDD	→	→	→	→	→	→	→
2	NC	→	→	→	→	→	→	Q0
3	NC	→	→	→	→	→	→	D0
4	D0	NC	→	→	→	→	→	D17
5	Q0	NC	→	→	→	→	→	Q17
6	*A10	→	→	→	→	→	→	→
7	D1	NC	→	→	DQ0'	NC	→	DQ1
8	Q1	DQ0	NC	→	DQ0	NC	→	DQ16
9	A9	→	→	→	→	→	→	→
10	VSS	→	→	→	→	→	→	→
11	W	→	→	→	→	→	→	→
12	D2	NC	→	CE1	CE1	NC	CE1	DQ2
13	Q2	CE1	→	CE2	CE2	CE1	CE2	DQ15
14	A8	→	→	→	→	→	→	→
15	A7	→	→	→	→	→	→	→
16	D3	NC	→	→	DQ1'	DQ0'	DQ'	DQ3
17	Q3	DQ1	DQ0	→	DQ1	DQ0	DQ	DQ14
18	A6	→	→	→	→	→	→	→
19	A5	→	→	→	→	→	→	→
20	A4	→	→	→	→	→	→	→
21	D4	NC	→	CE3	NC	→	CE3	DQ4
22	Q4	NC	CE2	CE4	NC	CE2	CE4	DQ13
23	A3	→	→	→	→	→	→	→
24	A2	→	→	→	→	→	→	→
25	D5	NC	→	→	DQ2'	NC	→	DQ5
26	Q5	DQ2	NC	→	DQ2	NC	→	DQ12
27	A1	→	→	→	→	→	→	→
28	A0	→	→	→	→	→	→	→
29	D6	NC	→	CE5	NC	→	CE5	DQ6
30	Q6	NC	CE2	Q6	NC	CE3	CE6	DQ11
31	VSS	→	→	→	→	→	→	→
32	D7	NC			DQ3'	DQ1'	NC	DQ7
33	Q7	DQ3	DQ1	NC	DQ3	DQ1	NC	DQ10
34	CE	CE2	CE4	CE7	CE3	CE4	CE7	CE1
35	NC	→	→	CE8	CE4	NC	CE8	CE2
36	RE	→	→	→	RE1	→	→	→
37	NC	→	→	→	RE2	→	→	→
38	D8	NC	→	→	→	→	→	DQ8
39	Q8	NC	→	→	→	→	→	DQ9
40	VDD	→	→	→	→	→	→	→

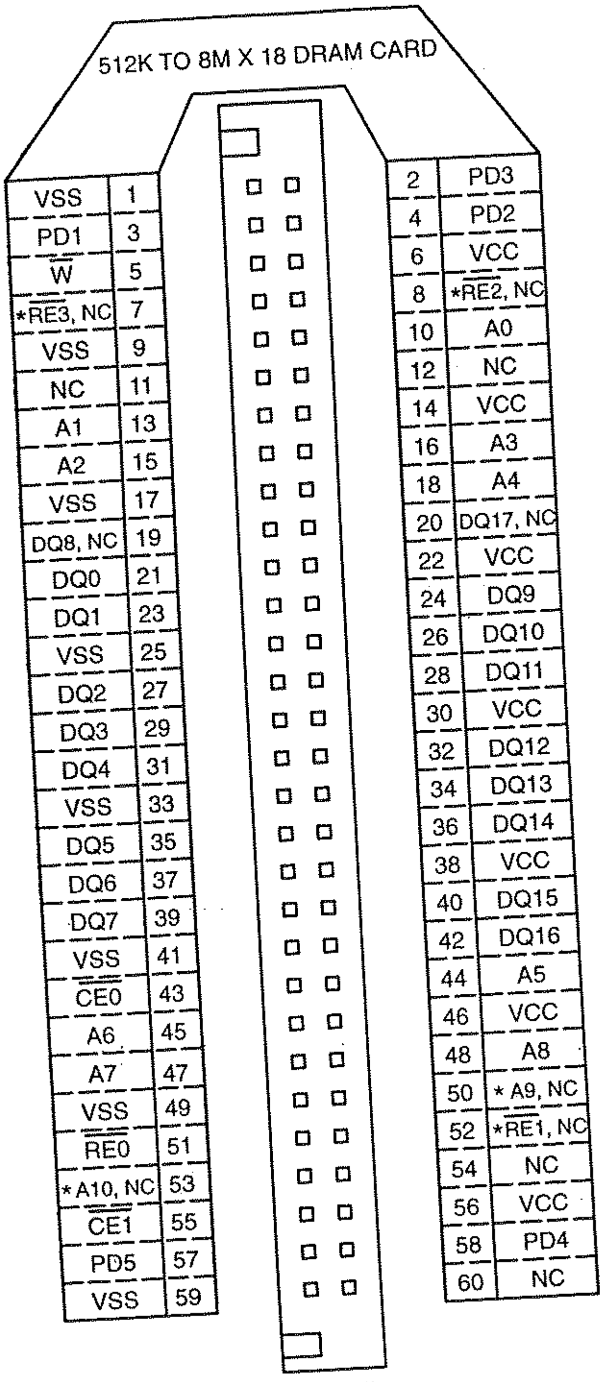
* PIN 5 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

@ N X 18 MODULE CAN BE USED AS A 2N X 9 BY CONNECTING ADJACENT D, Q, & DQ PINS TOGETHER

CONFIGURATION GIVES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE GIVING LENGTH AND NUMBER OF SIDED POPULATED, VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

THOSE PIN NAMES LABELED "'" (PRIME) ARE CONNECTED TO THE BACK SIDE OF THE MODULE ON THE DOUBLE SIDED CONFIGURATIONS.

FIGURE 4.3–2
40 PIN DRAM MODULE FAMILY



Signal	Pin	Pin	Signal
VSS	1	2	PD3
PD1	3	4	PD2
$\overline{W}$	5	6	VCC
*$\overline{RE3}$, NC	7	8	*$\overline{RE2}$, NC
VSS	9	10	A0
NC	11	12	NC
A1	13	14	VCC
A2	15	16	A3
VSS	17	18	A4
DQ8, NC	19	20	DQ17, NC
DQ0	21	22	VCC
DQ1	23	24	DQ9
VSS	25	26	DQ10
DQ2	27	28	DQ11
DQ3	29	30	VCC
DQ4	31	32	DQ12
VSS	33	34	DQ13
DQ5	35	36	DQ14
DQ6	37	38	VCC
DQ7	39	40	DQ15
VSS	41	42	DQ16
$\overline{CE0}$	43	44	A5
A6	45	46	VCC
A7	47	48	A8
VSS	49	50	* A9, NC
$\overline{RE0}$	51	52	*$\overline{RE1}$, NC
* A10, NC	53	54	NC
$\overline{CE1}$	55	56	VCC
PD5	57	58	PD4
VSS	59	60	NC

* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

	PD4	PD5
SPEED (tRAC)	58	57
80 NS	VSS	VSS
70 NS	VSS	NC
60 NS	NC	VSS
50 NS	NC	NC

PD SPEED TABLE

	PD1	PD2	PD3
CONFIGURATION	3	4	2
512K X 16/18 2 $\overline{RE}$	VSS	NC	VSS
1M X 16/18 4 $\overline{RE}$	VSS	NC	NC
2M X 16/18 2 $\overline{RE}$	NC	VSS	VSS
4M X 16/18 4 $\overline{RE}$	NC	VSS	NC
1M X 16/18 1 $\overline{RE}$	VSS	VSS	VSS
4M X 16/18 1 $\overline{RE}$	NC	NC	VSS
8M X 16/18 2 $\overline{RE}$	VSS	VSS	NC
NO CARD	NC	NC	NC

PD CONFIGURATION TABLE

	PIN NUMBER				
CONFIGURATION	50	53	52	8	7
512K X 16/18 2 $\overline{RE}$	NC	NC	RE1	NC	NC
1M X 16/18 4 $\overline{RE}$	NC	NC	RE1	RE2	RE3
2M X 16/18 2 $\overline{RE}$	A9	NC	RE1	NC	NC
4M X 16/18 4 $\overline{RE}$	A9	NC	RE1	RE2	RE3
1M X 16/18 1 $\overline{RE}$	A9	NC	NC	NC	NC
4M X 16/18 1 $\overline{RE}$	A9	A10	NC	NC	NC
8M X 16/18 2 $\overline{RE}$	A9	A10	RE1	NC	NC

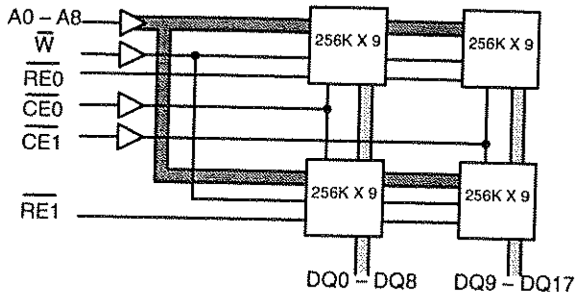
CONFIGURATION PIN ASSIGNMENT TABLE

Pins 19 & 20 (DQ8 & DQ 17) are NC for X16 Versions

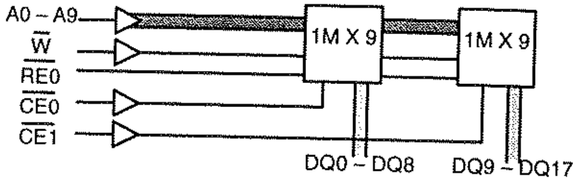
FIGURE 4.3-3A

60 PIN x16 or 18 DRAM CARD FAMILY PIN CONNECTIONS

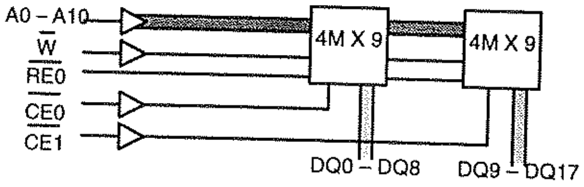
BLOCK DIAGRAM – 512K W 2 RE



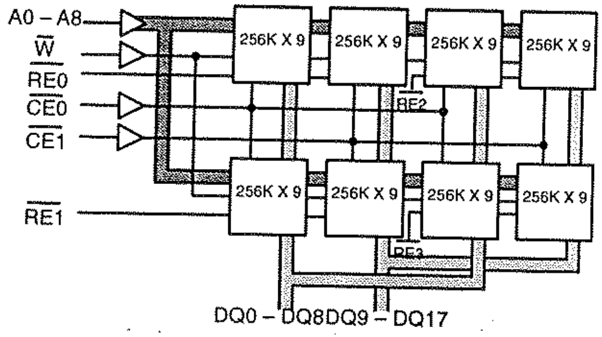
BLOCK DIAGRAM – 1 MW 1 RE



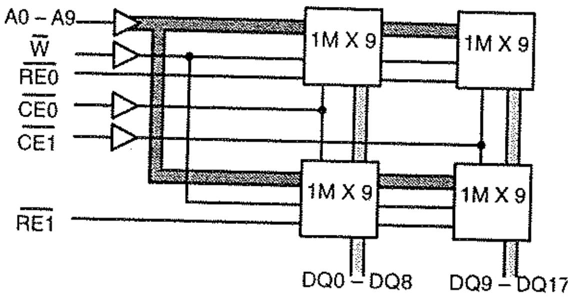
BLOCK DIAGRAM – 4 MW 1 RE



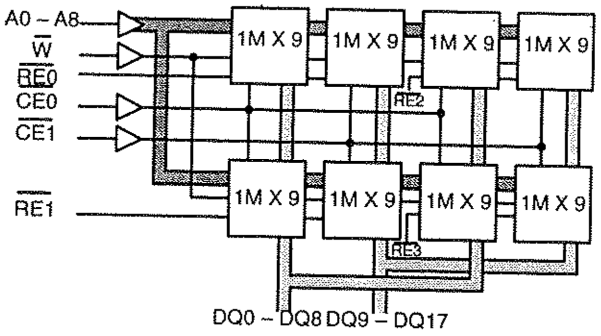
BLOCK DIAGRAM – 1 MW 4 RE



BLOCK DIAGRAM – 2 MW 2 RE



BLOCK DIAGRAM – 4 MW 4 RE



BLOCK DIAGRAM – 8 MW 2 RE

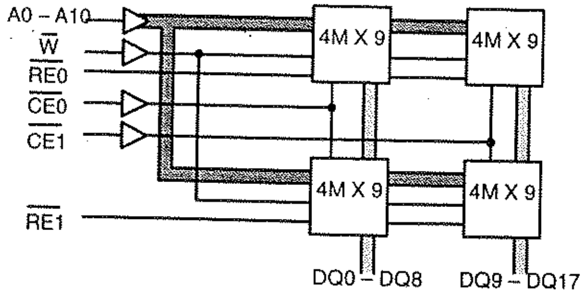


FIGURE 4.3–3B
60 PIN x16 or 18 DRAM CARD FAMILY BLOCK DIAGRAMS

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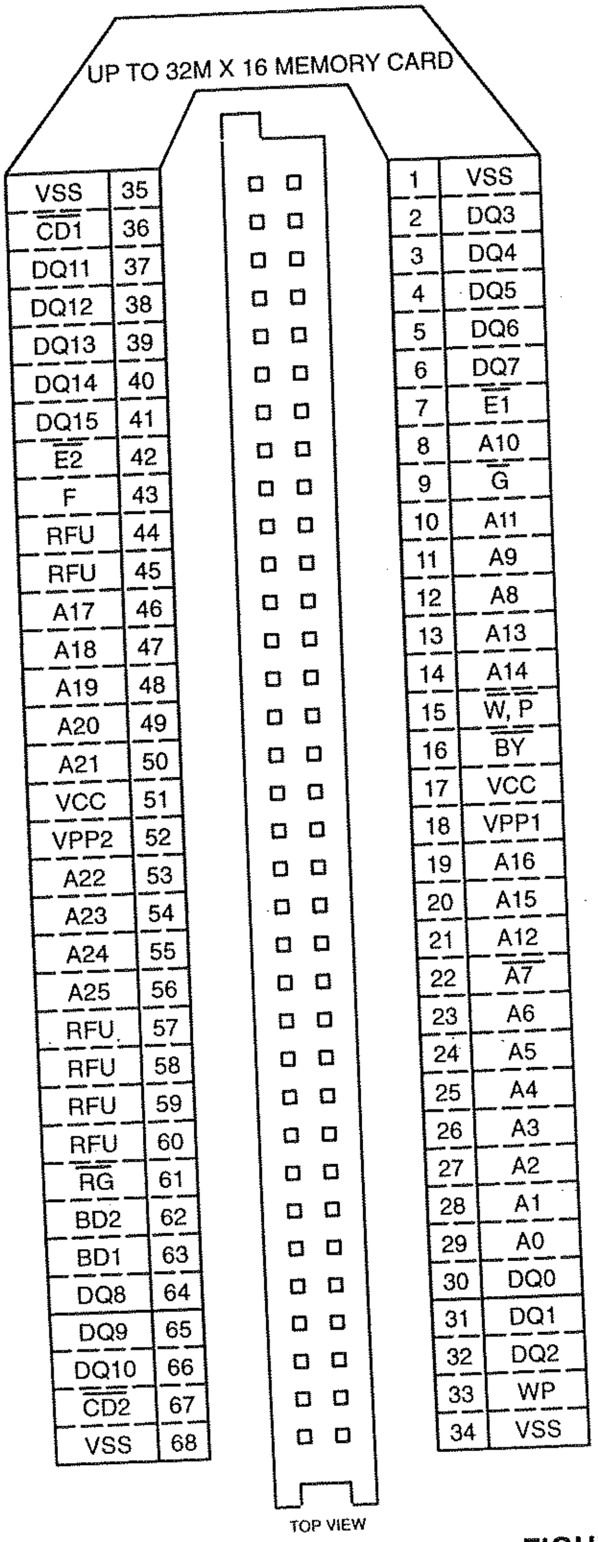

VSS	35	1	VSS
$\overline{CD1}$	36	2	DQ3
DQ11	37	3	DQ4
DQ12	38	4	DQ5
DQ13	39	5	DQ6
DQ14	40	6	DQ7
DQ15	41	7	$\overline{E1}$
$\overline{E2}$	42	8	A10
F	43	9	$\overline{G}$
RFU	44	10	A11
RFU	45	11	A9
A17	46	12	A8
A18	47	13	A13
A19	48	14	A14
A20	49	15	$\overline{W}, \overline{P}$
A21	50	16	$\overline{BY}$
VCC	51	17	VCC
VPP2	52	18	VPP1
A22	53	19	A16
A23	54	20	A15
A24	55	21	A12
A25	56	22	A7
RFU	57	23	A6
RFU	58	24	A5
RFU	59	25	A4
RFU	60	26	A3
$\overline{RG}$	61	27	A2
BD2	62	28	A1
BD1	63	29	A0
DQ8	64	30	DQ0
DQ9	65	31	DQ1
DQ10	66	32	DQ2
$\overline{CD2}$	67	33	WP
VSS	68	34	VSS

* NOTE: This Standard is applicable to SRAM, EPROM, OTPROM, EEPROM, and FLASH Memory. It is not applicable to DRAM.

FIGURE 4.3–4A

68 PIN MULTIPLE TECHNOLOGY CARD FAMILY

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Main Memory Read Function for all types of Memory Card except DRAM

MODE	$\overline{\text{RG}}$	$\overline{\text{E2}}$	$\overline{\text{E1}}$	A0	$\overline{\text{G}}$	$\overline{\text{W}}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	H	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	H	H	L	H	L	H	VCC	VCC	High–Z	Odd–Byte
Word Access (16 bits)	H	L	L	X	L	H	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	L	H	VCC	VCC	Odd–Byte	High–Z

Main Memory Write Function for SRAM and EEPROM

MODE	$\overline{\text{RG}}$	$\overline{\text{E2}}$	$\overline{\text{E1}}$	A0	$\overline{\text{G}}$	$\overline{\text{W}}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	H	H	L	H	H	L	VCC	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VCC	VCC	Odd–Byte	High–Z

Main Memory Write Function for OTPROM, EPROM, and FLASH Memory

MODE	$\overline{\text{RG}}$	$\overline{\text{E2}}$	$\overline{\text{E1}}$	A0	$\overline{\text{G}}$	$\overline{\text{W}}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	H	H	L	H	H	L	VPP	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VPP	VPP	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VPP	VCC	Odd–Byte	XXX

Attribute Memory Read Function

MODE	$\overline{\text{RG}}$	$\overline{\text{E2}}$	$\overline{\text{E1}}$	A0	$\overline{\text{G}}$	$\overline{\text{W}}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	L	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	L	H	L	H	L	H	VCC	VCC	High–Z	Not Valid
Word Access (16 bits)	L	L	L	X	L	H	VCC	VCC	Not Valid	Even–Byte
Odd–Byte Only Access	L	L	H	X	L	H	VCC	VCC	Not Valid	High–Z

Attribute Memory Write Function for SRAM and EEPROM

MODE	$\overline{\text{RG}}$	$\overline{\text{E2}}$	$\overline{\text{E1}}$	A0	$\overline{\text{G}}$	$\overline{\text{W}}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VCC	VCC	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VCC	VCC	XXX	XXX

Attribute Memory Write Function for OTPROM, EPROM, and FLASH Memory

MODE	$\overline{\text{RG}}$	$\overline{\text{E2}}$	$\overline{\text{E1}}$	A0	$\overline{\text{G}}$	$\overline{\text{W}}$	VPP2	VPP1	XXX	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VPP	VPP	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VPP	VCC	XXX	XXX

NOTE: For those pins in the above tables where "VCC, VPP" is specified, either supply may be used for programming at the option of the manufacturer. However those cards which use VCC must be able to withstand VPP without damage.

FIGURE 4.3–4B

68 PIN MULTIPLE TECHNOLOGY CARD FAMILY FUNCTION TABLES

4.4 Four Byte Modules & Cards

4.4.1 – 64 & 72 PIN ZIP/SIMM SRAM MODULE

4.4.2 – 72 PIN SIMM DRAM MODULE FAMILY

– 72 PIN SIMM DRAM ECC MODULE FAMILY

4.4.3 – 88 PIN DRAM CARD FAMILY

4.4.4 – 72 PIN DRAM SO–DIMM FAMILY

4.4.5 – 88 PIN DRAM SO–DIMM FAMILY

4.4.6 – 112 PIN MPDRAM DIMM FAMILY

4.4.7 – 80 PIN EEPROM SIMM FAMILY

4.4.8 – 100 PIN DRAM, SDRAM & ROM DIMM FAMILY

4.4.1 – 64 & 72 PIN ZIP/SIMM SRAM MODULE

CAPACITY—16K, 32K, 64K, 128K, 256K, 512K, 1M, 2M, or 4M WORDS OF 32 BITS
CONFIGURATION—FOUR BANK MODULE
—SELECTABLE BY BYTE GROUPS
LOGIC FEATURE—The 72 pin modules are supersets of the 64 pin family with added capacity.
PACKAGE—64 and 72 PIN SIP MODULEWITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.4.1–1

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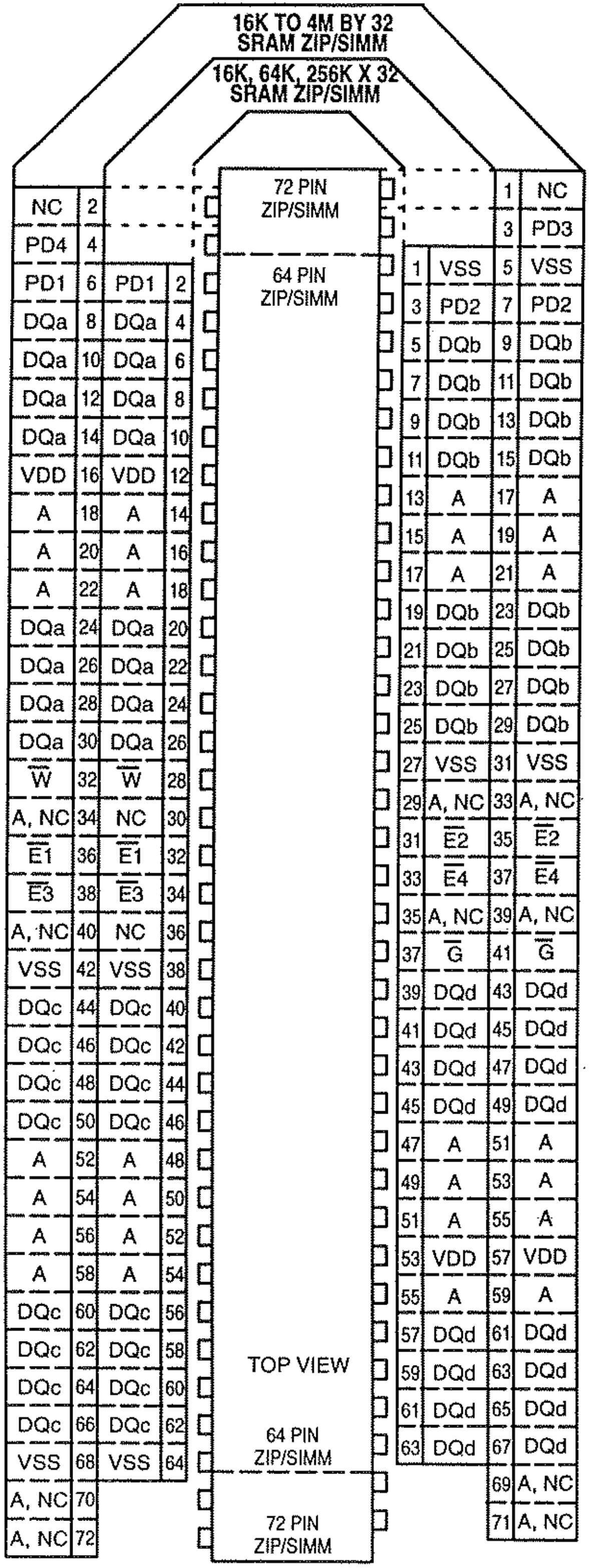

72 PIN		64 PIN		64 PIN		72 PIN	
NC	2					1	NC
PD4	4					3	PD3
PD1	6	PD1	2	1	VSS	5	VSS
DQa	8	DQa	4	3	PD2	7	PD2
DQa	10	DQa	6	5	DQb	9	DQb
DQa	12	DQa	8	7	DQb	11	DQb
DQa	14	DQa	10	9	DQb	13	DQb
VDD	16	VDD	12	11	DQb	15	DQb
A	18	A	14	13	A	17	A
A	20	A	16	15	A	19	A
A	22	A	18	17	A	21	A
DQa	24	DQa	20	19	DQb	23	DQb
DQa	26	DQa	22	21	DQb	25	DQb
DQa	28	DQa	24	23	DQb	27	DQb
DQa	30	DQa	26	25	DQb	29	DQb
$\overline{W}$	32	$\overline{W}$	28	27	VSS	31	VSS
A, NC	34	NC	30	29	A, NC	33	A, NC
$\overline{E1}$	36	$\overline{E1}$	32	31	$\overline{E2}$	35	$\overline{E2}$
$\overline{E3}$	38	$\overline{E3}$	34	33	$\overline{E4}$	37	$\overline{E4}$
A, NC	40	NC	36	35	A, NC	39	A, NC
VSS	42	VSS	38	37	$\overline{G}$	41	$\overline{G}$
DQc	44	DQc	40	39	DQd	43	DQd
DQc	46	DQc	42	41	DQd	45	DQd
DQc	48	DQc	44	43	DQd	47	DQd
DQc	50	DQc	46	45	DQd	49	DQd
A	52	A	48	47	A	51	A
A	54	A	50	49	A	53	A
A	56	A	52	51	A	55	A
A	58	A	54	53	VDD	57	VDD
DQc	60	DQc	56	55	A	59	A
DQc	62	DQc	58	57	DQd	61	DQd
DQc	64	DQc	60	59	DQd	63	DQd
DQc	66	DQc	62	61	DQd	65	DQd
VSS	68	VSS	64	63	DQd	67	DQd
A, NC	70					69	A, NC
A, NC	72					71	A, NC

NOTES for 72-pin ZIP/SIMM module pinout:
1. $\overline{E1}$ enables DQa pins 8, 10, 12, 14, and 24, 26, 28, 30; $\overline{E2}$ enables DQb pins 9, 11, 13, 15, and 23, 25, 27, 29; $\overline{E3}$ enables DQc pins 44, 46, 48, 50, and 60, 62, 64, 66; $\overline{E4}$ enables DQd pins 43, 45, 47, 49, and 61, 63, 65, 67.
2. $\overline{W}$ enables writing into all enabled devices.
3. $\overline{G}$ enables outputs from any and all enabled devices.
4. This footprint is a superset of the 64-pin JEDEC standard. Any 64 pin JEDEC standard module may be used in the 72-pin footprint. PD3 and PD4 become NC (OPEN) in this case.
5. Two pins (1 & 2) are available for future definition.

PRESENCE DETECT TRUTH TABLE

MOD CONFIG	PD4	PD3	PD2	PD1
72P MOD	PIN 68	PIN 67	PIN 66	PIN 11
# 16K X 32	O	O	O	S
32K X 32	S	S	O	O
# 64K X 32	O	O	S	O
128K X 32	S	O	O	O
# 256K X 32	O	O	S	S
512K X 32	O	S	O	O
1M X 32	O	S	O	S
2M X 32	O	S	S	O
4M X 32	O	S	S	S

O = OPEN CIRCUIT (NO CONNECTION)
S = CONNECTED TO VSS

# Indicates configurations duplicated in 64P package. Use PD1 & PD2 only.

PRESENCE DETECT NOTES
1. Compatibility has been maintained with existing 64-pin standard
2. PD signature has been added for 32K X 32 & 128K X 32 configurations that were not implemented in the 64-pin standard.
3. Six PD signatures are left undefined for future definition.

ADDRESS PIN ASSIGNMENTS

CONFIGURATION	ADDRESS PIN NUMBER							
72 P MODULES	33	34	40	39	69	70	71	72
16K X 32	NC	NC	NC	NC	NC	NC	NC	NC
32K X 32	A	NC	NC	NC	NC	NC	NC	NC
64K X 32	A	A	NC	NC	NC	NC	NC	NC
128K X 32	A	A	A	NC	NC	NC	NC	NC
256K X 32	A	A	A	A	NC	NC	NC	NC
512K X 32	A	A	A	A	A	NC	NC	NC
1M X 32	A	A	A	A	A	A	NC	NC
2M X 32	A	A	A	A	A	A	A	NC
4M X 32	A	A	A	A	A	A	A	A
64 P MODULES	29	30	35	36				
16K X 32	NC	NC	NC	NC				
64K X 32	A	A	NC	NC				
256K X 32	A	A	A	A				

FIGURE 4.4.1-1
16K TO 4M BY 32 SRAM ZIP/SIMM MODULE

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NOTE: The 72 pin module standards that follow describe two separate devices. Both have a 4 byte data interface. One is intended to be used with or without parity bits while the other contains error correction bits ECC). The one with ECC is similar to the parity module but is not completely pin compatible

4.4.2 – 72 PIN SIMM DRAM MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 32 or 36 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES

LOGIC FEATURES, These modules contain a "presence detect" feature which conists of output pins which supply an encoded value which defines the storage capacity and speed of the module.

PACKAGE—72 PIN SIMM MODULE

PIN ASSIGNMENTS—Fig. 4.4.2–2A

BLOCK DIAGRAMS—Fig. 4.4.2–2 A⇒K. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–2 B⇒K

POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

– 72 PIN SIMM DRAM ECC MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 36 or 39 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES

LOGIC FEATURES, These modules are optimized for ECC applications. They are similar to but not the same as the modules described in Fig. 4–6. The Standard defines a "presence detect" feature which consists of output pins which supply an encoded value which defines the storage capacity and speed of the module. The PD code identifies the presence of an ECC module as well as the speed and organization of the module. The Standard also defines the logic organization of the modules in Figs. 4.4.2–3B & 4.4.2–3C.

PACKAGE—72 PIN SIMM MODULE

PIN ASSIGNMENTS—Fig. 4.4.2–3A

BLOCK DIAGRAMS—Figs. 4.4.2–3 B & C. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–3 B & C

POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

72 Pin SIMM Block Diagrams

The block diagrams given in the 12 pages, Figs 4.4.2–2 B ⇒ K and Figs 4.4.2–3 B & C), are applicable to the 72 Pin SIMM pinouts shown in Figures 4.4.2–2 A and 4.4.2–3 A. These block diagrams are provided for guidance only. **Other implementations with different block configurations are also acceptable**.

The following table shows the applicability of the block configurations given to the 5 V and 3.3 V Non–ECC and ECC modules.

Configuration	# Banks	Applies to: 5 V SIMM	Applies to: 3.3 V SIMM
Parity, Non–Parity			
X32/36 W/X4, X1 (X36)	1 or 2	X	X
X32/36 W/X16, X18	1 or 2	X	X
X36 W/X4, X4/4CE	1 or 2	X	X
X36 W/X4, X2/2CE	1 or 2	X	X
X36 W/X16, X4/4CE	1 or 2	X	X
X36 W/X16, X2/2CE	1 or 2	X	X
X32 W/X8	1 or 2		X
X36 W/X8, X2/2CE	1 or 2		X
X32 W/X32	1 or 2		X
X36 W/X32, X2/2CE	1 or 2		X
ECC			
X36/40 W/X4	1 or 2	X	X (X36 only)
Note: To reduce the number of diagrams, only 2 bank versions are shown. In addition, in cases where one SIMM I/O width can be described as a depopulation of another SIMM (i.e. X36⇒X32), the depopulated devices are shown by a "dashed" outline.			

$\overline{\text{RE}}$ AND $\overline{\text{G}}$ WIRING FOR BYTE WRITE SIMMS.		
SIGNAL NAME	5 V SIMMs	3.3 V SIMMs
$\overline{\text{G}}$	Tied to GND	Wired to Pin 46
$\overline{\text{RE0}}$	Connected as shown. Tied to pin 44 ($\overline{\text{RE0}}$)	$\overline{\text{RE0}}$, $\overline{\text{RE2}}$ nets connected together and tied to pin 44 ($\overline{\text{RE0}}$)
$\overline{\text{RE1}}$	Connected as shown. Tied to pin 45 ($\overline{\text{RE1}}$)	$\overline{\text{RE1}}$, $\overline{\text{RE3}}$ nets connected together and tied to pin 45 ($\overline{\text{RE1}}$)
$\overline{\text{RE2}}$	Connected as shown. Tied to pin 34 ($\overline{\text{RE2}}$)	$\overline{\text{RE0}}$, $\overline{\text{RE2}}$ nets connected together and tied to pin 44 ($\overline{\text{RE0}}$)
$\overline{\text{RE3}}$	Connected as shown. Tied to pin 33 ($\overline{\text{RE3}}$)	$\overline{\text{RE1}}$, $\overline{\text{RE3}}$ nets connected together and tied to pin 45 ($\overline{\text{RE1}}$)

FIGURE 4.4.2–1
72 PIN DRAM SIMM APPLICABILITY TABLE

	5 V Byte Write	3.3 V Byte Write		5 V Byte Write	3.3 V Byte Write
PIN #	PIN NAME	PIN NAME	PIN #	PIN NAME	PIN NAME
1	VSS	VSS	37	PDQ17, NC	PDQ17, NC
2	DQ0	DQ0	38	PDQ35,, NC	PDQ35,, NC
3	DQ18	DQ18	39	VSS	VSS
4	DQ1	DQ1	40	$\overline{\text{CE0}}$	$\overline{\text{CE0}}$
5	DQ19	DQ19	41	$\overline{\text{CE2}}$	$\overline{\text{CE2}}$
6	DQ2	DQ2	42	$\overline{\text{CE3}}$	$\overline{\text{CE3}}$
7	DQ20	DQ20	43	$\overline{\text{CE1}}$	$\overline{\text{CE1}}$
8	DQ3	DQ3	44	$\overline{\text{RE0}}$	$\overline{\text{RE0}}$
9	DQ21	DQ21	45	NC, $\overline{\text{RE1}}$	NC, $\overline{\text{RE1}}$
10	VDD	VDD	46	NC	$\overline{\text{G}}$
11	NU	PD5	47	$\overline{\text{W}}$	$\overline{\text{W}}$
12	A0	A0	48	PD(ECC)	PD(ECC)
13	A1	A1	49	DQ9	DQ9
14	A2	A2	50	DQ27	DQ27
15	A3	A3	51	DQ10	DQ10
16	A4	A4	52	DQ28	DQ28
17	A5	A5	53	DQ11	DQ11
18	A6	A6	54	DQ29	DQ29
19	NC, A10	NC, A10	55	DQ12	DQ12
20	DQ4	DQ4	56	DQ30	DQ30
21	DQ22	DQ22	57	DQ13	DQ13
22	DQ5	DQ5	58	DQ31	DQ31
23	DQ23	DQ23	59	VDD	VDD
24	DQ6	DQ6	60	DQ32	DQ32
25	DQ24	DQ24	61	DQ14	DQ14
26	DQ7	DQ7	62	DQ33	DQ33
27	DQ25	DQ25	63	DQ15	DQ15
28	A7	A7	64	DQ34	DQ34
29	NC, A11	NC, A11	65	DQ16	DQ16
30	VDD	VDD	66	NC	$\overline{\text{EDO}}$
31	A8	A8	67	PD1	PD1
32	NC, A9	NC, A9	68	PD2	PD2
33	NC, $\overline{\text{RE3}}$	NC, A12	69	PD3	PD3
34	$\overline{\text{RE2}}$	NC, A13	70	PD4	PD4
35	PDQ26, NC	PDQ26, NC	71	NC	PD(REF)
36	PDQ8, NC	PDQ8, NC	72	VSS	VSS

See Figure 4–18 for applicable block diagrams

PRESENCE DETECT TRUTH TABLE

CONFIGURATION	tRAC	$\overline{\text{ECC}}$	PD1	PD2	PD3	PD4
1MB (256K X 36) 64MB (16M X 32/36)	100 nS	O	S	O	S	S
	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
2MB (512K X 36) 128MB (32M X 32/36)	100 nS	O	O	S	S	S
	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O
4MB (1M X 36) 256MB (64M X 32/36)	100 nS	O	S	S	S	S
	80 nS	O	S	S	O	S
	70 nS	O	S	S	S	O
	60 nS	O	S	S	O	O
8MB (2M X 36) 0.5GB (128M X 32/36)	100 nS	O	O	O	S	S
	80 nS	O	O	O	O	S
	70 nS	O	O	O	S	O
	60 nS	O	O	O	O	O
16MB (4M X 36) 1GB (256M X 32/36)	50 nS	O	S	O	S	S
	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
32MB (8M X 36) 2GB (512M X 36)	50 nS	O	O	S	S	S
	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O

O = NO CONNECTION S = CONNECTED TO VSS

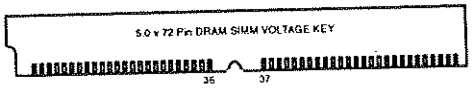
$\overline{\text{EDO}}$ Pin: VSS for EDO, NC for Fast Page.

Note: The $\overline{\text{ECC}}$ Function (Pin 48) is not a defined function for the devices in this standard, however, it is used in a companion Standard for 72 pin ECC modules shown in Fig. 4–10. The presence of a VSS connection on this pin signifies that an ECC module has been inserted.

CONFIGURATION PIN ASSIGNMENT TABLE

	MODULE SIZE, 36 BIT WORDS											
PIN #	256K	512K	1M	2M	4M	8M	16M	32M	64M	128M	256M	512M
19	NC	NC	NC	NC	A10	A10	A10	A10	A10	A10	A10	A10
*29	NC	NC	NC	NC	A11	A11	A11	A11	A11	A11	A11	A11
32	NC	NC	A9	A9	A9	A9	A9	A9	A9	A9	A9	A9
*33	NC	$\overline{\text{RE3}}$	NC	$\overline{\text{RE3}}$	NC	$\overline{\text{RE3}}$	A12	A12	A12	A12	A12	A12
*34	NC	$\overline{\text{RE2}}$	NC	$\overline{\text{RE2}}$	NC	$\overline{\text{RE2}}$	NC	NC	A13	A13	A13	A13
45	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	RE1

* A11, A12, or A13 on Pins 29, 33, or 34 are used on modules containing devices that require asymetric ROW/ COLUMN addresses.
NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.



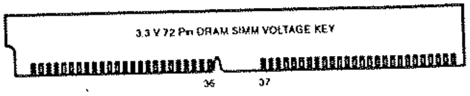


FIGURE 4.4.2–2 A
256K TO 256M BY 36, 72 PIN DRAM MODULE PINOUT

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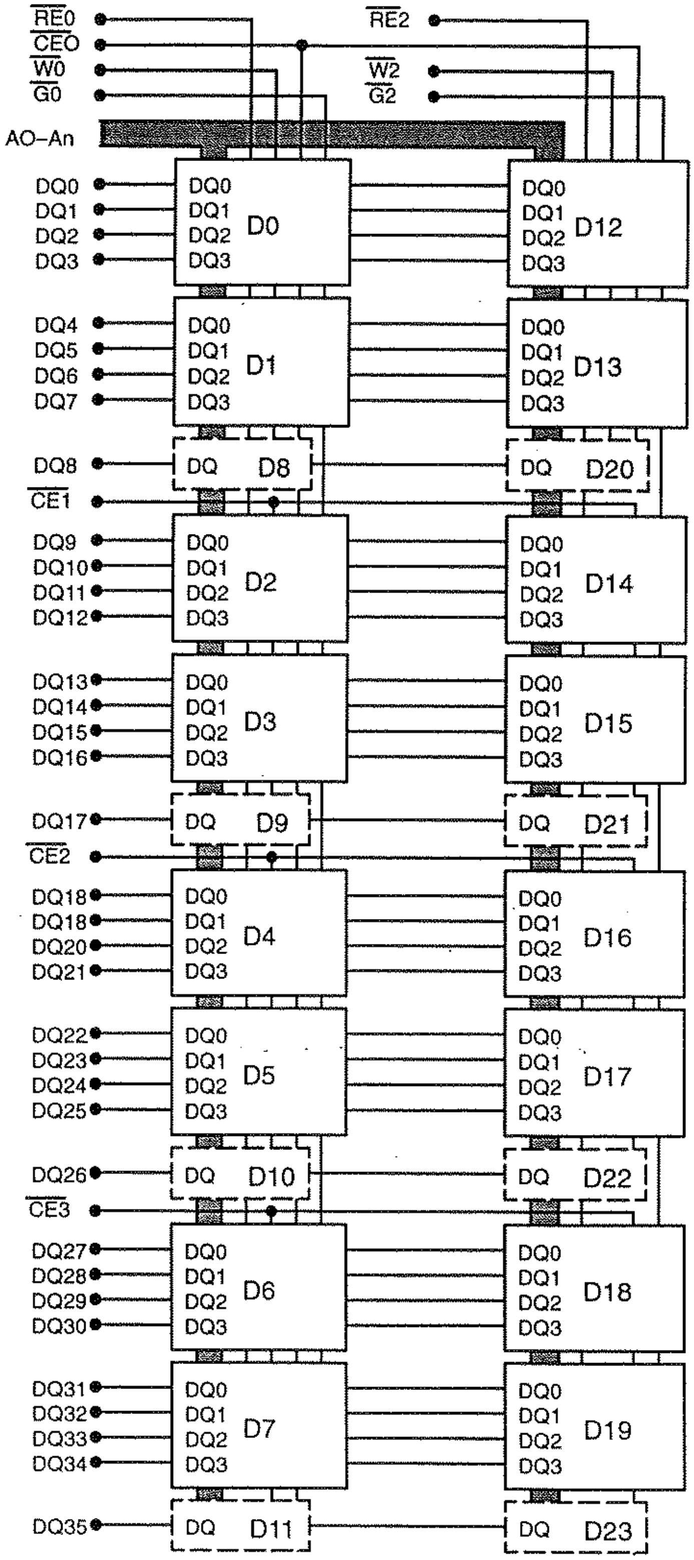

FIGURE 4.4.2-2 B
X32/36 DRAM SIMM, 2 Banks with X4 & X1 DRAMs

Release 6-7

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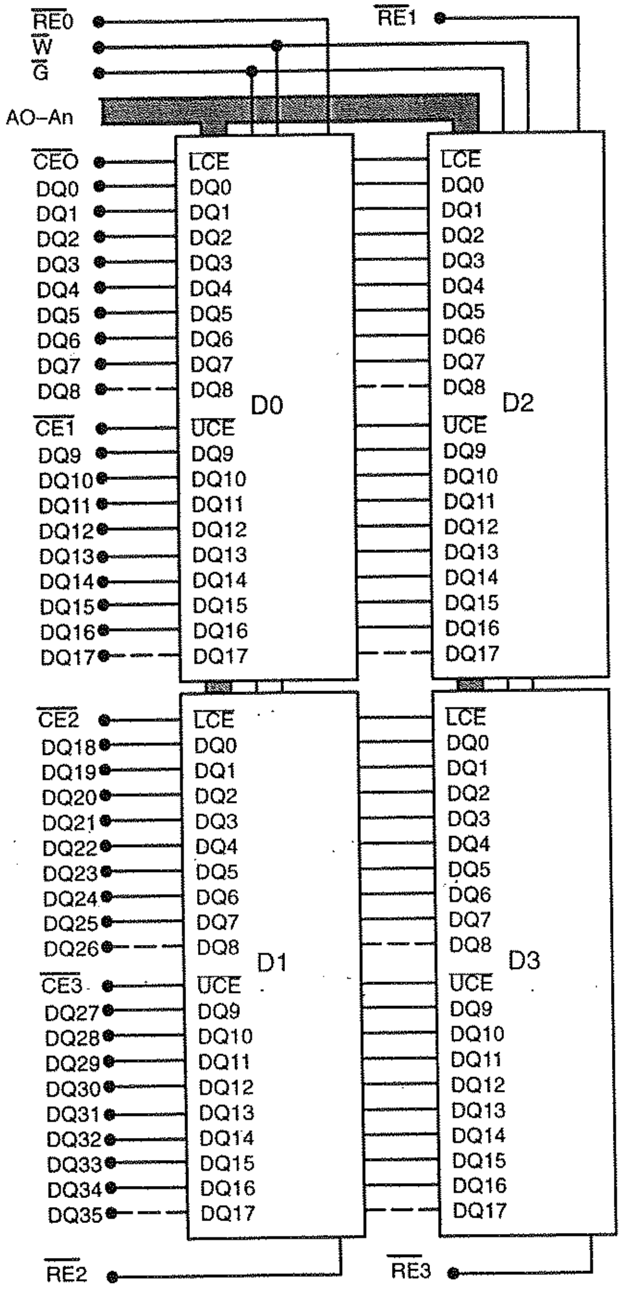

DQ8, DQ17, DQ26, & DQ35 ARE NOT USED
ON THE X32 MODULE USING X16 DRAM

FIGURE 4.4.2-2 C
X32/36 DRAM SIMM, 2 Banks with X16/18 DRAMs

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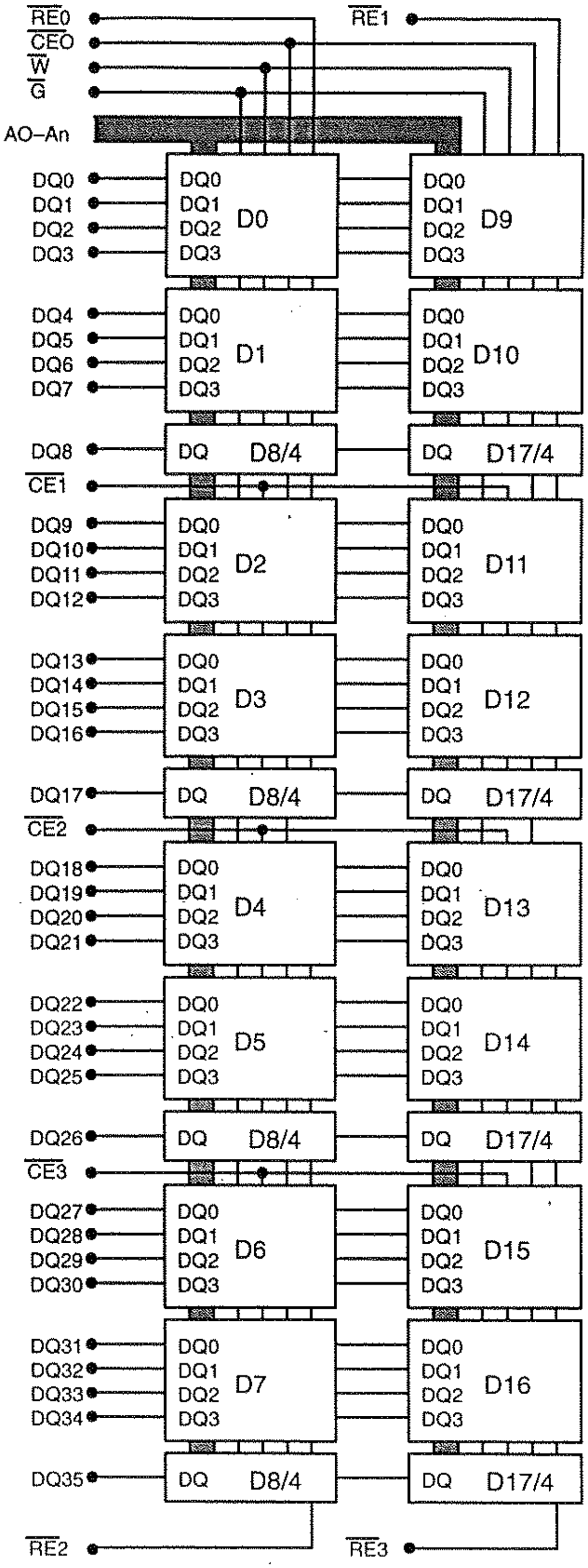

FIGURE 4.4.2-2 D
X36 DRAM SIMM, 2 Banks with X4 & X4 W/4 $\overline{CE}$ DRAMs

Release 6-7

1)75

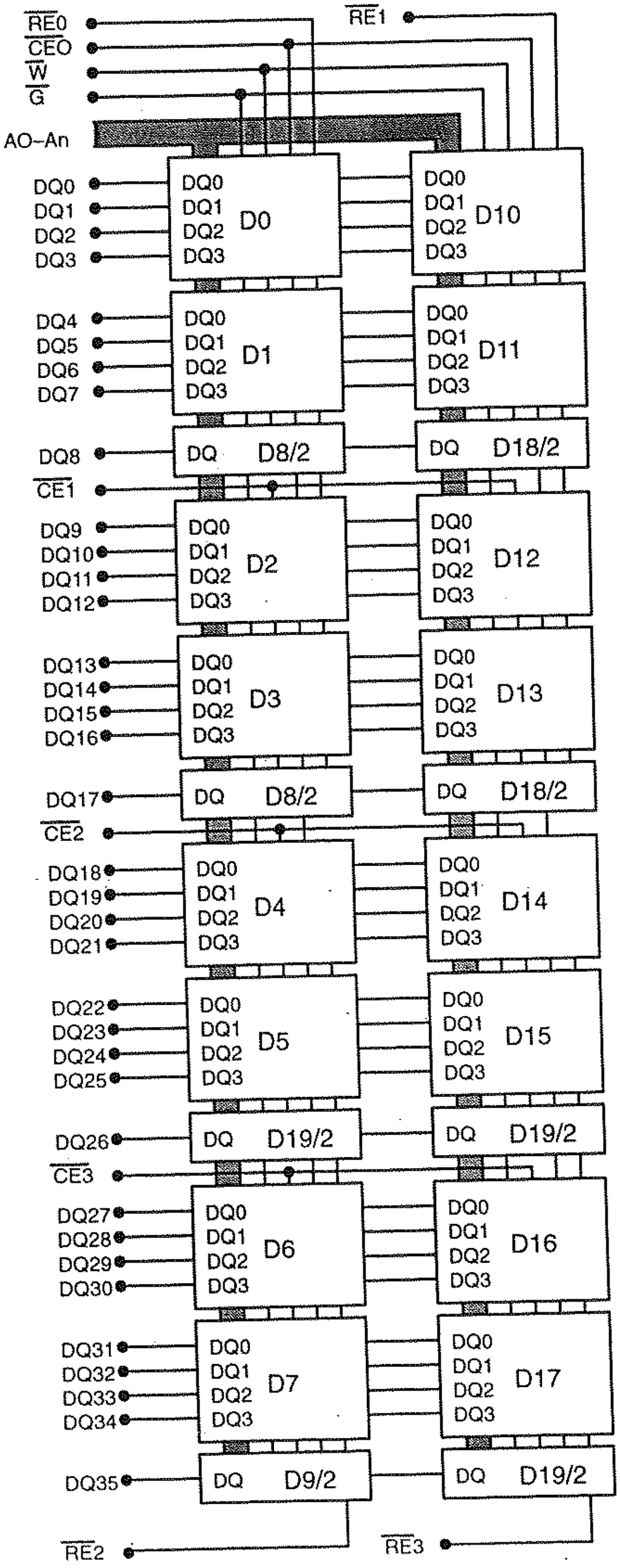

FIGURE 4.4.2–2 E

X36 DRAM SIMM, 2 Banks with X4 & X2 W/2 $\overline{\text{CE}}$ DRAMs

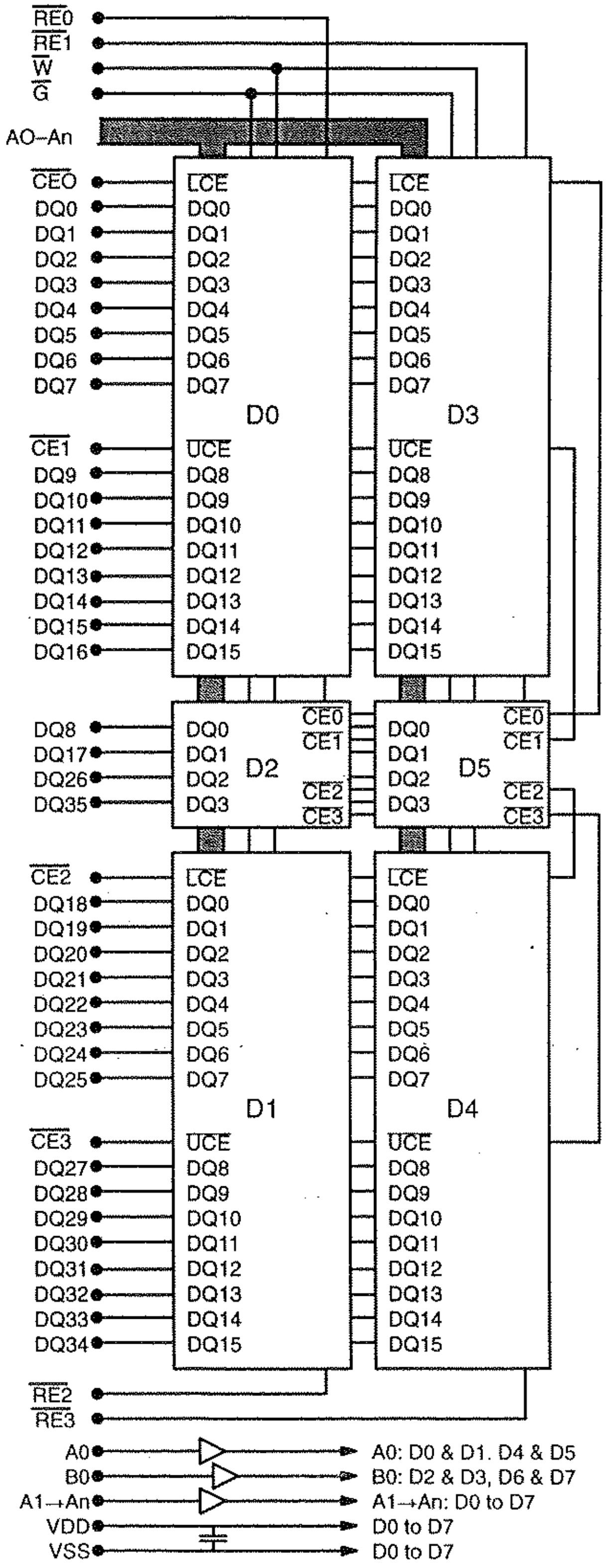

FIGURE 4.4.2–2 F
X36 DRAM SIMM, 2 Banks with X16 & X4 W/4 $\overline{CE}$ DRAMs

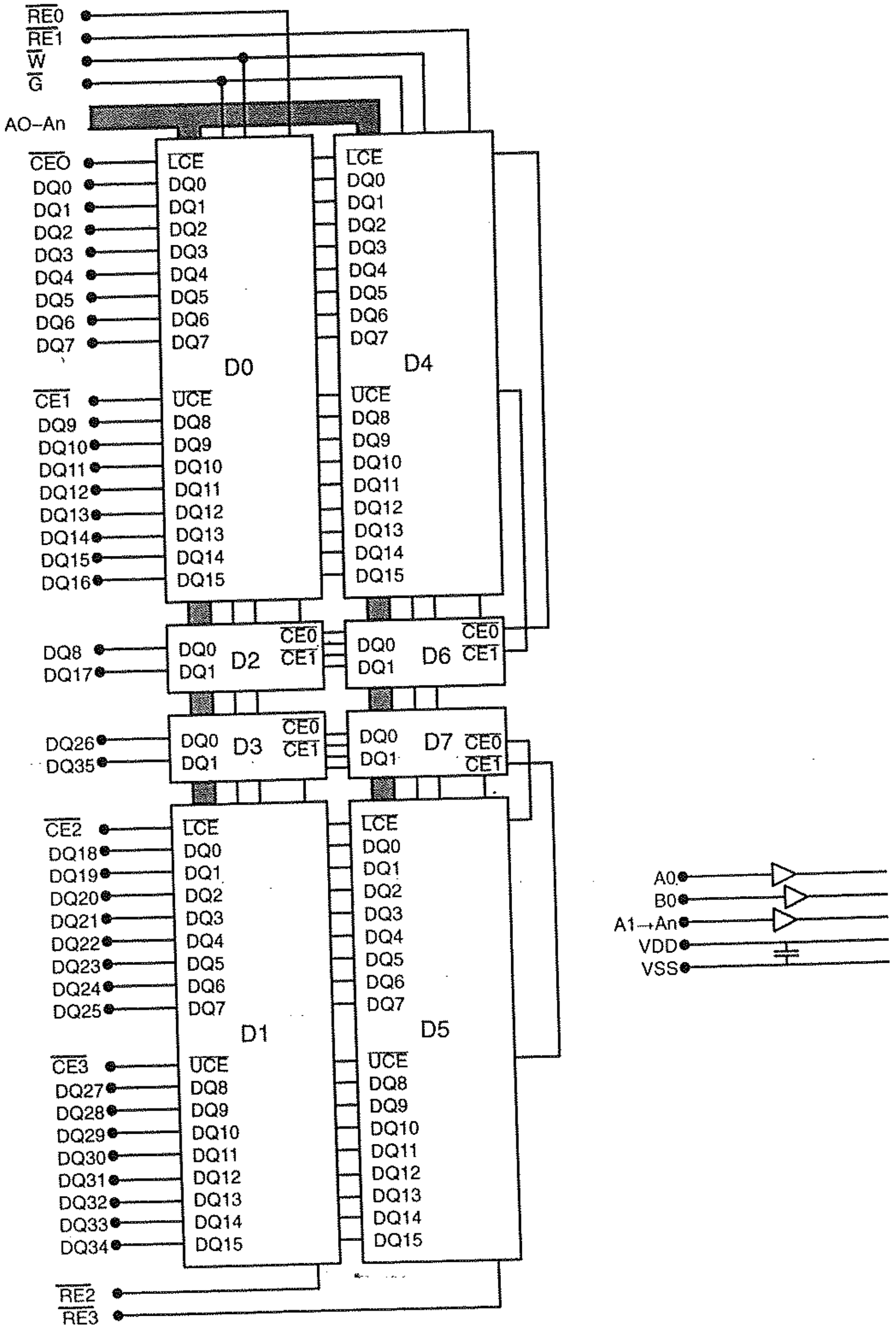

FIGURE 4.4.2–2 G
X36 DRAM SIMM, 2 bank with X16 & X2 W/2 $\overline{\text{CE}}$ DRAMs

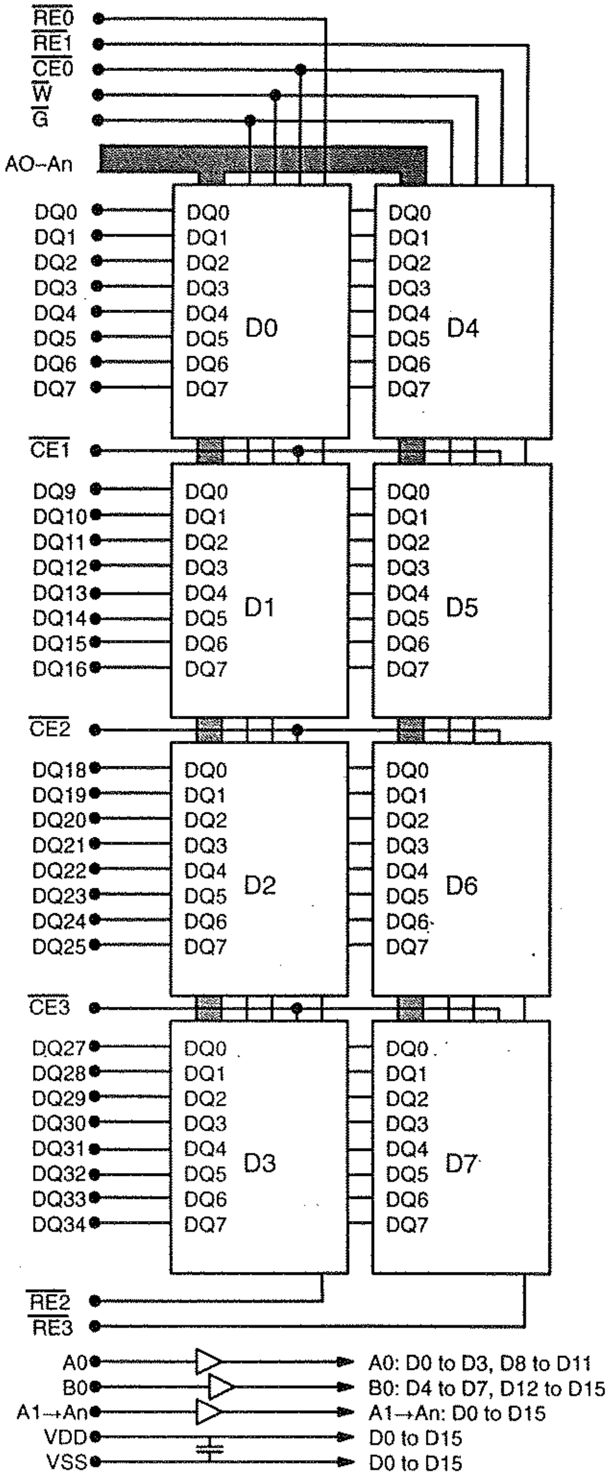

FIGURE 4.4.2–2 H
X32 DRAM SIMM, 2 Banks with X8 DRAMs

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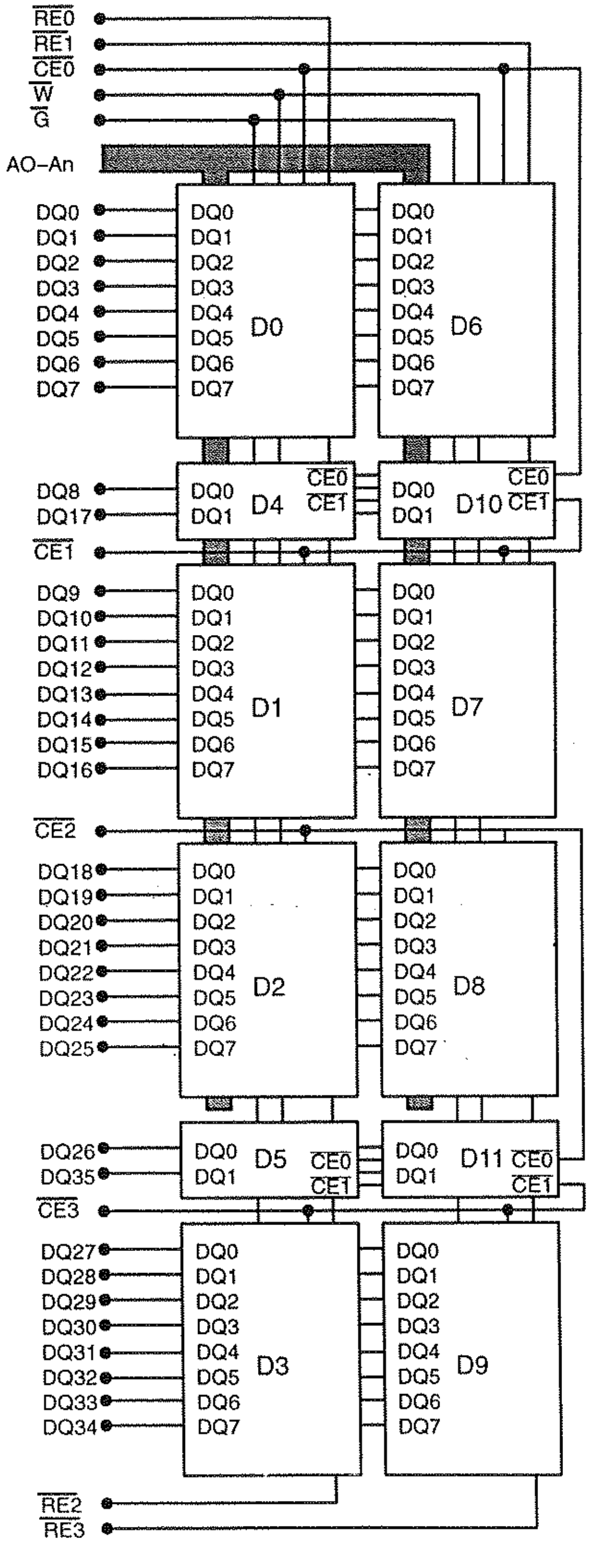

FIGURE 4.4.2–2 I

X36 DRAM SIMM, 2 Banks with X8 & X2 W/2 $\overline{\text{CE}}$ DRAMs

130

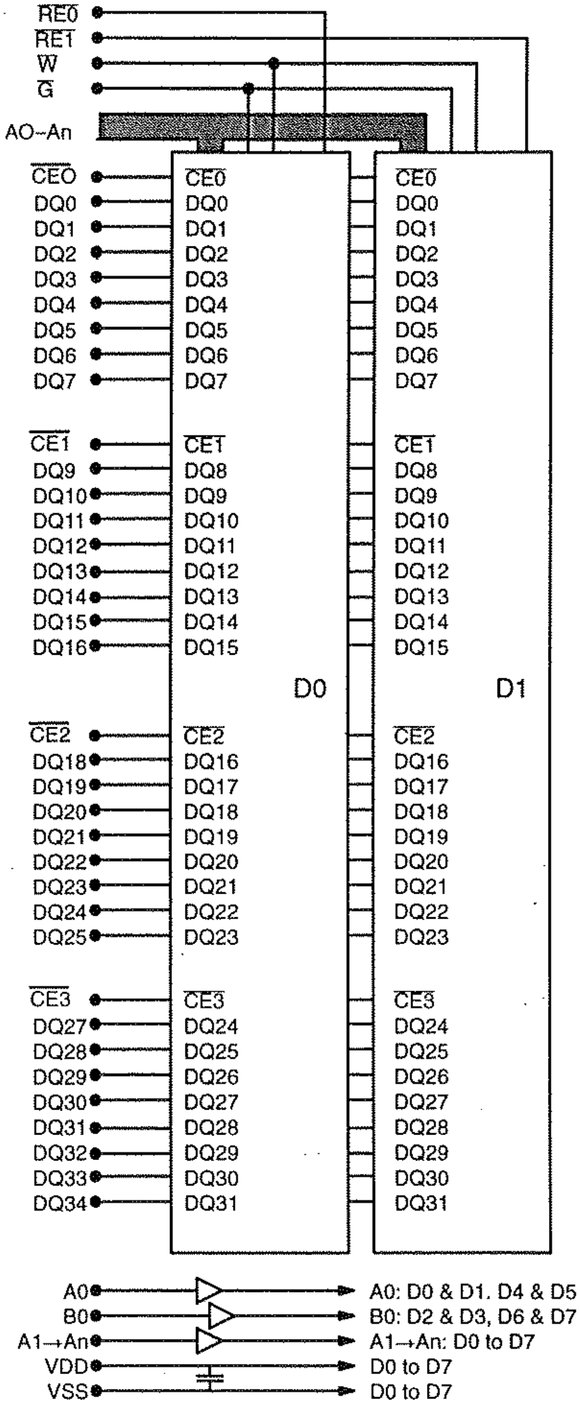

FIGURE 4.4.2–2 J
X32 DRAM SIMM, 2 bank with X32 DRAMs

131

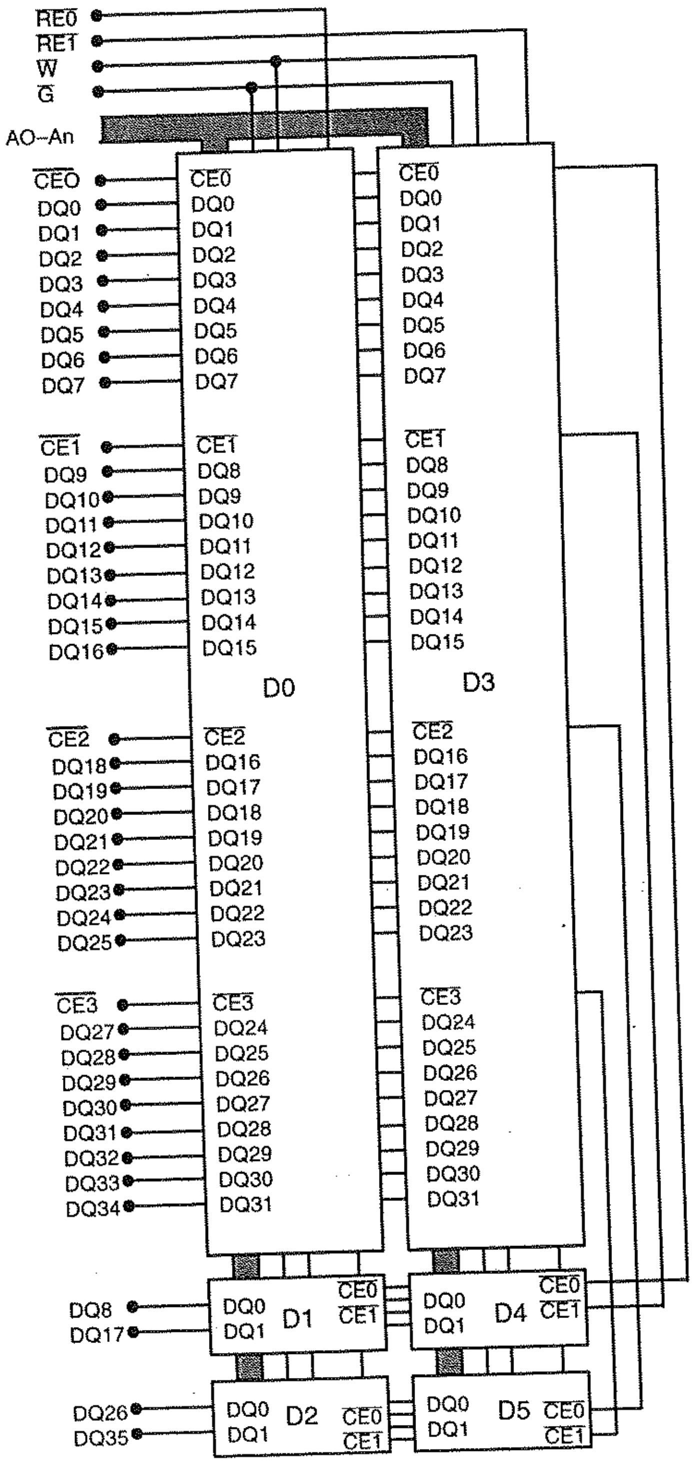

FIGURE 4.4.2–2 K
X36 DRAM SIMM, 2 bank with X32 & X2 W/2 $\overline{\text{CE}}$ DRAMs

B3

	5 V ECC	3.3 V ECC
PIN #	PIN NAME	PIN NAME
1	VSS	VSS
2	DQ0	DQ0
3	DQ1	DQ1
4	DQ2	DQ2
5	DQ3	DQ3
6	DQ4	DQ4
7	DQ5	DQ5
8	DQ6	DQ6
9	DQ7	DQ7
10	VDD	VDD
11	PD5	PD5
12	A0	A0
13	A1	A1
14	A2	A2
15	A3	A3
16	A4	A4
17	A5	A5
18	A6	A6
19	$\overline{\text{G}}$	$\overline{\text{G}}$
20	DQ8	DQ8
21	DQ9	DQ9
22	DQ10	DQ10
23	DQ11	DQ11
24	DQ12	DQ12
25	DQ13	DQ13
26	DQ14	DQ14
27	DQ15	DQ15
28	A7	A7
29	DQ16	DQ16
30	VDD	VDD
31	A8	A8
32	A9	A9
33	NC	NC, A12
34	NC	NC, A13
35	DQ17	DQ17
36	DQ18	DQ18

	5 V ECC	3.3 V ECC
PIN #	PIN NAME	PIN NAME
37	DQ19	DQ19
38	DQ20	DQ20
39	VSS	VSS
40	$\overline{\text{CE0}}$	$\overline{\text{CE0}}$
41	NC, A10	A10
42	NC, A11	A11
43	NC, $\overline{\text{CE1}}$	$\overline{\text{CE1}}$
44	$\overline{\text{RE0}}$	$\overline{\text{RE0}}$
45	NC, $\overline{\text{RE1}}$	$\overline{\text{RE1}}$
46	DQ21	DQ21
47	$\overline{\text{W}}$	$\overline{\text{W}}$
48	$\overline{\text{ECC}}$	$\overline{\text{ECC}}$
49	DQ22	DQ22
50	DQ23	DQ23
51	DQ24	DQ24
52	DQ25	DQ25
53	DQ26	DQ26
54	DQ27	DQ27
55	DQ28	DQ28
56	DQ29	DQ29
57	DQ30	DQ30
58	DQ31	DQ31
59	VDD	VDD
60	DQ32	DQ32
61	DQ33	DQ33
62	DQ34	DQ34
63	DQ35	DQ35
64	DQ36,NC	NC
65	DQ37,NC	NC
66	DQ38,NC	$\overline{\text{EDO}}$
67	PD1	PD1
68	PD2	PD2
69	PD3	PD3
70	PD4	PD4
71	DQ39,NC	PD(REF)
72	VSS	VSS

PRESENCE DETECT TRUTH TABLE

TYPE	tRAC	$\overline{\text{ECC}}$	PD1	PD2	PD3	PD4	#PD5
256K X 36 or 40 16M X 36/39	100 nS	S	S	O	S	S	O
	80 nS	S	S	O	O	S	O
	70 nS	S	S	O	S	O	O
	60 nS	S	S	O	O	O	O
512K X 36 or 40 32M X 36/39	100 nS	S	O	S	S	S	O
	80 nS	S	O	S	O	S	O
	70 nS	S	O	S	S	O	O
	60 nS	S	O	S	O	O	O
1M X 36 or 40 64M X 36/39	100 nS	S	S	S	S	S	O
	80 nS	S	S	S	O	S	O
	70 nS	S	S	S	S	O	O
	60 nS	S	S	S	O	O	O
2M X 36 or 40 128M X 36/39	100 nS	S	O	O	S	S	O
	80 nS	S	O	O	O	S	O
	70 nS	S	O	O	S	O	O
	60 nS	S	O	O	O	O	O
4M X 36 or 40 256M X 36/39	80 nS	S	S	O	O	S	S
	70 nS	S	S	O	S	O	S
	60 nS	S	S	O	O	O	S
	50 nS	S	S	O	S	S	S
8M X 36 or 40 512M X 36/39	80 nS	S	O	S	O	S	S
	70 nS	S	O	S	S	O	S
	60 nS	S	O	S	O	O	S
	50 nS	S	O	S	S	S	S

O = NC CONNECTION) S = CONNECTED TO VSS

$\overline{\text{EDO}}$ Pin: VSS FOR EDO, NC for Fast Page.

$\overline{\text{ECC}}$ Pin: VSS for ECC Module, OPEN for NON ECC Module

The connection of PD5 to VSS must be made through a 2..6 KΩ resistor

CONFIGURATION PIN ASSIGNMENT TABLE

	MODULE SIZE, 36 or 39/40 BITS											
PIN #	256K	512K	1M	2M	4M	8M	16M	32M	64M	128M	256M	512M
19	NC	NC	NC	NC	A10	A10	A10	A10	A10	A10	A10	A10
*29	NC	NC	NC	NC	A11	A11	A11	A11	A11	A11	A11	A11
32	NC	NC	A9	A9	A9	A9	A9	A9	A9	A9	A9	A9
*33	NC	$\overline{\text{RE3}}$	NC	$\overline{\text{RE3}}$	NC	$\overline{\text{RE3}}$	A12	A12	A12	A12	A12	A12
*34	NC	$\overline{\text{RE2}}$	NC	$\overline{\text{RE2}}$	NC	$\overline{\text{RE2}}$	NC	NC	A13	A13	A13	A13
45	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	$\overline{\text{RE1}}$	NC	RE1

*A11, A12, or A13 on Pins 29, 33, or 34 are used on modules containing devices that require asymetric ROW/ COLUMN addresses.

NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.

FIGURE 4.4.2-3 A
256K TO 8M BY 36 or 40, 72 PIN ECC DRAM MODULE PINOUT

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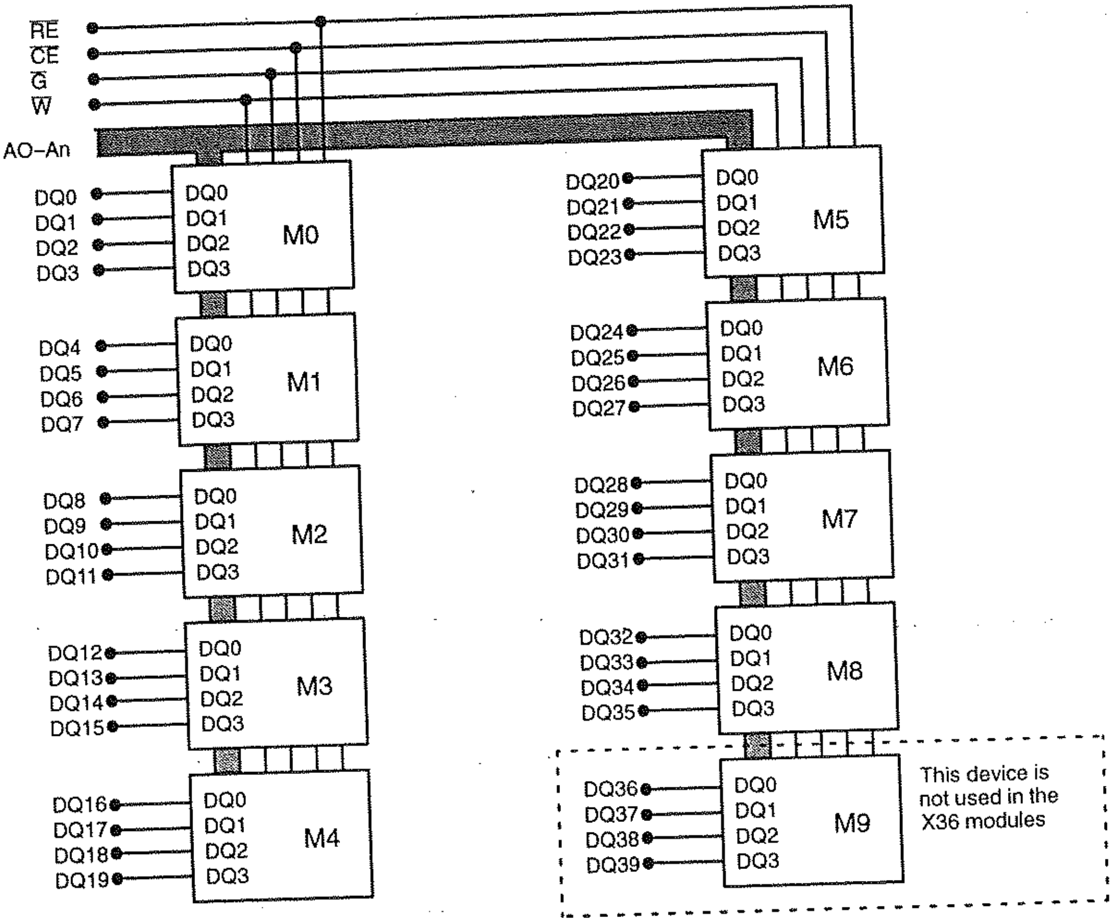
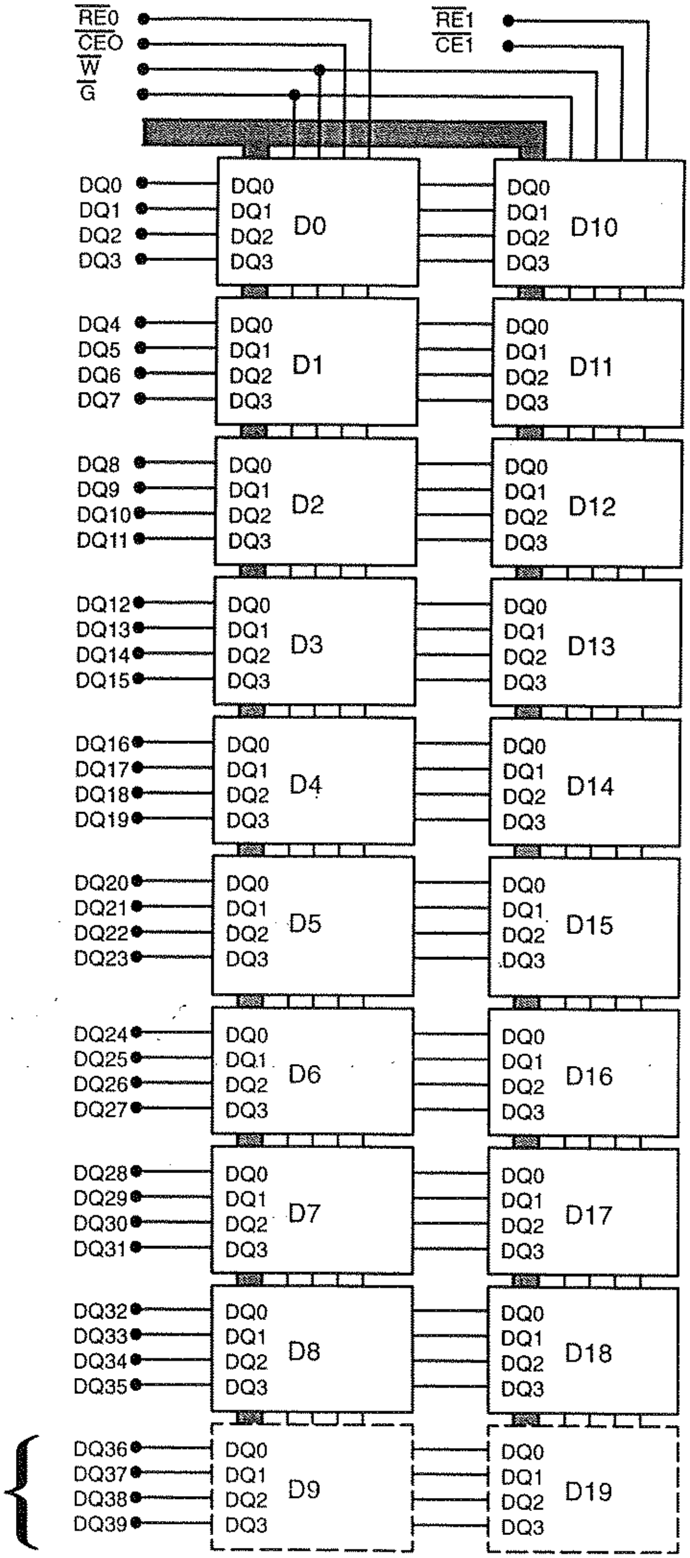


BLOCK DIAGRAM for 256K/1M/4M X 36 or 40 USING X4 DRAM

FIGURE 4.4.2-3 B

36/40 BIT 72 PIN ECC DRAM SIMM, 1 Bank with X4 DRAMs

18-1



These devices are not applicable to 3.3V SIMMs

FIGURE 4.4.2–3 C
36/40 BIT 72 PIN ECC DRAM SIMM, 2 Banks with X4 DRAMs

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4.4.3 – 88 PIN DRAM CARD FAMILIES

NOTE: There are two versions of this Card, shown in Figure 4.4.3–1 describing X 32 & 36/39 configurations, & 4.4.3–2 describing a X 40 configuration. They are similar but not fully compatible. Caution should be exercised in using these standards.

CAPACITY—256K TO 128M WORDS OF 32, 36, 39 OR 40 BITS
CONFIGURATION—16 Different Configurations Using 1mb, 4mb, 16mb, 64mb, & 256mb Devices And With 2, Or 4 $\overline{\text{Re}}$ Clocks.
LOGIC FEATURES—The cards may be used with DATA BUS widths of X16/18 or X32/36 or X39— The cards contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PIN ASSIGNMENTS, 32, 36, & 39 bit—Fig. 4.4.3–1 A
PRESENCE DETECT TABLE 32, 36, & 39 bit—Fig. 4.4.3–1 B
CONFIGURATION BLOCK DIAGRAMS 32, 36, & 39 bit—Figs. 4.4.3–1 C, 4.4.3–1 D, 4.4.3–1 E, & 4.4.3–1 F
PIN ASSIGNMENTS, 40 bit—Fig. 4.4.3–2 A
PRESENCE DETECT TABLE 40 bit—Fig. 4.4.3–2 B
CONFIGURATION BLOCK DIAGRAMS 40 bit—Figs. 4.4.3–2 C, 4.4.3–2 D, 4.4.3–2 E, & 4.4.3–2 F
PACKAGE—88 PIN JEDEC MEMORY CARD

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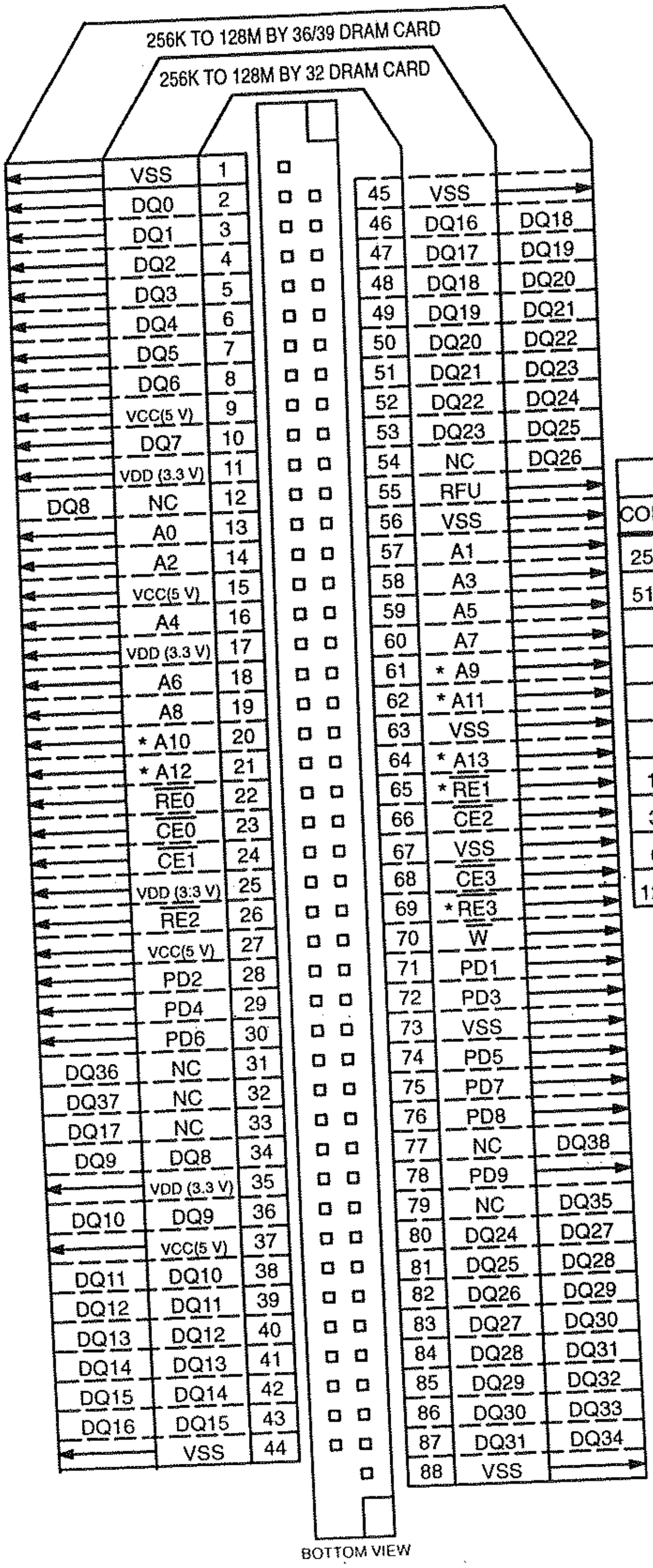

	PD7	PD6
SPEED (tRAC)	75	30
100 nS	VSS	VSS
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PIN NUMBER						
CONFIGURATION	20	21	61	62	64	65	69
256K X 36, 2 $\overline{\text{RE}}$	NC	NC	NC	NC	NC	NC	NC
512K X 36, 4 $\overline{\text{RE}}$	NC	NC	NC	NC	NC	RE1	RE3
1M X 36, 2 $\overline{\text{RE}}$	NC	NC	A9	NC	NC	NC	NC
2M X 36, 4 $\overline{\text{RE}}$	NC	NC	A9	NC	NC	RE1	RE3
4M X 36, 2 $\overline{\text{RE}}$	A10	NC	A9	A11	NC	NC	NC
8M X 36, 4 $\overline{\text{RE}}$	A10	NC	A9	A11	NC	RE1	RE3
16M X 36, 2 $\overline{\text{RE}}$	A10	A12	A9	A11	NC	NC	NC
32M X 36, 4 $\overline{\text{RE}}$	A10	A12	A9	A11	NC	RE1	RE3
64M X 36, 2 $\overline{\text{RE}}$	A10	A12	A9	A11	A13	NC	NC
128M X 36, 4 $\overline{\text{RE}}$	A10	A12	A9	A11	A13	RE1	RE3

ADDRESS AND CLOCK PIN ASSIGNMENTS

Data Access Mode	PD9
FAST PAGE	NC
EDO	VSS

* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

FIGURE 4.4.3–1 A

88 PIN, BY 32 and 36/39 DRAM CARD PINOUT

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	CARD ADDR. REQ'D	RE ADDR.	CE ADDR.	AVAIL. PAGE DEPTH	AVERAGE REFRESH INTERVAL	NOTES
1 1 1 1 1	NO CARD							NO CARD INSTALLED
1 0 0 0 0	1 MB	256K X 1, 4, 16, 18	18	9	9	512	125 ms	
0 0 0 0 0	2 MB	256K X 1, 4, 16, 18	18	9	9	512	125 ms	
1 0 0 0 1	2 MB	512K X 8, 9	19	10	9	512	125 ms	
0 0 0 0 1	4 MB	512K X 8, 9	19	10	9	512	125 ms	
1 0 0 1 0	4 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 ms	
0 0 0 1 0	8 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 ms	
1 1 0 1 0	4 MB	1M X 16, 18	20	12	8	256	62 ms	
0 1 0 1 0	8 MB	1M X 16, 18	20	12	8	256	62 ms	
1 0 0 1 1	8 MB	2M X 8, 9	21	11	10	1024	125 ms	
0 0 0 1 1	16 MB	2M X 8, 9	21	11	10	1024	125 ms	
1 0 1 0 0	16 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 ms	SUPPORT 12/10 AND 11/11 ADDRESS
0 0 1 0 0	32 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 ms	SUPPORT 12/10 AND 11/11 ADDRESS
1 0 1 0 1	32 MB	8M X 8, 9	23	13	*11	**1024	62 ms	SUPPORT 13/10 AND 12/11 ADDRESS
0 0 1 0 1	64 MB	8M X 8, 9	23	13	*11	**1024	62 ms	SUPPORT 13/10 AND 12/11 ADDRESS
1 0 1 1 0	64 MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 ms	SUPPORT 13/11 AND 14/10 ADDRESS
0 0 1 1 0	128MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 ms	SUPPORT 13/11 AND 14/10 ADDRESS

* INDICATES REDUNDANT ADDRESS THAT MUST BE PROVIDED AT CE\ TIME (TO ALLOW USE OF MIXED DRAM ADDRESSING)
** PAGE DEPTH DETERMINED BY THE SMALLEST CE\ ADDRESS DRAM
*** ALL DENSITIES ASSUME 4 BYTE CARD DATA WIDTH (32 OR 36 BITS)
FOR THE PDn PINS, 1 = NC, 0 = VSS

MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

BASE DEVICE	CONFIG'N	PIN NUMBER							
		9	11	15	17	25	27	35	37
1M	256K X 36, 2 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
1M	512K X 36, 4 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
4M	1M X 36, 2 $\overline{RE}$	5 V,NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
4M	2M X 36, 4 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	4M X 36, 2 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	8M X 36, 4 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
64M	16M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
64M	32M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	64M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	128M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC

VDD POWER PIN ASSIGNMENT TABLE

FIGURE 4.4.3-1 B
88 PIN, BY 32 AND 36/39 DRAM CARD CONFIGURATION TABLES

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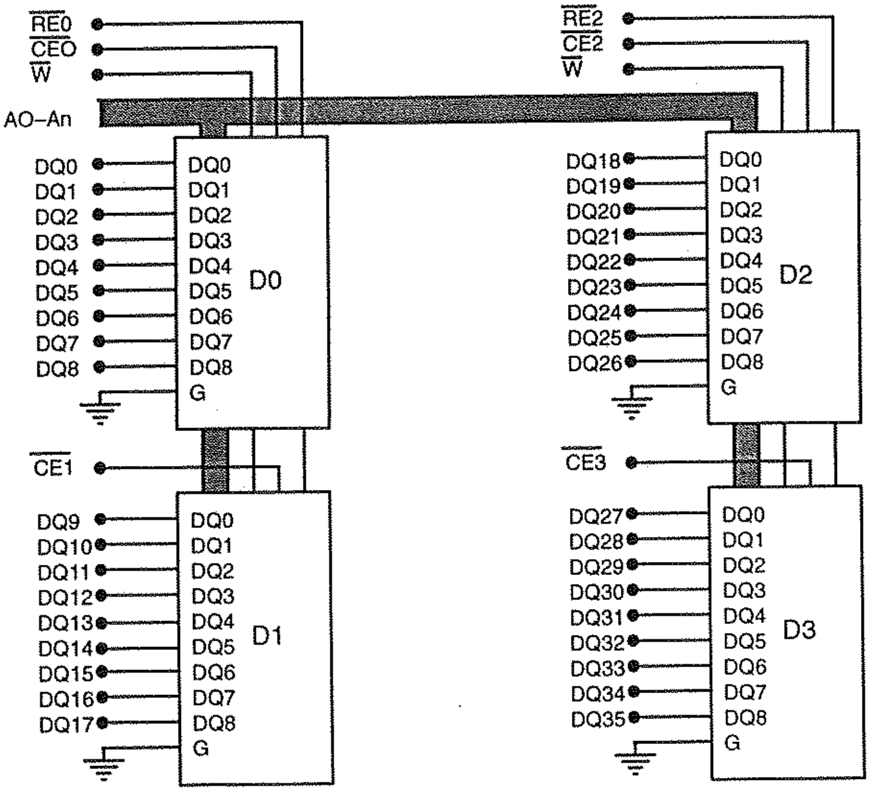
BLOCK DIAGRAM for 512K /2M/8M/32M X 36 or 1M/4M/16M/64M X 18 USING X8 or X9 DRAM



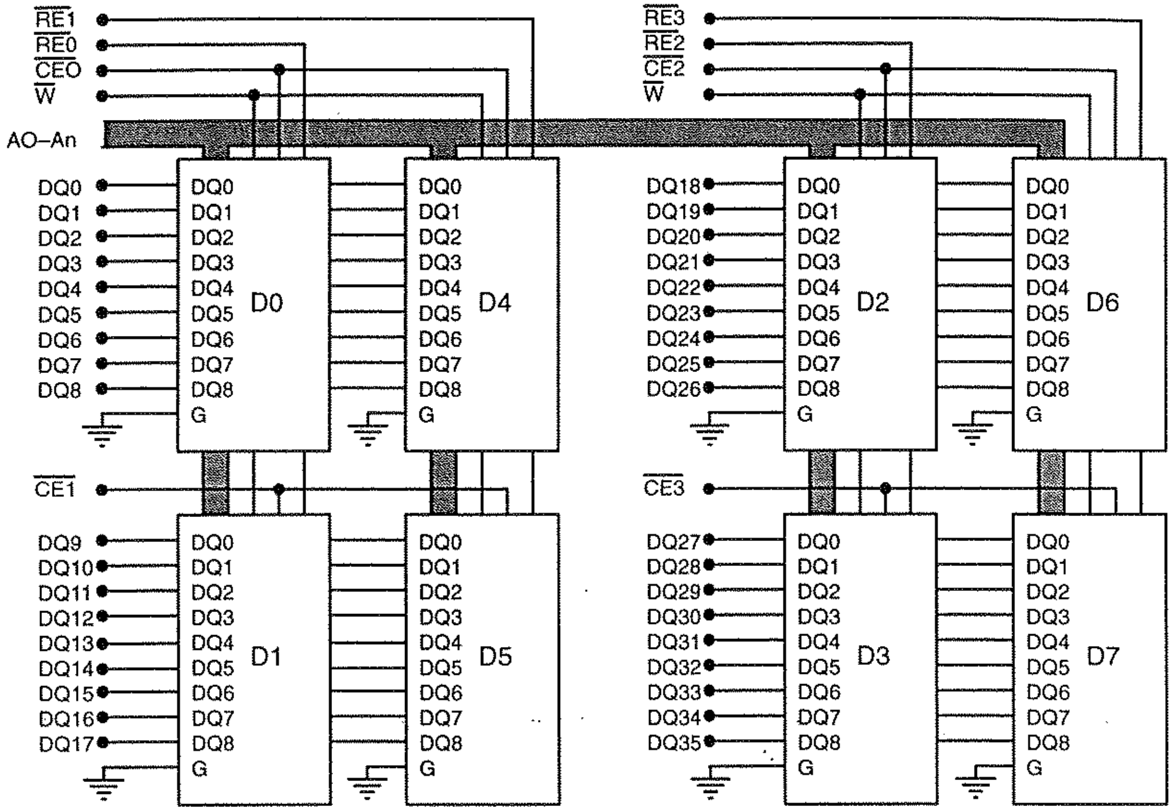
WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D3	ADDRESS
512K X 36 or 1M X 18	4M (X9)	A0 – A9
2M X 36 or 4M X 18	16M (X9)	A0 – A10
8M X 36 or 16M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, RE0 and RE2 will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, RE0 and RE2 will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3-1 C
88 PIN, BY 36, DRAM CARD 1 BANK USING BY 9 DEVICES

BLOCK DIAGRAM for 1M /4M/16M/64M X 36 or 2M/8M/32M/128M X 18 USING X8 or X9 DRAM



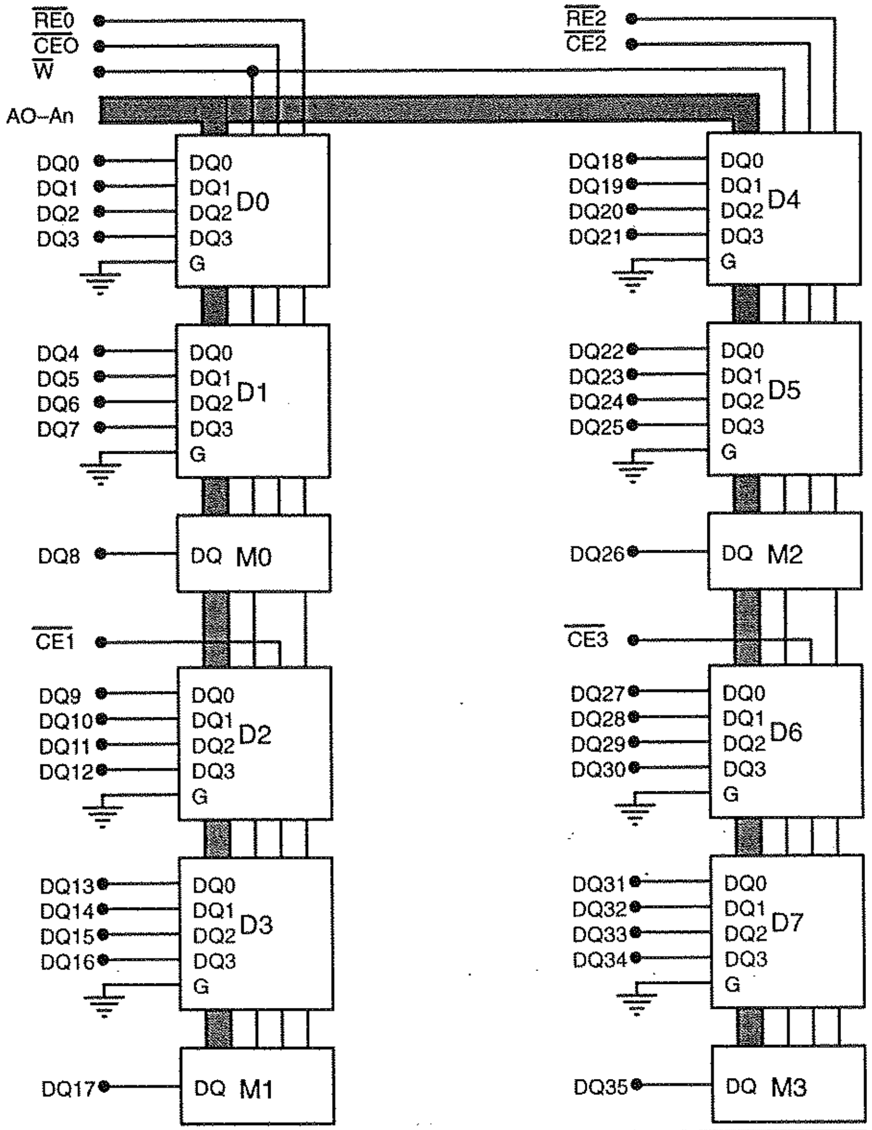
WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D7	ADDRESS
1M X 36 or 2M X 18	4M (X9)	A0 – A9
4M X 36 or 8M X 18	16M (X9)	A0 – A10
16M X 36 or 32M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, $\overline{\text{RE0}}$ and $\overline{\text{RE2}}$ (also $\overline{\text{RE1}}$ and $\overline{\text{RE3}}$) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, $\overline{\text{RE0}}$ and $\overline{\text{RE2}}$ (also $\overline{\text{RE1}}$ and $\overline{\text{RE3}}$) will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 D
88 PIN, BY 36, DRAM CARD 2 BANK USING BY 9 DEVICES

BLOCK DIAGRAM for 256K /1M/4M/16M/64M X 36 or 512K/2M/8M/32M/128M X 18 USING X4 and X1 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D7	M0 – M3	ADDRESS
256K X 36 or 512K X 18	1M (X4)	256K (X1)	A0 – A8
1M X 36 or 2M X 18	4M (X4)	1M (X1)	A0 – A9
4M X 36 or 8M X 18	16M (X4)	4M (X1)	A0 – A11
16M X 36 or 32M X 18	64M (X4)	16M (X1)	A0 – A13

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

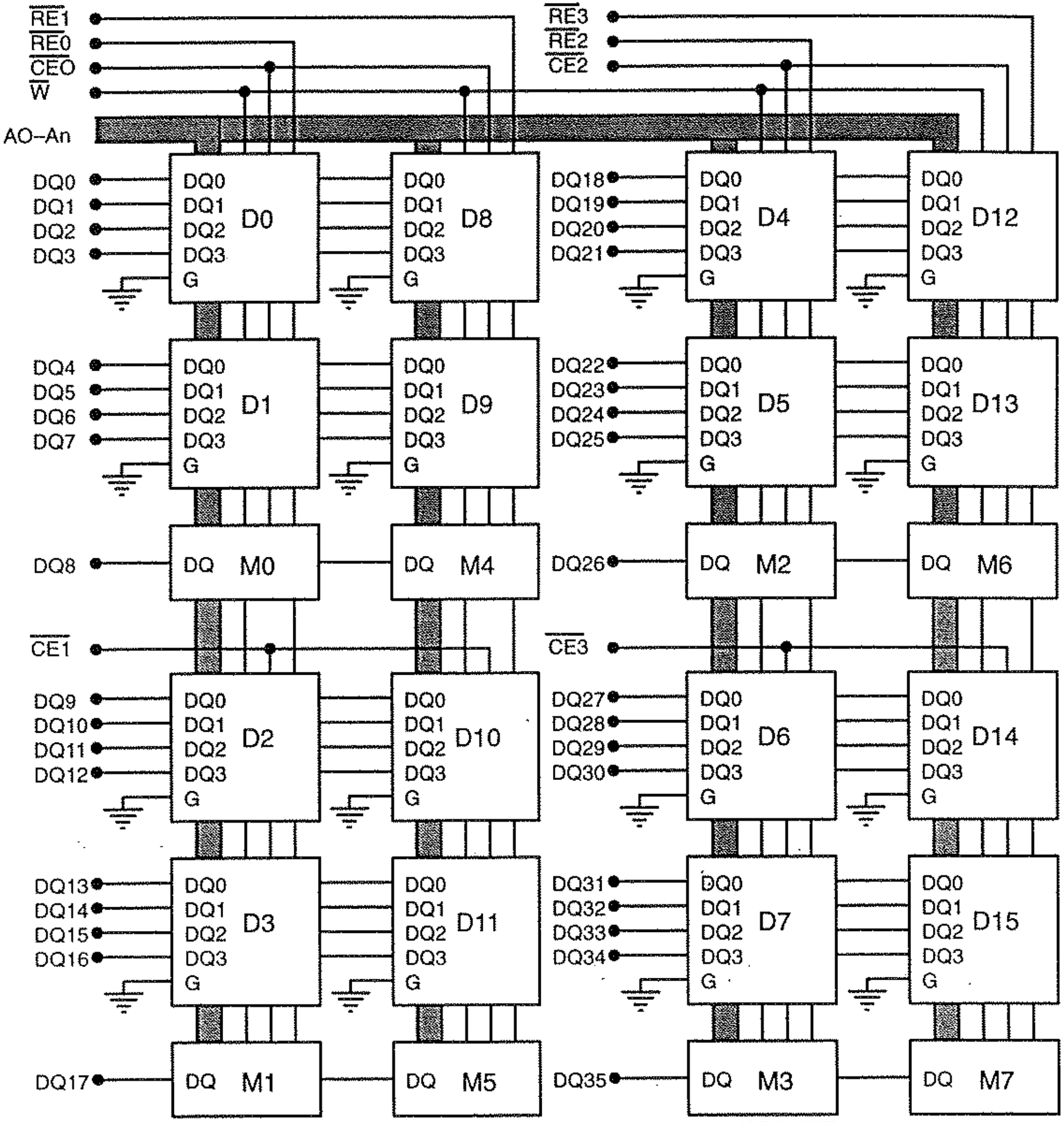
note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ will be controlled independently and the data bus will be connected to for an 18 bit bus ouside the card
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ will be actuated simultaneously

note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3-1 E

88 PIN, 36, DRAM CARD 1 BANK USING BY 4 & BY 1 DEVICES

BLOCK DIAGRAM for 512K/2M/8M/32M/32M/128M X 36 or 1M/4M/16M/256M X 18 USING X4 and X1 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D15	M0 – M7	ADDRESS
512K X 36 or 1M X 18	1M (X4)	256K(X1)	A0 – A8
2M X 36 or 4M X 18	4M (X4)	1M (X1)	A0 – A9
8M X 36 or 16M X 18	16M (X4)	4M (X1)	A0 – A11
32M X 36 or 64M X 18	64M (X4)	16M (X1)	A0 – A13

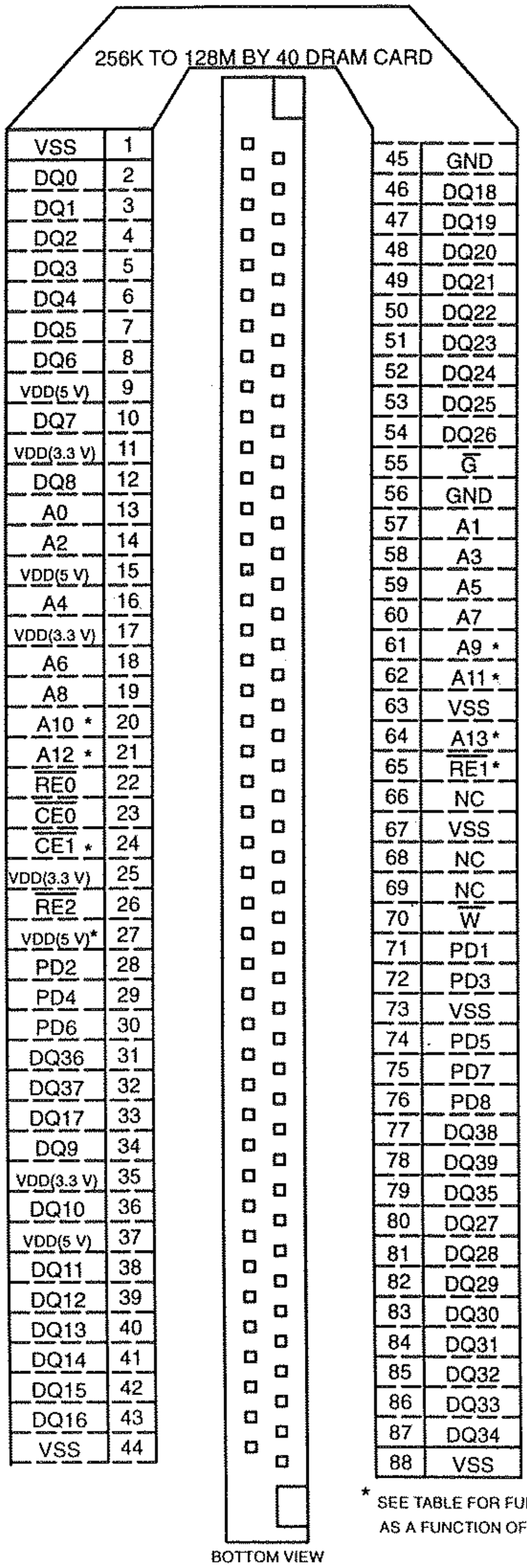
* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, RE0 and RE2 (also RE1 AND RE3) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card,
In a 36 bit system, RE0 and RE2 (also RE1 and RE3) will be actuated simultaneously

note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3-1 F

88 PIN, BY 36 DRAM CARD 2 BANK USING BY 4 & BY 1 DEVICES



Signal	Pin	Pin	Signal
VSS	1	45	GND
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
VDD(5 V)	9	53	DQ25
DQ7	10	54	DQ26
VDD(3.3 V)	11	55	$\overline{G}$
DQ8	12	56	GND
A0	13	57	A1
A2	14	58	A3
VDD(5 V)	15	59	A5
A4	16	60	A7
VDD(3.3 V)	17	61	A9 *
A6	18	62	A11 *
A8	19	63	VSS
A10 *	20	64	A13 *
A12 *	21	65	$\overline{RE1}$ *
$\overline{RE0}$	22	66	NC
$\overline{CE0}$	23	67	VSS
$\overline{CE1}$ *	24	68	NC
VDD(3.3 V)	25	69	NC
$\overline{RE2}$	26	70	$\overline{W}$
VDD(5 V)*	27	71	PD1
PD2	28	72	PD3
PD4	29	73	VSS
PD6	30	74	PD5
DQ36	31	75	PD7
DQ37	32	76	PD8
DQ17	33	77	DQ38
DQ9	34	78	DQ39
VDD(3.3 V)	35	79	DQ35
DQ10	36	80	DQ27
VDD(5 V)	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
VSS	44	88	VSS

Pin Assignment, Cards based on X4 DRAM

	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
256K X 40 (1M)	NC	NC	NC	5 V, NC	NC	NC	NC	NC
512K X 40 (1M)	NC	NC	$\overline{CE1}$	5 V, NC	NC	NC	NC	$\overline{RE1}$
1M X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
2M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
4M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
8M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
16M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
32M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
64M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
128M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

Pin Assignment, Cards based on X8 DRAM

	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
512K X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
1M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
2M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
4M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
8M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
16M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
32M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
64M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

ADDRESS AND CLOCK PIN ASSIGNMENTS

* SEE TABLE FOR FUNCTIONAL ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

FIGURE 4.4.3–2 A
88 PIN, BY 40 DRAM CARD

	PD7	PD6
SPEED (tRAC)	P 75	P 30
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PD8
REFRESH MODE	P 76
80 nS	VSS
70 nS	NC

PD REFRESH MODE TABLE

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	RE ADDR.	CE ADDR.	REFRESH PERIOD (mS)	
					NORMAL	SLOW
1 1 1 1 1	NO CARD					
1 0 0 0 0	1 MB	256K X 4	9	9	8	64
0 0 0 0 0	2 MB	256K X 4	9	9	8	64
1 0 0 0 1	2 MB	512K X 8	10	9	16	128
0 0 0 0 1	4 MB	512K X 8	10	9	16	128
1 0 0 1 0	4 MB	1M X 4	10	10	16	128
0 0 0 1 0	8 MB	1M X 4	10	10	16	128
1 0 0 1 1	8 MB	2M X 8	11	10	32	256
0 0 0 1 1	16 MB	2M X 8	11	10	32	256
1 0 1 0 0	16 MB	4M X 4	11/12	11/10	64	256
0 0 1 0 0	32 MB	4M X 4	11/12	11/10	64	256
1 0 1 0 1	32 MB	8M X 8	12/13	11/10	TBD	TBD
0 0 1 0 1	64 MB	8M X 8	12/13	11/10	TBD	TBD
1 0 1 1 0	64 MB	16M X 4	13	11	TBD	TBD
0 0 1 1 0	128 MB	16M X 4	13	11	TBD	TBD
1 0 1 0 1	128 MB	32M X 8	TBD	TBD	TBD	TBD
0 0 1 0 1	256 MB	32M X 8	TBD	TBD	TBD	TBD
1 0 1 1 0	256 MB	64M X 4	TBD	TBD	TBD	TBD
0 0 1 1 0	512 MB	64M X 4	TBD	TBD	TBD	TBD

FOR THE PDn PINS, 1 = NC, 0 = VSS
NOTE: In the above address table, optional address configurations are given for some devices to allow for different approved refresh counts.

MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

NOTE: The DRAM densities are shown in parentheses (xxxM)

FIGURE 4.4.3–2 B
88 PIN, BY 40 DRAM CARD PD TRUTH TABLE

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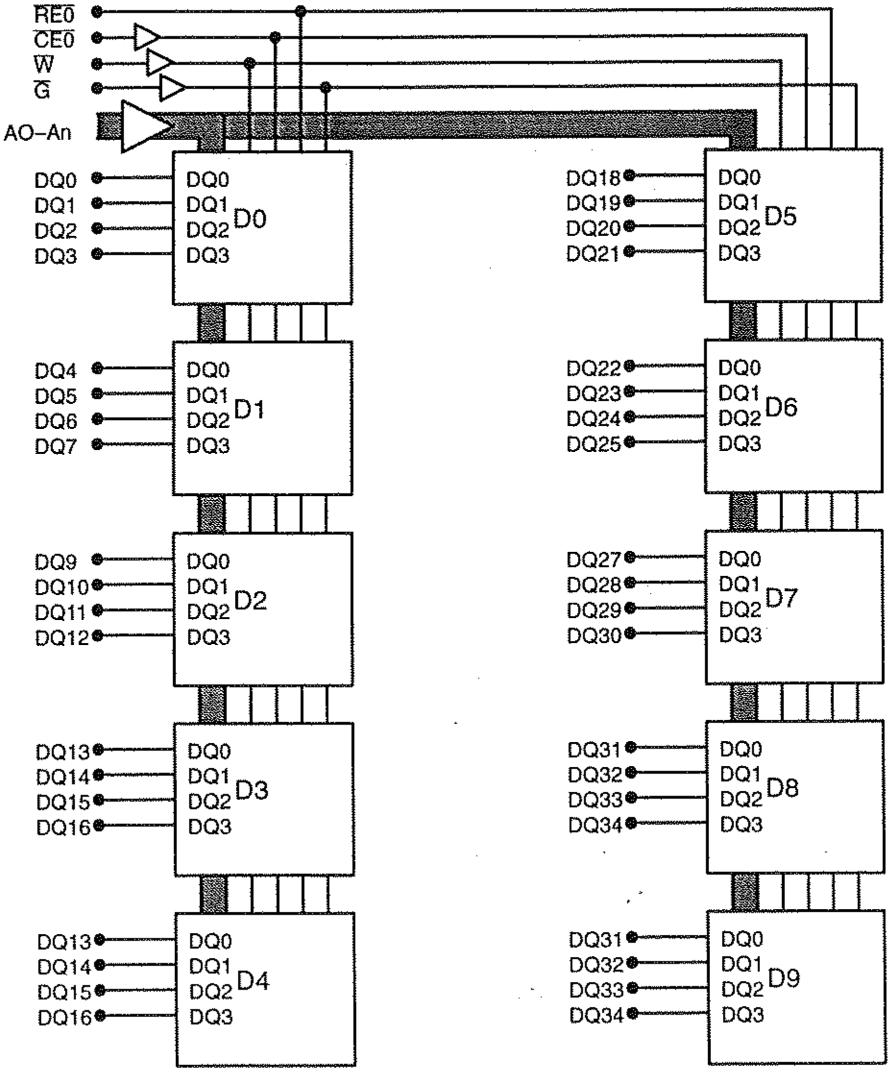
BLOCK DIAGRAM for 256K/1M/4M/16M/64M X 40 USING X4 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD	OPTIONAL ADDRESS
256K X 40	1M (X4)	A0 – A8	NA
1M X 40	4M (X8)	A0 – A9	NA
4M X 40	16M (X8)	A0 – A10	A0–A11
16M X 40	64M (X8)	A0 – A11	A0–A12
64M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card.

FIGURE 4.4.3-2 C
88 PIN, BY 40 DRAM CARD 1 BANK USING BY 4 DEVICES

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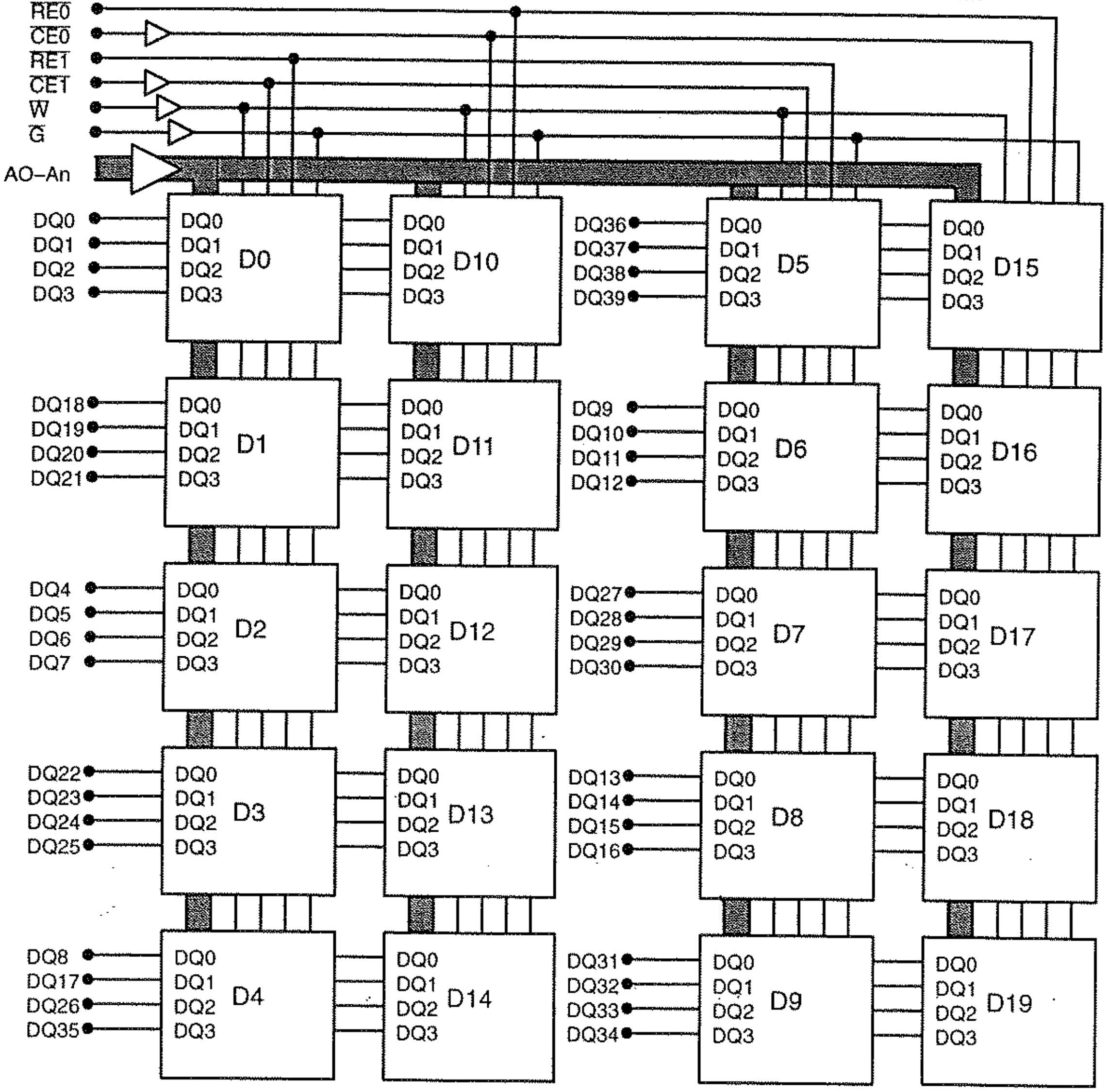
BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



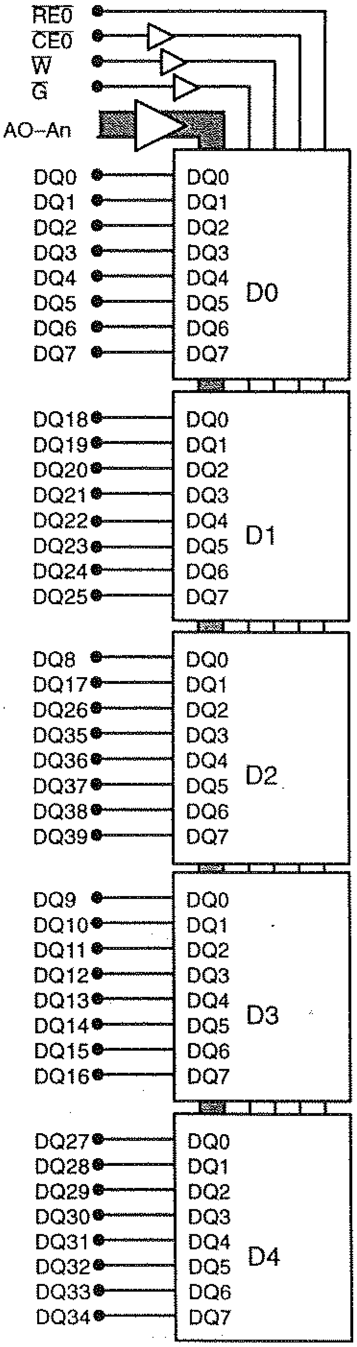
WORD ORGANIZATION	*Base Memory Device D0 to D19	ADDRESS FIELD	OPTIONAL ADDRESS
512K X 40	1M (X4)	A0 – A8	NA
2M X 40	4M (X8)	A0 – A9	NA
8M X 40	16M (X8)	A0 – A10	A0–A11
32M X 40	64M (X8)	A0 – A11	A0–A12
128M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 D
88 PIN, BY 40 DRAM CARD 2 BANK USING BY 4 DEVICES

BLOCK DIAGRAM for 512K/2M/8M/32M X 40 USING X8 DRAM



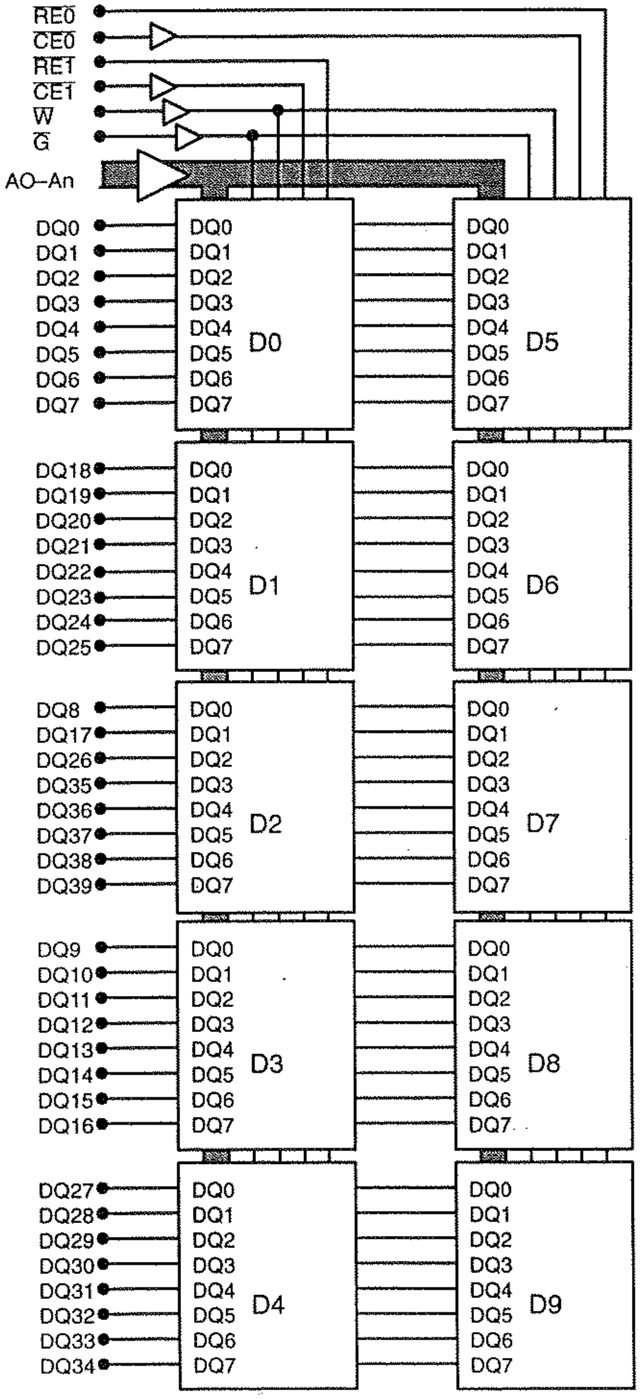
WORD ORGANIZATION	*Base Memory Device D0 to D4	ADDRESS FIELD
512K X 40	4M (X8)	A0 – A9
2M X 40	16M (X8)	A0 – A10
8M X 40	8M (X8)	A0 – A11
32M X 40	32M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 E
88 PIN, BY 40 DRAM CARD 1 BANK USING BY 8 DEVICES

BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD
1M X 40	4M (X8)	A0 – A9
4M X 40	16M (X8)	A0 – A10
16M X 40	64M (X8)	A0 – A11
64M X 40	256M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 F
88 PIN, BY 40 DRAM CARD 2 BANK USING BY 8 DEVICES

4.4.4 – 72 PIN DRAM SO–DIMM FAMILY

CAPACITY—512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 32, OR 36 BITS
DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—32 BIT
—36 BIT
CONFIGURATION—3 Different Configurations are defined using various combinationa of X4, X8, X9 memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" features that consist of output pins in the PDn field that supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
VDD CHOICE—The choice of VDD value will be determined by the memory device used and defined by a mechanical interlock KEY
ENHANCEMENTS: In Release 6 Refresh was defined and new configurations were added.
PACKAGE—72 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.4.4–A
CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4.4.4–A
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.4–B through 4.4.4–D

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PIN NAME	PIN #	PIN #	PIN NAME
VSS	1	2	DQ0
DQ1	3	4	DQ2
DQ3	5	6	DQ4
DQ5	7	8	DQ6
DQ7	9	10	&VDD
PD1	11	12	A0
A1	13	14	A2
A3	15	16	A4
A5	17	18	A6
A10	19	20	@ DQ8, NC
DQ9	21	22	DQ10
DQ11	23	24	DQ12
DQ13	25	26	DQ14
DQ15	27	28	A7
A11	29	30	&VDD
A8	31	32	A9
$\overline{RE}3$	33	34	$\overline{RE}2$
DQ16	35	36	@ DQ17, NC
DQ18	37	38	DQ19
VSS	39	40	$\overline{CE}0$
$\overline{CE}2$	41	42	$\overline{CE}3$
$\overline{CE}1$	43	44	$\overline{RE}0$
$\overline{RE}1$	45	46	A12
$\overline{W}$	47	48	A13
DQ20	49	50	DQ21
DQ22	51	52	DQ23
DQ24	53	54	DQ25
@ DQ26, NC	55	56	DQ27
DQ28	57	58	DQ29
DQ31	59	60	DQ30
&VDD	61	62	DQ32
DQ33	63	64	DQ34
@ DQ35, NC	65	66	PD2
PD3	67	68	PD4
PD5	69	70	PD6
PD7	71	72	VSS

TOP VIEW

PRESENCE DETECT TRUTH TABLE

MOD CONFIG	DEVICE	ADDR		PD4	PD3	PD2	PD1	Ave Refresh Interval (µs)	
		ROW	COL	Pin 68	Pin 67	Pin 66	Pin 11	Normal	Long
NO MODULE				O	O	O	O		
512K X 32/36	512K X 8/9	10	9	O	S	S	S	15.6	125
1M X 32/36	512K X 8/9	10	9	S	S	S	S	15.6	125
1M X 32/36	1M X 2/4/16/18	10	10	O	S	S	O	15.6	125
1M X 32/36	1M X 16/18	12	8	O	O	S	O	15.6	31.2
2M X 32/36	1M X 2/4/16/18	10	10	S	S	S	O	15.6	125
2M X 32/36	1M X 16/18	12	8	S	O	S	O	15.6	31.2
2M X 32/36	2M X 8/9	11	10	O	S	O	S	15.6	62.4
4M X 32/36	2M X 8/9	11	10	S	S	O	S	15.6	62.4
4M X 32/36	4M X 2/416/18	12*	10*	O	S	O	O	15.6	31.2
	or	11*	11*						62.4
8M X 32/36	4M X 2/4/16/18	12*	10*	S	S	O	O	15.6	31.2
	or	11*	11*						62.4
8M X 32/36	8M X 8/9	12	11	O	O	S	S	15.6	31.2
16M X 32/36	8M X 8/9	12	11	S	O	S	S	15.6	31.2
16M X 32/36	16M X 2/4/16/18	13	11	O	O	O	S	15.6	TBD
32M X 32/36	16M X 2/4/16/18	13	11	S	O	O	S	15.6	TBD
32M X 32/36	32M X 8/9	TBD	TBD	O	S	S	S	TBD	TBD
64M X 32/36	32M X 8/9	TBD	TBD	S	S	S	S	TBD	TBD
64M X 32/36	64M X 2/4	TBD	TBD	O	S	S	O	TBD	TBD

* Indicates that 12/10 or 11/11 may be used on this assembly. The application must determine the appropriate addressing version or provide redundant (12/11) addressing to allow the use of either.

** The DRAM organization is provided for reference and clarification only. X2 implies X2 DRAM with 2 $\overline{CE}$s. X4 can be either X4 or X4 with 4 CEs. X1 options are allowed if approved dimensions are met.

O = OPEN CIRCUIT (NO CONNECTION)

S = CONNECTED TO VSS

	PD6	PD5
SPEED (tRAC)	Pin 70	Pin 69
80 ns	S	O
70 ns	O	S
60 ns	O	O
50 ns	S	S

PD SPEED TABLE

	PD7
REFRESH MODE	Pin 71
NORMAL	O
* SELF–REFRESH	S

REFRESH MODE

*SELF–REFRESH/LONG INTERVA

&Note: This standard allows for the use of different values of VDD depending on the memory device requirements. A mechanical key is used to define the voltage as described in the package registration document, MO–160.

@ These Pins are NC for X32, and DQn for X36 modules

FIGURE 4.4.4–A
32 OR 36 BIT DRAM SO–DIMM PINOUT

5,01

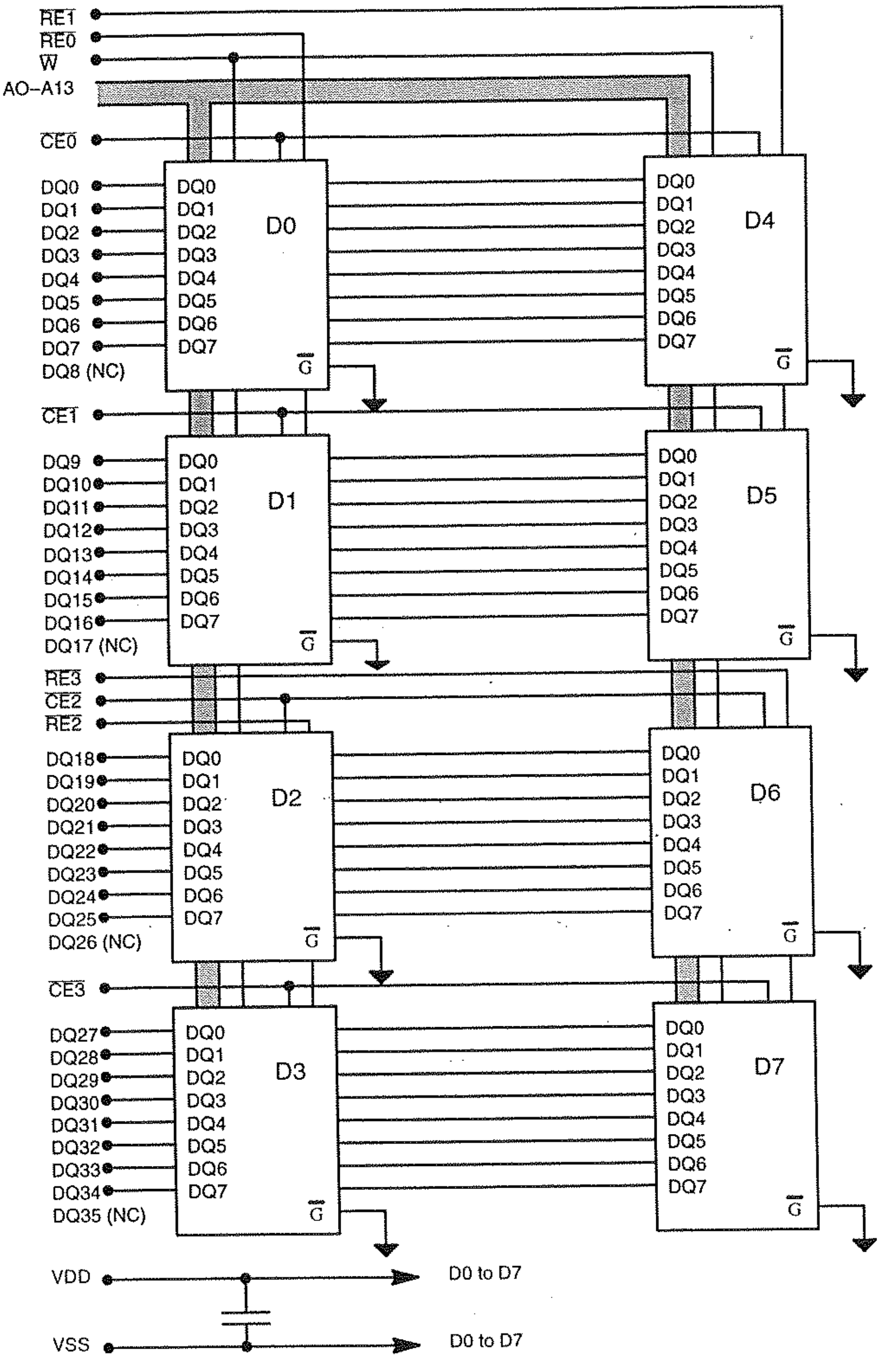


FIGURE 4.4.4-B
BLOCK DIAGRAM for X 32 DRAM SO-DIMM USING X8 DRAM

Release 5c7

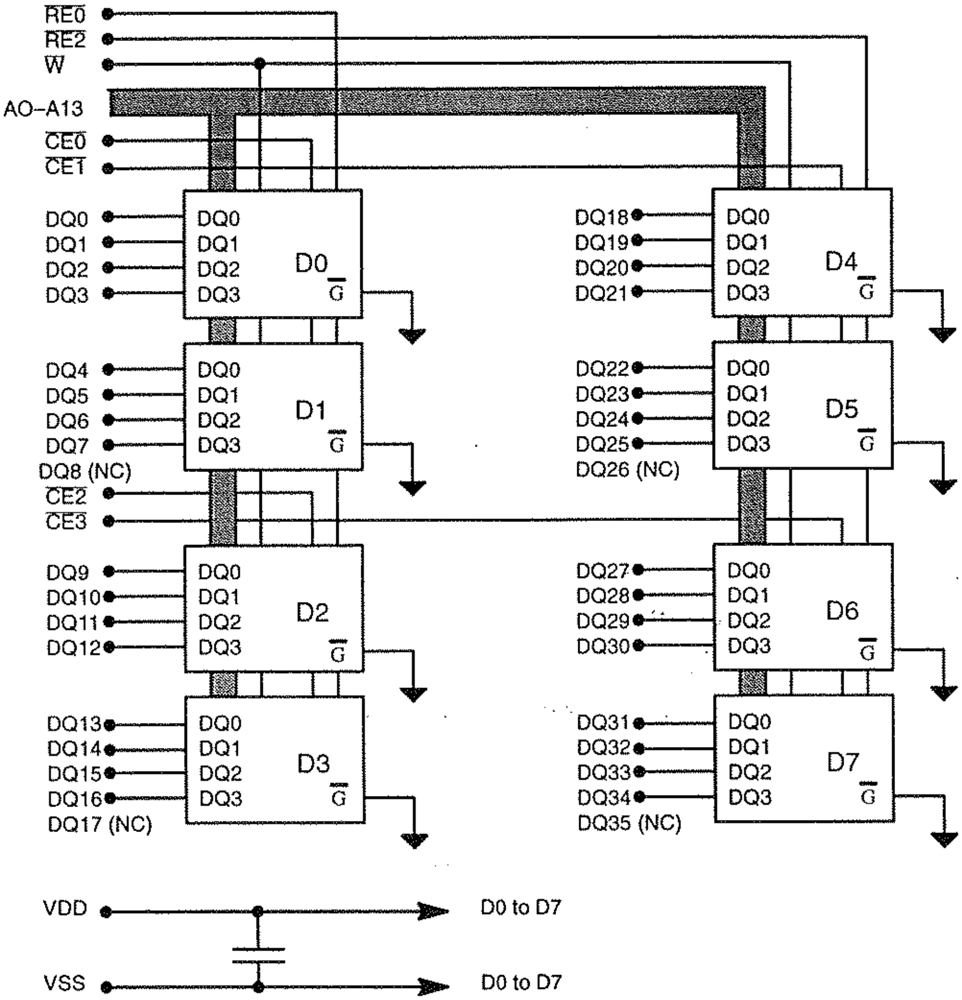


FIGURE 4.4.4–C
BLOCK DIAGRAM for X 32 DRAM SO–DIMM USING X4 DRAM

203

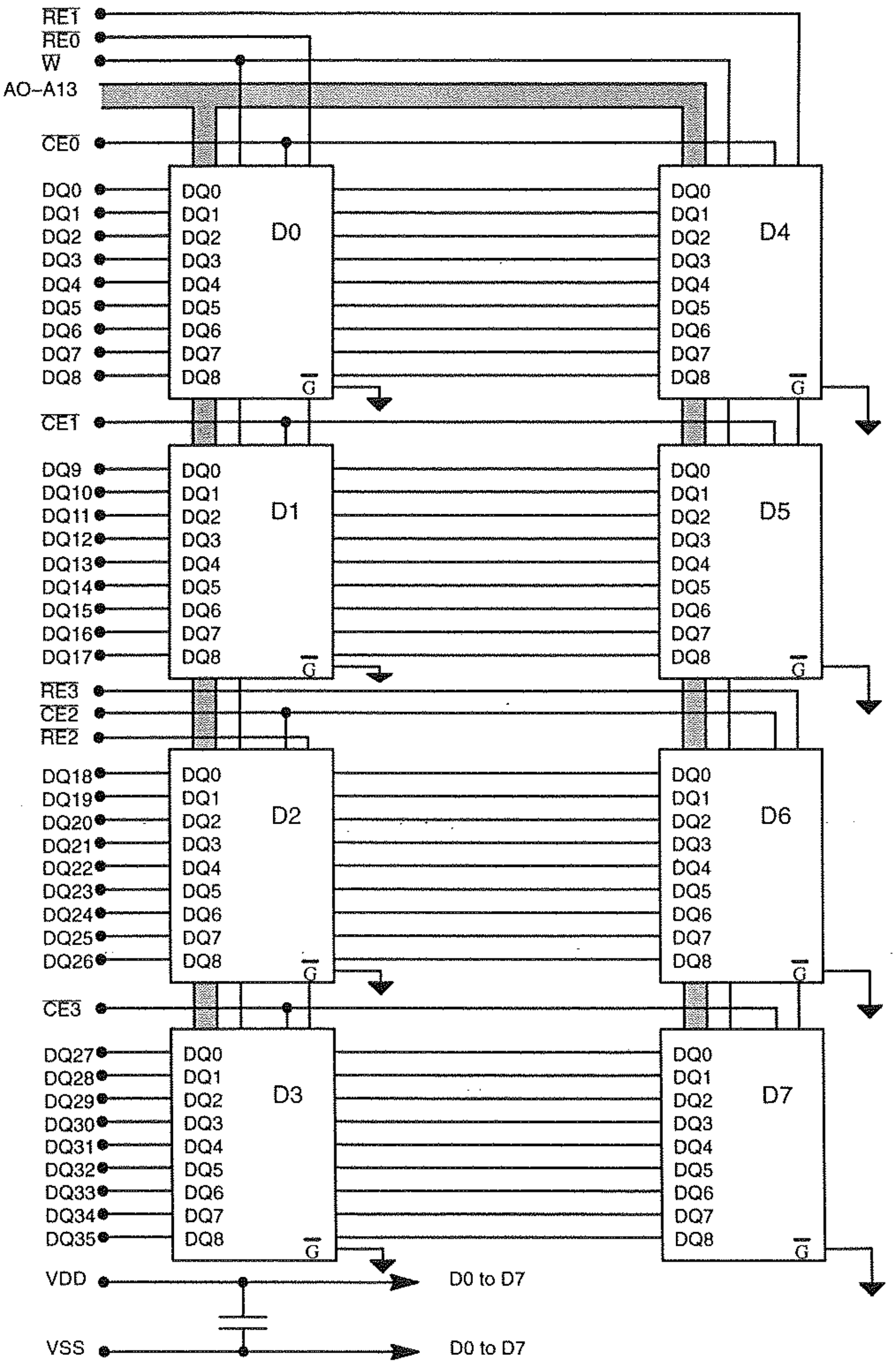
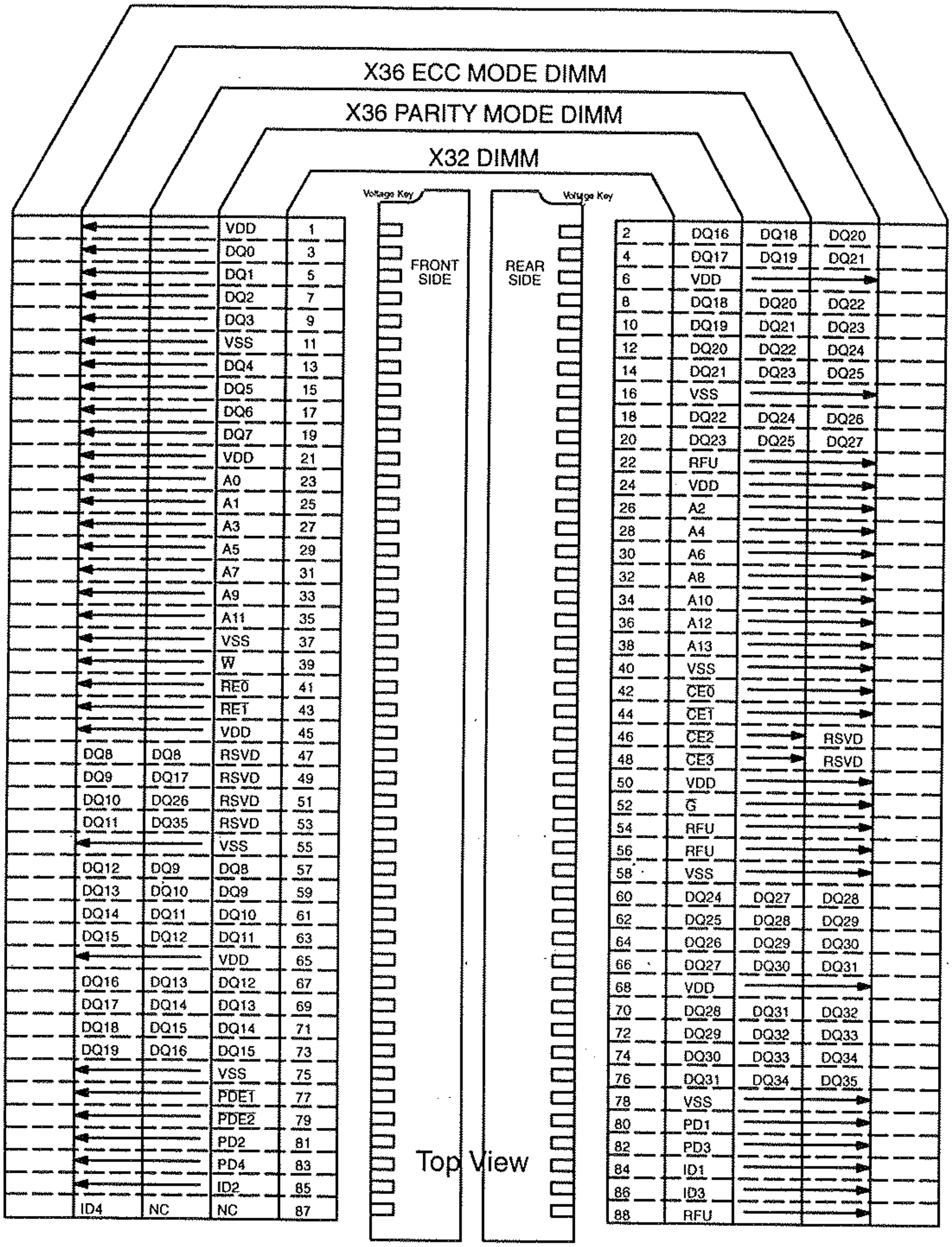


FIGURE 4.4.4-D
BLOCK DIAGRAM for X 36 DRAM SO-DIMM USING X9 DRAM

Release 5c7

4.4.5 – 88 PIN DRAM SO–DIMM FAMILY

CAPACITY—512K TO 128M WORDS OF 32, OR 36 BITS
DATA CONFIGURATIONS—Two DATA Word configurations are defined: X32 & X36
CONFIGURATION—4 Different Configurations are defined using various combinationa of X1, X4, X8, memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" features that consist of output pins in the PDn field that supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
VDD CHOICE—The choice of VDD value will be determined by the memory device used and defined by a mechanical interlock KEY
PACKAGE—88 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.4.5–A
PD, CAPACITY / DEVICE CONFIGURATION TABLES—Fig. 4.4.5–B
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.5–C through 4.4.5–F



X36 ECC MODE DIMM	X36 PARITY MODE DIMM	X32 DIMM	Pin
←	←	VDD	1
←	←	DQ0	3
←	←	DQ1	5
←	←	DQ2	7
←	←	DQ3	9
←	←	VSS	11
←	←	DQ4	13
←	←	DQ5	15
←	←	DQ6	17
←	←	DQ7	19
←	←	VDD	21
←	←	A0	23
←	←	A1	25
←	←	A3	27
←	←	A5	29
←	←	A7	31
←	←	A9	33
←	←	A11	35
←	←	VSS	37
←	←	$\overline{W}$	39
←	←	$\overline{RE0}$	41
←	←	$\overline{RE1}$	43
←	←	VDD	45
DQ8	DQ8	RSVD	47
DQ9	DQ17	RSVD	49
DQ10	DQ26	RSVD	51
DQ11	DQ35	RSVD	53
←	←	VSS	55
DQ12	DQ9	DQ8	57
DQ13	DQ10	DQ9	59
DQ14	DQ11	DQ10	61
DQ15	DQ12	DQ11	63
←	←	VDD	65
DQ16	DQ13	DQ12	67
DQ17	DQ14	DQ13	69
DQ18	DQ15	DQ14	71
DQ19	DQ16	DQ15	73
←	←	VSS	75
←	←	$\overline{PDE1}$	77
←	←	$\overline{PDE2}$	79
←	←	PD2	81
←	←	PD4	83
←	←	ID2	85
ID4	NC	NC	87

Pin	X32 DIMM	X36 PARITY MODE DIMM	X36 ECC MODE DIMM
2	DQ16	DQ18	DQ20
4	DQ17	DQ19	DQ21
6	VDD	→	→
8	DQ18	DQ20	DQ22
10	DQ19	DQ21	DQ23
12	DQ20	DQ22	DQ24
14	DQ21	DQ23	DQ25
16	VSS	→	→
18	DQ22	DQ24	DQ26
20	DQ23	DQ25	DQ27
22	RFU	→	→
24	VDD	→	→
26	A2	→	→
28	A4	→	→
30	A6	→	→
32	A8	→	→
34	A10	→	→
36	A12	→	→
38	A13	→	→
40	VSS	→	→
42	$\overline{CE0}$	→	→
44	$\overline{CE1}$	→	→
46	$\overline{CE2}$	→	RSVD
48	$\overline{CE3}$	→	RSVD
50	VDD	→	→
52	$\overline{G}$	→	→
54	RFU	→	→
56	RFU	→	→
58	VSS	→	→
60	DQ24	DQ27	DQ28
62	DQ25	DQ28	DQ29
64	DQ26	DQ29	DQ30
66	DQ27	DQ30	DQ31
68	VDD	→	→
70	DQ28	DQ31	DQ32
72	DQ29	DQ32	DQ33
74	DQ30	DQ33	DQ34
76	DQ31	DQ34	DQ35
78	VSS	→	→
80	PD1	→	→
82	PD3	→	→
84	ID1	→	→
86	ID3	→	→
88	RFU	→	→

FIGURE 4.4.5-A
X32 and X36 DRAM SO-DIMM PINOUT

PREOENCE DETECT TRUTH TABLE							
MOD CONFIG	DEVICE	ADDR		PD14	PD13	PD12	PD11
		ROW	COL				
NO MODULE				1	1	1	1
512K X 32/36	512K X 8/9	10	9	1	0	0	0
1M X 32/36	512K X 8/9	10	9	0	0	0	0
1M X 32/36	1M X 1/4/16/18	10	10	1	0	0	1
1M X 32/36	1M X 16/18	12	8	1	0	1	0
2M X 32/36	1M X 1/4/16/18	10	10	0	0	0	1
2M X 32/36	1M X 16/18	12	8	0	0	1	0
2M X 32/26	2M X 1/2/8/9	11	10	1	0	1	1
4M X 32/36	2M X 1/2/8/9	11	10	0	0	1	1
4M X 32/36	4M X 4/16/18	12	10	1	1	0	0
4M X 32/36	4M X 1/4/16/18	11	11	1	1	0	1
8M X 32/36	4M X 4/16/18	12	10	0	1	1	1
8M X 32/36	4M X 1/4/16/18	11	11	0	1	0	1
8M X 32/36	8M X 1/2/8/9	12	11	1	1	1	0
16M X 32/36	8M X 1/2/8/9	12	11	0	1	1	0
16M X 32/36	16M X 1/4/16/18	13/12*	11/12*	1	0	0	0
32M X 32/36	16M X 1/4/16/18	13/12*	11/12*	0	0	0	0
32M X 32/36	32M X 1/2/8/9	TBD	TBD	1	0	0	1
64M X 32/36	32M X 1/2/8/9	TBD	TBD	0	0	0	1
64M X 32/36	64M X 1/4	TBD	TBD	1	0	1	0
128M X 32/36	64M X 1/4	TBD	TBD	0	0	1	0

NOTE 1 – * This addressing includes a redundant address to allow mixing of 13/11 and 12/12 devices.

NOTE 2 – The PDmn & IDn values given in the tables have the following significance:
1 = Driven to LOGIC HIGH for PD, OPEN CIRCUIT FOR ID
0 = Driven to LOGIC LOW for PD, SHORT TO VSS FOR ID

NOTE 3 – #The PDmn values are multiplexed onto the PDn pins under the control of $\overline{PDE1}$ and $\overline{PDE2}$ as follows:
PD11 ⇒ PD14 to PD1 ⇒ PD4 WITH $\overline{PDE1}$ = LOW
PD21 ⇒ PD24 to PD1 ⇒ PD4 WITH $\overline{PDE2}$ = LOW

NOTE4: This standard allows for the use of different values of VDD depending on the memory device requirements. A mechanical key is used to define the voltage as described in the package registration document.

	ID3
PARITY	
X32 NO–PAR.	0
X36 PARITY	1
PARITY STRUCTURE	

	ID2
REFRESH MODE	
NORMAL	0
SELF–REFRESH	1
REFRESH MODE	

	ID1
REFRESH	
NORMAL	0
SLOW	1
REFRESH PERIOD	

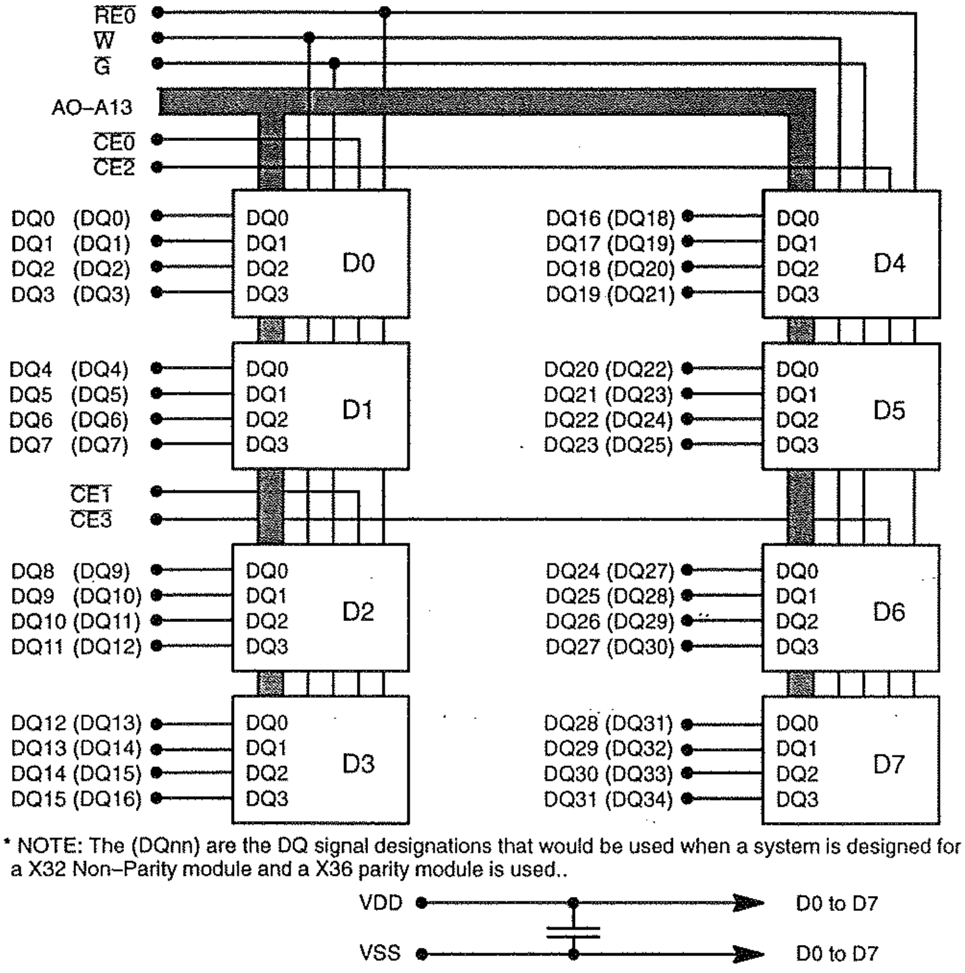
	PD24
ECC	
X32/X36 PARITY	1
X36 ECC	0
DATA STRUCTURE	

	PD23
MODE	
FAST PAGE	1
EDO/BURST EDO	0
DATA I/O MODE	

	PD22	PD21
SPEED (tRAC)	81	80
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1
PD SPEED TABLE		

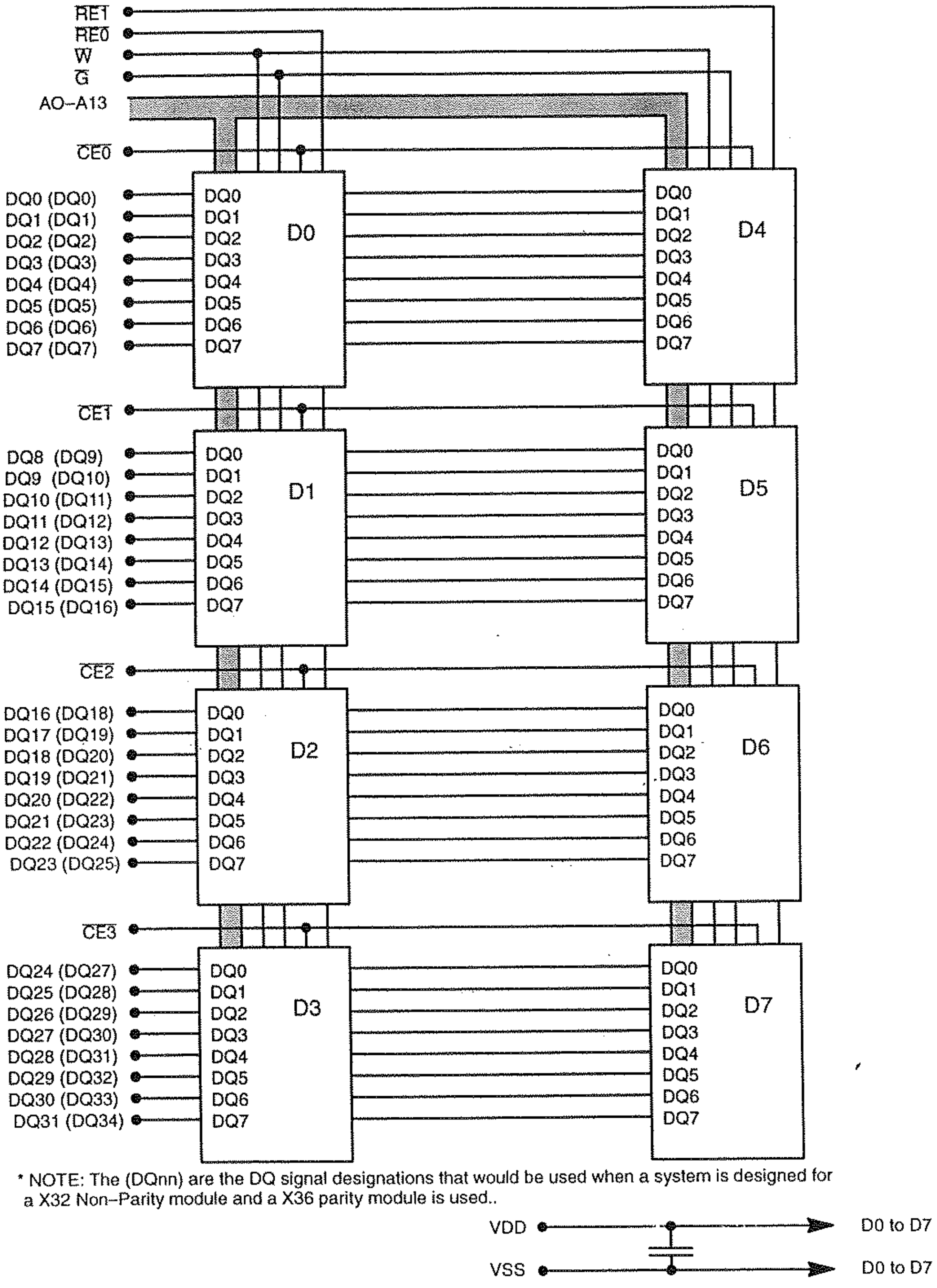
&

FIGURE 4.4.5–B
X32 and X36 DRAM SO–DIMM PD and ID TRUTH TABLES



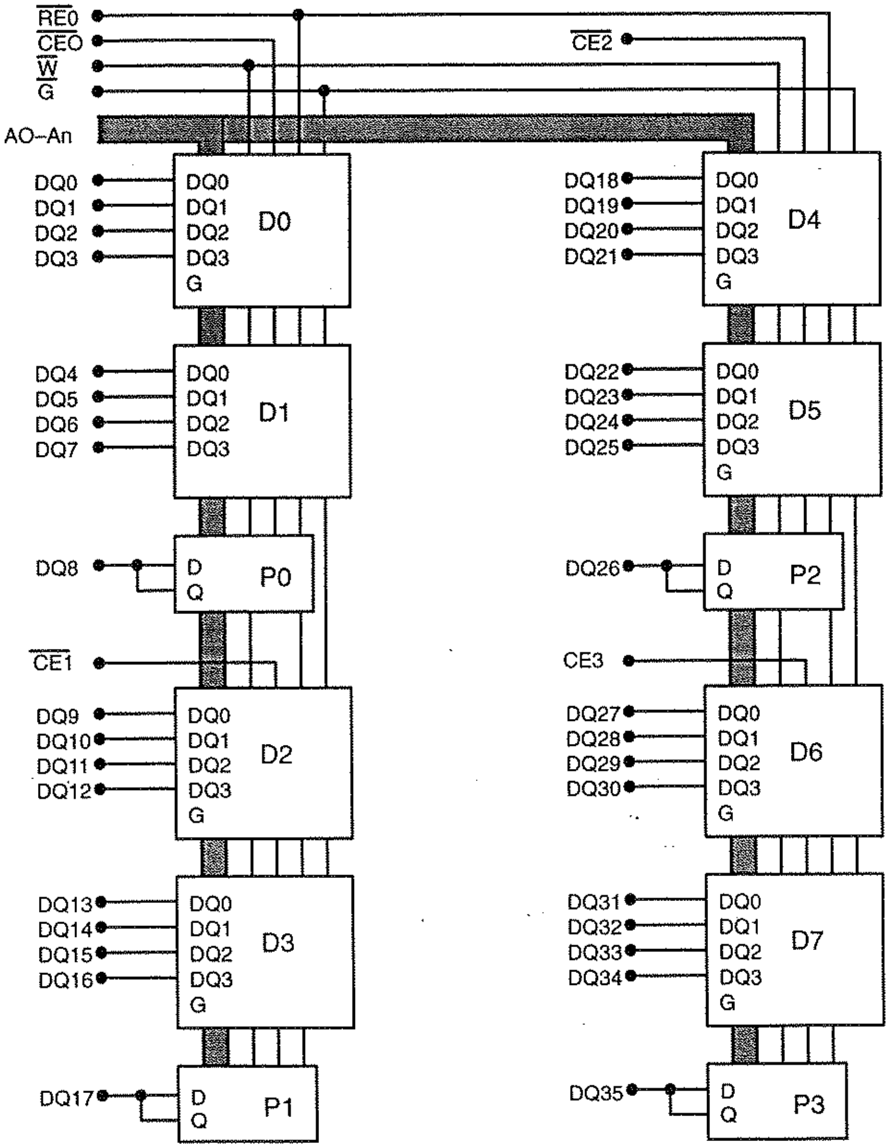
* NOTE: The (DQnn) are the DQ signal designations that would be used when a system is designed for a X32 Non–Parity module and a X36 parity module is used..

FIGURE 4.4.5–C
X 32 DRAM SO–DIMM USING X4 DEVICES



* NOTE: The (DQnn) are the DQ signal designations that would be used when a system is designed for a X32 Non–Parity module and a X36 parity module is used..

FIGURE 4.4.5–D
X 32 DRAM SO–DIMM USING X8 DEVICES



* NOTE: For the parity bit devices, P0 ⇒ P3, X1 DRAMs are showed, but Multi CE DRAM may be used.

FIGURE 4.4.5–E
X 36 DRAM PARITY SO–DIMM USING X4/X1 DEVICES

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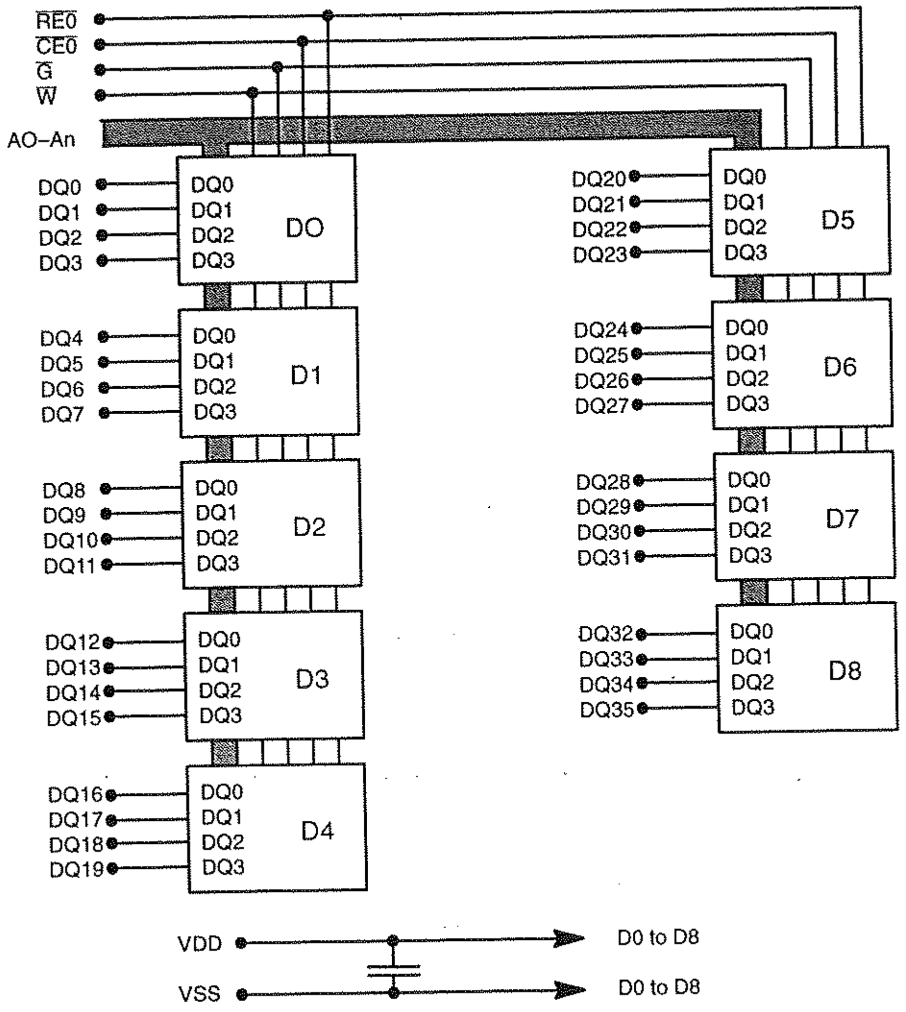
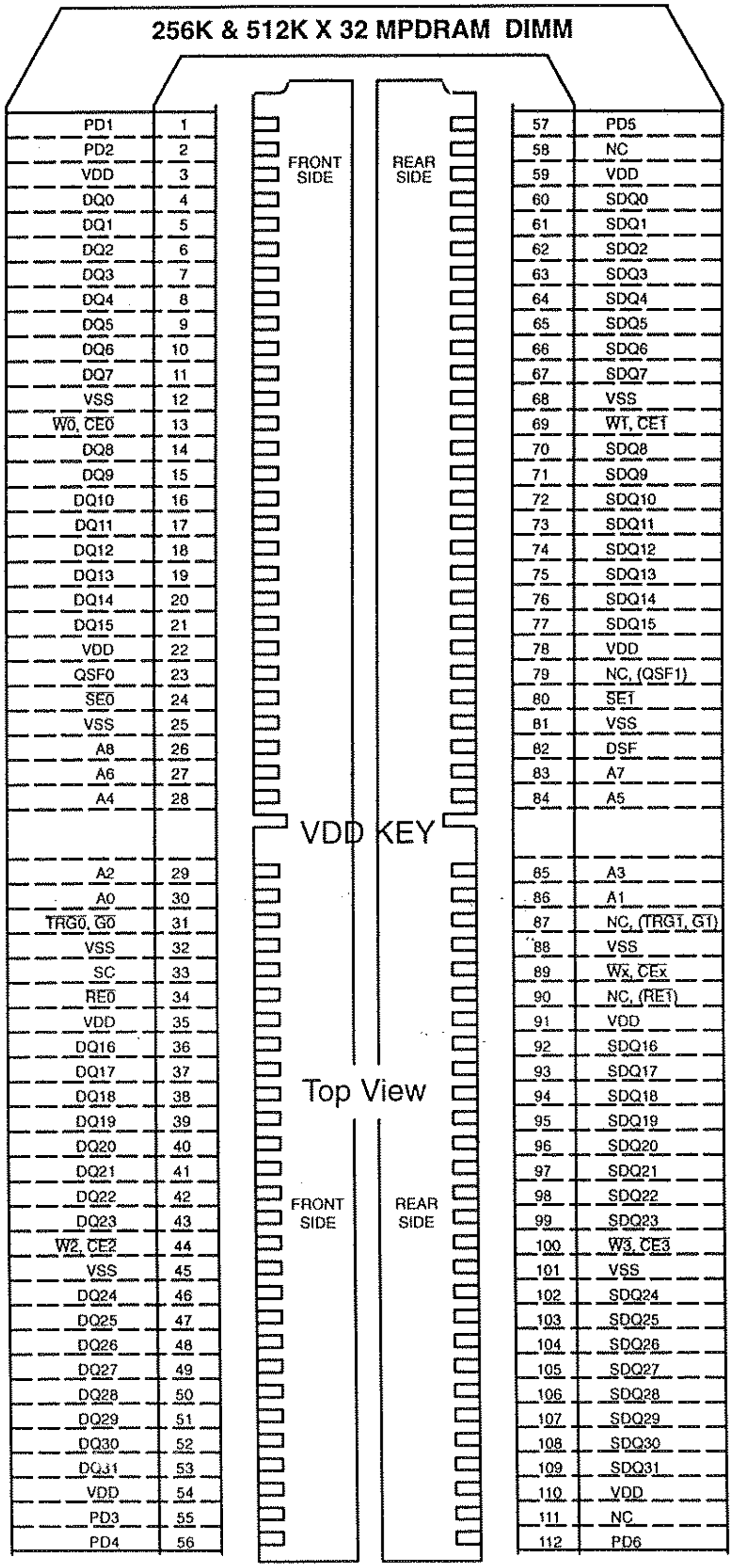


FIGURE 4.4.5–F
X 36 DRAM ECC SO–DIMM USING X4 DEVICES

.311

4.4.6 – 112 PIN MPDRAM DIMM FAMILY

CAPACITY—256K, and 512K WORDS OF 32 BITS ON THE SERIAL AND PARALLEL PORTS.
DATA CONFIGURATIONS—Two DEVICE configurations are defined: using X8 and X16 MPDRAM
CONFIGURATION—2 Different Configurations are defined using X4 & X8 memories with 2 banks.
LOGIC FEATURES—The modules contain independent clock control of the 4 separate BYTE groups of data bits and "PRESENCE DETECT" features that consists of output pins in the PDn field which supplies encoded values that define the storage capacity, SAM length, read mode, refresh mode, $\overline{CE}/\overline{W}$ logic configuration, and speed of the module.
PACKAGE—112 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.4.6–A
PRESENCE DETECT TABLES—Fig. 4.4.6–B
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.6–B & 4.4.6–C



	Pin	Pin	
PD1	1	57	PD5
PD2	2	58	NC
VDD	3	59	VDD
DQ0	4	60	SDQ0
DQ1	5	61	SDQ1
DQ2	6	62	SDQ2
DQ3	7	63	SDQ3
DQ4	8	64	SDQ4
DQ5	9	65	SDQ5
DQ6	10	66	SDQ6
DQ7	11	67	SDQ7
VSS	12	68	VSS
$\overline{\text{W0}}$, $\overline{\text{CE0}}$	13	69	$\overline{\text{W1}}$, $\overline{\text{CE1}}$
DQ8	14	70	SDQ8
DQ9	15	71	SDQ9
DQ10	16	72	SDQ10
DQ11	17	73	SDQ11
DQ12	18	74	SDQ12
DQ13	19	75	SDQ13
DQ14	20	76	SDQ14
DQ15	21	77	SDQ15
VDD	22	78	VDD
QSF0	23	79	NC, (QSF1)
$\overline{\text{SE0}}$	24	80	$\overline{\text{SE1}}$
VSS	25	81	VSS
A8	26	82	DSF
A6	27	83	A7
A4	28	84	A5
A2	29	85	A3
A0	30	86	A1
$\overline{\text{TRG0}}$, $\overline{\text{G0}}$	31	87	NC, ($\overline{\text{TRG1}}$, $\overline{\text{G1}}$)
VSS	32	88	VSS
SC	33	89	$\overline{\text{Wx}}$, $\overline{\text{CEx}}$
$\overline{\text{RE0}}$	34	90	NC, ($\overline{\text{RE1}}$)
VDD	35	91	VDD
DQ16	36	92	SDQ16
DQ17	37	93	SDQ17
DQ18	38	94	SDQ18
DQ19	39	95	SDQ19
DQ20	40	96	SDQ20
DQ21	41	97	SDQ21
DQ22	42	98	SDQ22
DQ23	43	99	SDQ23
$\overline{\text{W2}}$, $\overline{\text{CE2}}$	44	100	$\overline{\text{W3}}$, $\overline{\text{CE3}}$
VSS	45	101	VSS
DQ24	46	102	SDQ24
DQ25	47	103	SDQ25
DQ26	48	104	SDQ26
DQ27	49	105	SDQ27
DQ28	50	106	SDQ28
DQ29	51	107	SDQ29
DQ30	52	108	SDQ30
DQ31	53	109	SDQ31
VDD	54	110	VDD
PD3	55	111	NC
PD4	56	112	PD6

NOTE: Pin functions in ( ) may be re;quired on certain 2–bank 512K X 32 module implementations

FIGURE 4.4.6–A
256K & 512K MPDRAM DIMM

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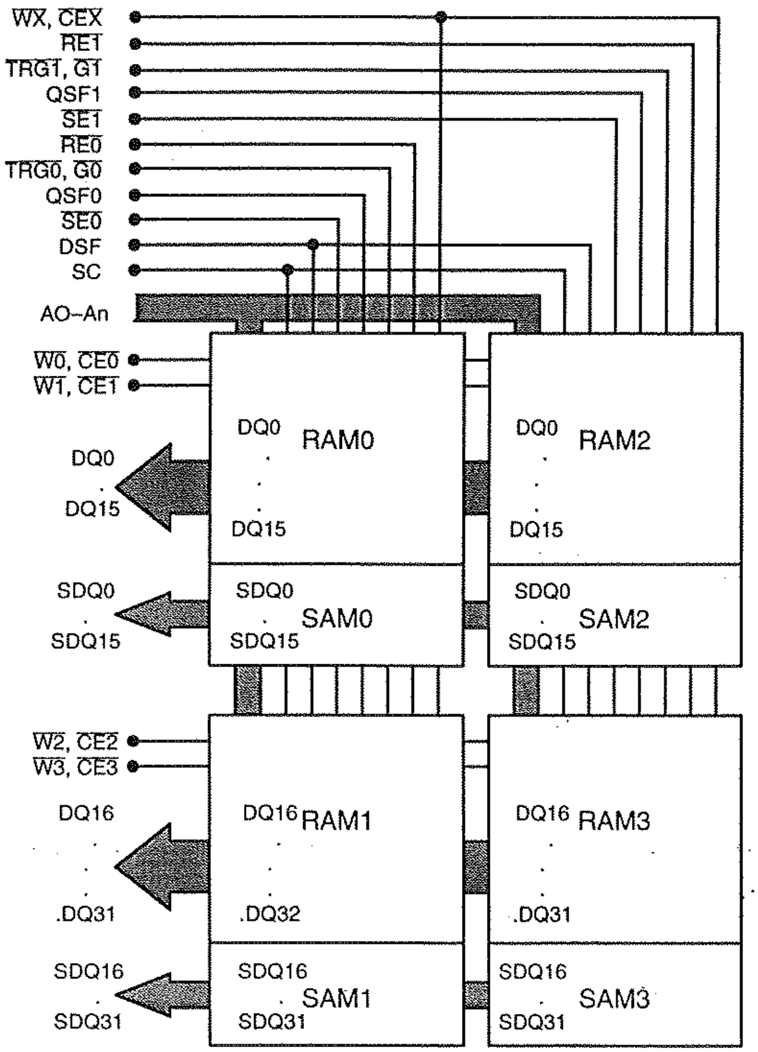

BLOCK DIAGRAM for 256K/512K X 32 DIMM WITH 256K BY 16 MPDRAM

CAPACITY	
	PD1
	Pin 1
1MB	S
2MB	O

SAM LENGTH	
	PD2
	Pin 2
256	S
512	O

OPERATIONAL MODE	
	PD3
	Pin 55
Fast Page	S
EDO	O

BYTE CONTROL	
	PD6
	Pin 112
4 $\overline{CE}$	S
4 $\overline{W}$	O

PD SPEED TABLE		
	PD4	PD5
SPEED (tRELQV)	Pin 56	Pin 57
80 ns	O	O
70 ns	S	O
60 ns	O	S
50 ns	S	S

S = CONNECTED TO VSS
O = NO CONNECTION

PD TRUTH TABLES for 256K/512K X 32 DIMM WITH 256K BY 8 or 16 MPDRAM

FIGURE 4.4.6–B

256K/512K BY 32 MPDRAM DIMM WITH 256K BY 16 MPDRAM

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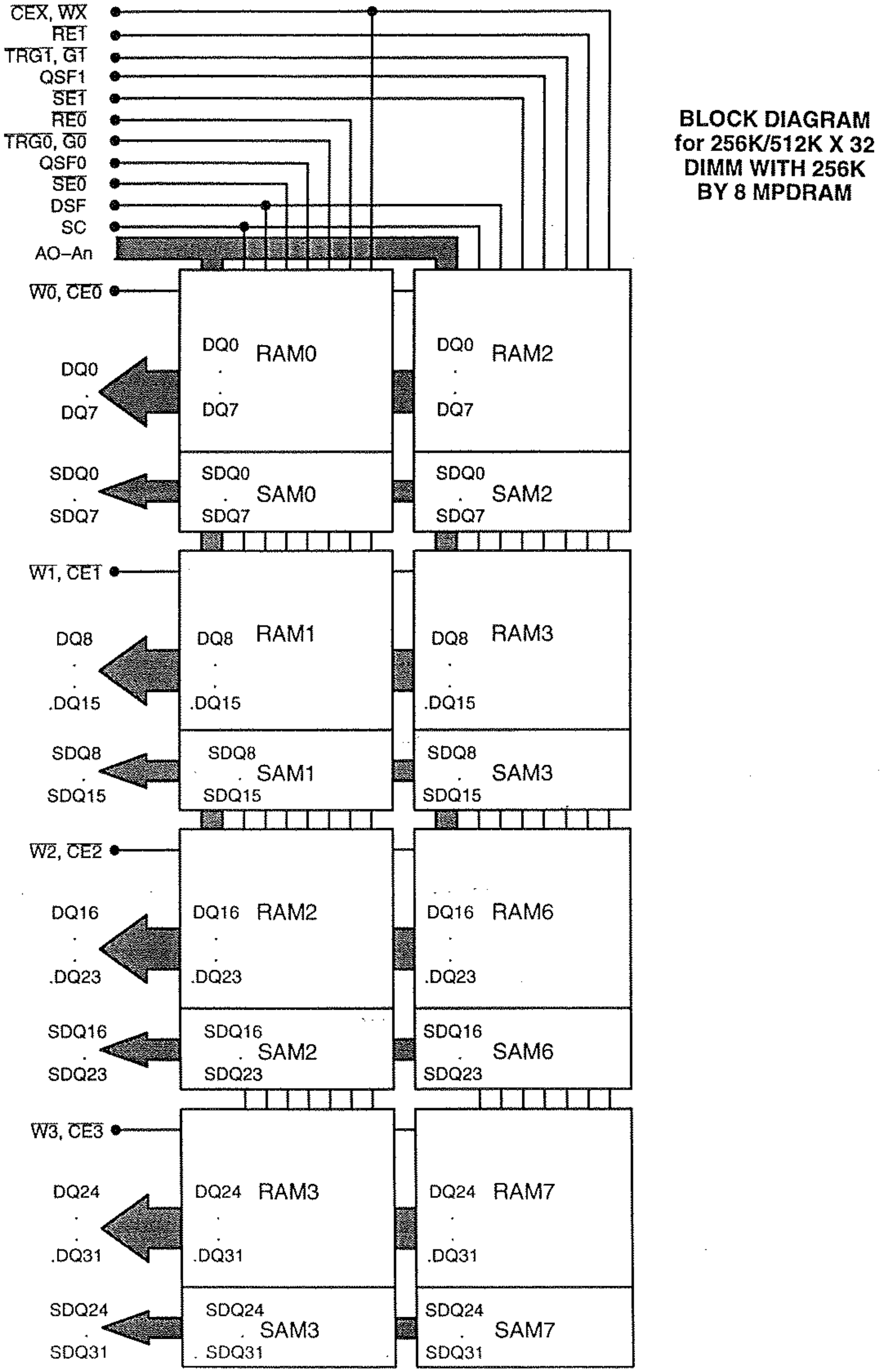

FIGURE 4.4.6–C

256K/512K BY 32 MPDRAM DIMM WITH 256K BY 8 MPDRAM

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4.4.7 – 80 PIN EEPROM SIMM FAMILY

CAPACITY—128K, 256K, 512K, 1M, 2M, 4M, & 8M WORDS OF 32 BITS
CONFIGURATION—Fifteen Different Configurations Using 1mb, 4mb, & 16mb Devices.
LOGIC FEATURES—The modules contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the module.
PACKAGE—88 PIN JEDEC MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Fig. 4.4.7–A
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.7–B

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PIN #	PIN NAME	PIN #	PIN NAME
1	VSS	41	A11
2	VDD	42	A10
3	VPP/NC	43	A9
4	$\overline{G}$	44	A8
5	$\overline{W0}$	45	A7
6	$\overline{W1}$	46	A6
7	RFU	47	A5
8	DQ16	48	A4
9	DQ17	49	A3
10	DQ18	50	A2
11	DQ19	51	A1
12	DQ20	52	A0
13	DQ21	53	$\overline{W3}$
14	DQ22	54	VSS
15	DQ23	55	DQ15
16	DQ24	56	DQ14
17	DQ25	57	DQ13
18	DQ26	58	DQ12
19	DQ27	59	DQ11
20	DQ28	60	DQ10
21	$\overline{E3}$	61	DQ9
22	$\overline{E2}$	62	DQ8
23	$\overline{E1}$	63	DQ7
24	$\overline{E0}$	64	DQ6
25	VSS	65	DQ5
26	DQ29	66	DQ4
27	DQ30	67	DQ3
28	DQ31	68	DQ2
29	$\overline{W2}$	69	DQ1
30	A22	70	DQ0
31	A21	71	VPP/NC
32	A20	72	VDD
33	A19	73	PD1
34	A18	74	PD2
35	A17	75	PD3
36	A16	76	PD4
37	A15	77	PD5
38	A14	78	PD6
39	A13	79	PD7
40	A12	80	VSS

PRESENCE DETECT TRUTH TABLE

Module Organization	Device Density	# of Dev.	Module Capacity	PD1	PD2	PD3	PD4
No Module				1	1	1	1
128K X 32	1M	4	512KB	0	1	1	1
256K X 32	1M	8	1MB	1	0	1	1
512K X 32	1M	16	2MB	0	0	1	1
256K X 32	2M	4	1MB	1	1	0	1
512K X 32	2M	8	2MB	0	1	0	1
1M X 32	2M	16	4MB	1	0	0	1
512K X 32	4M	4	2MB	0	0	0	1
1M X 32	4M	8	4MB	1	1	1	0
2M X 32	4M	16	8MB	0	1	1	0
1M X 32	8M	4	4MB	1	0	1	0
2M X 32	8M	8	8MB	0	0	1	0
4M X 32	8M	16	16MB	1	1	0	0
2M X 32	16M	4	8MB	0	1	0	0
4M X 32	16M	8	16MB	1	0	0	0
8M X 32	16M	16	32MB	0	0	0	0

1 = OPEN CIRCUIT (NO CONNECTION)
0 = CONNECTED TO VSS

MODULE SPEED IDENTIFICATION

MAX ACCESS TIME	PRESENCE DETECT PIN		
	PD5	PD6	PD7
NOT DEFINED	1	1	1
45 nS	0	1	1
55 nS	1	0	1
70 nS	0	0	1
90 nS	1	1	0
120 nS	0	1	0
150 nS	1	0	0
200 nS	0	0	0

NOTE – This family of pinouts is approved for use in SIMM package that is nominally 4.65" long and a height of 0.85" See JEDEC Publication 95, section MO–XXX.

FIGURE 4.4.7–A
128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES

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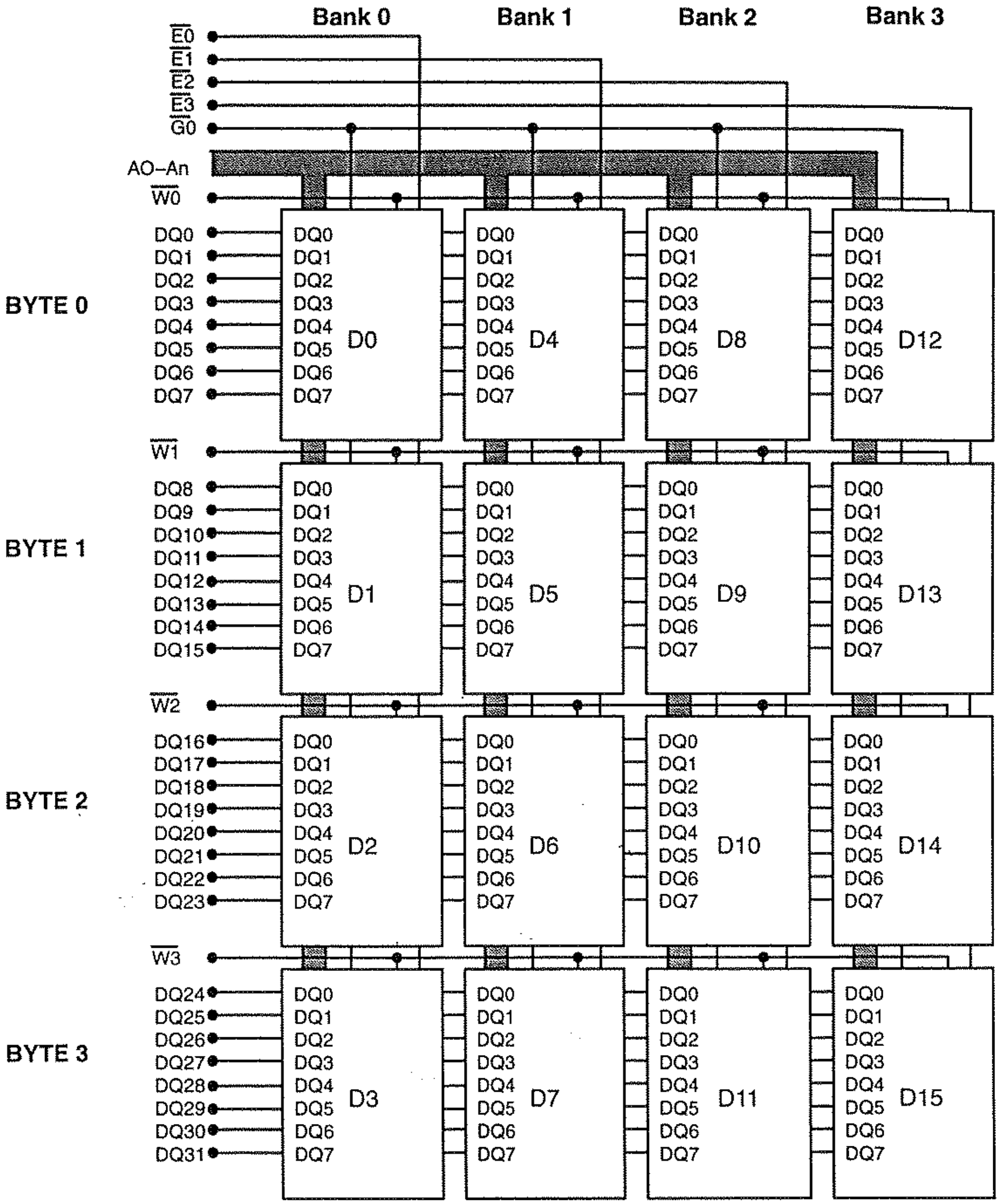

FIGURE 4.4.7–B
128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM

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4.4.8 – 100 PIN DRAM, SDRAM & ROM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.
DATA CONFIGURATIONS—Seven DATA Word configurations are defined:
—32 BIT DRAM & SDRAM without PARITY
—36 BIT DRAM & SDRAM for ECC CODES
—40 BIT DRAM & SDRAM for ECC CODES
—32 BIT MULTIPLEXED ROM without PARITY.
CONFIGURATION—26 Different Configurations are defined using various combinationa of X1, X4, X8, and X16 DRAM & SDRAM memories including 2 bank configurations, 5 for DRAM and 21 for SDRAM.
LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—100 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.4.8–A & 4.4.8–B
TECHNOLOGY COMPARISON TABLE — Fig. 4.4.8–C
SDRAM CLOCK WIRING DIAGRAMS — Fig. 4.4.8–D
SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–E through 4.4.8–Z
DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–AA through 4.4.8–AE

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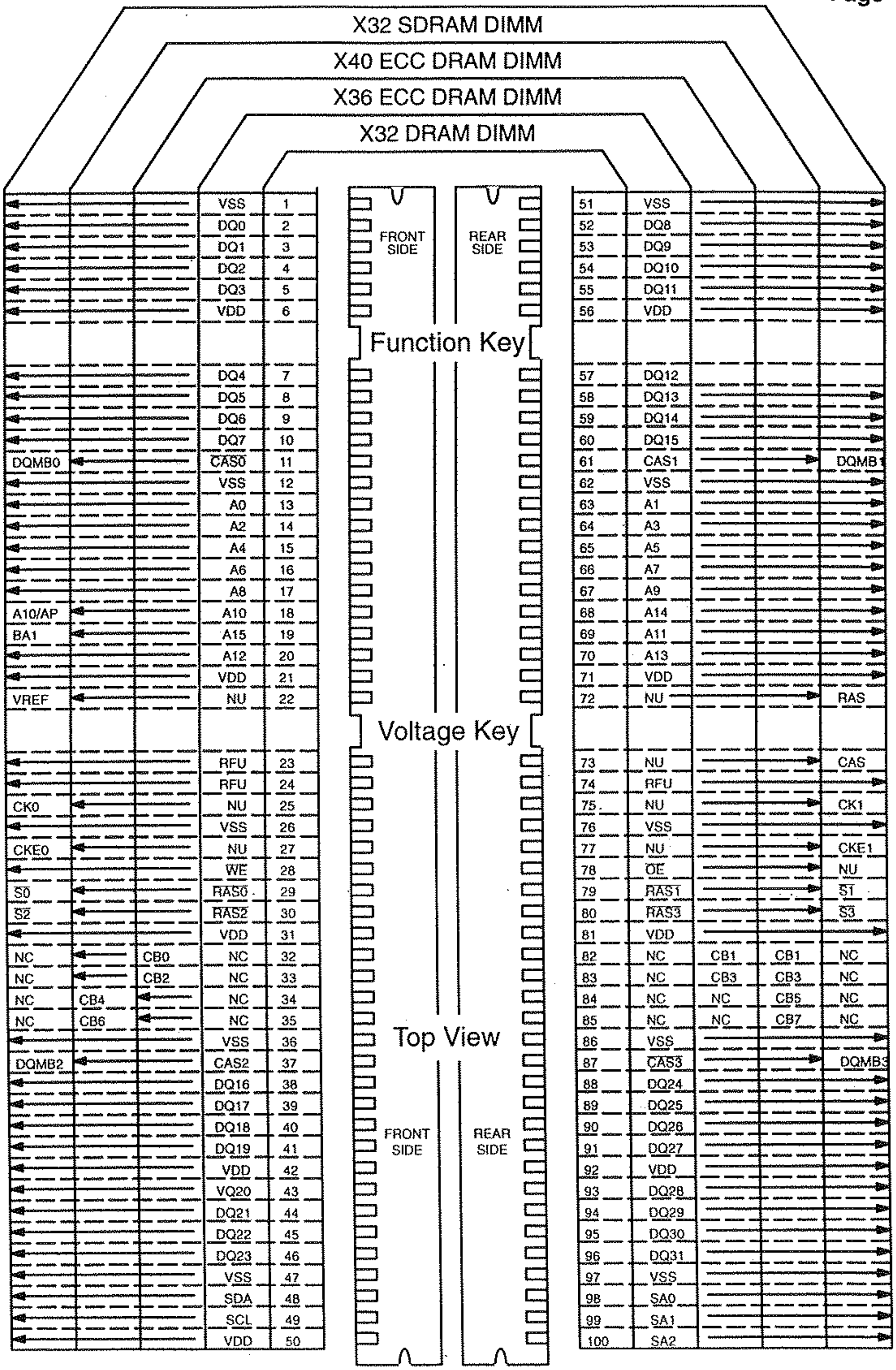
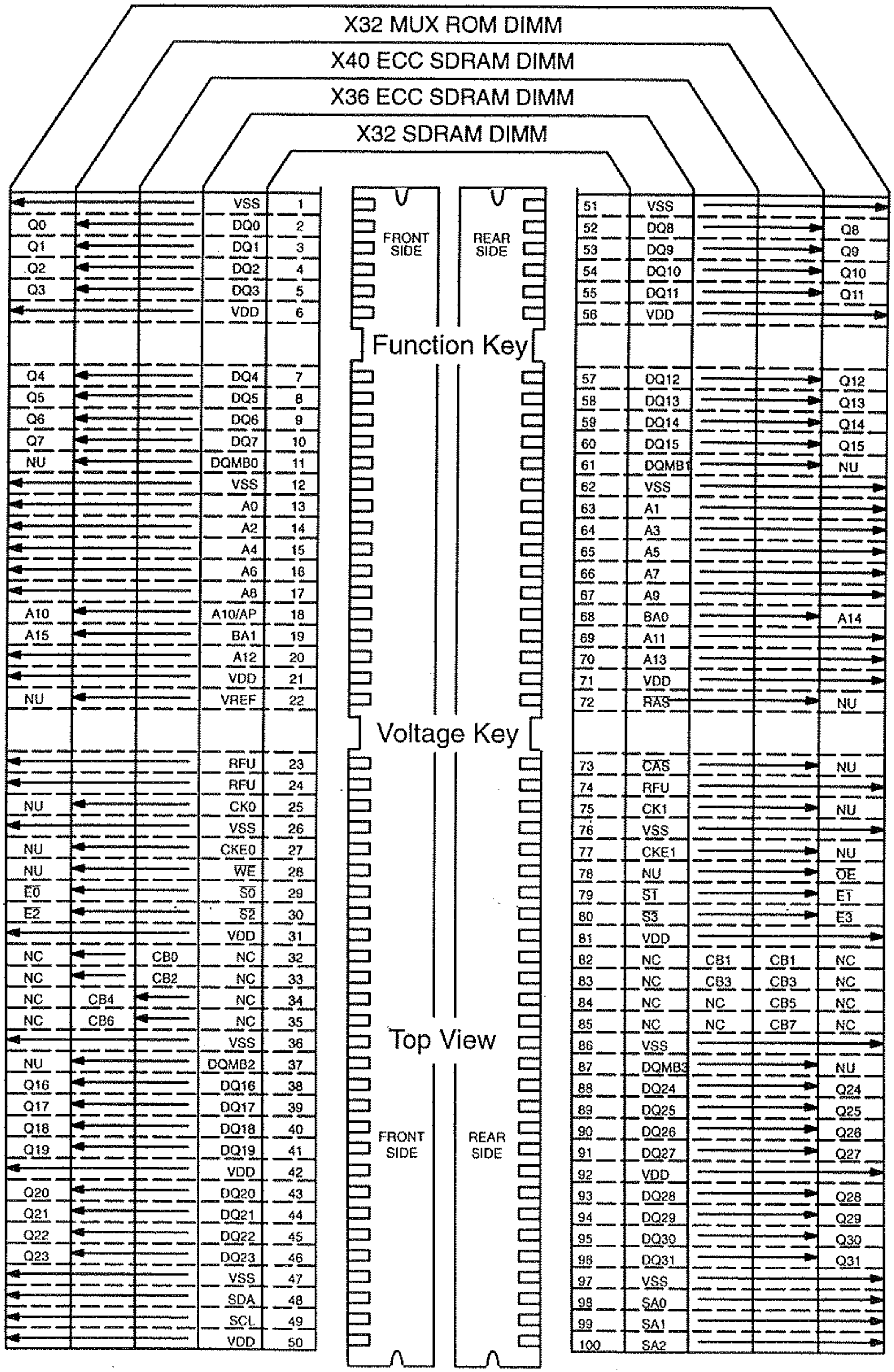


Pin	X32 DRAM DIMM	X36 ECC DRAM DIMM	X40 ECC DRAM DIMM	X32 SDRAM DIMM
1	VSS			
2	DQ0			
3	DQ1			
4	DQ2			
5	DQ3			
6	VDD			
7	DQ4			
8	DQ5			
9	DQ6			
10	DQ7			
11	$\overline{\text{CAS0}}$			DQMB0
12	VSS			
13	A0			
14	A2			
15	A4			
16	A6			
17	A8			
18	A10			A10/AP
19	A15			BA1
20	A12			
21	VDD			
22	NU			VREF
23	RFU			
24	RFU			
25	NU			CK0
26	VSS			
27	NU			CKE0
28	$\overline{\text{WE}}$			
29	$\overline{\text{RAS0}}$			$\overline{\text{S0}}$
30	$\overline{\text{RAS2}}$			$\overline{\text{S2}}$
31	VDD			
32	NC	CB0		NC
33	NC	CB2		NC
34	NC		CB4	NC
35	NC		CB6	NC
36	VSS			
37	CAS2			DQMB2
38	DQ16			
39	DQ17			
40	DQ18			
41	DQ19			
42	VDD			
43	VQ20			
44	DQ21			
45	DQ22			
46	DQ23			
47	VSS			
48	SDA			
49	SCL			
50	VDD			
51	VSS			
52	DQ8			
53	DQ9			
54	DQ10			
55	DQ11			
56	VDD			
57	DQ12			
58	DQ13			
59	DQ14			
60	DQ15			
61	CAS1			DQMB1
62	VSS			
63	A1			
64	A3			
65	A5			
66	A7			
67	A9			
68	A14			
69	A11			
70	A13			
71	VDD			
72	NU			RAS
73	NU			CAS
74	RFU			
75	NU			CK1
76	VSS			
77	NU			CKE1
78	$\overline{\text{OE}}$			NU
79	$\overline{\text{RAS1}}$			$\overline{\text{S1}}$
80	$\overline{\text{RAS3}}$			$\overline{\text{S3}}$
81	VDD			
82	NC	CB1	CB1	NC
83	NC	CB3	CB3	NC
84	NC	NC	CB5	NC
85	NC	NC	CB7	NC
86	VSS			
87	$\overline{\text{CAS3}}$			DQMB3
88	DQ24			
89	DQ25			
90	DQ26			
91	DQ27			
92	VDD			
93	DQ28			
94	DQ29			
95	DQ30			
96	DQ31			
97	VSS			
98	SA0			
99	SA1			
100	SA2			

FIGURE 4.4.8– B

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT



X32 MUX ROM DIMM	X40 ECC SDRAM DIMM	X36 ECC SDRAM DIMM	X32 SDRAM DIMM	Pin
←	←	←	VSS	1
Q0	←	←	DQ0	2
Q1	←	←	DQ1	3
Q2	←	←	DQ2	4
Q3	←	←	DQ3	5
←	←	←	VDD	6
Q4	←	←	DQ4	7
Q5	←	←	DQ5	8
Q6	←	←	DQ6	9
Q7	←	←	DQ7	10
NU	←	←	DQMB0	11
←	←	←	VSS	12
←	←	←	A0	13
←	←	←	A2	14
←	←	←	A4	15
←	←	←	A6	16
←	←	←	A8	17
A10	←	←	A10/AP	18
A15	←	←	BA1	19
←	←	←	A12	20
←	←	←	VDD	21
NU	←	←	VREF	22
←	←	←	RFU	23
←	←	←	RFU	24
NU	←	←	CK0	25
←	←	←	VSS	26
NU	←	←	CKE0	27
NU	←	←	$\overline{WE}$	28
$\overline{E0}$	←	←	$\overline{S0}$	29
$\overline{E2}$	←	←	$\overline{S2}$	30
←	←	←	VDD	31
NC	←	CB0	NC	32
NC	←	CB2	NC	33
NC	CB4	←	NC	34
NC	CB6	←	NC	35
←	←	←	VSS	36
NU	←	←	DQMB2	37
Q16	←	←	DQ16	38
Q17	←	←	DQ17	39
Q18	←	←	DQ18	40
Q19	←	←	DQ19	41
←	←	←	VDD	42
Q20	←	←	DQ20	43
Q21	←	←	DQ21	44
Q22	←	←	DQ22	45
Q23	←	←	DQ23	46
←	←	←	VSS	47
←	←	←	SDA	48
←	←	←	SCL	49
←	←	←	VDD	50

Pin	X32 SDRAM DIMM	X36 ECC SDRAM DIMM	X40 ECC SDRAM DIMM	X32 MUX ROM DIMM
51	VSS	→	→	→
52	DQ8	→	→	Q8
53	DQ9	→	→	Q9
54	DQ10	→	→	Q10
55	DQ11	→	→	Q11
56	VDD	→	→	→
57	DQ12	→	→	Q12
58	DQ13	→	→	Q13
59	DQ14	→	→	Q14
60	DQ15	→	→	Q15
61	DQMB1	→	→	NU
62	VSS	→	→	→
63	A1	→	→	→
64	A3	→	→	→
65	A5	→	→	→
66	A7	→	→	→
67	A9	→	→	→
68	BA0	→	→	A14
69	A11	→	→	→
70	A13	→	→	→
71	VDD	→	→	→
72	$\overline{RAS}$	→	→	NU
73	$\overline{CAS}$	→	→	NU
74	RFU	→	→	→
75	CK1	→	→	NU
76	VSS	→	→	→
77	CKE1	→	→	NU
78	NU	→	→	$\overline{OE}$
79	$\overline{S1}$	→	→	$\overline{E1}$
80	$\overline{S3}$	→	→	$\overline{E3}$
81	VDD	→	→	→
82	NC	CB1	CB1	NC
83	NC	CB3	CB3	NC
84	NC	NC	CB5	NC
85	NC	NC	CB7	NC
86	VSS	→	→	→
87	DQMB3	→	→	NU
88	DQ24	→	→	Q24
89	DQ25	→	→	Q25
90	DQ26	→	→	Q26
91	DQ27	→	→	Q27
92	VDD	→	→	→
93	DQ28	→	→	Q28
94	DQ29	→	→	Q29
95	DQ30	→	→	Q30
96	DQ31	→	→	Q31
97	VSS	→	→	→
98	SA0	→	→	→
99	SA1	→	→	→
100	SA2	→	→	→

FIGURE 4.4.8– C

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT

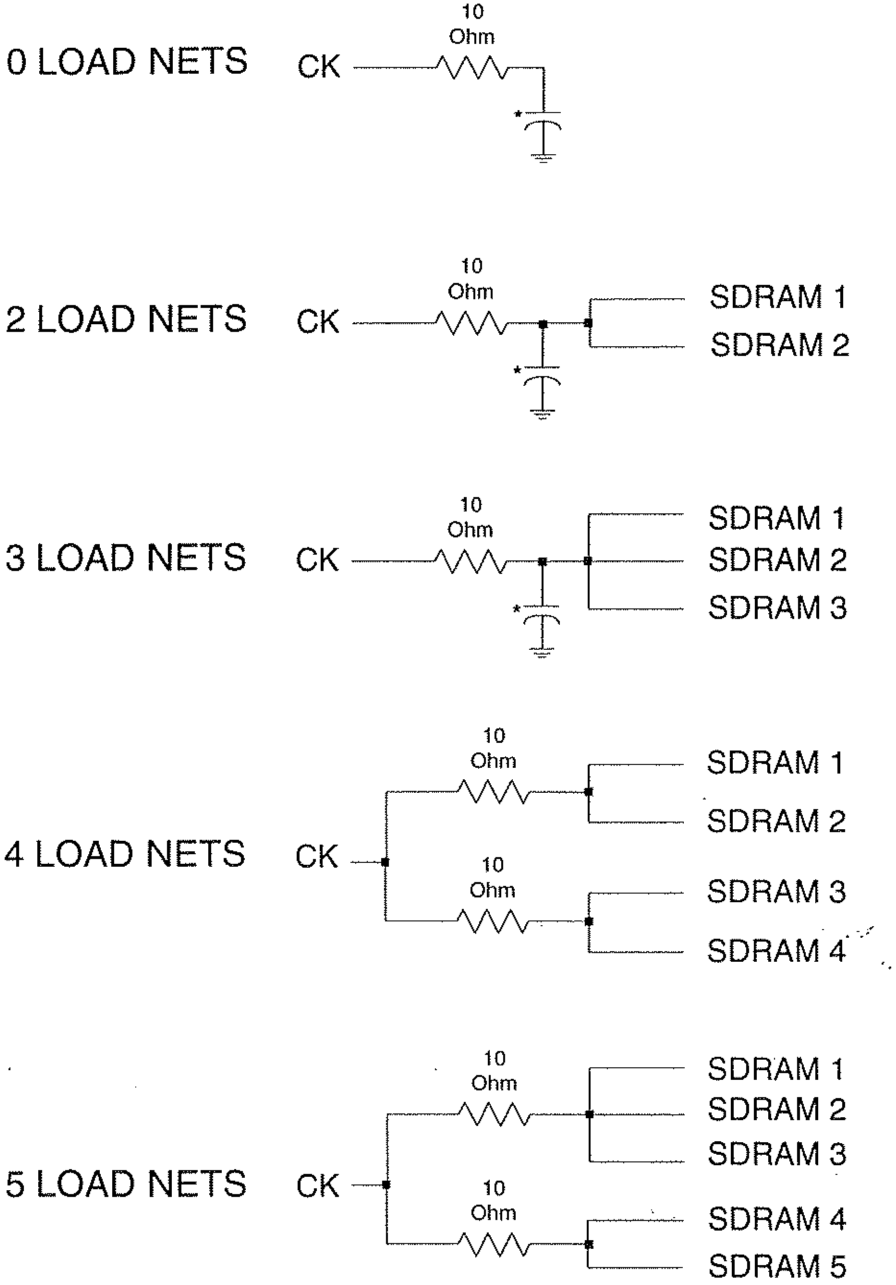
100 PIN DRAM/SDRAM DIMM PINOUT COMPARISON

PIN	DRAM DIMM	SDRAM DIMM	MUX ROM
11	$\overline{CAS0}$	DQMB0	NU
18	A10	A10/AP	A10
19	A12	BA1	A12
20	NU	A12	A14
22	NU	Vref	NU
25	NU	CK0	NU
27	NU	CKE0	NU
28	$\overline{WE}$	$\overline{WE}$	NU
29	$\overline{RAS0}$	$\overline{S0}$	$\overline{E0}$
30	$\overline{RAS2}$	$\overline{S2}$	$\overline{E2}$
37	$\overline{CAS2}$	DQMB2	NU
61	$\overline{CAS1}$	DQMB1	NU
68	A11	BA0	A11
69	A13	A11	A13
70	NU	A13	A15
72	NU	$\overline{RAS}$	NU
73	NU	$\overline{CAS}$	NU
75	NU	CK1	NU
77	NU	CKE1	NU
78	$\overline{OE}$	NU	$\overline{OE}$
79	$\overline{RAS1}$	$\overline{S1}$	$\overline{E1}$
80	$\overline{RAS3}$	$\overline{S3}$	$\overline{E3}$
87	$\overline{CAS3}$	DQMB3	NU

Notes:

1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A14 on DRAM DIMM is also BA0 on SDRAM DIMM
3. A15 on DRAM DIMM is also BA1 on SDRAM DIMM (for 4 Bank SDRAM).

Figure 4.4.8-D
100 Pin DRAM, SDRAM, & ROM DIMM, PIN COMPARISON

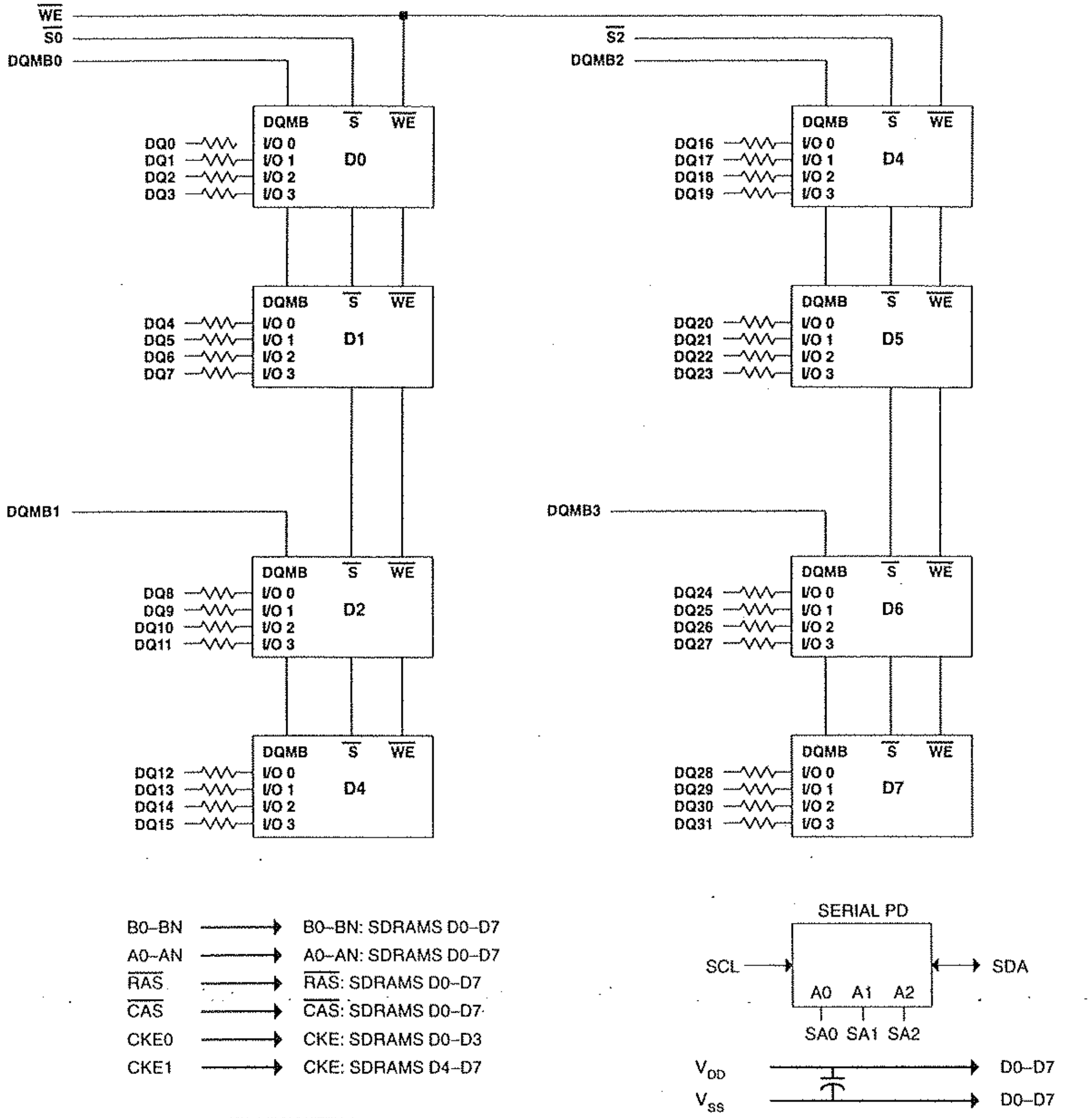


Notes:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .4ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PADDING CAPACITOR). (EG: THIS IS APPROXIMATELY 2" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2.) THE VARIATION OF CK INPUT DELAY WILL BE +/– .1NS FOR BOTH CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/– 3pf IN TOTAL CK INPUT CAPACITANCE).

Figure 4.4.8-E
100 Pin SDRAM DIMM, CLOCK WIRING



Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Figure 4.4.8–F
100 Pin X32 SDRAM DIMM, 1 Bank with X4 SDRAMs

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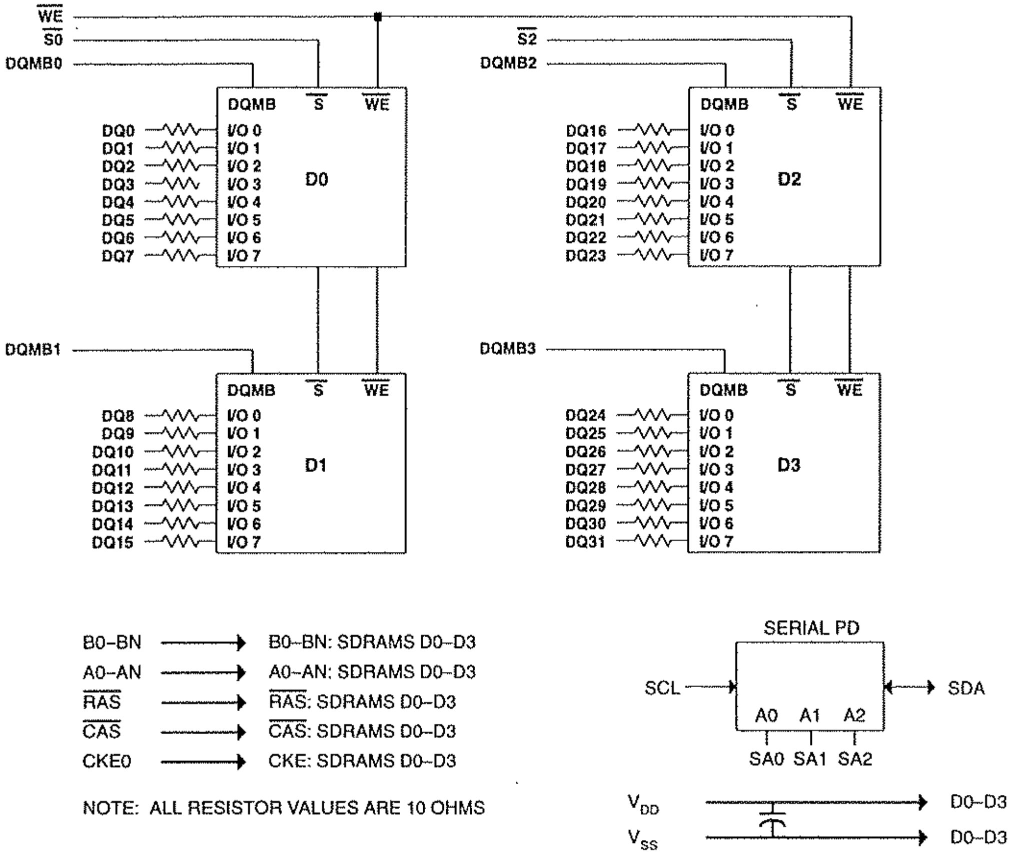


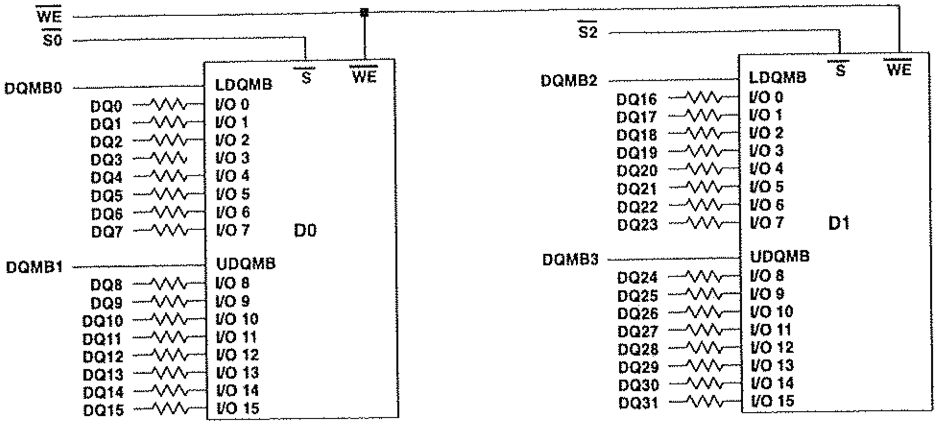
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

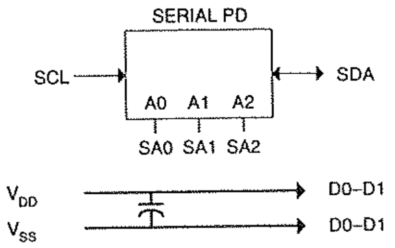
Figure 4.4.8–G
100 Pin X32 SDRAM DIMM, 1 Bank with X8 SDRAMs

3:27



B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0–D1

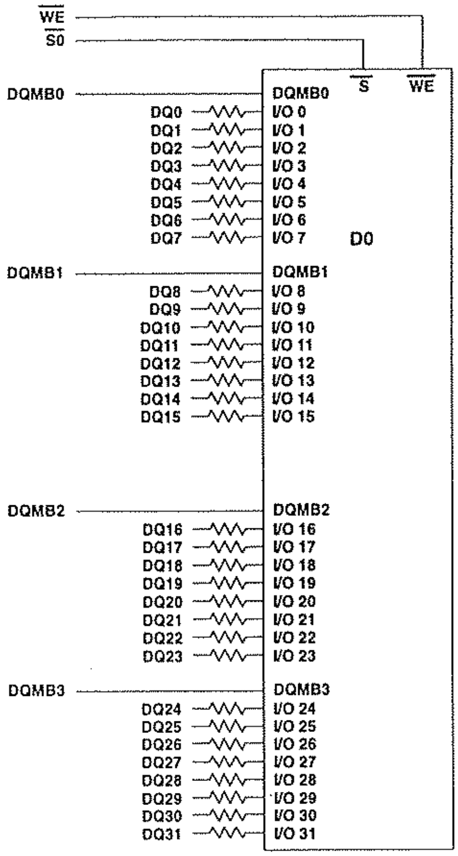
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



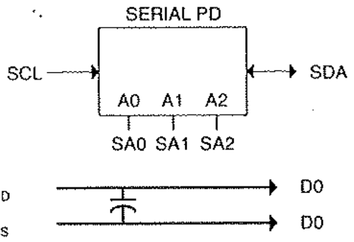
Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–H
100 Pin X32 SDRAM DIMM, 1 Bank with X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0
A0–AN → A0–AN: SDRAMS D0
$\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMS D0
$\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMS D0
CKE0 → CKE: SDRAMS D0

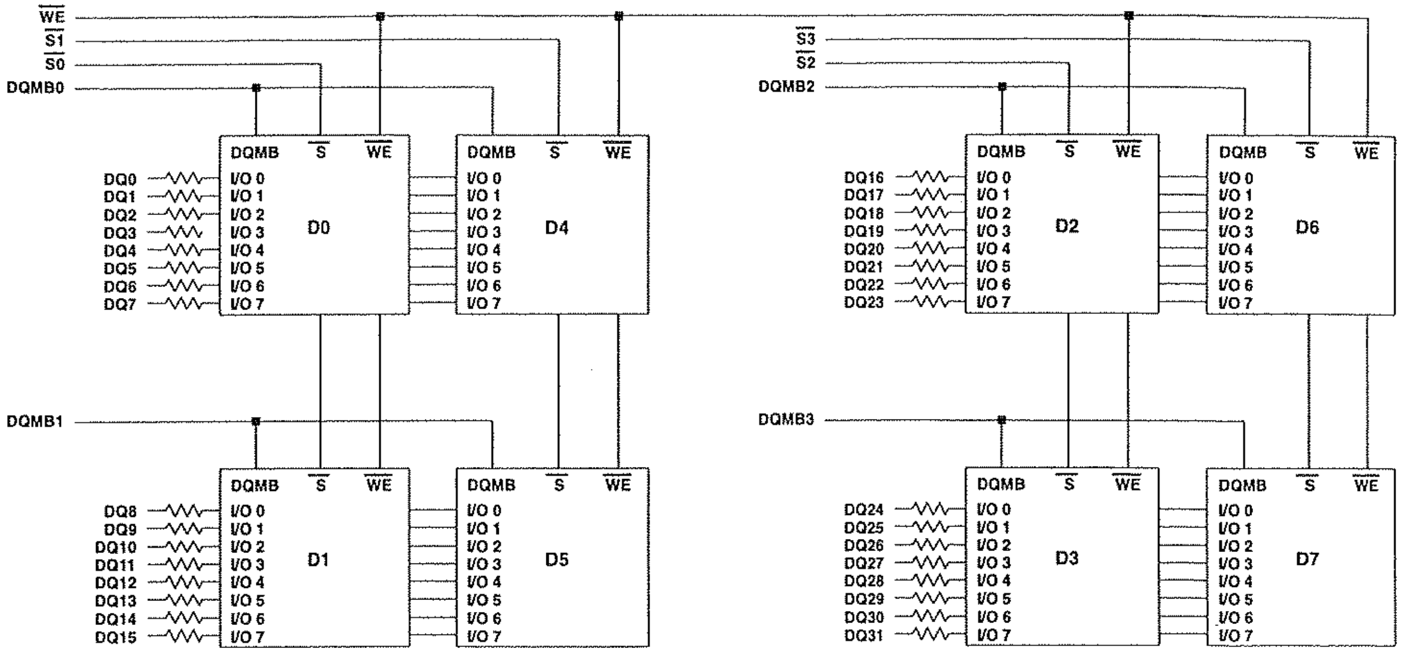


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

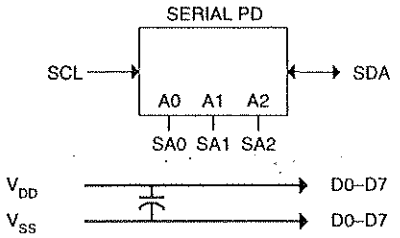
Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	1 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–I
100 Pin X32 SDRAM DIMM, 1 Bank with X32 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D7
A0–AN → A0–AN: SDRAMS D0–D7
$\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMS D0–D7
$\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMS D0–D7
CKE0 → CKE: SDRAMS D0–D3
CKE1 → CKE: SDRAMS D4–D7



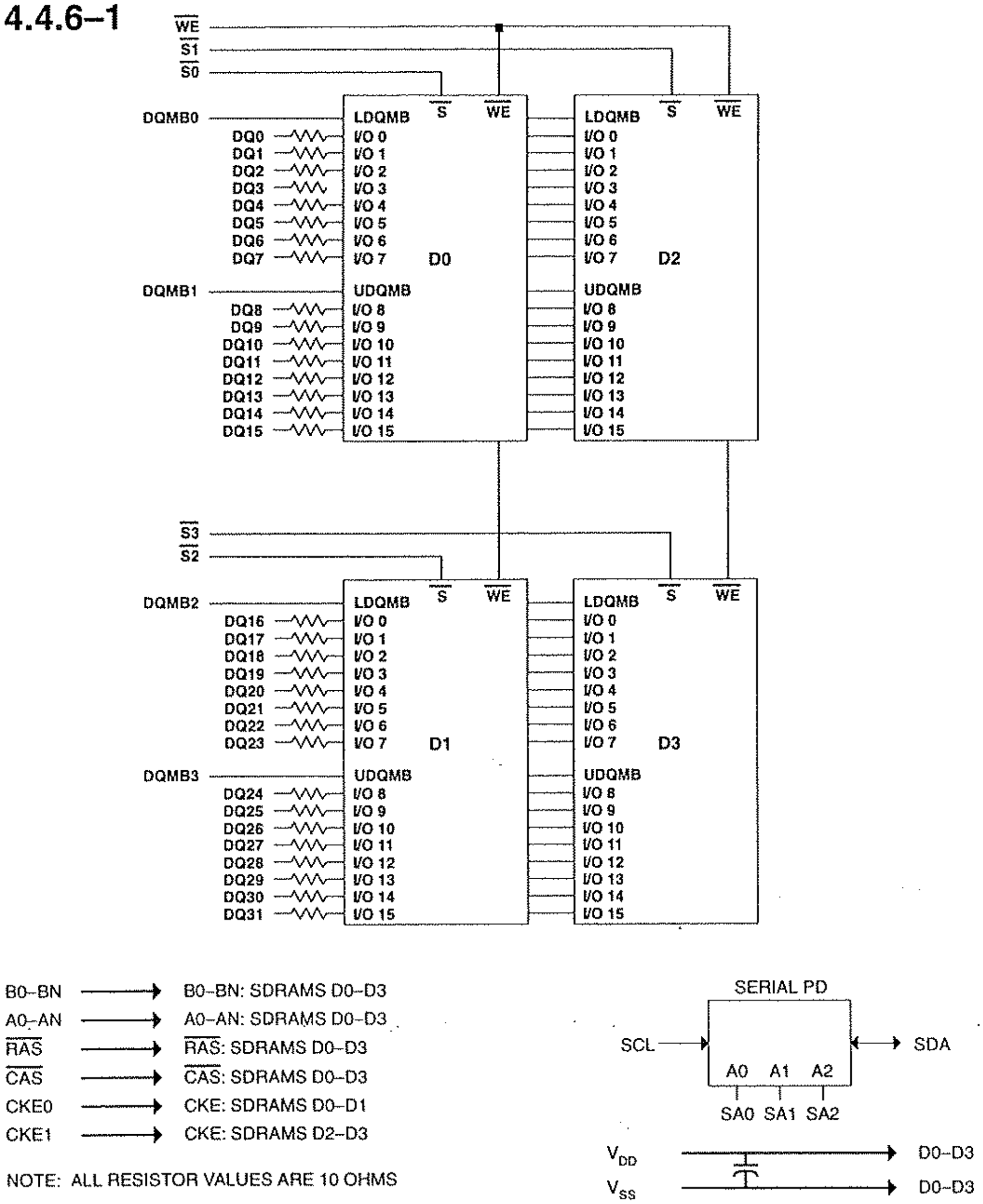
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–J
100 Pin X32 SDRAM DIMM, 2 Bank with X8 SDRAMs

4.4.6–1

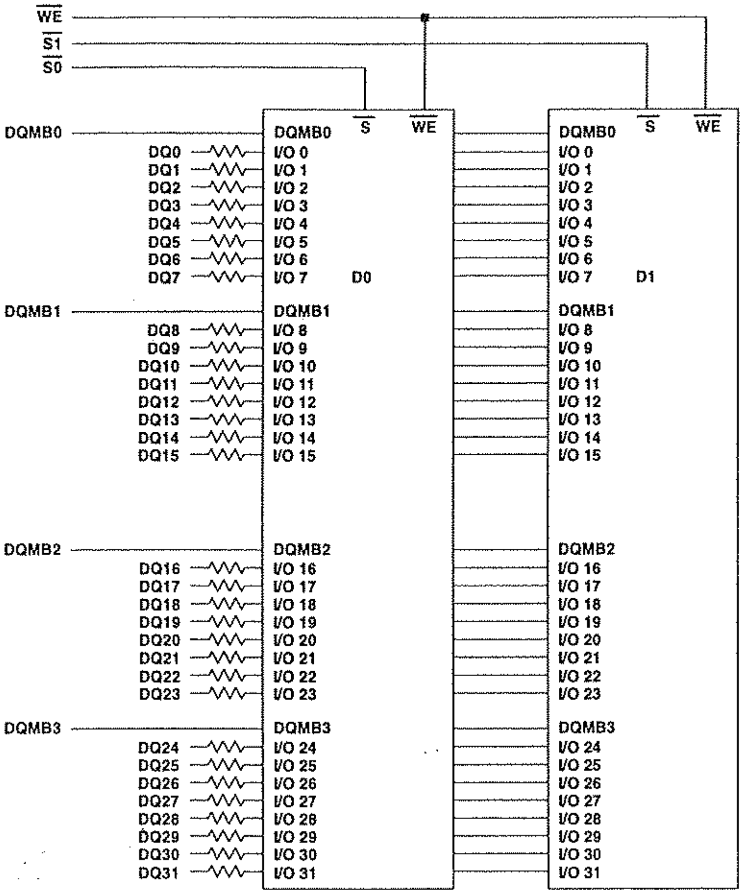


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

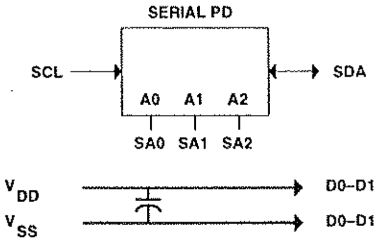
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–K
100 Pin X32 SDRAM DIMM, 2 Bank with X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMS D0–D1
$\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0
CKE1 → CKE: SDRAMS D1

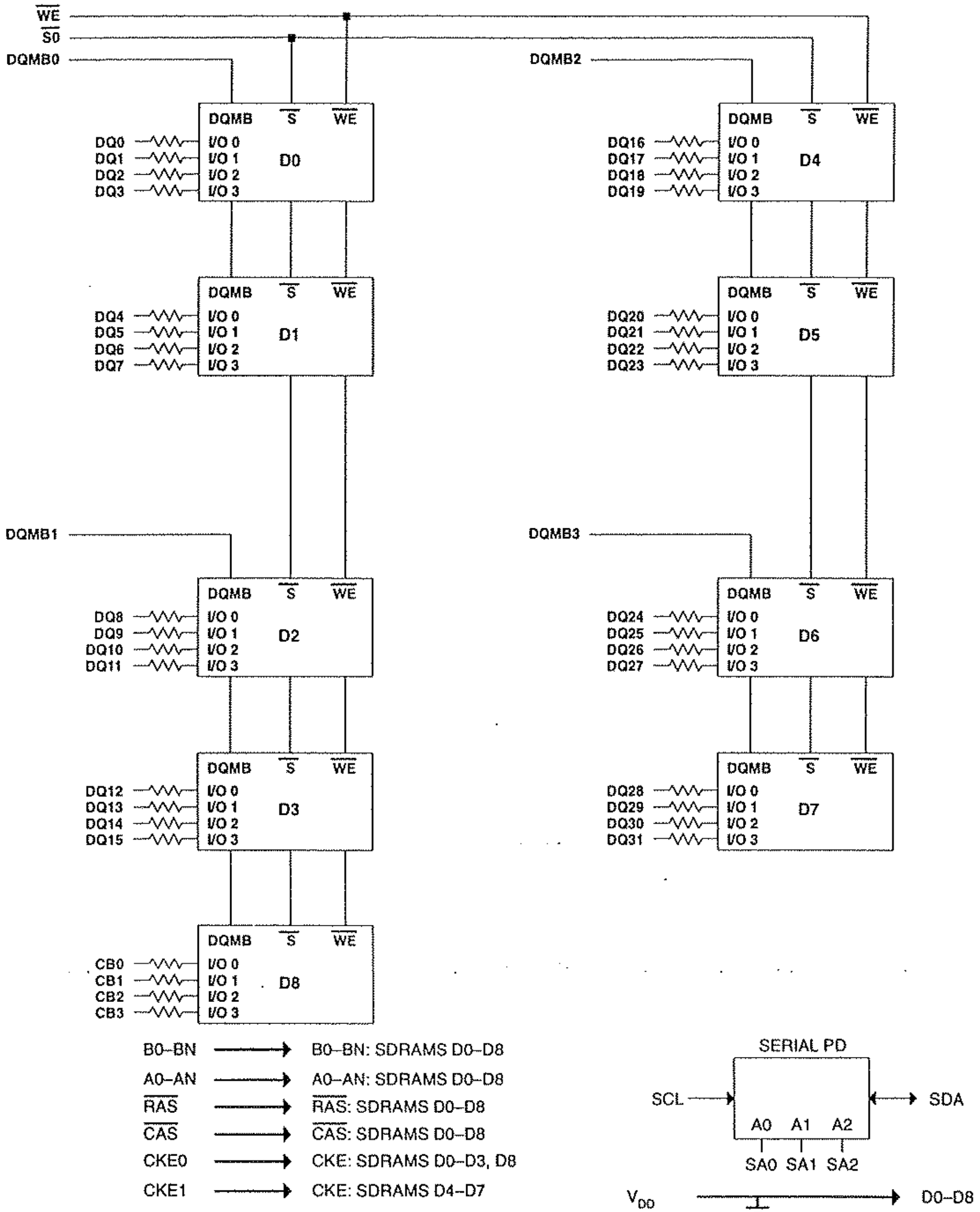
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	1 SDRAM
*CK1	1 SDRAM

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–L
100 Pin X32 SDRAM DIMM, 2 Bank with X32 SDRAMs

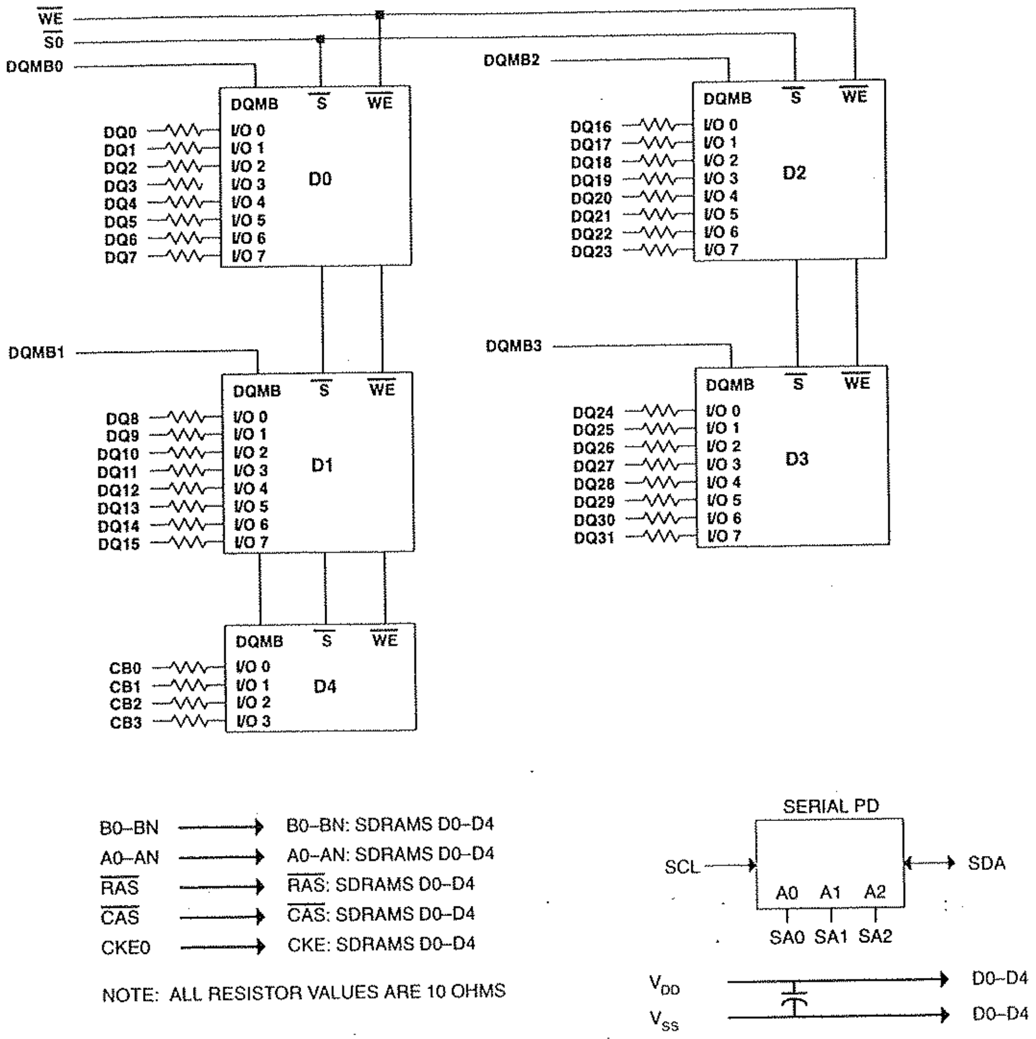


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	4 or 5 SDRAMS 4 or 5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

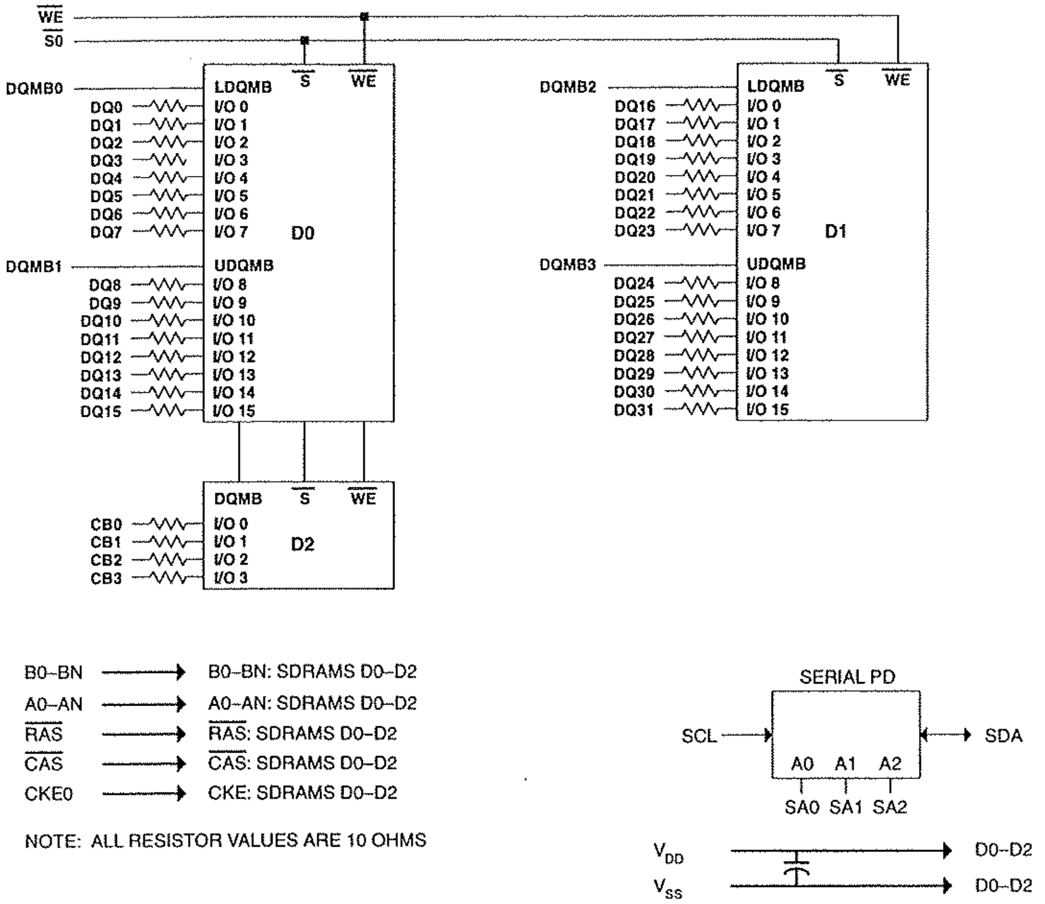
Figure 4.4.8–M
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–N
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X8 SDRAMs



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–O
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X16 SDRAMs

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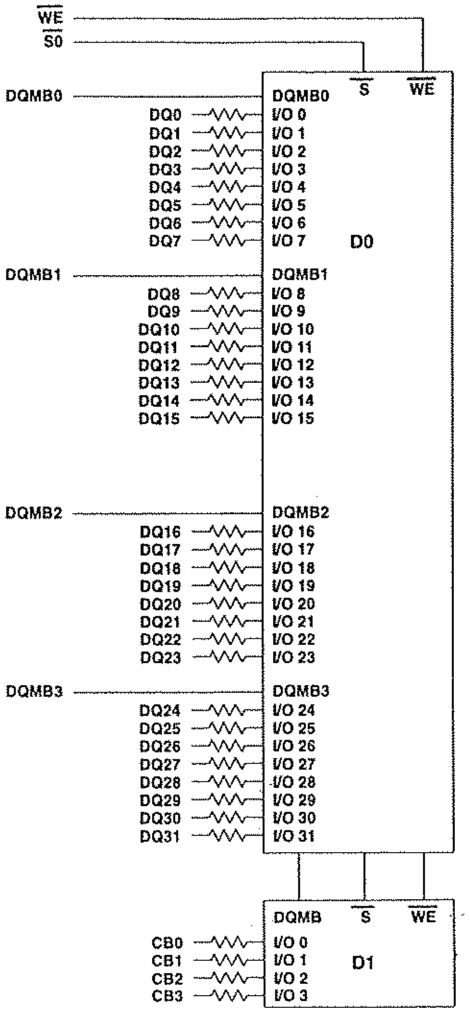
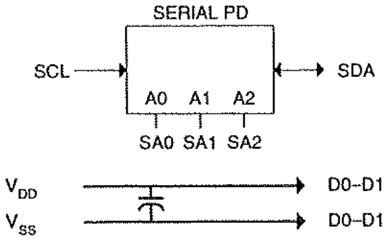


B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMS D0–D1
$\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0–D1

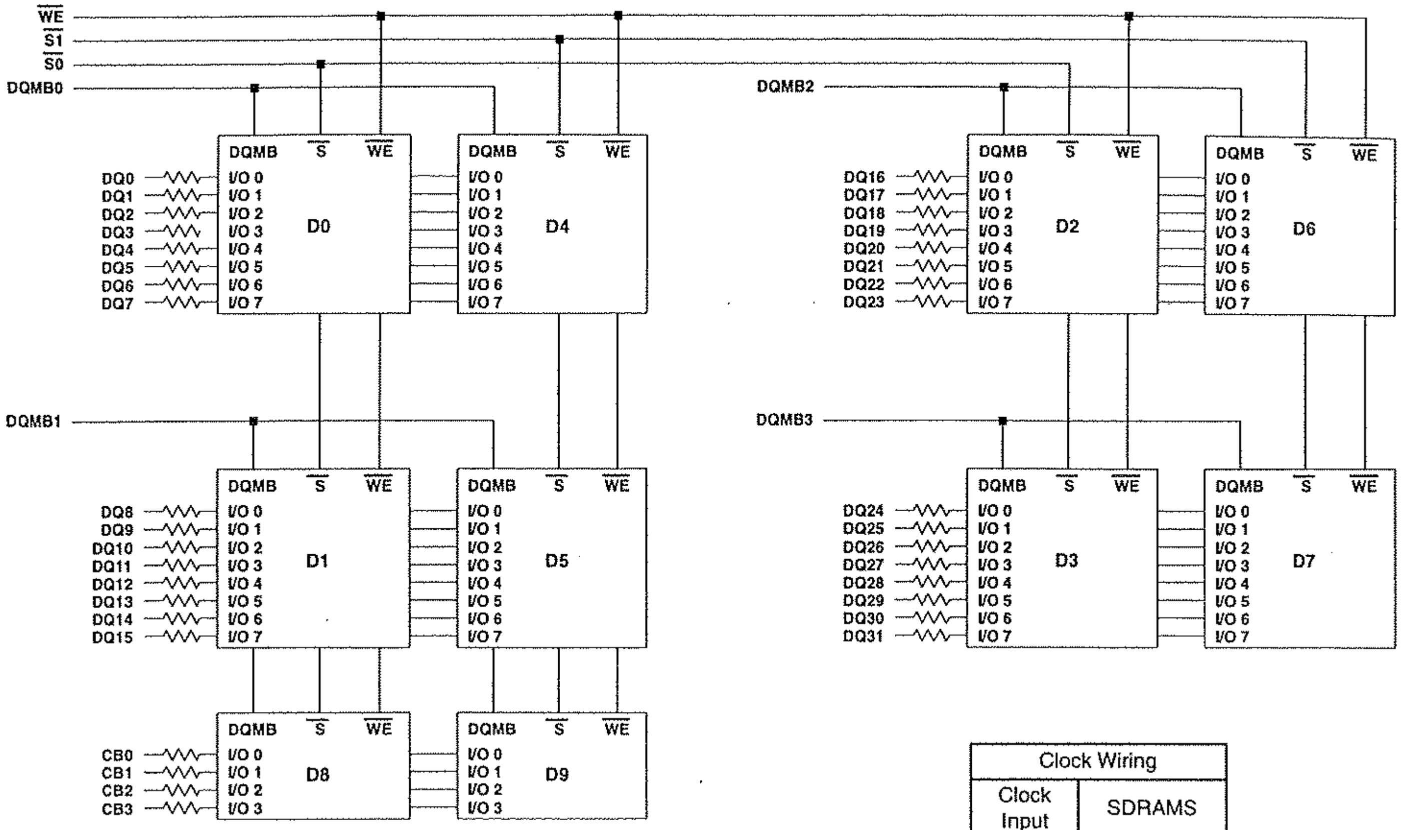
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–P
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X32 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS 5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

B0–BN → B0–BN: SDRAMS D0–D9

A0–AN → A0–AN: SDRAMS D0–D9

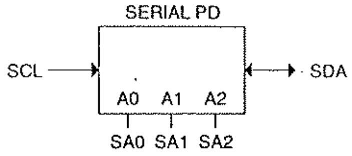
$\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMS D0–D9

$\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMS D0–D9

CKE0 → CKE: SDRAMS D0–D3, D8

CKE1 → CKE: SDRAMS D4–D7, D9

NOTE: ALL RESISTOR VALUES ARE 10 OHMS



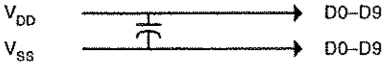
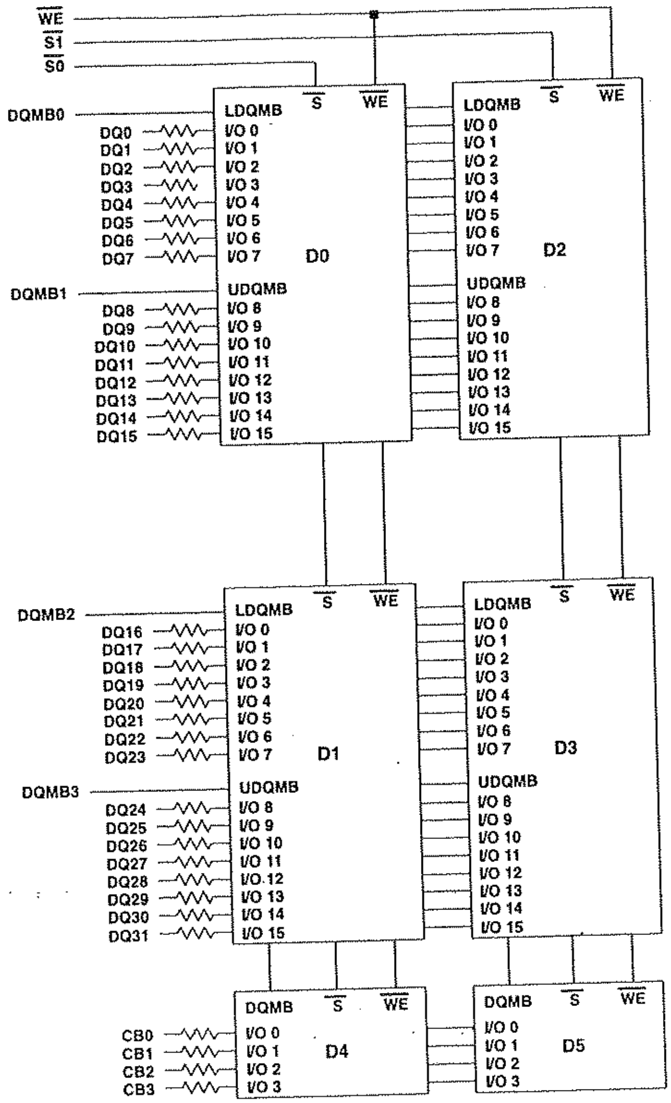
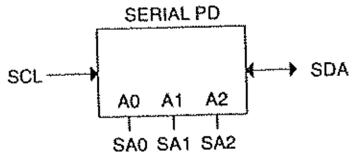


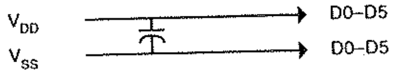
Figure 4.4.8–Q
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X8 SDRAMs



B0-BN → B0-BN: SDRAMS D0-D5
A0-AN → A0-AN: SDRAMS D0-D5
RAS → RAS: SDRAMS D0-D5
CAS → CAS: SDRAMS D0-D5
CKE0 → CKE: SDRAMS D0-D1, D4
CKE1 → CKE: SDRAMS D2-D3, D5



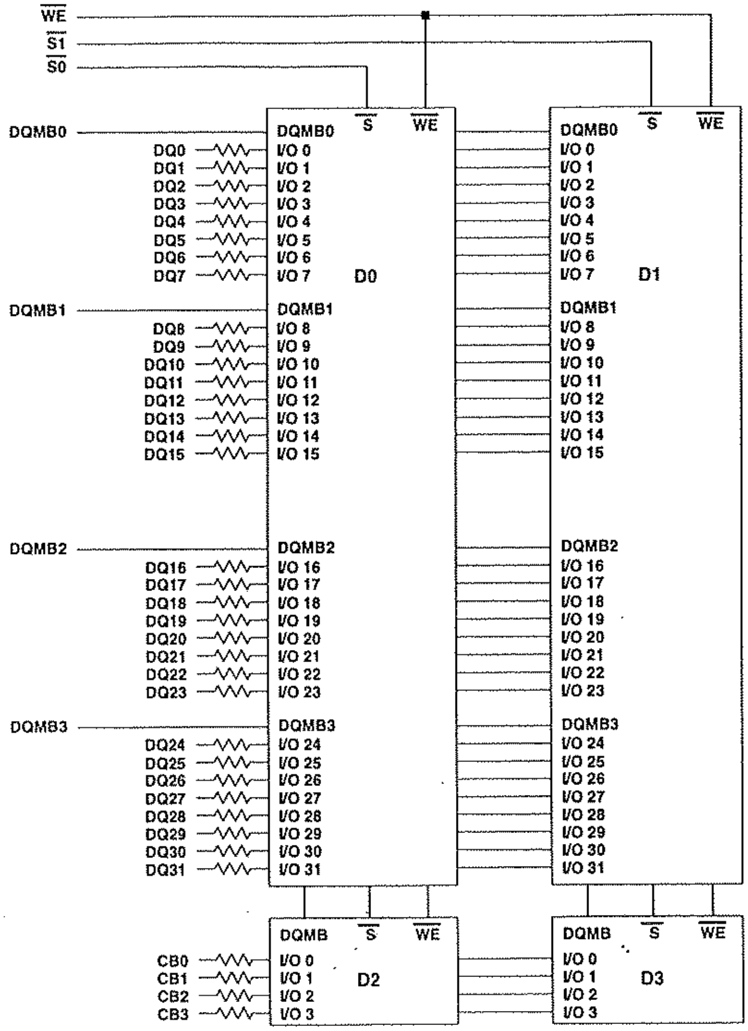
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

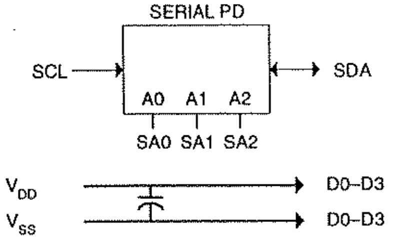
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8-R
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D3
A0–AN → A0–AN: SDRAMS D0–D3
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D3
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D3
CKE0 → CKE: SDRAMS D0, D2
CKE1 → CKE: SDRAMS D1, D3

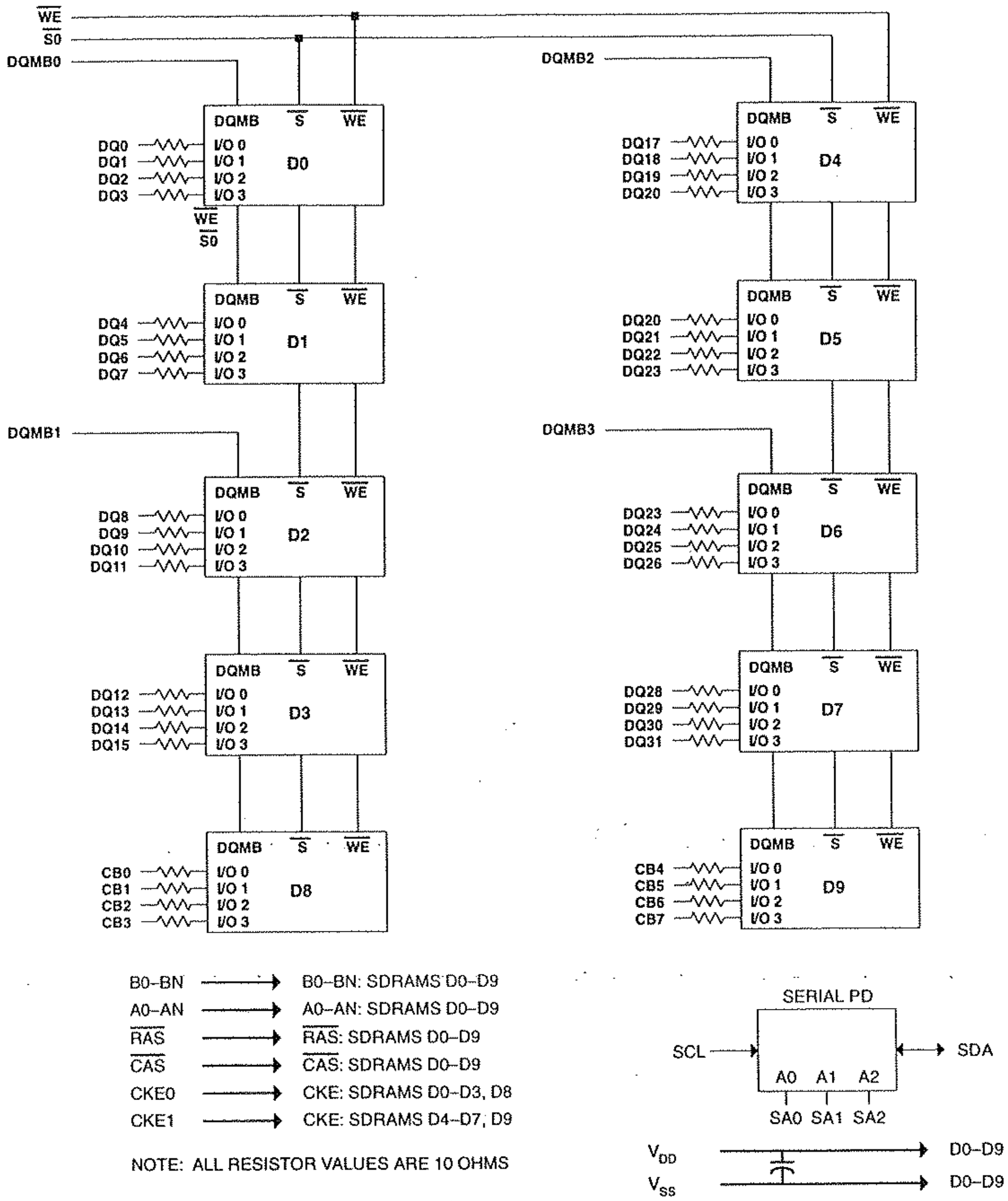
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS 2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–S
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X32 SDRAMs

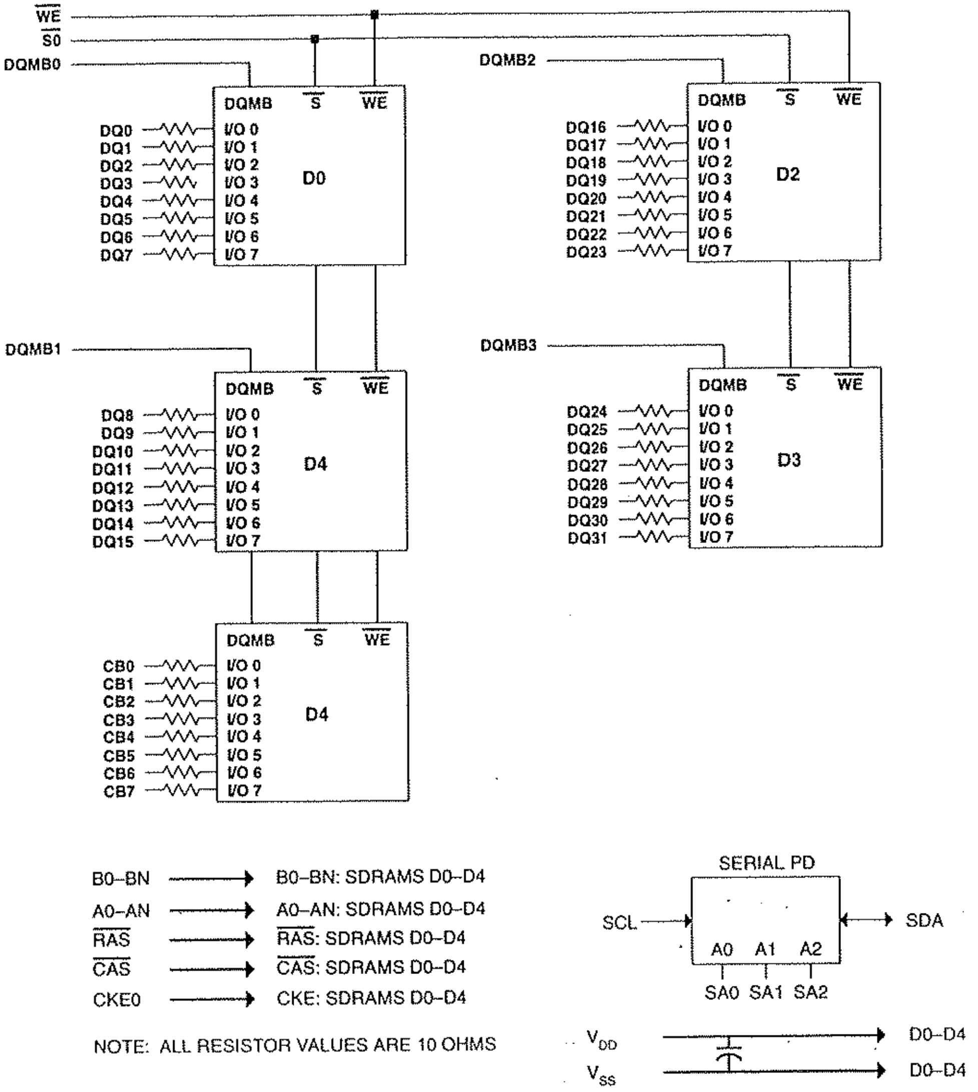


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS 5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8-T
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs

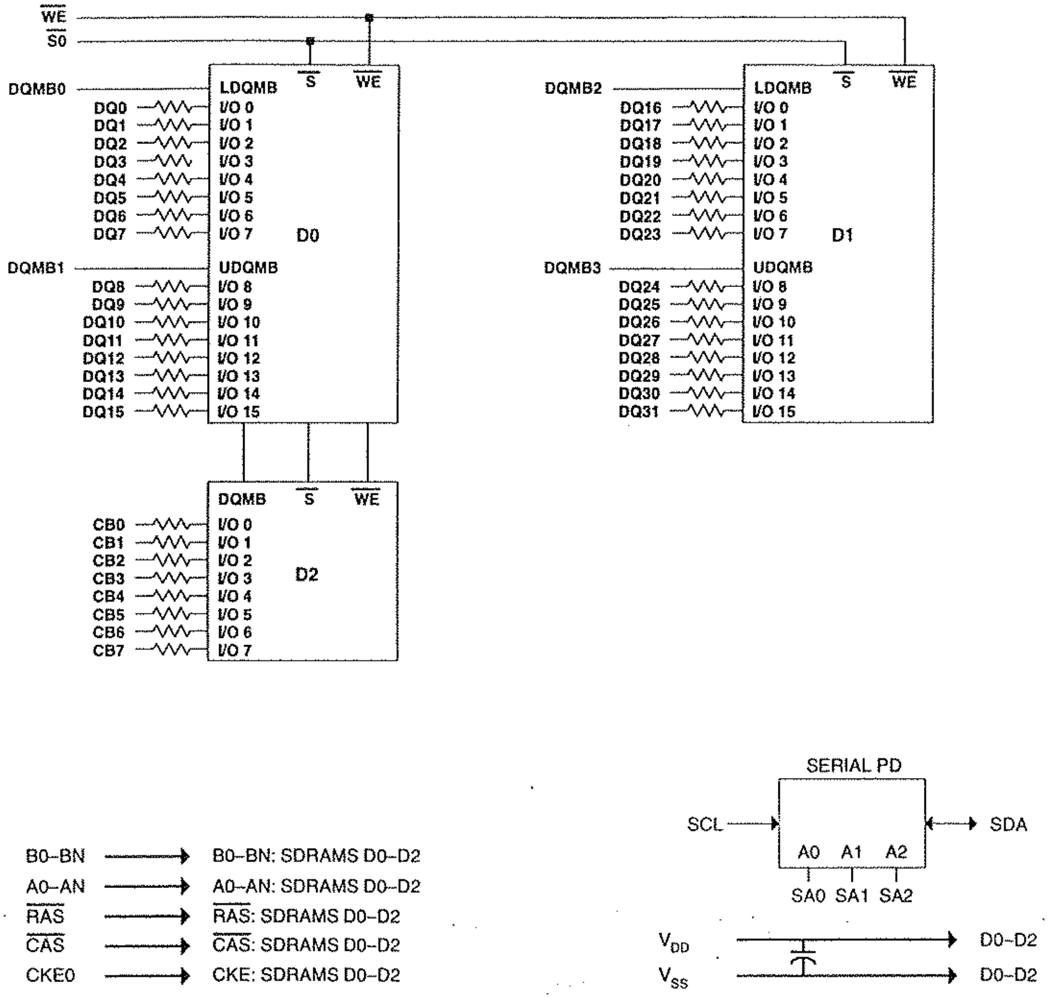


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–U
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs

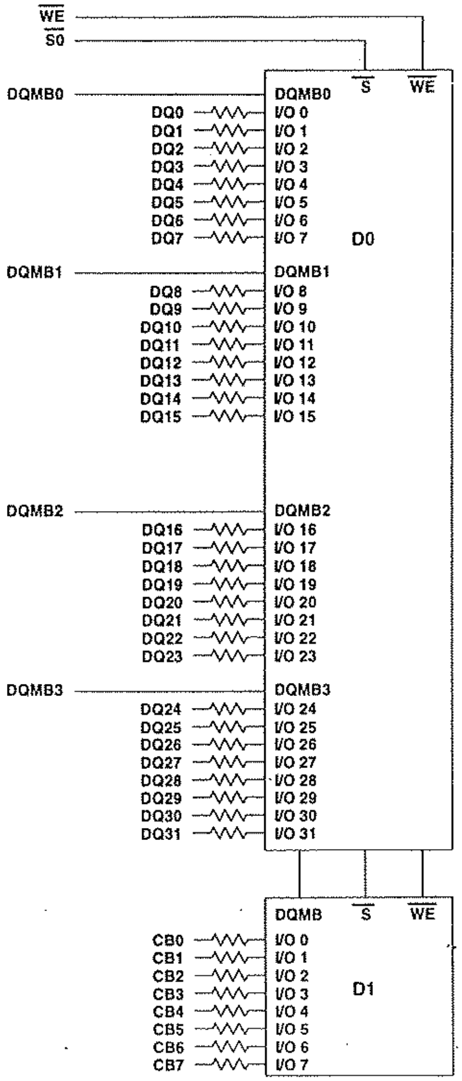


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

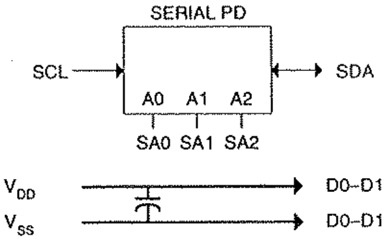
Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–V
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D2
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0–D1



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–W

100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X32 SDRAMs

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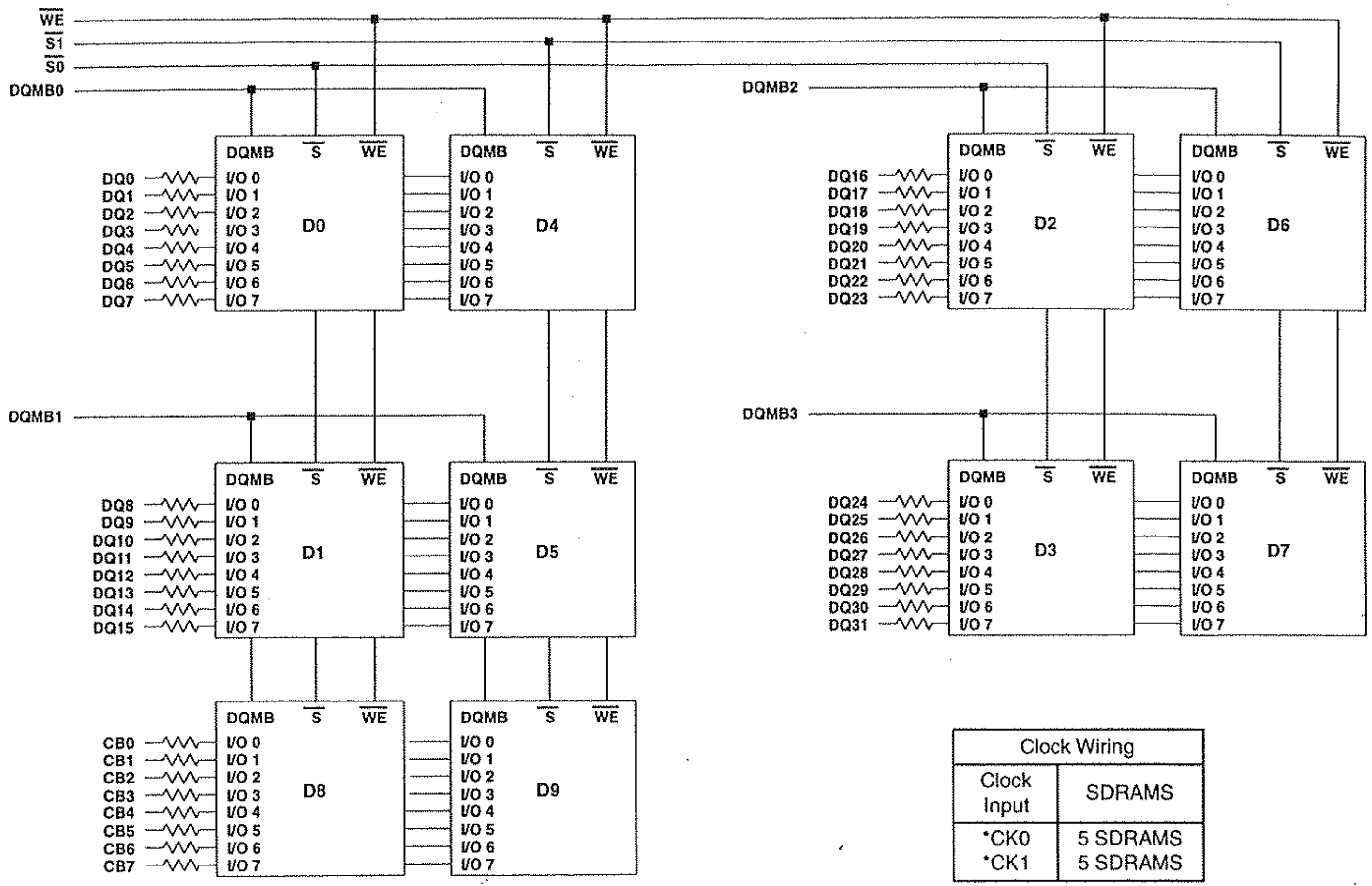


Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

B0–BN → B0–BN: SDRAMS D0–D9
A0–AN → A0–AN: SDRAMS D0–D9
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D9
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D9
CKE0 → CKE: SDRAMS D0–D3, D8
CKE1 → CKE: SDRAMS D4–D7, D9

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

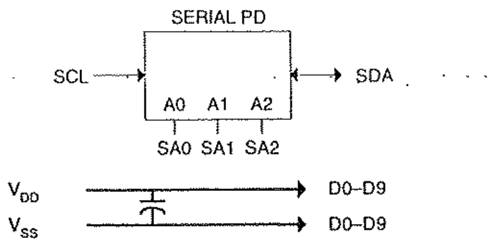
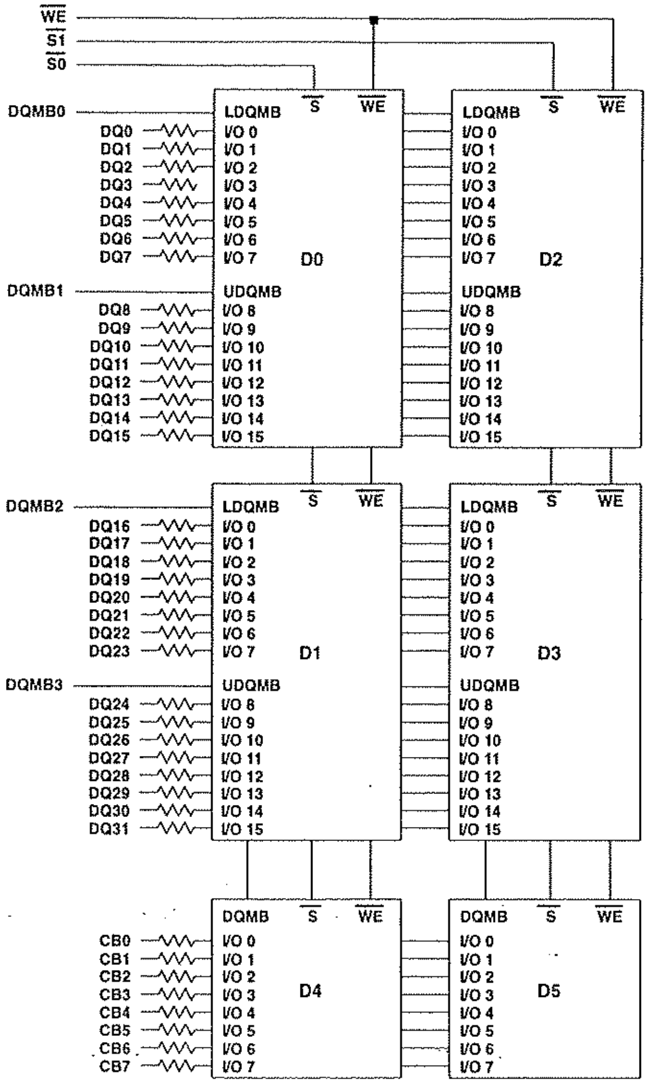
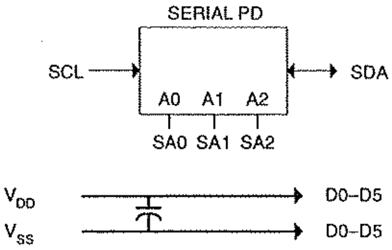


Figure 4.4.8–X
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 SDRAMs

344



B0–BN → B0–BN: SDRAMS D0–D5
A0–AN → A0–AN: SDRAMS D0–D5
$\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMS D0–D5
$\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMS D0–D5
CKE0 → CKE: SDRAMS D0–D1, D4
CKE1 → CKE: SDRAMS D2–D3, D5



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–Y
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X16 SDRAMs

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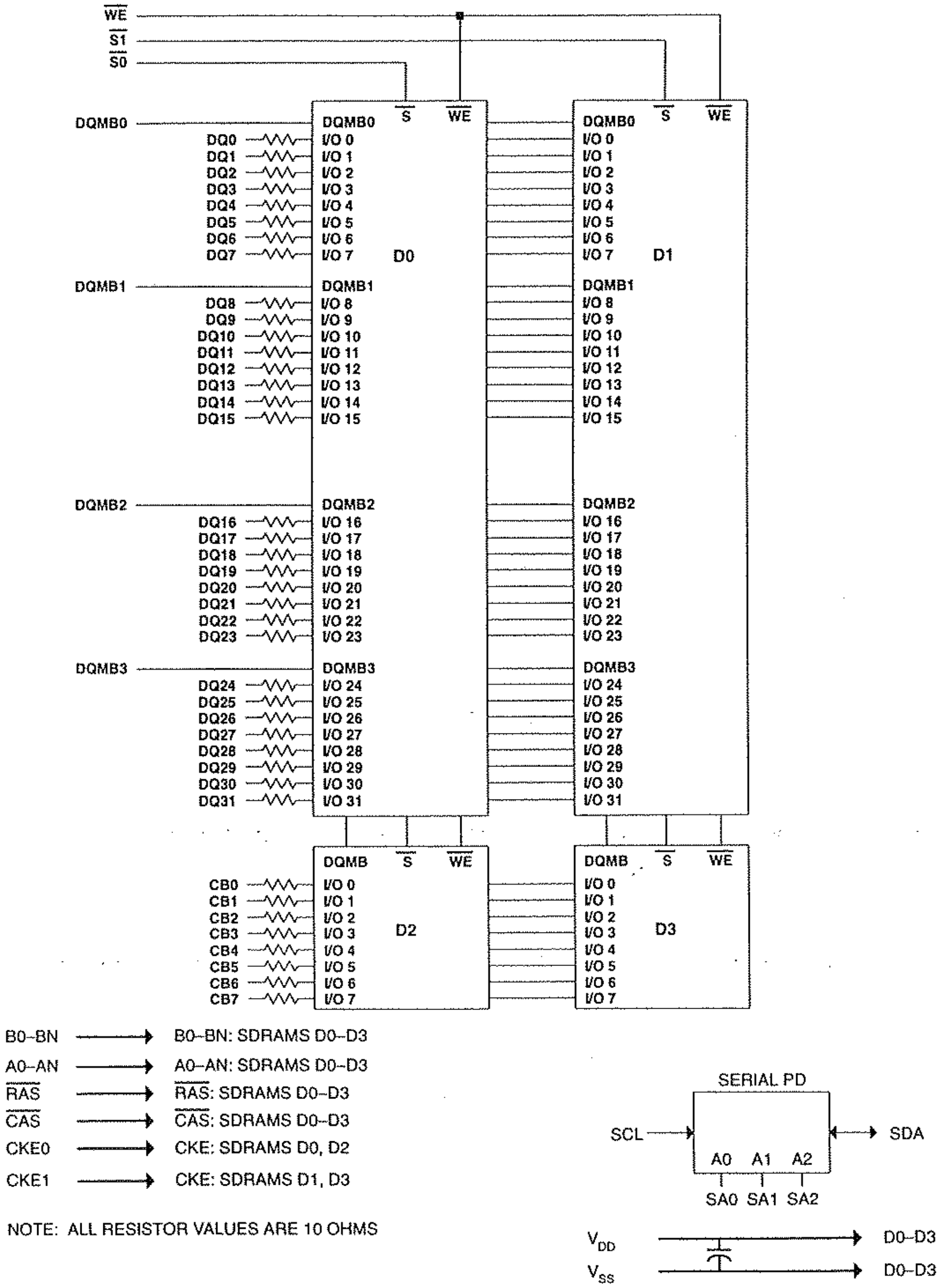


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8-Z
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X32 SDRAMs

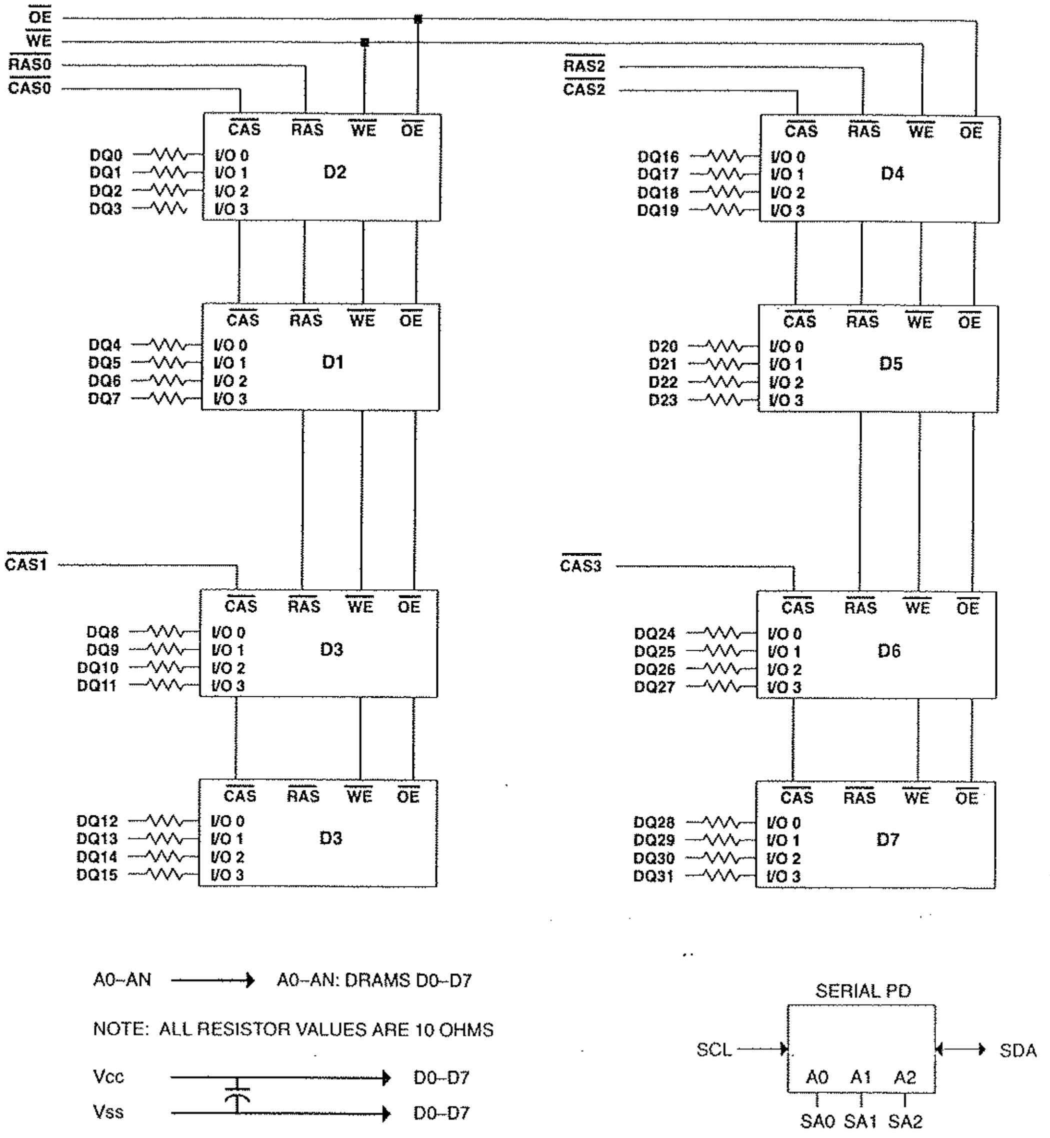


Figure 4.4.8–AA
100 Pin X32 DRAM DIMM, 1 Bank with X4 DRAMs

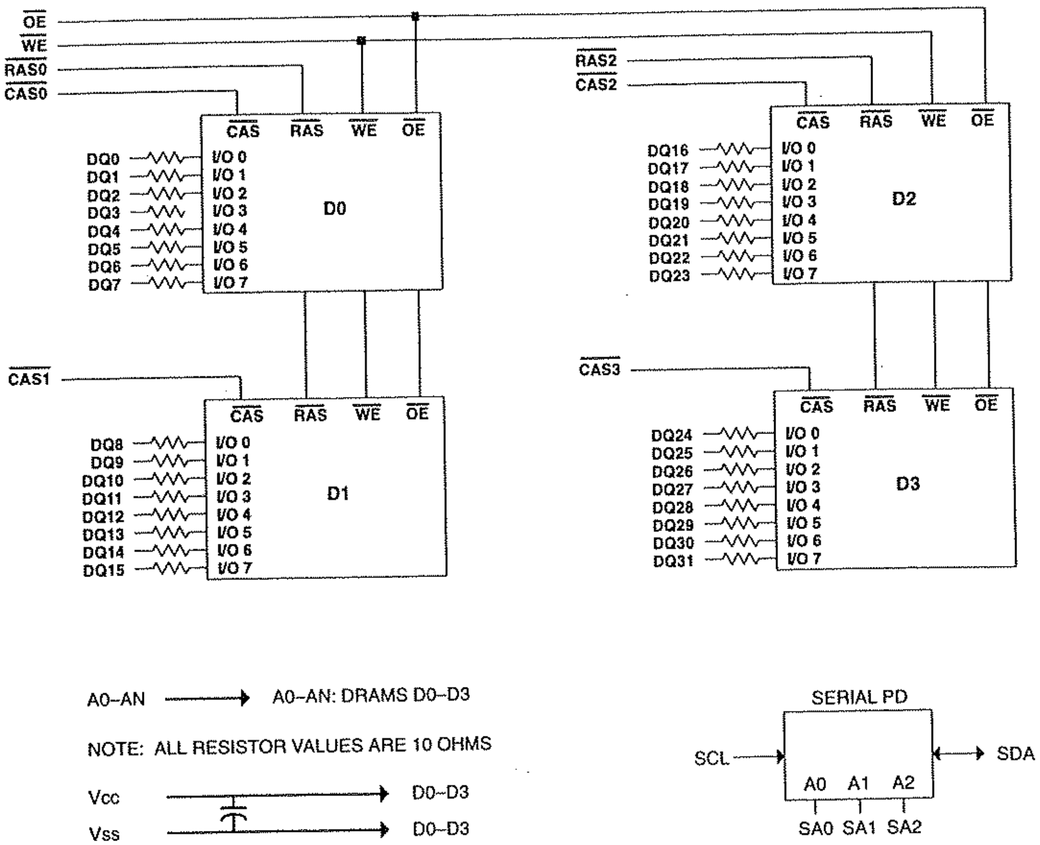


Figure 4.4.8–AB
100 Pin X32 DRAM DIMM, 1 Bank with X8 DRAMs

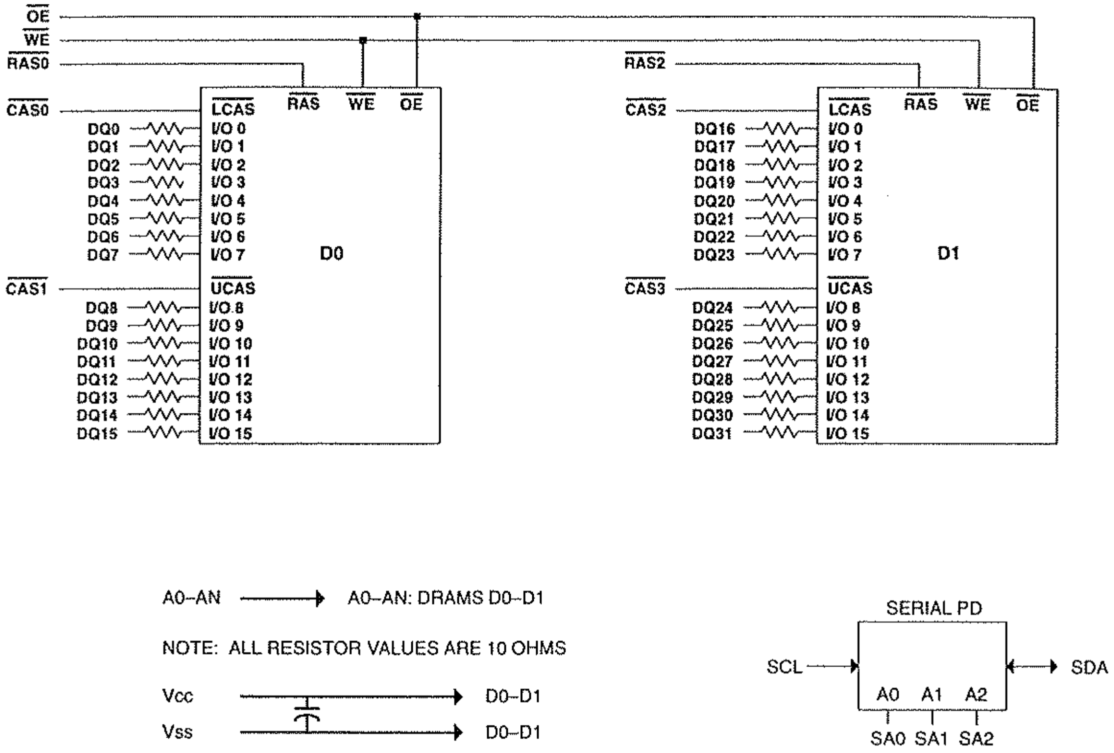


Figure 4.4.8–AC
100 Pin X32 DRAM DIMM, 1 Bank with X16 DRAMs

349

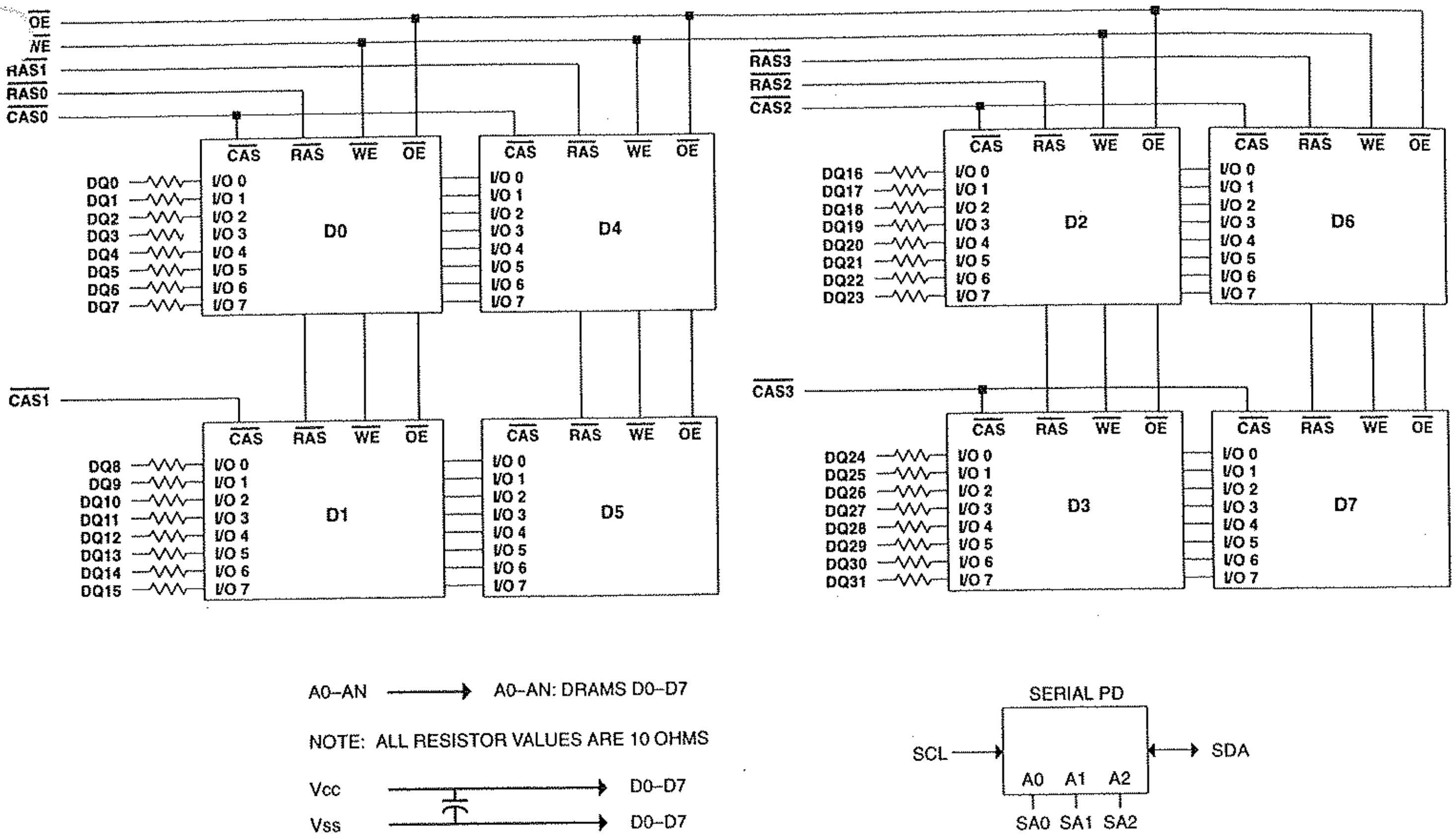
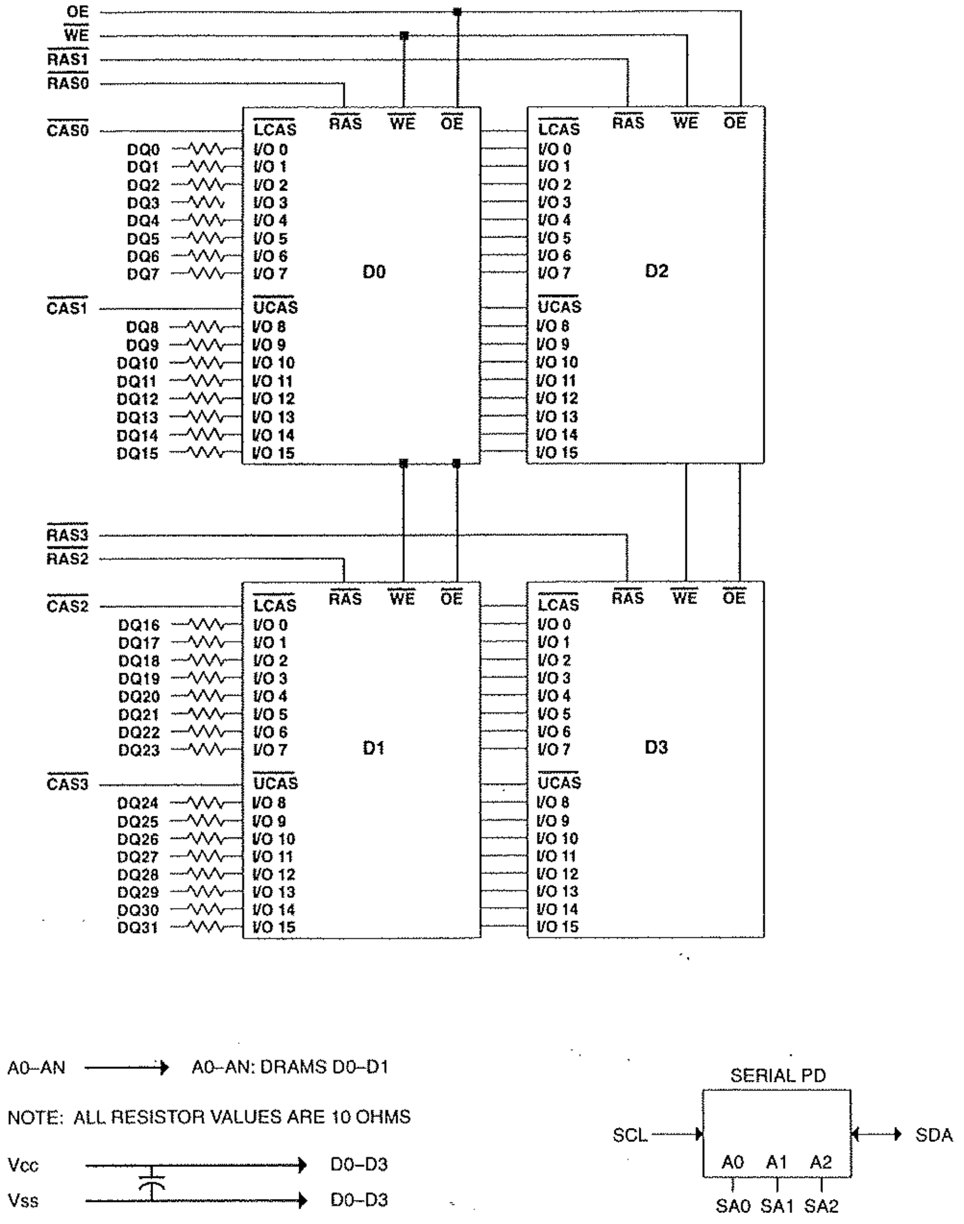


Figure 4.4.8–AD
100 Pin X32 DRAM DIMM, 2 Bank with X8 DRAMs



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Figure 4.4.8–AE
100 Pin X32 DRAM DIMM, 2 Bank with X16 DRAMs

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4.5 Eight Byte Memory Modules

4.5.1 – 168 PIN DRAM DIMM FAMILY

4.5.2 – 200 PIN DRAM DIMM FAMILY

4.5.3 – 168 PIN UNBUFFERED DRAM DIMM FAMILY

4.5.4 – 168 PIN UNBUFFERED SDRAM DIMM FAMILY

4.5.5 – 144 PIN DRAM SO–DIMM FAMILY

4.5.6 – 144 PIN SDRAM SO–DIMM FAMILY

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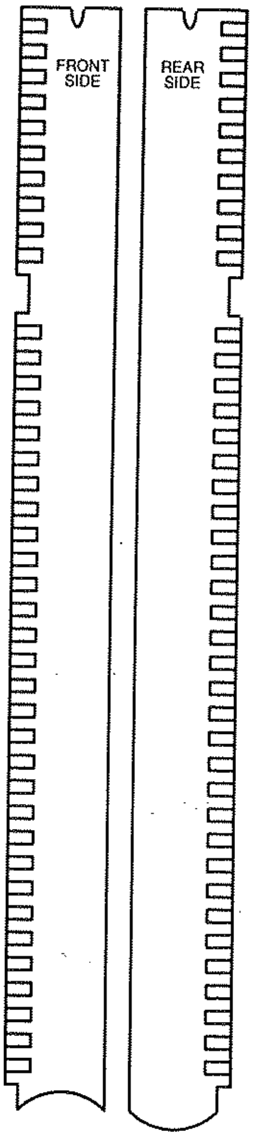
4.5.1 – 168 PIN DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES
CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memories including 2 bank configurations using X4 devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.1–A, 4.5.1–B, & 4.5.1–C
CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4.5.1–D
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.1–E through 4.5.1–AB

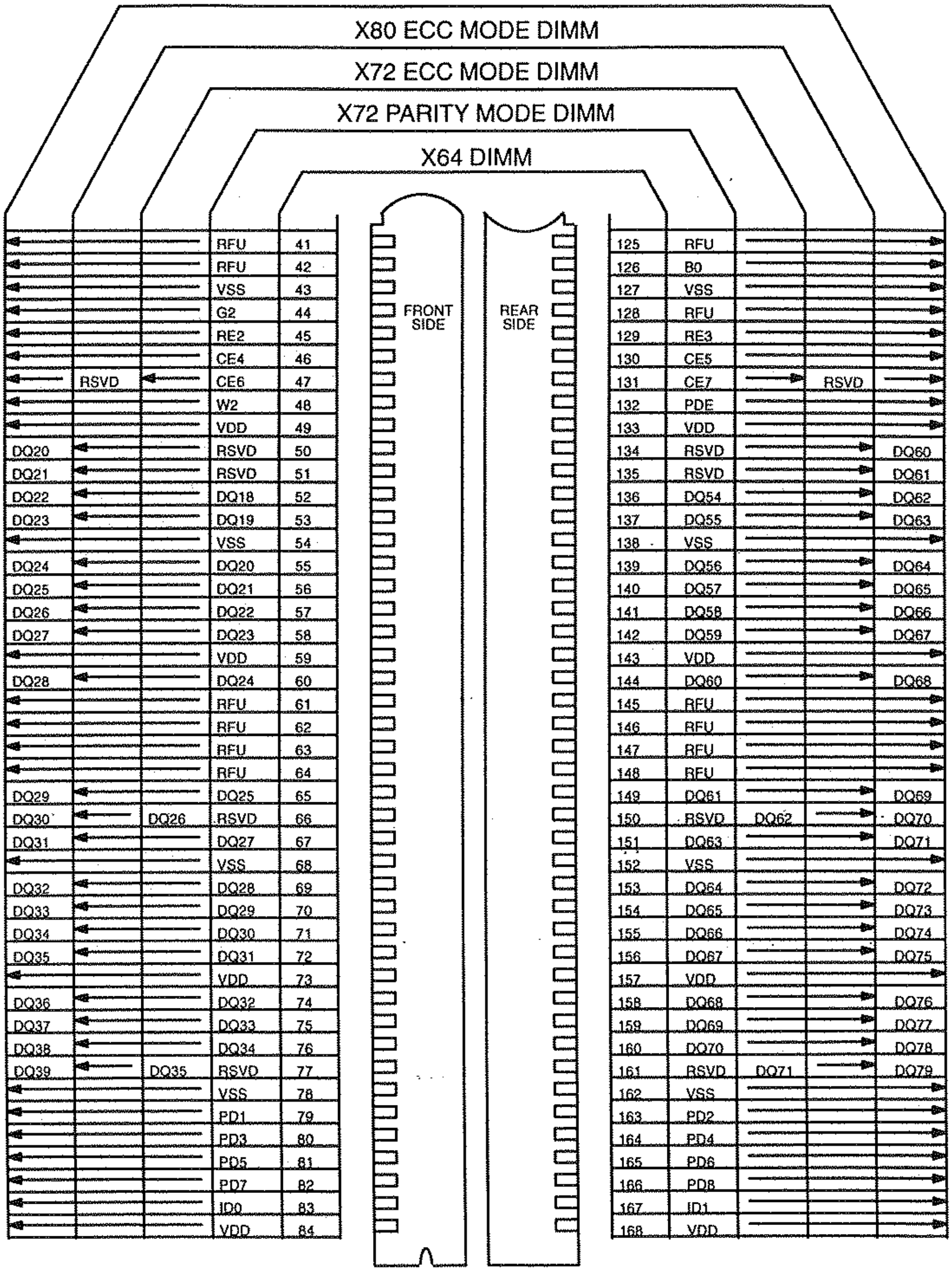
X80 ECC MODE DIMM	X72 ECC MODE DIMM	X72 PARITY MODE DIMM	X64 DIMM	
			VSS	1
			DQ0	2
			DQ1	3
			DQ2	4
			DQ3	5
			VDD	6
			DQ4	7
			DQ5	8
			DQ6	9
			DQ7	10
		DQ8	RSVD	11
			VSS	12
			DQ9	13
			DQ10	14
			DQ11	15
			DQ12	16
			DQ13	17
			VDD	18
			DQ14	19
			DQ15	20
			DQ16	21
		DQ17	RSVD	22
			VSS	23
DQ18			RSVD	24
DQ19			RSVD	25
			VDD	26
			W0	27
			CE0	28
	RSVD		CE2	29
			RE0	30
			G0	31
			VSS	32
			A0	33
			A2	34
			A4	35
			A6	36
			A8	37
			A10	38
			A12	39
			VDD	40



	X64 DIMM	X72 PARITY MODE DIMM	X72 ECC MODE DIMM	X80 ECC MODE DIMM
85	VSS			
86	DQ36			DQ40
87	DQ37			DQ41
88	DQ38			DQ42
89	DQ39			DQ43
90	VDD			
91	DQ40			DQ44
92	DQ41			DQ45
93	DQ42			DQ46
94	DQ43			DQ47
95	RSVD	DQ44		DQ48
96	VSS			
97	DQ45			DQ49
98	DQ46			DQ50
99	DQ47			DQ51
100	DQ48			DQ52
101	DQ49			DQ53
102	VDD			
103	DQ50			DQ54
104	DQ51			DQ55
105	DQ52			DQ56
106	RSVD	DQ53		DQ57
107	VSS			
108	RSVD			DQ58
109	RSVD			DQ59
110	VDD			
111	RFU			
112	CE1			
113	CE3		RSVD	
114	RE1			
115	RFU			
116	VSS			
117	A1			
118	A3			
119	A5			
120	A7			
121	A9			
122	A11			
123	A13			
124	VDD			

Top Half
Top View

Figure 4.5.1–A
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, TOP HALF



X80 ECC MODE DIMM	X72 ECC MODE DIMM	X72 PARITY MODE DIMM	X64 DIMM			X64 DIMM	X72 PARITY MODE DIMM	X72 ECC MODE DIMM	X80 ECC MODE DIMM
←	←	←	RFU	41	125	RFU	→	→	→
←	←	←	RFU	42	126	B0	→	→	→
←	←	←	VSS	43	127	VSS	→	→	→
←	←	←	G2	44	128	RFU	→	→	→
←	←	←	RE2	45	129	RE3	→	→	→
←	←	←	CE4	46	130	CE5	→	→	→
←	RSVD	←	CE6	47	131	CE7	→	RSVD	→
←	←	←	W2	48	132	PDE	→	→	→
←	←	←	VDD	49	133	VDD	→	→	→
DQ20	←	←	RSVD	50	134	RSVD	→	→	DQ60
DQ21	←	←	RSVD	51	135	RSVD	→	→	DQ61
DQ22	←	←	DQ18	52	136	DQ54	→	→	DQ62
DQ23	←	←	DQ19	53	137	DQ55	→	→	DQ63
←	←	←	VSS	54	138	VSS	→	→	→
DQ24	←	←	DQ20	55	139	DQ56	→	→	DQ64
DQ25	←	←	DQ21	56	140	DQ57	→	→	DQ65
DQ26	←	←	DQ22	57	141	DQ58	→	→	DQ66
DQ27	←	←	DQ23	58	142	DQ59	→	→	DQ67
←	←	←	VDD	59	143	VDD	→	→	→
DQ28	←	←	DQ24	60	144	DQ60	→	→	DQ68
←	←	←	RFU	61	145	RFU	→	→	→
←	←	←	RFU	62	146	RFU	→	→	→
←	←	←	RFU	63	147	RFU	→	→	→
←	←	←	RFU	64	148	RFU	→	→	→
DQ29	←	←	DQ25	65	149	DQ61	→	→	DQ69
DQ30	←	DQ26	RSVD	66	150	RSVD	DQ62	→	DQ70
DQ31	←	←	DQ27	67	151	DQ63	→	→	DQ71
←	←	←	VSS	68	152	VSS	→	→	→
DQ32	←	←	DQ28	69	153	DQ64	→	→	DQ72
DQ33	←	←	DQ29	70	154	DQ65	→	→	DQ73
DQ34	←	←	DQ30	71	155	DQ66	→	→	DQ74
DQ35	←	←	DQ31	72	156	DQ67	→	→	DQ75
←	←	←	VDD	73	157	VDD	→	→	→
DQ36	←	←	DQ32	74	158	DQ68	→	→	DQ76
DQ37	←	←	DQ33	75	159	DQ69	→	→	DQ77
DQ38	←	←	DQ34	76	160	DQ70	→	→	DQ78
DQ39	←	DQ35	RSVD	77	161	RSVD	DQ71	→	DQ79
←	←	←	VSS	78	162	VSS	→	→	→
←	←	←	PD1	79	163	PD2	→	→	→
←	←	←	PD3	80	164	PD4	→	→	→
←	←	←	PD5	81	165	PD6	→	→	→
←	←	←	PD7	82	166	PD8	→	→	→
←	←	←	ID0	83	167	ID1	→	→	→
←	←	←	VDD	84	168	VDD	→	→	→

Figure 4.5.1–B
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

PD 4	PD 3	PD 2	PD 1	DIMM CONFIGURATION (Parity, ECC)	# BANKS	DRAM CONFIGURATION	DRAM ROW ADDR	DRAM COL. ADDR	Av. REFRESH INTERVAL NORMAL (µS)	SLOW
0	0	0	0	256K X 64/72, 72	1	256K X 16/18	9	9	15.6	125
0	0	0	1	512K X 64/72, 72	2	256K X 16/18	9	9	15.6	125
0	0	1	0	512K X 64/72, 72/80	1	512K X 8/9	10	9	15.6	125
0	0	1	1	1M X 64/72, 72/80	2	512K X 8/9	10	9	15.6	125
0	1	0	0	1M X 64/72, 72/80	1	1M X 4/16/18	10	10#	15.6	125
0	1	0	1	2M X 64/72, 72/80	2	1M X 4/16/18	10	10#	15.6	125
0	1	1	0	1M X 64/72, 72	1	1M X 16/18	12	8	15.6	31.2
1	0	0	0	2M X 64/72, 72	2	1M X 16/18	12	8	15.6	31.2
1	0	0	1	2M X 64/72, 72/80	1	2M X 8	11	10	15.6	62.5
1	0	1	0	4M X 64/72, 72/80	2	2M X 8	11	10	15.6	62.5
1	0	1	1	4M X 72	1	4M X 1/4	12**	11**	15.6	31.2
1	0	1	1	4M X 64, 72/80	1	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	0	8M X 64/72, 72/80	2	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	1	8M X 64/72, 72/80	1	8M X 8	12	11	15.6	31.2
1	1	1	0	16M X 64/72, 72/80	2	8M X 8	12	11	15.6	31.2
1	1	1	1	16M X 64/72, 72/80	1	16M X 4	13/12	11/12	15.6	TBD/31.2
0	0	0	0	16M X 64/72, 72	1	16M X 16	13/12	11/12	15.6	TBD/31.2
0	0	0	1	32M X 64/72, 72/80	2	16M X 4/16	13/12	11/12	15.6	TBD/31.2
0	0	1	0	32M X 64/72, 72/80	1	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	0	1	1	64M X 64/72, 72/80	2	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	1	0	0	64M X 64/72, 72/80	1	64M X 4	14/13	12/13	7.8/15.6	TBD*
0	1	1	1	Expansion						

Note 1) * These modules using 256M devices are for reference only and will be further defined in the future.
Note 2) 1 = Logic high ; 0 = Logic low; In Table Information.
Note 3) ** This addressing includes a redundant address to allow mixing of 12/10(X4) and 11/11(X1) DRAMs
Note 4) # 1M X 16/18 DRAMS with 10/10 addressing may dissipate excessive power in many applications. Care must be taken to ensure device thermal limits are not exceeded. 12/8 addressing is provided as a lower power option.
PD Note: PD & ID terminals must each be pulled up through a resistor to VDD at the next higher level assembly. PDs will either be open or driven to VOH or driven to VOL via on–board buffer circuits.
ID Note: IDs will either be open (NC) or connected directly to VSS without a buffer.

	PD7	PD6
SPEED (tRAC)	82	165
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1

PD SPEED TABLE

	PD8	ID0
CONFIGURATION	166	83
X64	1	0
X72 PARITY	1	1
X72 ECC	0	0
X80 ECC	0	1

DATA CONFIGURATION

	ID1
REFRESH MODE	167
NORMAL	0
SELF–REFRESH	1

REFRESH MODE

DATA ACCESS MODE	PD5
	81
FAST PAGE	0
FP W/EDO	1

EDO DETECTION

Figure 4.5.1–C

168 PIN, 64, 72, or 80 BIT DIMM PRESENCE DETECT & CONFIGURATION TABLES

64, 72, & 80 BIT DRAM DIMM CAPACITY IN M BYTE																				
Memory Device / DIMM Configuration	4M DRAM					16M DRAM					64M DRAM					256M DRAM				
	256K		512K		1M	1M		2M		4M	4M		8M		16M	16M		32M		64M
	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4
256K X 64		4																		
256K X 72	4																			
256K X 72 (ECC)	4																			
256K X 80 (ECC)																				
512 X 64		8		8																
512K X 72	8		8																	
512K X 72 (ECC)	8		8	9																
512K X 80 (ECC)				10																
1M X 64				16	16		4													
1M X 72			16		18	4														
1M X 72 (ECC)			16	18	18	4														
1M X 80 (ECC)				20	20															
2M X 64							8		8											
2M X 72						8		8												
2M X 72 (ECC)						8		8	9											
2M X 80 (ECC)									10											
4M X 64									16	16		4								
4M X 72								16		18	4									
4M X 72 (ECC)								16	18	18	4									
4M X 80 (ECC)									20	20										
8M X 64												8		8						
8M X 72											8		8							
8M X 72 (ECC)											8		8	9						
8M X 80 (ECC)														10						
16M X 64														16	16		4			
16M X 72													16		18	4				
16M X 72 (ECC)													16	18	18	4				
16M X 80 (ECC)														20	20					
32M X 64																	8		8	
32M X 72																8		8		
32M X 72 (ECC)																8		8	9	
32M X 80 (ECC)																			10	
64M X 64																			16	16
64M X 72																		16		18
64M X 72 (ECC)																		16	18	18
64M X 80 (ECC)																			20	20

Figure 4.5.1–D
168 PIN, 64, 72, & 80 BIT DRAM DIMM Capacity Table

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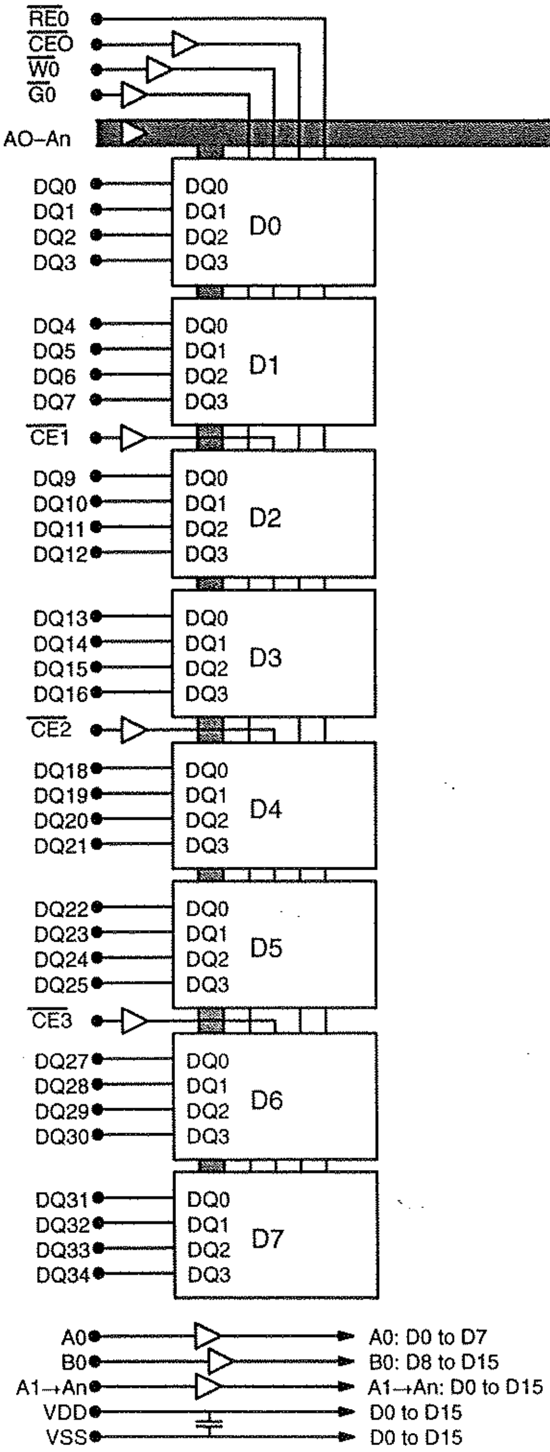

Figure 4.5.1–E
168 PIN, X64 DRAM DIMM, 1 bank with X4 DRAMs

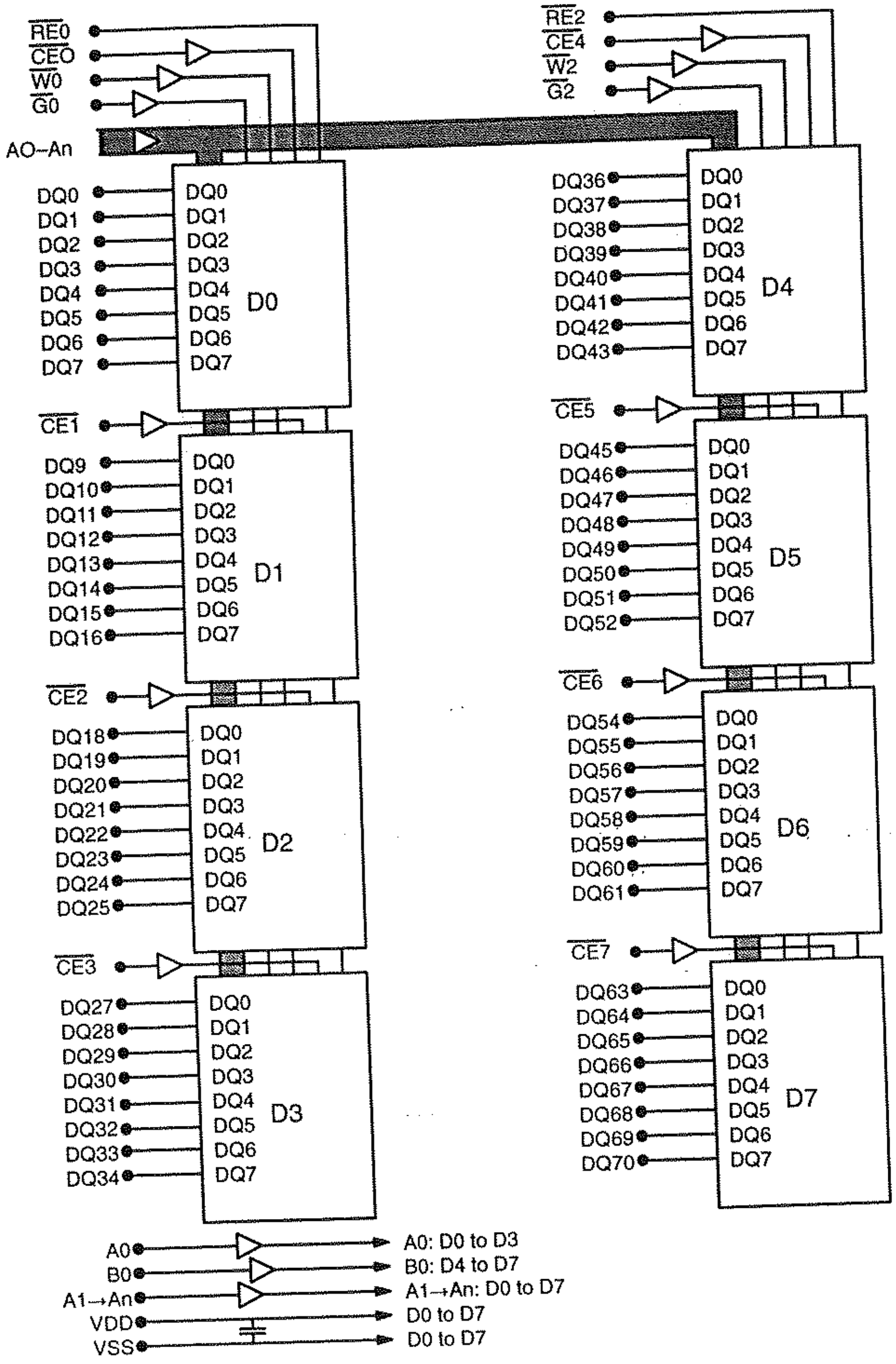

Figure 4.5.1–F
168 PIN, X64 DRAM DIMM, 1 bank with X8 DRAMs

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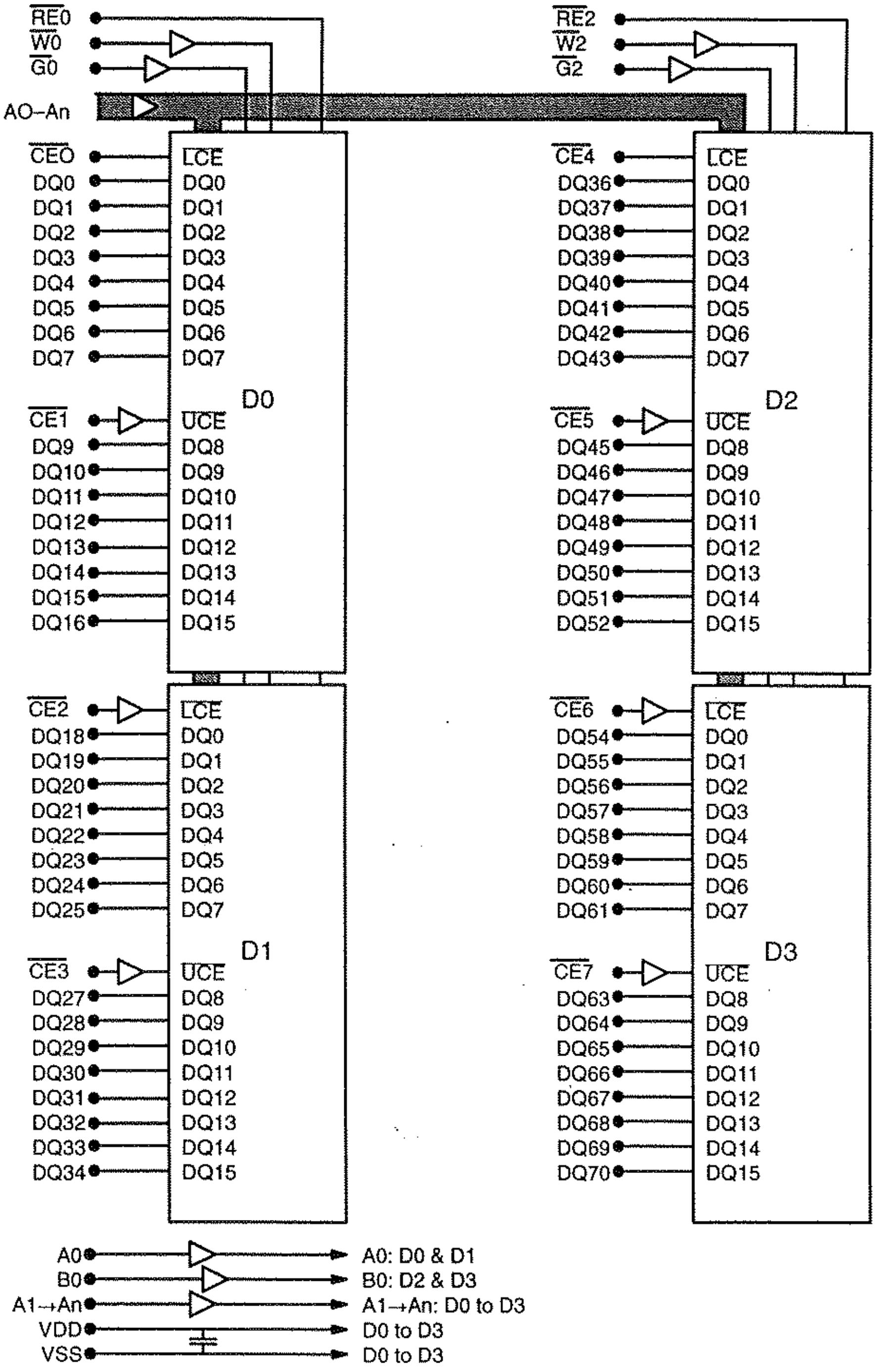

Figure 4.5.1–G
168 PIN, X64 DRAM DIMM, 1 bank with X16 DRAMs

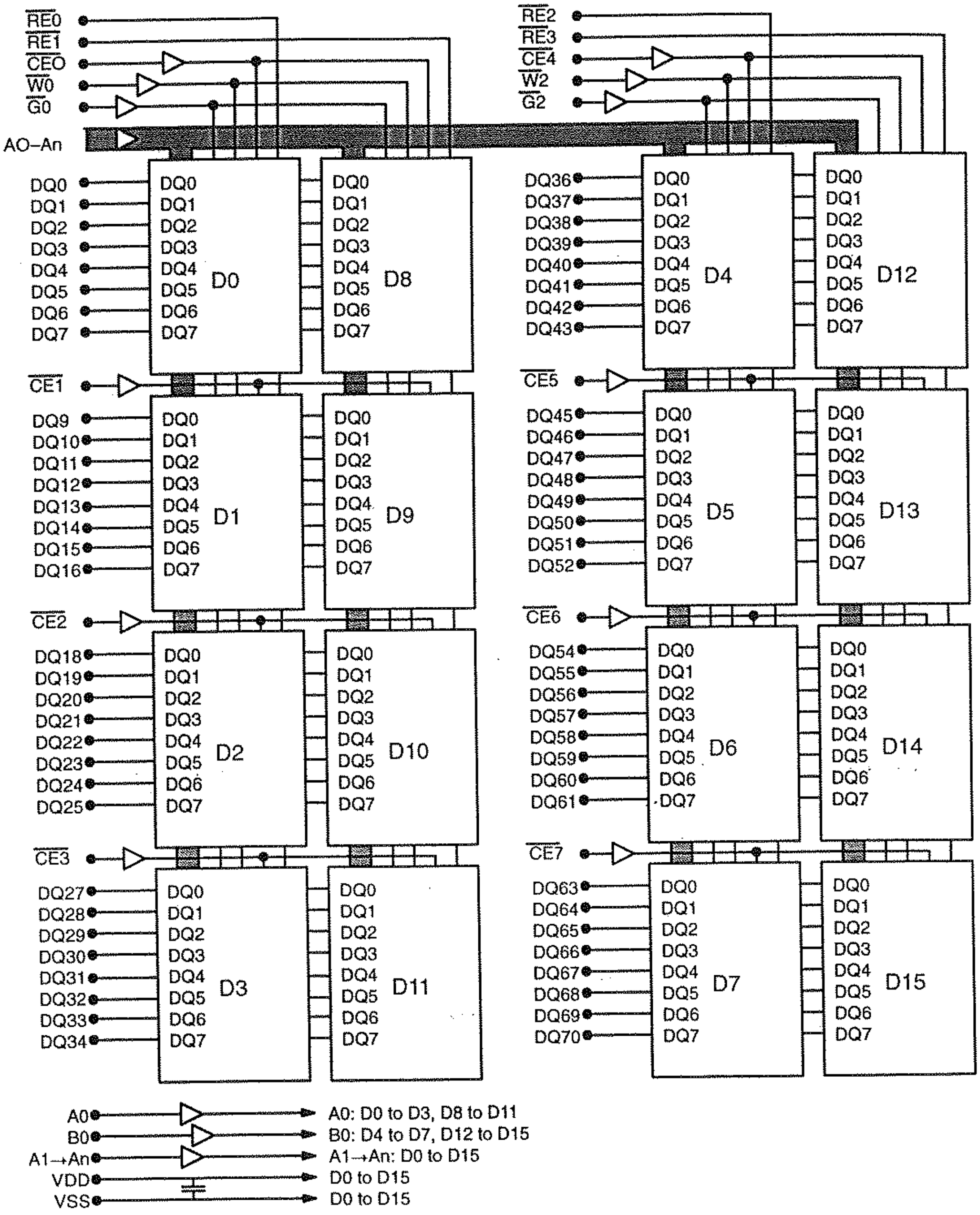

Figure 4.5.1–H
168 PIN, X64 DRAM DIMM, 2 banks with X8 DRAMs

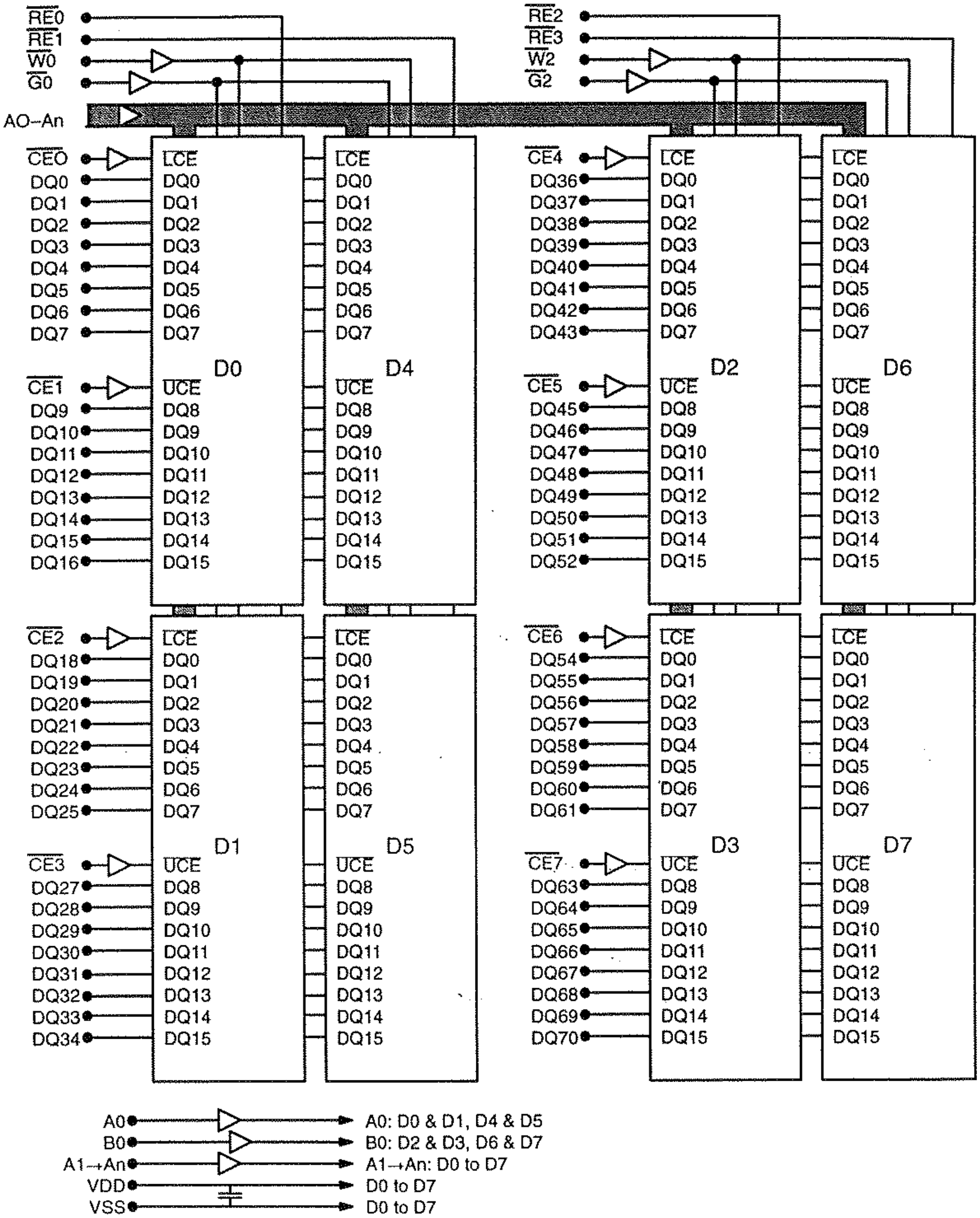

Figure 4.5.1–I
168 PIN, X64 DRAM DIMM, 2 banks with X16 DRAMs

Release 4c7

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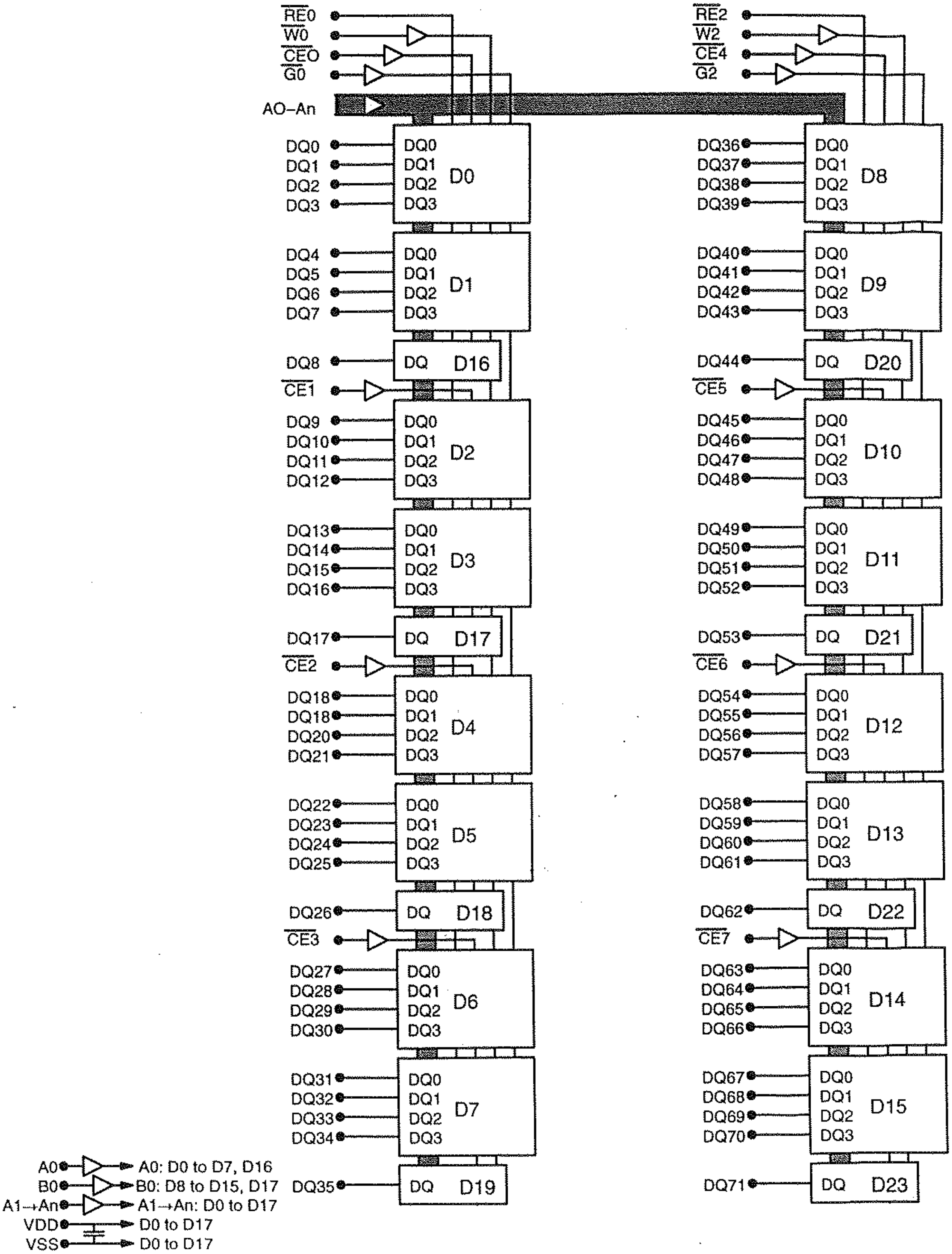

Figure 4.5.1–J

168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X1 DRAMs

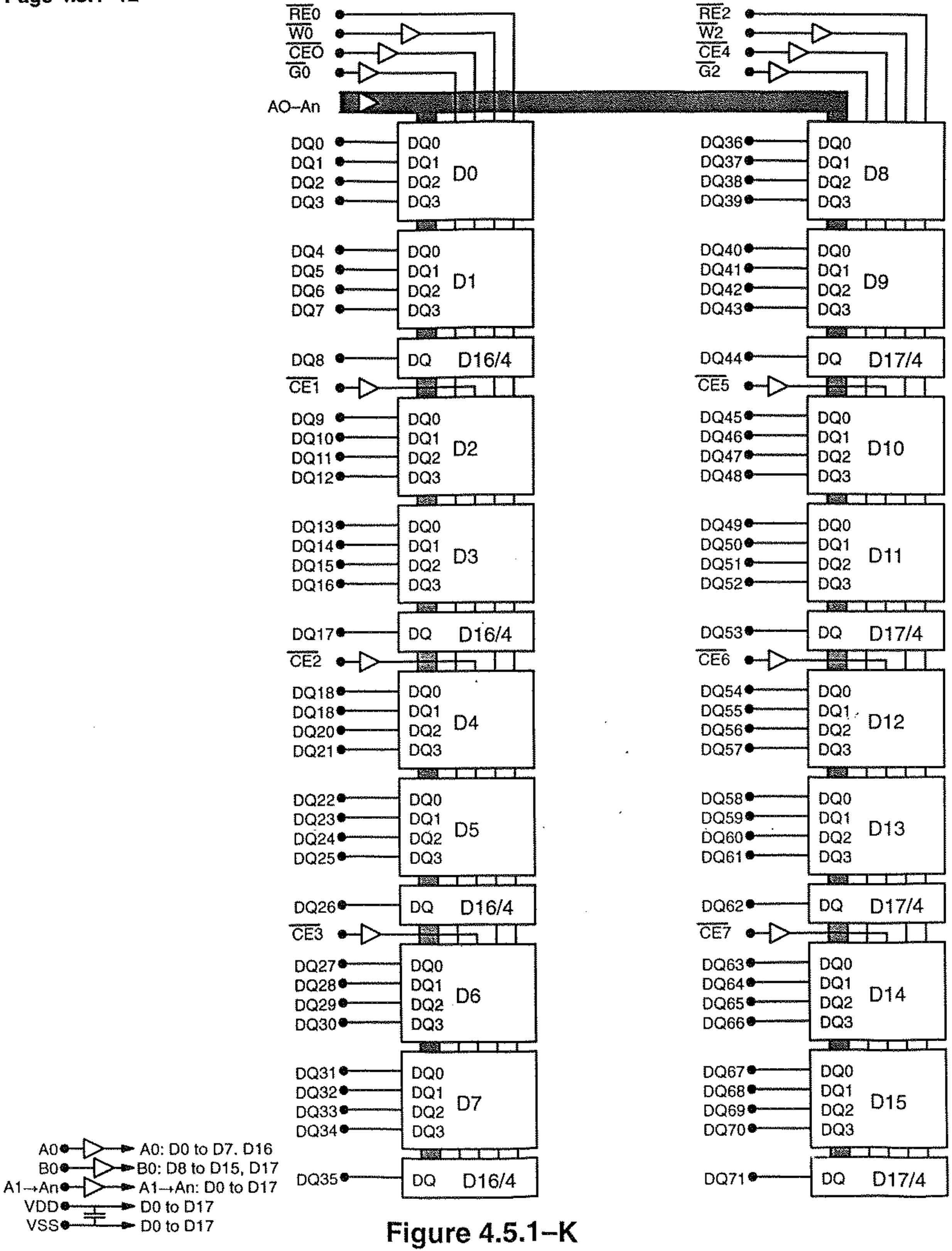

Figure 4.5.1–K

168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X4 W/4 $\overline{\text{CE}}$ DRAMs

Release 4c7

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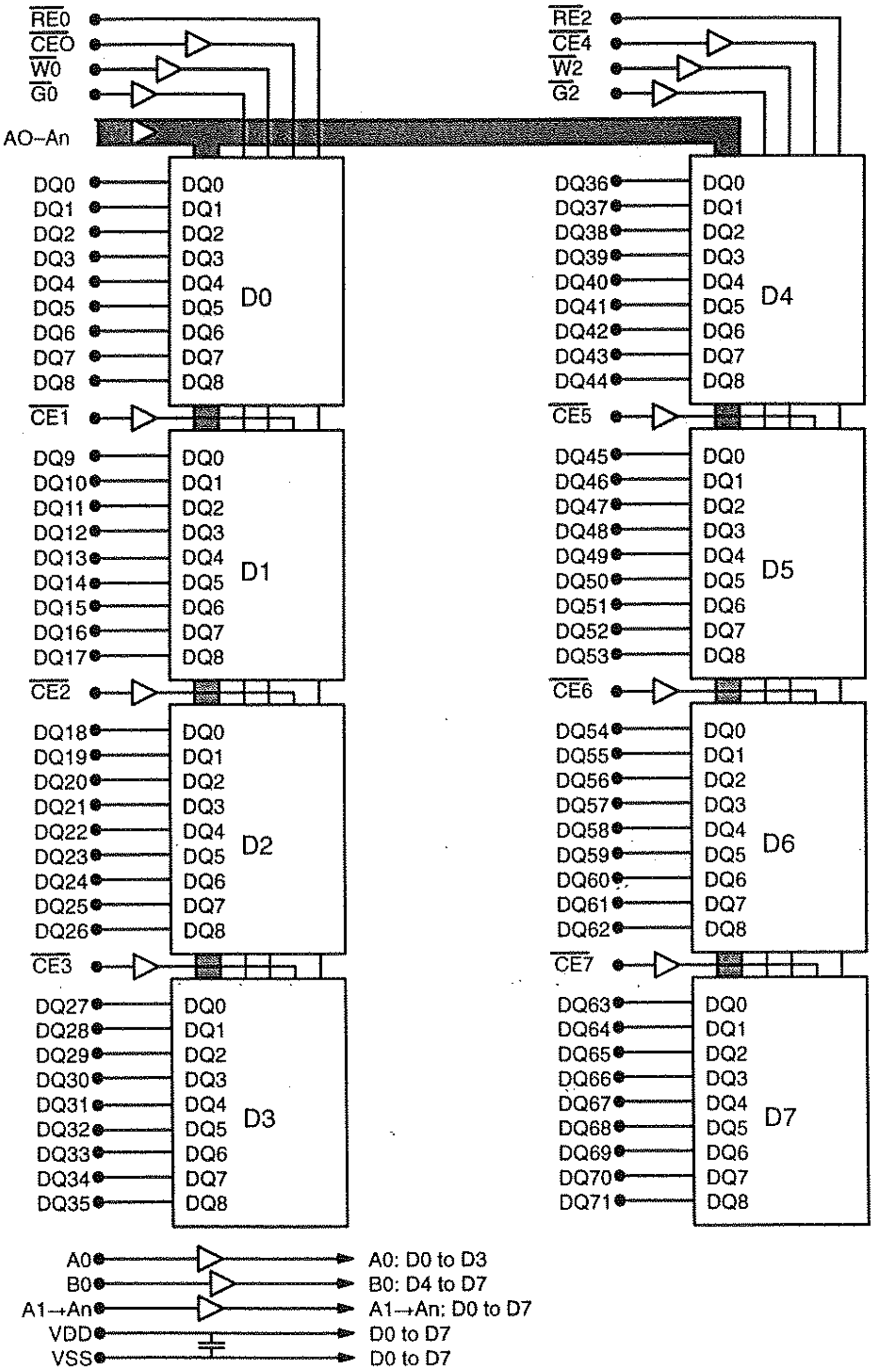


Figure 4.5.1-L
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X9 DRAMs

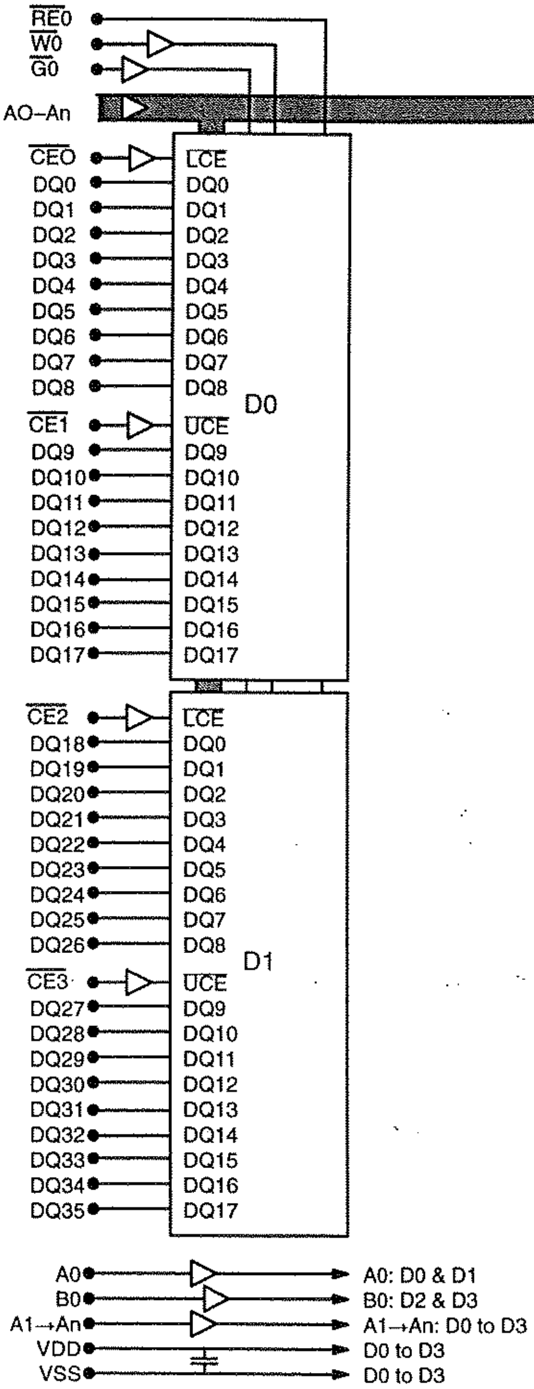


Figure 4.5.1–M
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X18 DRAMs
Release 4c7

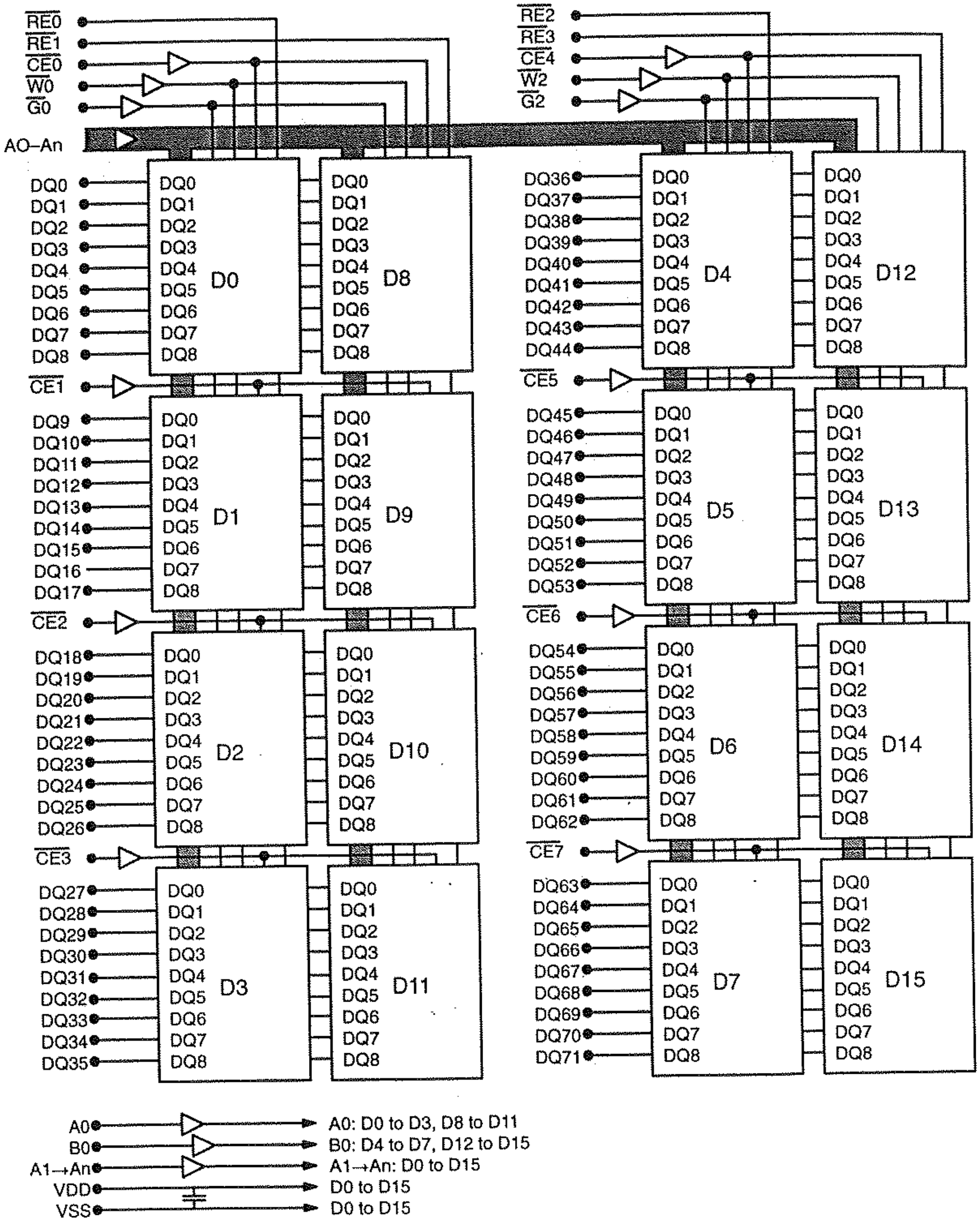


Figure 4.5.1–N
168 PIN, X72 (Parity mode) DRAM DIMM, 2 banks with X9 DRAMs

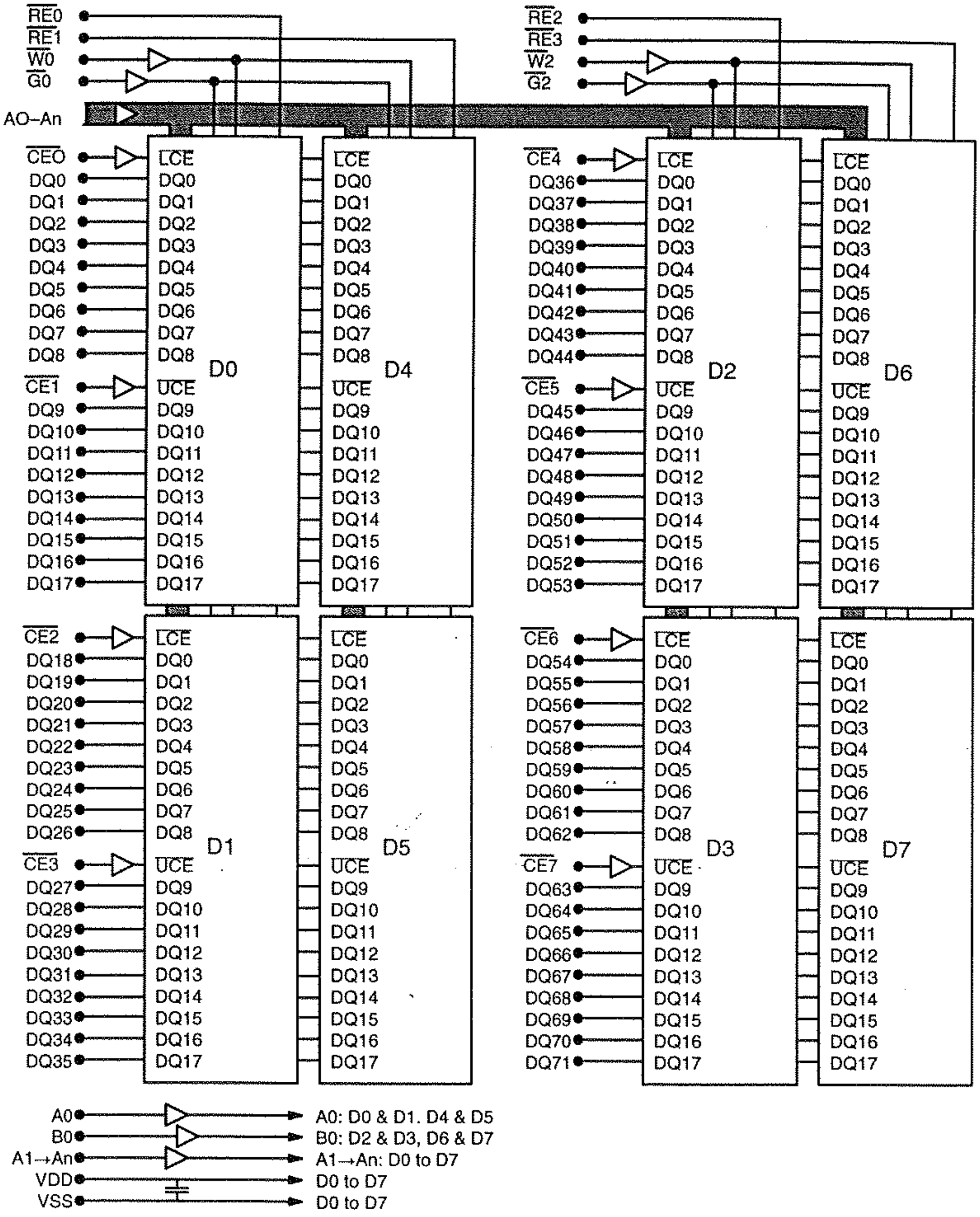


Figure 4.5.1–O
168 PIN, X72 (Parity mode) DRAM DIMM, 2 bank with X18 DRAMs

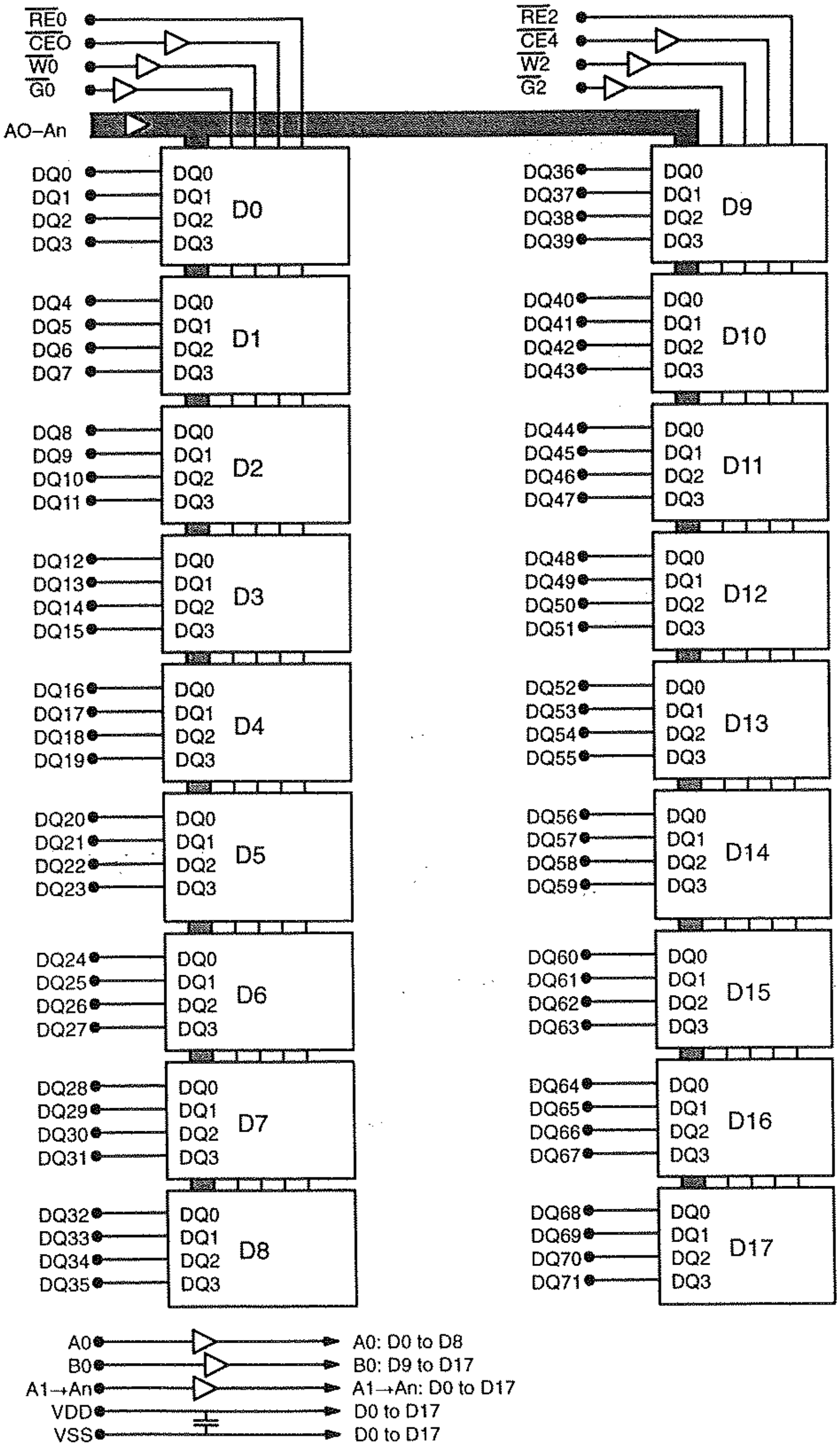
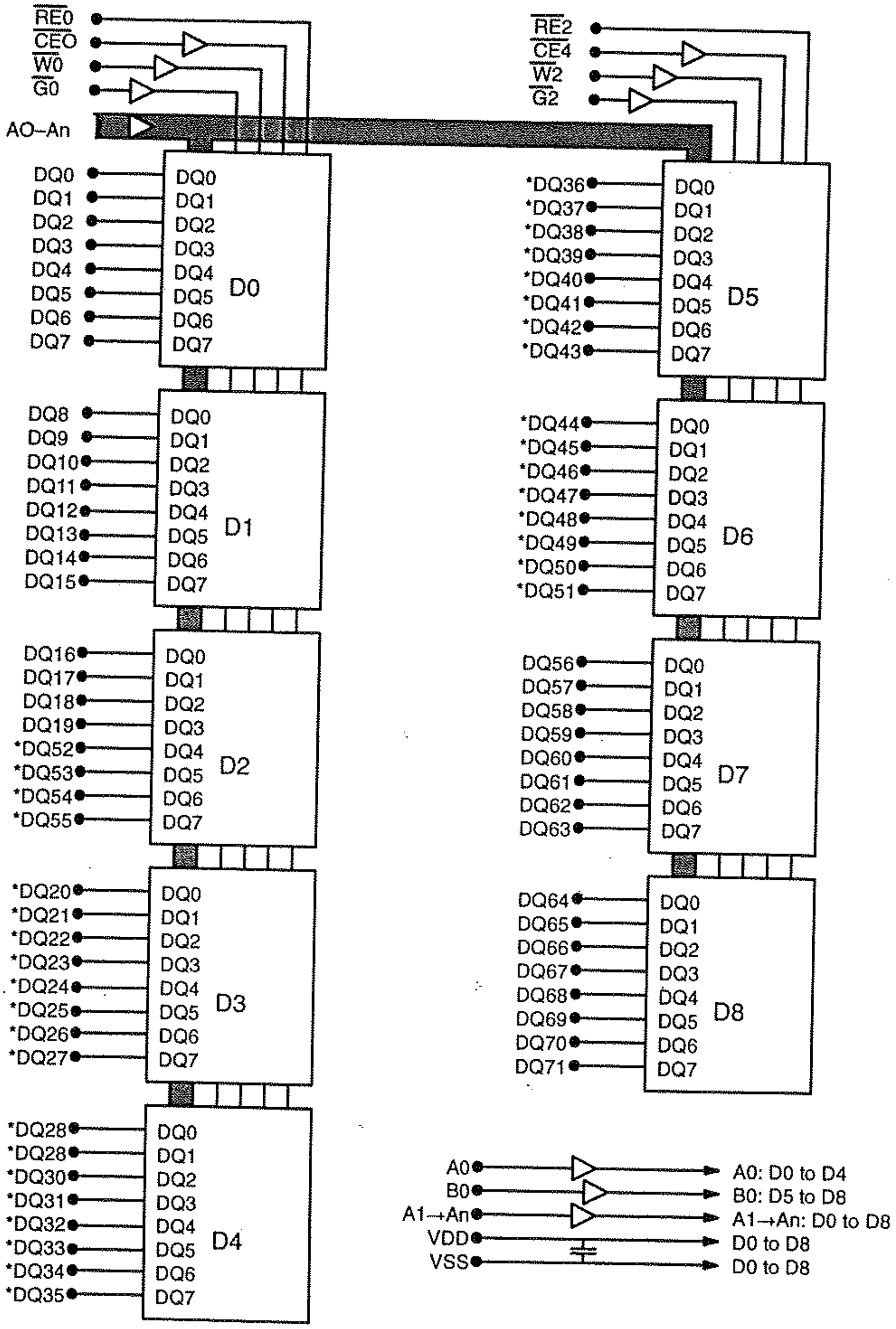


Figure 4.5.1–P

168 PIN, X 72 (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs

169



* Note: The location of data pins DQ–20 through DQ–55 have been changed in Release 7

Figure 4.5.1–Q
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs

Release 4–r7

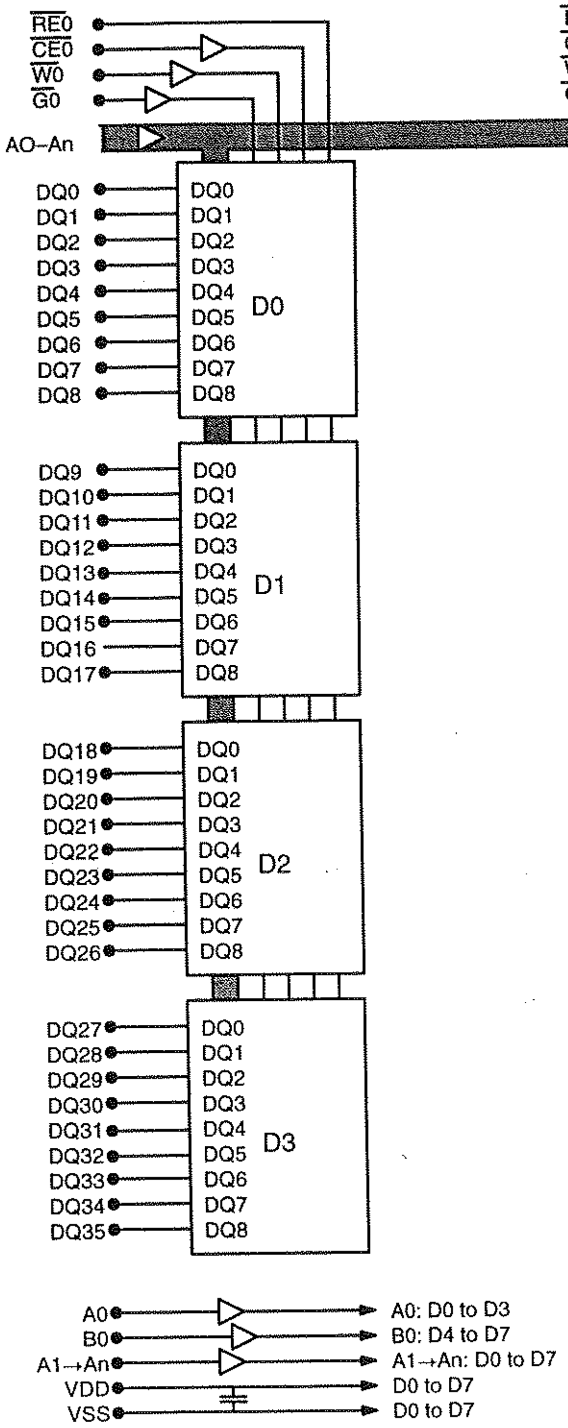


Figure 4.5.1-R

168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X9 DRAMs

Release 4c7

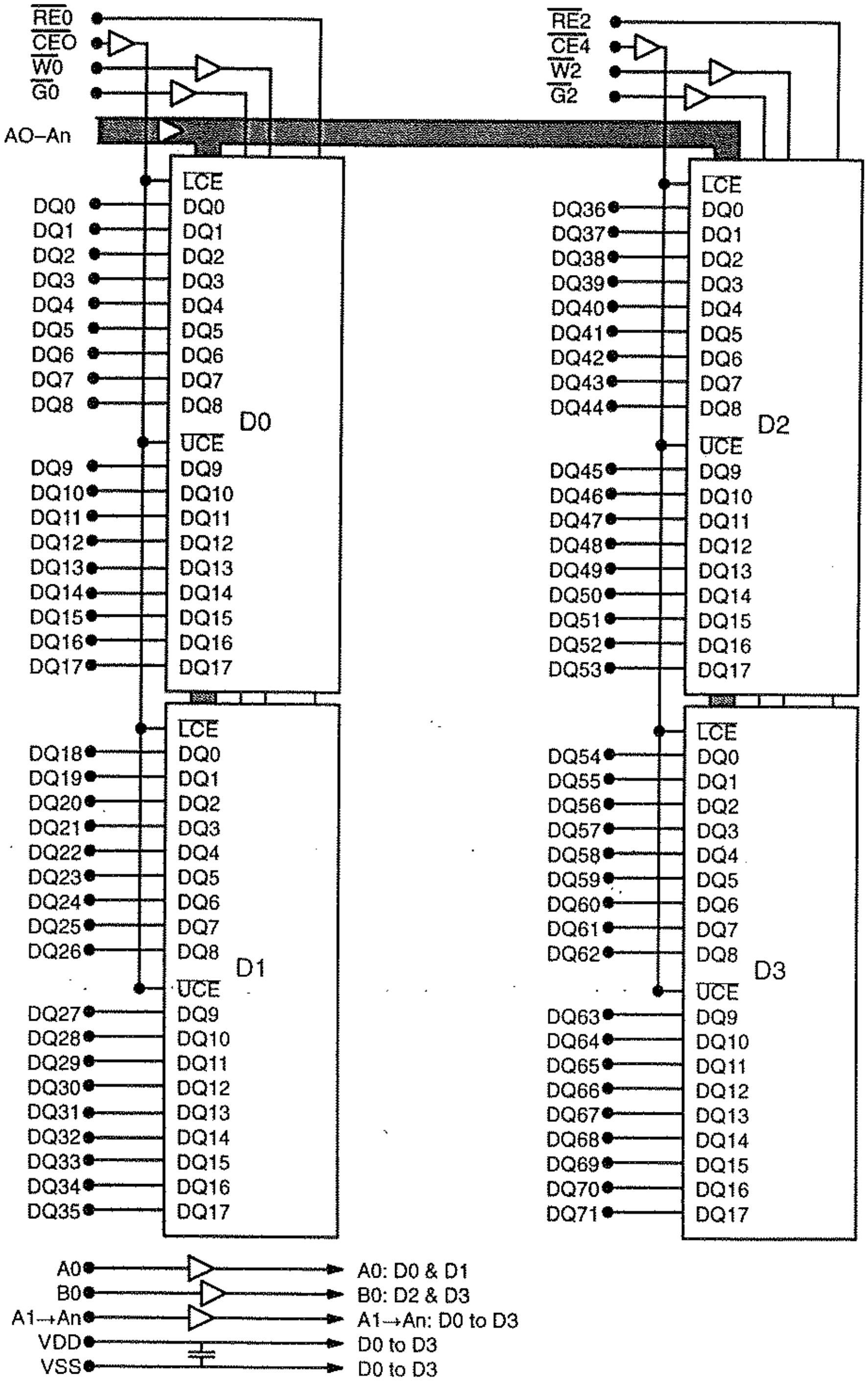


Figure 4.5.1–S
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X18 DRAMs

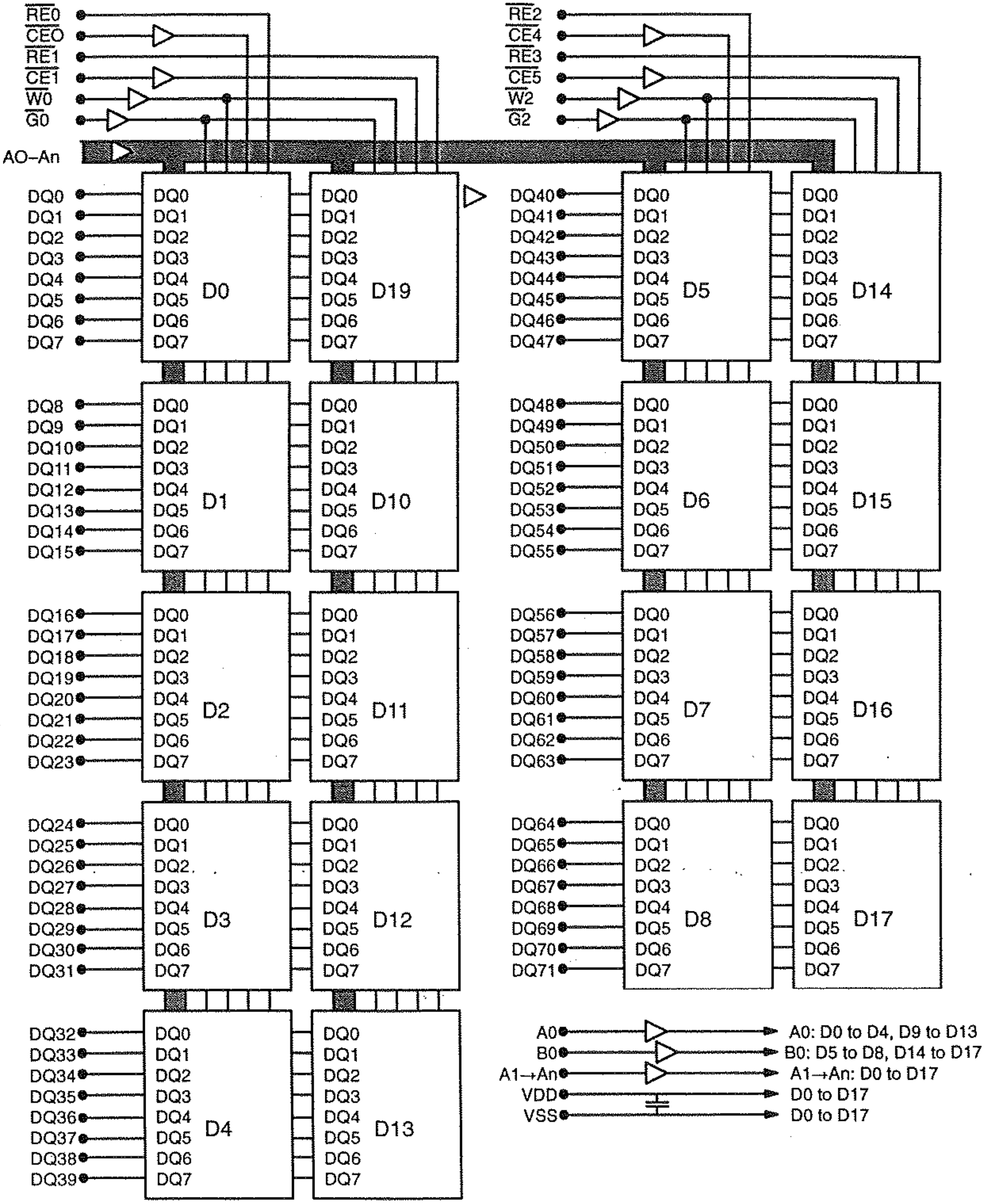


Figure 4.5.1–T

168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs

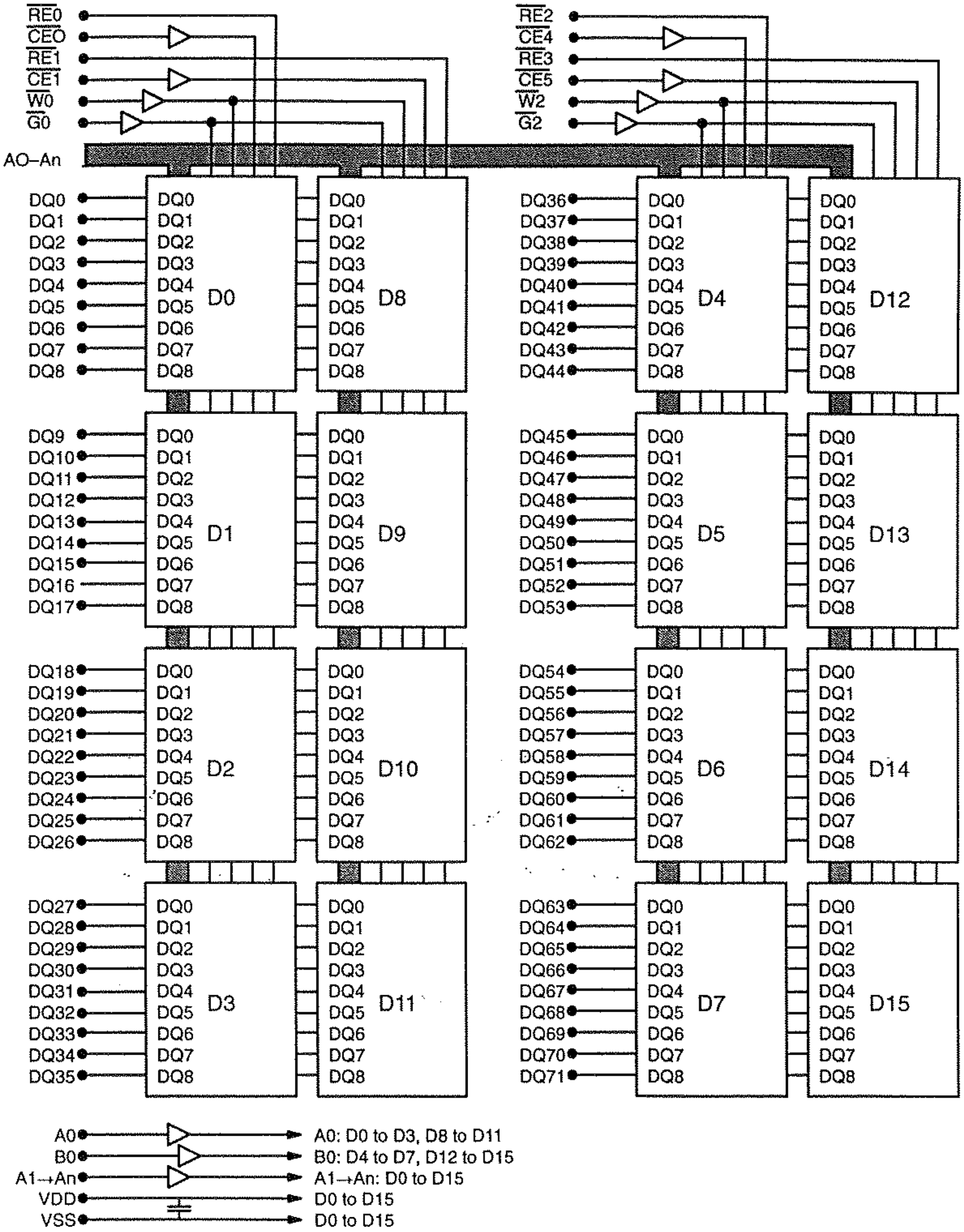


Figure 4.5.1–U
168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X9 DRAMs

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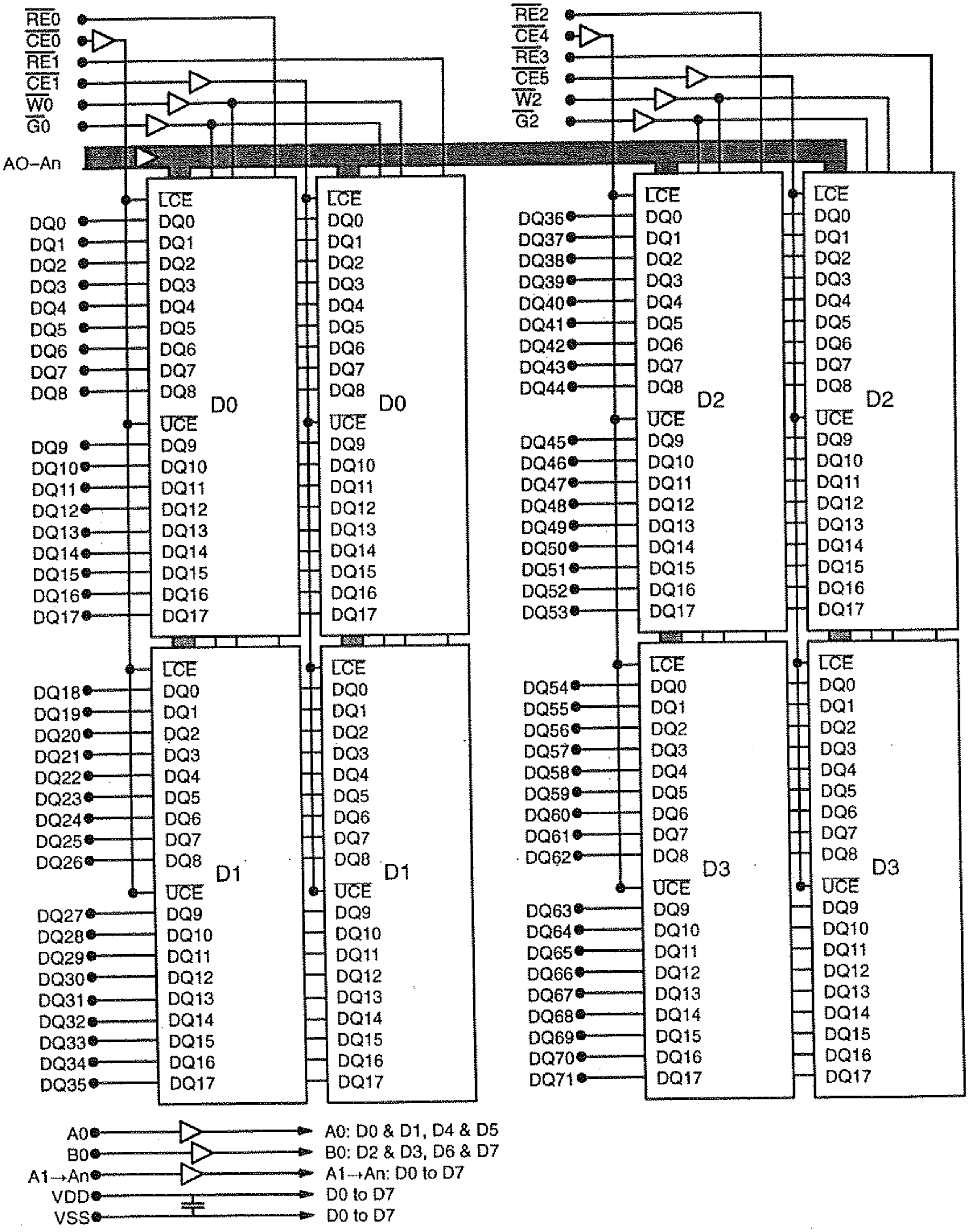

Figure 4.5.1–V

168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X18 DRAMs

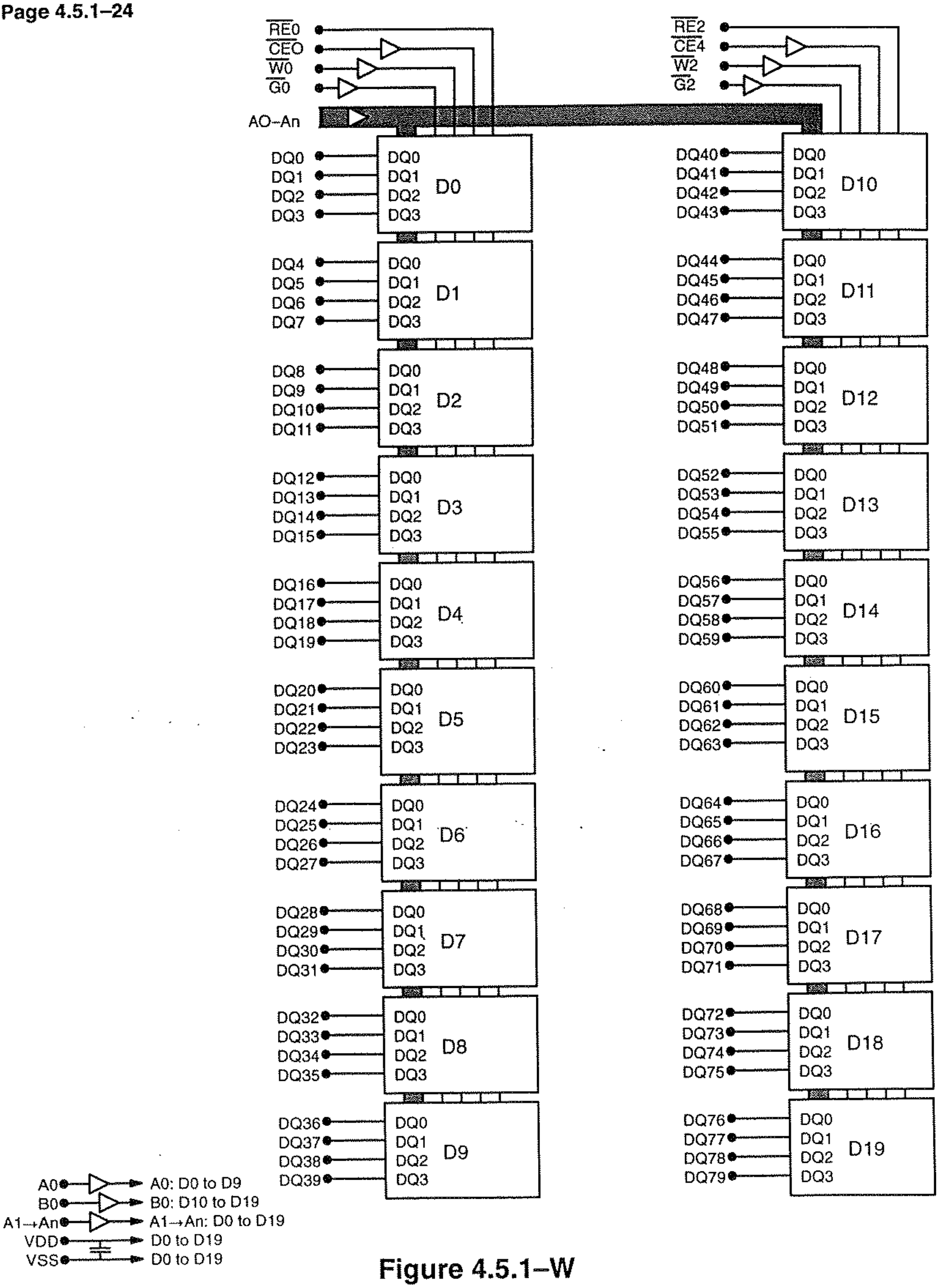

Figure 4.5.1–W

168 PIN, 80 BIT (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs

276

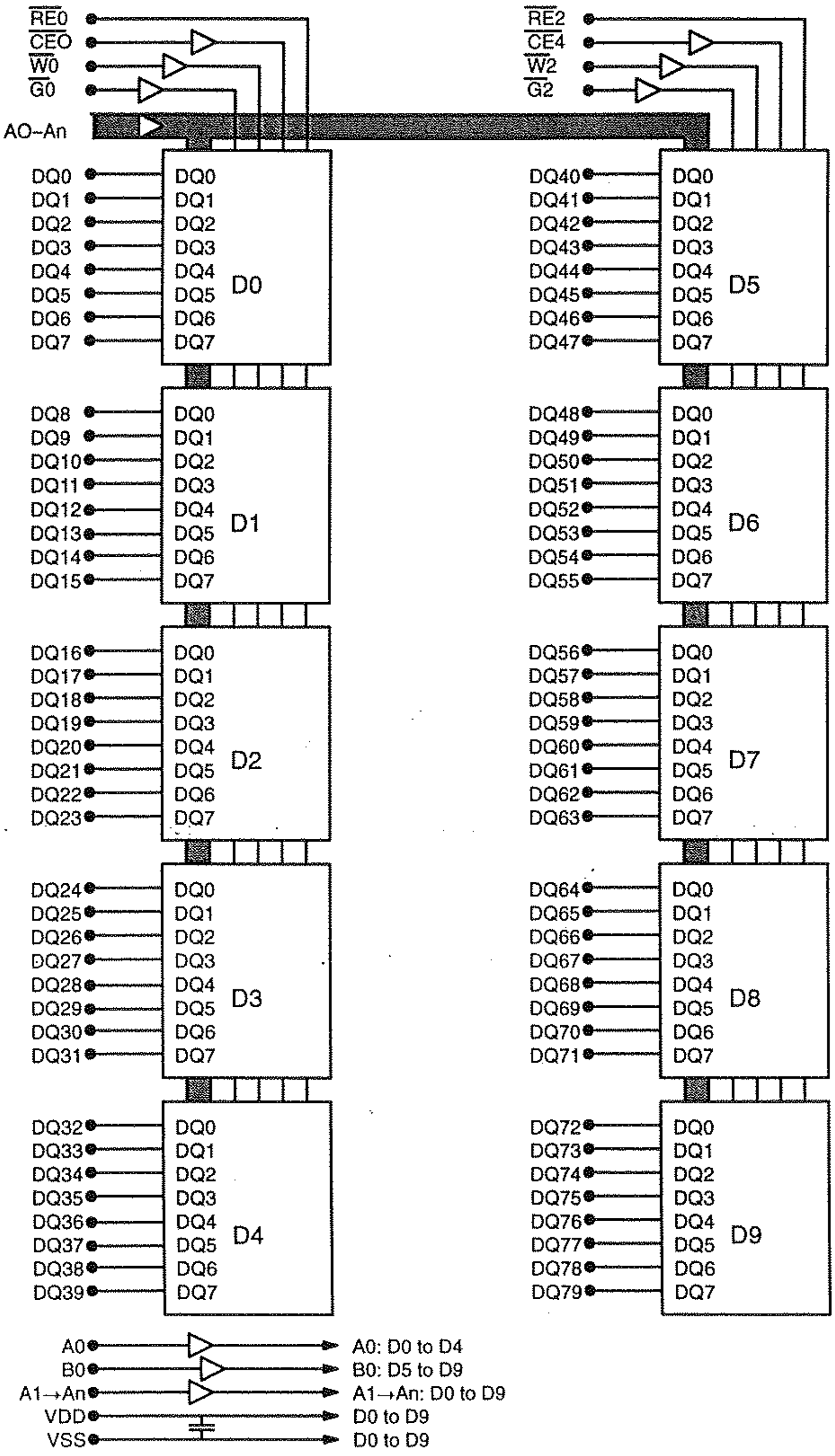

Figure 4.5.1–X
168 PIN, X80 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs

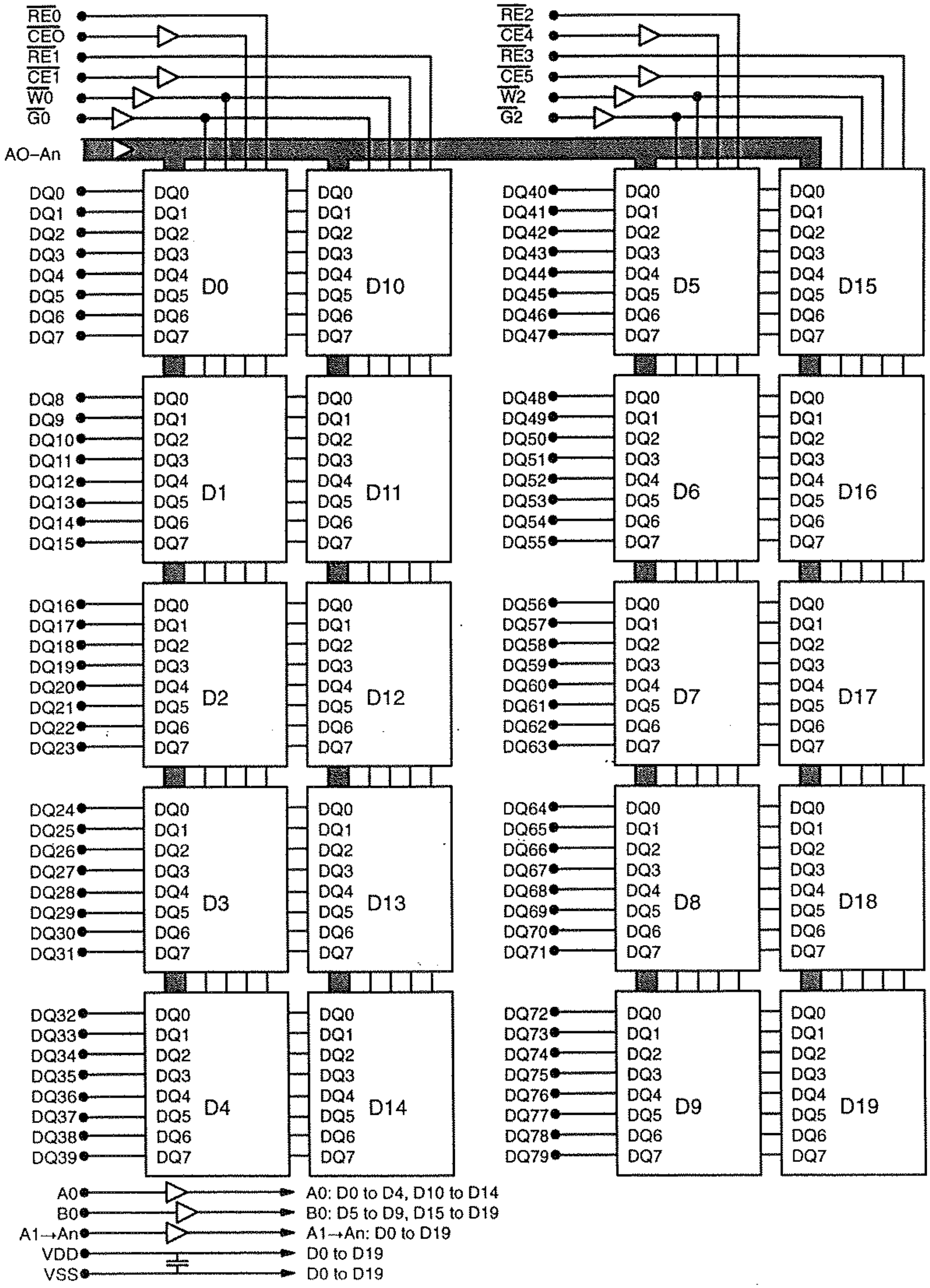

Figure 4.5.1–Y
168 PIN, X80 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs

278

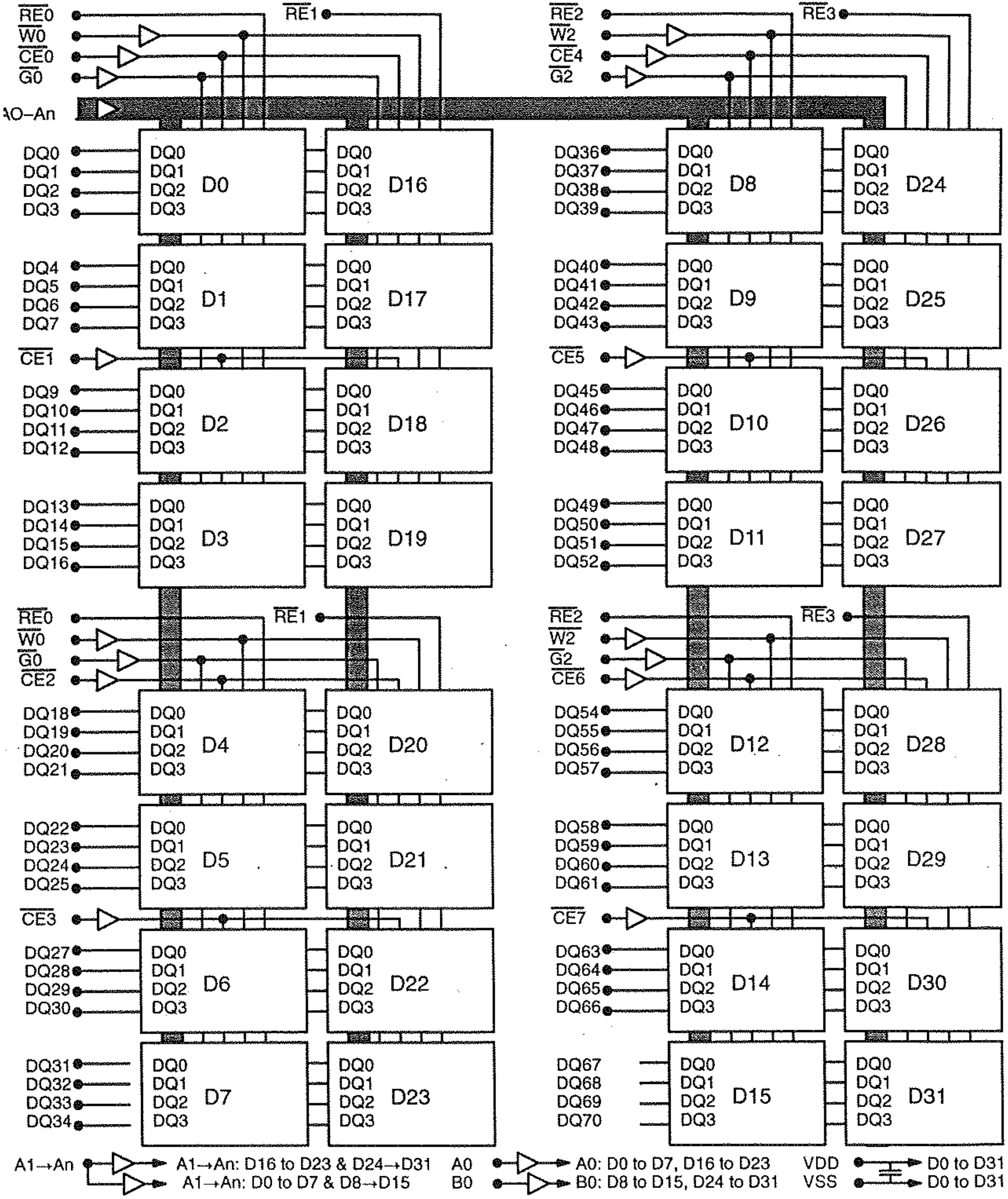

Figure 4.5.1–Z
168 PIN, X64 DRAM DIMM, 2 BANK with X4 DRAMs

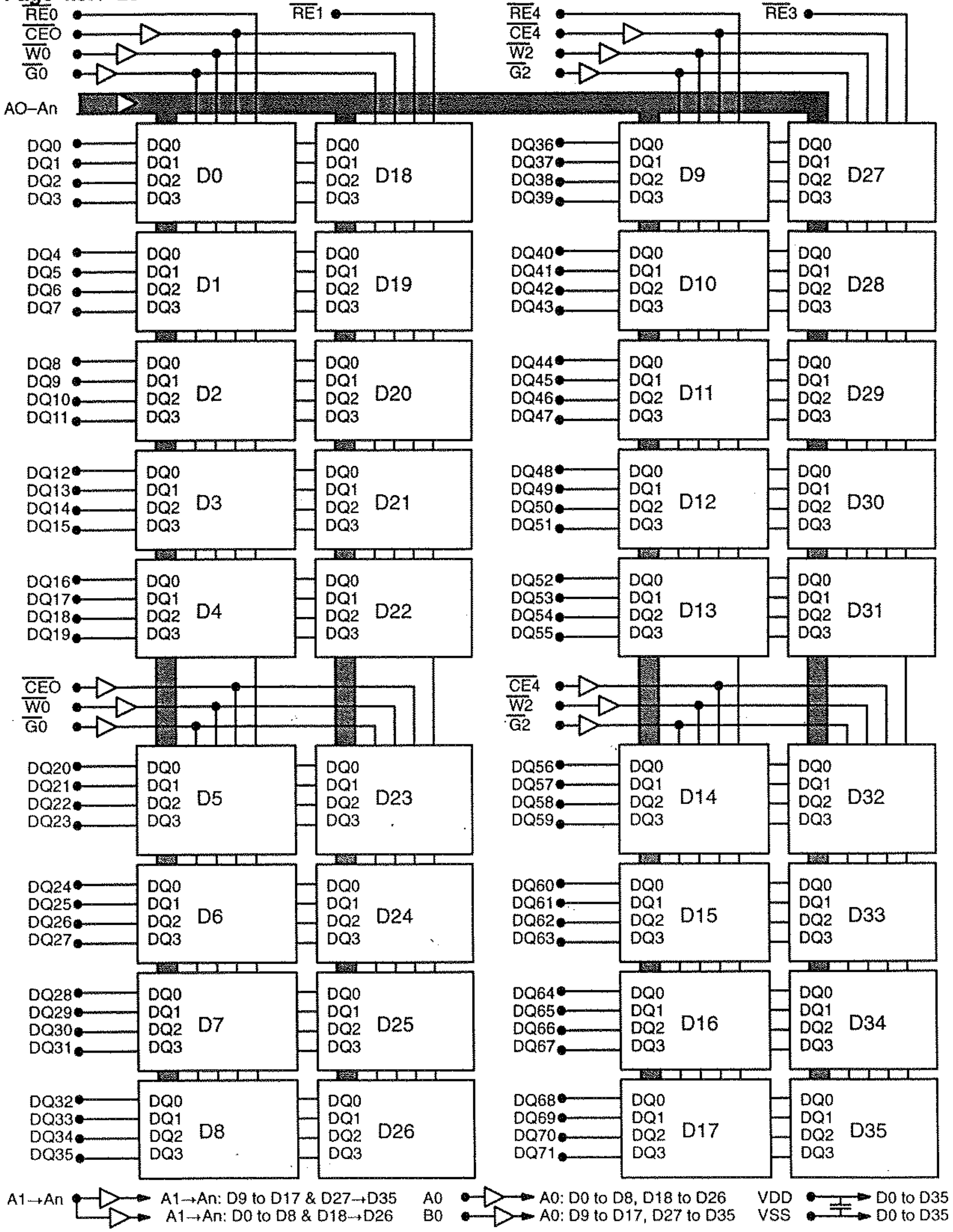

Figure 4.5.1–AA
168 PIN, X72 ECC DRAM DIMM, 2 BANK, X4 DRAMs

61D

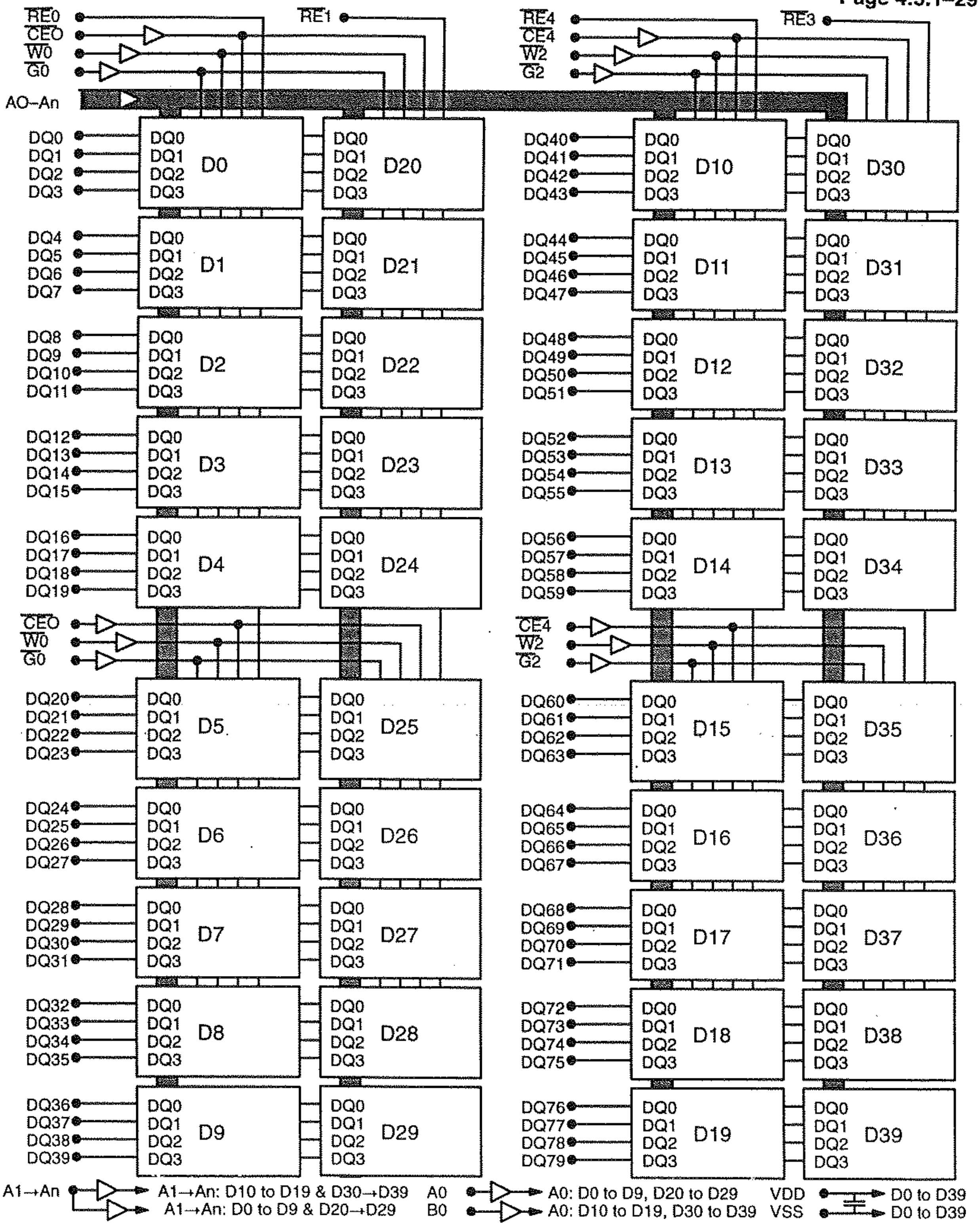

Figure 4.5.1–AB
168 PIN, X80 ECC DRAM DIMM, 2 BANK, X4 DRAMs

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4.5.2 – 200 PIN DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memory devices.

LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

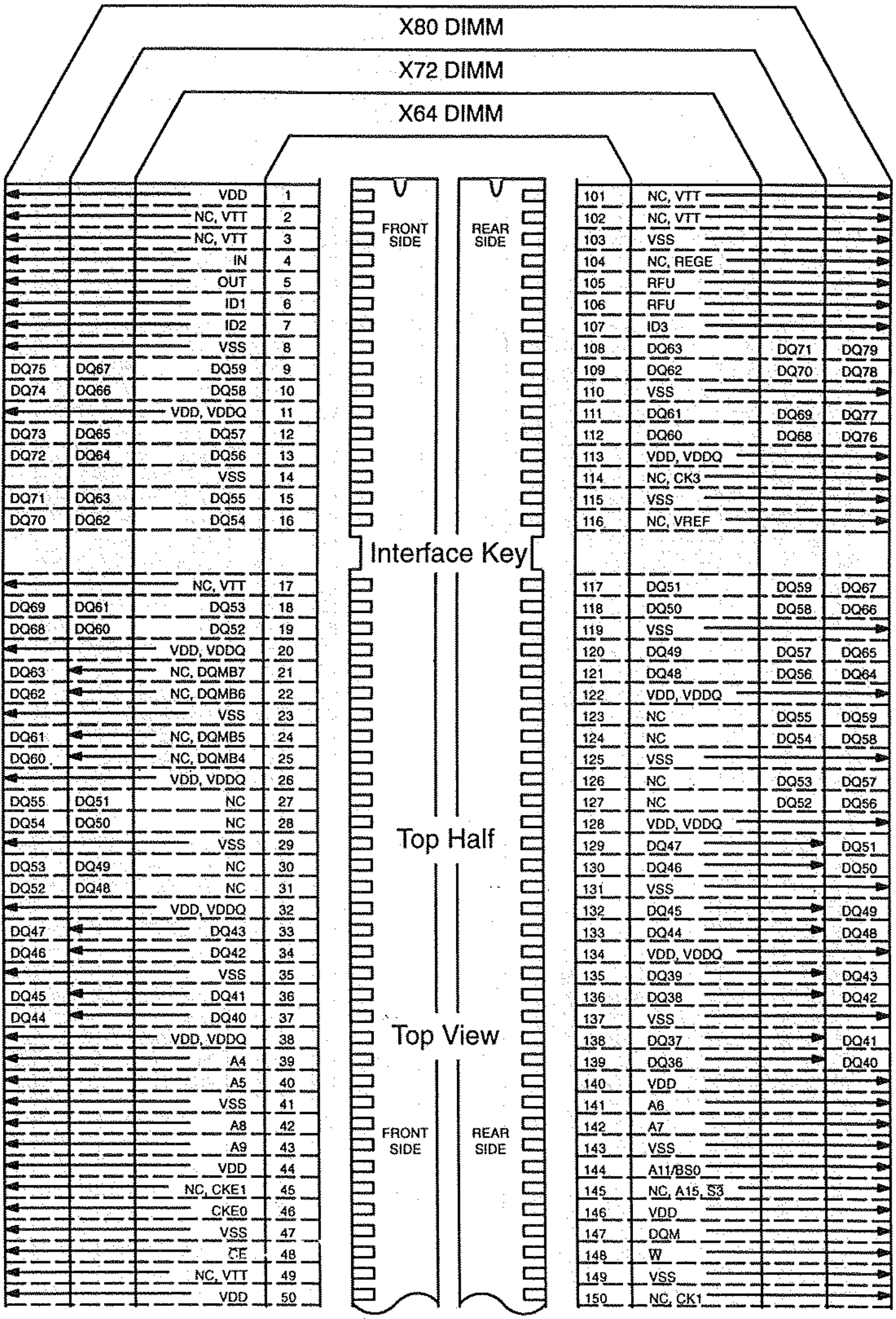
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.2–A, 4.5.2–B, & 4.5.2–C

MECHANICAL KEY DEFINITION—Fig. 4.5.2–D

PIN DEFINITIONS—Fig. 4.5.2–E

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.2–F through 4.5.2–M



X80 DIMM	X72 DIMM	X64 DIMM			X64 DIMM	X72 DIMM	X80 DIMM
←	←	VDD	1	101	NC, VTT	→	→
←	←	NC, VTT	2	102	NC, VTT	→	→
←	←	NC, VTT	3	103	VSS	→	→
←	←	IN	4	104	NC, REGE	→	→
←	←	OUT	5	105	RFU	→	→
←	←	ID1	6	106	RFU	→	→
←	←	ID2	7	107	ID3	→	→
←	←	VSS	8	108	DQ63	DQ71	DQ79
DQ75	DQ67	DQ59	9	109	DQ62	DQ70	DQ78
DQ74	DQ66	DQ58	10	110	VSS	→	→
←	←	VDD, VDDQ	11	111	DQ61	DQ69	DQ77
DQ73	DQ65	DQ57	12	112	DQ60	DQ68	DQ76
DQ72	DQ64	DQ56	13	113	VDD, VDDQ	→	→
		VSS	14	114	NC, CK3	→	→
DQ71	DQ63	DQ55	15	115	VSS	→	→
DQ70	DQ62	DQ54	16	116	NC, VREF	→	→
←	←	NC, VTT	17	117	DQ51	DQ59	DQ67
DQ69	DQ61	DQ53	18	118	DQ50	DQ58	DQ66
DQ68	DQ60	DQ52	19	119	VSS	→	→
←	←	VDD, VDDQ	20	120	DQ49	DQ57	DQ65
DQ63	←	NC, DQMB7	21	121	DQ48	DQ56	DQ64
DQ62	←	NC, DQMB6	22	122	VDD, VDDQ	→	→
←	←	VSS	23	123	NC	DQ55	DQ59
DQ61	←	NC, DQMB5	24	124	NC	DQ54	DQ58
DQ60	←	NC, DQMB4	25	125	VSS	→	→
←	←	VDD, VDDQ	26	126	NC	DQ53	DQ57
DQ55	DQ51	NC	27	127	NC	DQ52	DQ56
DQ54	DQ50	NC	28	128	VDD, VDDQ	→	→
←	←	VSS	29	129	DQ47	→	DQ51
DQ53	DQ49	NC	30	130	DQ46	→	DQ50
DQ52	DQ48	NC	31	131	VSS	→	→
←	←	VDD, VDDQ	32	132	DQ45	→	DQ49
DQ47	←	DQ43	33	133	DQ44	→	DQ48
DQ46	←	DQ42	34	134	VDD, VDDQ	→	→
←	←	VSS	35	135	DQ39	→	DQ43
DQ45	←	DQ41	36	136	DQ38	→	DQ42
DQ44	←	DQ40	37	137	VSS	→	→
←	←	VDD, VDDQ	38	138	DQ37	→	DQ41
←	←	A4	39	139	DQ36	→	DQ40
←	←	A5	40	140	VDD	→	→
←	←	VSS	41	141	A6	→	→
←	←	A8	42	142	A7	→	→
←	←	A9	43	143	VSS	→	→
←	←	VDD	44	144	A11/BS0	→	→
←	←	NC, CKE1	45	145	NC, A15, S3	→	→
←	←	CKE0	46	146	VDD	→	→
←	←	VSS	47	147	DQM	→	→
←	←	CE	48	148	W	→	→
←	←	NC, VTT	49	149	VSS	→	→
←	←	VDD	50	150	NC, CK1	→	→

Figure 4.5.2–A
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF

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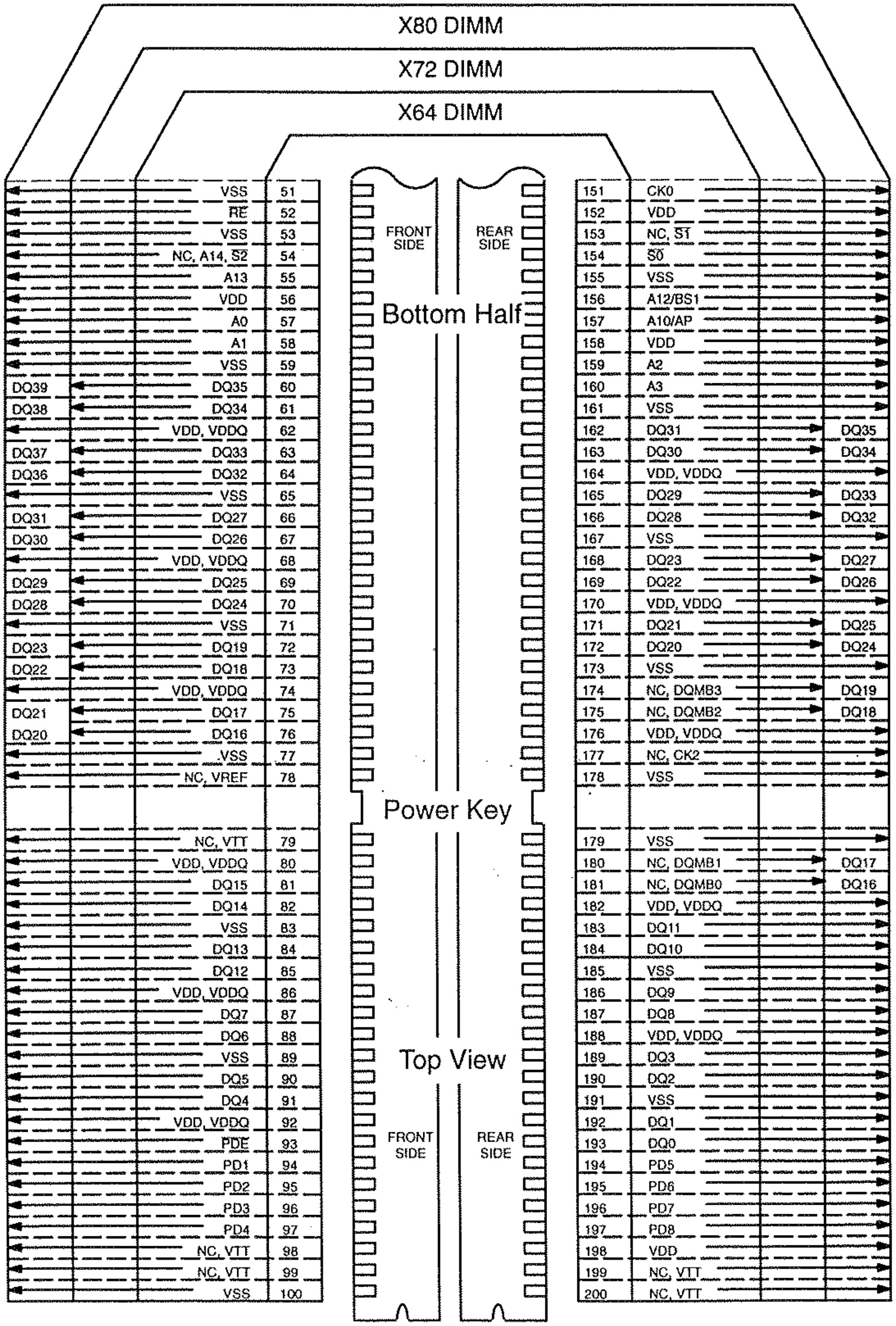

	VSS	51
	$\overline{RE}$	52
	VSS	53
	NC, A14, $\overline{S2}$	54
	A13	55
	VDD	56
	A0	57
	A1	58
	VSS	59
DQ39	DQ35	60
DQ38	DQ34	61
	VDD, VDDQ	62
DQ37	DQ33	63
DQ36	DQ32	64
	VSS	65
DQ31	DQ27	66
DQ30	DQ26	67
	VDD, VDDQ	68
DQ29	DQ25	69
DQ28	DQ24	70
	VSS	71
DQ23	DQ19	72
DQ22	DQ18	73
	VDD, VDDQ	74
DQ21	DQ17	75
DQ20	DQ16	76
	VSS	77
	NC, VREF	78
	NC, VTT	79
	VDD, VDDQ	80
	DQ15	81
	DQ14	82
	VSS	83
	DQ13	84
	DQ12	85
	VDD, VDDQ	86
	DQ7	87
	DQ6	88
	VSS	89
	DQ5	90
	DQ4	91
	VDD, VDDQ	92
	$\overline{PDE}$	93
	PD1	94
	PD2	95
	PD3	96
	PD4	97
	NC, VTT	98
	NC, VTT	99
	VSS	100

151	CK0	
152	VDD	
153	NC, $\overline{S1}$	
154	$\overline{S0}$	
155	VSS	
156	A12/BS1	
157	A10/AP	
158	VDD	
159	A2	
160	A3	
161	VSS	
162	DQ31	DQ35
163	DQ30	DQ34
164	VDD, VDDQ	
165	DQ29	DQ33
166	DQ28	DQ32
167	VSS	
168	DQ23	DQ27
169	DQ22	DQ26
170	VDD, VDDQ	
171	DQ21	DQ25
172	DQ20	DQ24
173	VSS	
174	NC, DQMB3	DQ19
175	NC, DQMB2	DQ18
176	VDD, VDDQ	
177	NC, CK2	
178	VSS	
179	VSS	
180	NC, DQMB1	DQ17
181	NC, DQMB0	DQ16
182	VDD, VDDQ	
183	DQ11	
184	DQ10	
185	VSS	
186	DQ9	
187	DQ8	
188	VDD, VDDQ	
189	DQ3	
190	DQ2	
191	VSS	
192	DQ1	
193	DQ0	
194	PD5	
195	PD6	
196	PD7	
197	PD8	
198	VDD	
199	NC, VTT	
200	NC, VTT	

Figure 4.5.2–B
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

PD BITS 4 3 2 1	MODULE CONFIGURATION	SDRAM ORGANIZATION	RE ADDR.	CE ADDR
1 1 1 1	NO MODULE			
1 0 0 0	1M X 64/72/80	1M X 16	12	8
0 0 0 0	2M X 64/72/80	1M X 16	12	8
1 0 0 1	2M X 64/72/80	2M X 8	12	9
0 0 0 1	4M X 64/72/80	2M X 8	12	9
1 0 1 0	4M X 64/72/80	4M X 4/16	12	10
0 0 1 0	8M X 64/72/80	4M X 4/16	12	10
1 0 1 1	8M X 64/72/80	8M X 8	TBD	TBD
0 0 1 1	16M X 64/72/80	8M X 8	TBD	TBD
1 1 0 0	16M X 64/72/80	16M X 4	TBD	TBD
0 1 0 0	32M X 64/72/80	16M X 4	TBD	TBD
1 1 0 1	RFU	TBD	TBD	TBD
0 1 0 1	RFU	TBD	TBD	TBD
1 1 1 0	RFU	TBD	TBD	TBD
0 1 1 0	RFU	TBD	TBD	TBD
0 1 1 1	Expansion			

Note 1 Presence Detect pins PD1—PD8 are buffered and enabled by $\overline{\text{PDE}}$. The "1" outputs are NC and the "0" outputs are driven low by on–module drivers when $\overline{\text{PDE}}$ is asserted active low.

Note 2 Buffered DIMMs (PD7=1) with PD8=0 (Byte–Write) shall be capable of both Word–Write and Byte–Write operations

	PD6	PD5
SPEED (tCYC)	195	194
15 ns	1	1
12 ns	1	0
10 ns	0	1
8 ns	0	0

PD SPEED TABLE

	PD7
INTERFACE	196
UNBUFFERED	0
BUFFERED	1

MODULE INTERFACE

	PD8
WRITE MODE	197
BYTE	0
WORD	1

WRITE MODE DETECT

	ID3
POWER	107
NORMAL	0
LOW–POWER	1

POWER LEVEL DETECT

	ID2
RAS TIMING	7
NO EARLY RAS	0
EARLY RAS	1

READ PRECHARGE TIMING

	ID1
INTERVAL	6
2 CLOCKS	0
1 CLOCK	1

COMMAND INTERVAL

Figure 4.5.2–C

200 PIN, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES

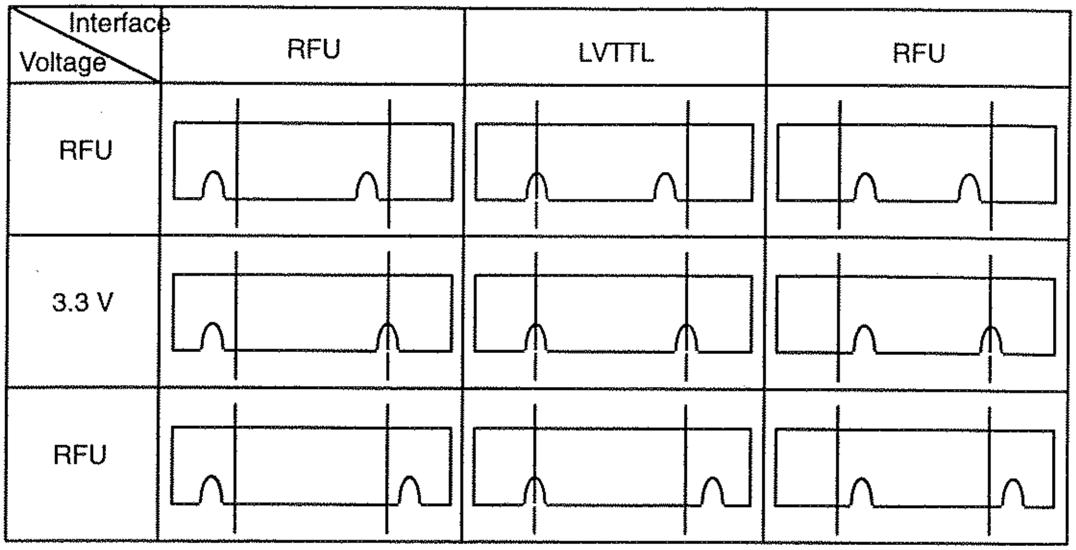

Figure 4.5.2–D

200 PIN, 8 BYTE SDRAM DIMM MECHANICAL KEY DEFINITION

Pin Name	Number	Function
A0....A15	16	Address Input (multiplexed)
DQ0....DQ79	80	Data Input/Output (common)
CK0....CK3	4	Clock Input
CKE0....CKE1	2	Clock Enable Input
$\overline{S0}$....$\overline{S3}$	4	Chip Select Input
$\overline{RE}$	1	Row Enable (RAS) Input
$\overline{CE}$	1	Column Enable (CAS) Input
$\overline{W}$	1	Write Enable Input
DQM	1	Data Mask
DQMB0....DQMB7	8	Byte Data Mask
REGE	1	Buffer/Register Enable
$\overline{PDE}$	1	Presence Detect Enable
PD1....PD8	8	Buffered Logic Presence Detect Output
ID1....ID3	3	Identification Output
IN, OUT	2	Unbuffered Physical Detect Input/Output
VDD	9	Primary Positive Power Supply
VDDQ	20	Posivite Power for Input/Output
VREF	2	Reference Power Supply
VSS	33	Ground
VTT	11	Termination Power Supply
RFU	2	Reserved for Future Use

Notes:

1. Pin A14 is shared with S2, and pin A15 is shared with pin S3.
2. Pins DQMB0...DQMB7 are shared with pins defined as NC for X64 and X72 configurations.
3. REGE (Register Enable) operates similarly to the SAB pin on the 74AC11652 "Octal Bus Transceiver and Register with 3–State Outputs". When it is asserted, active high, the buffer–register operates in Register mode, as opposed to when it is de–asserted, inactive low, the buffer –register operates in "real–time" buffer mode.
4. The unbuffered physical detect pins IN and OUT are shorted together on the DIMM.

Figure 4.5.2–E

8 BYTE SDRAM DIMM PIN DEFINITIONS

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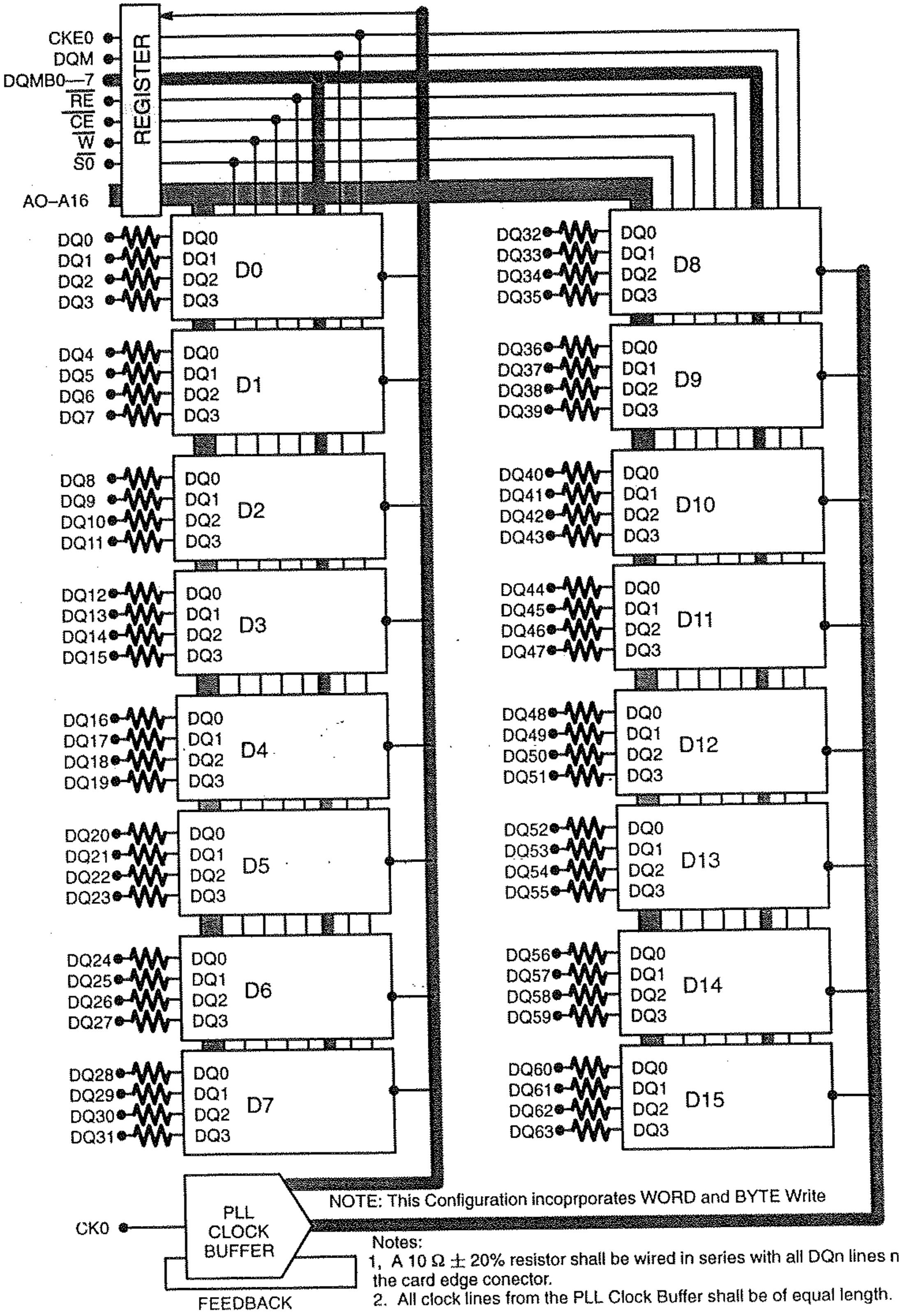
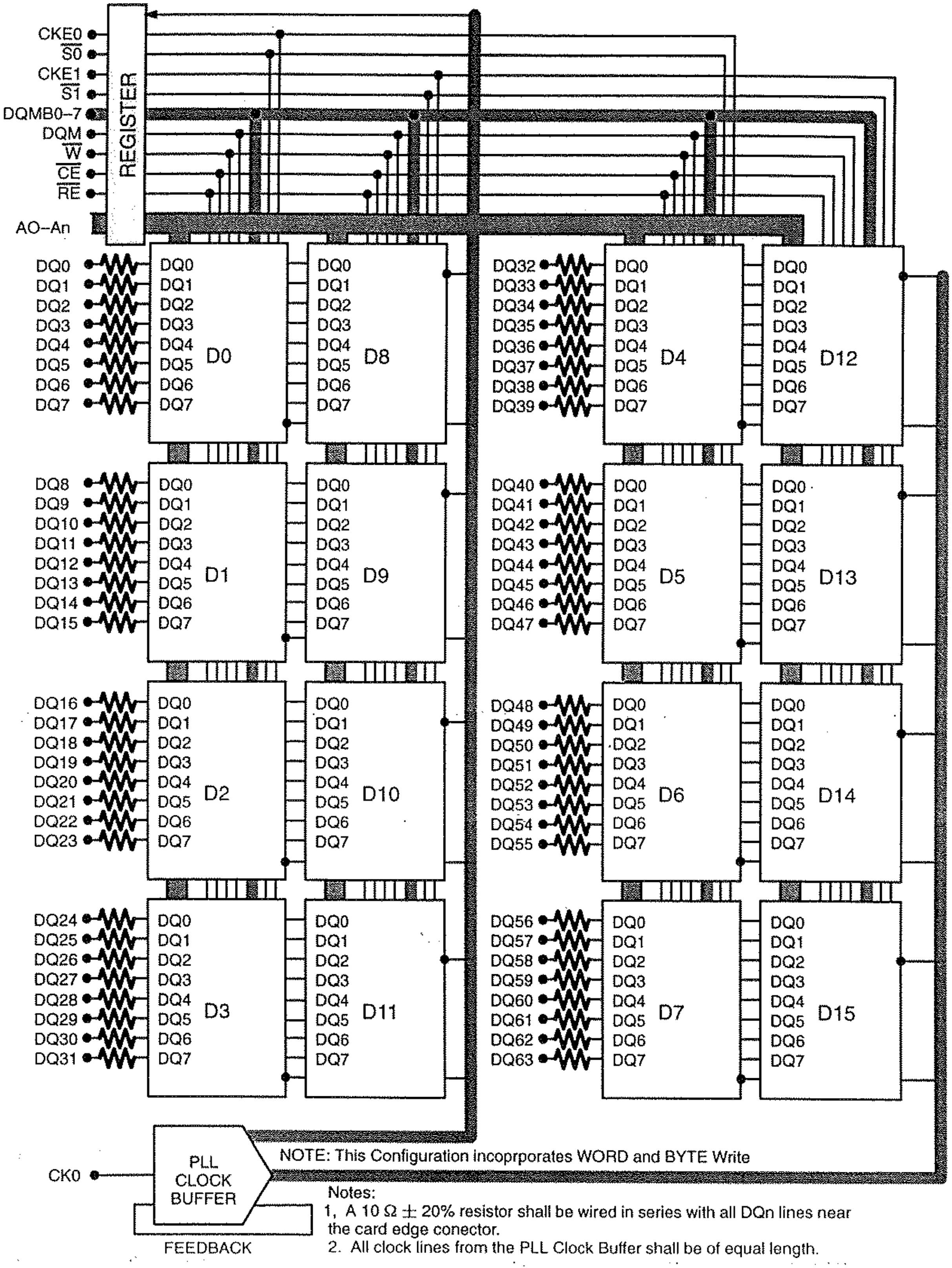


NOTE: This Configuration incoprporates WORD and BYTE Write

Notes:
1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–F

200 PIN, X64 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs

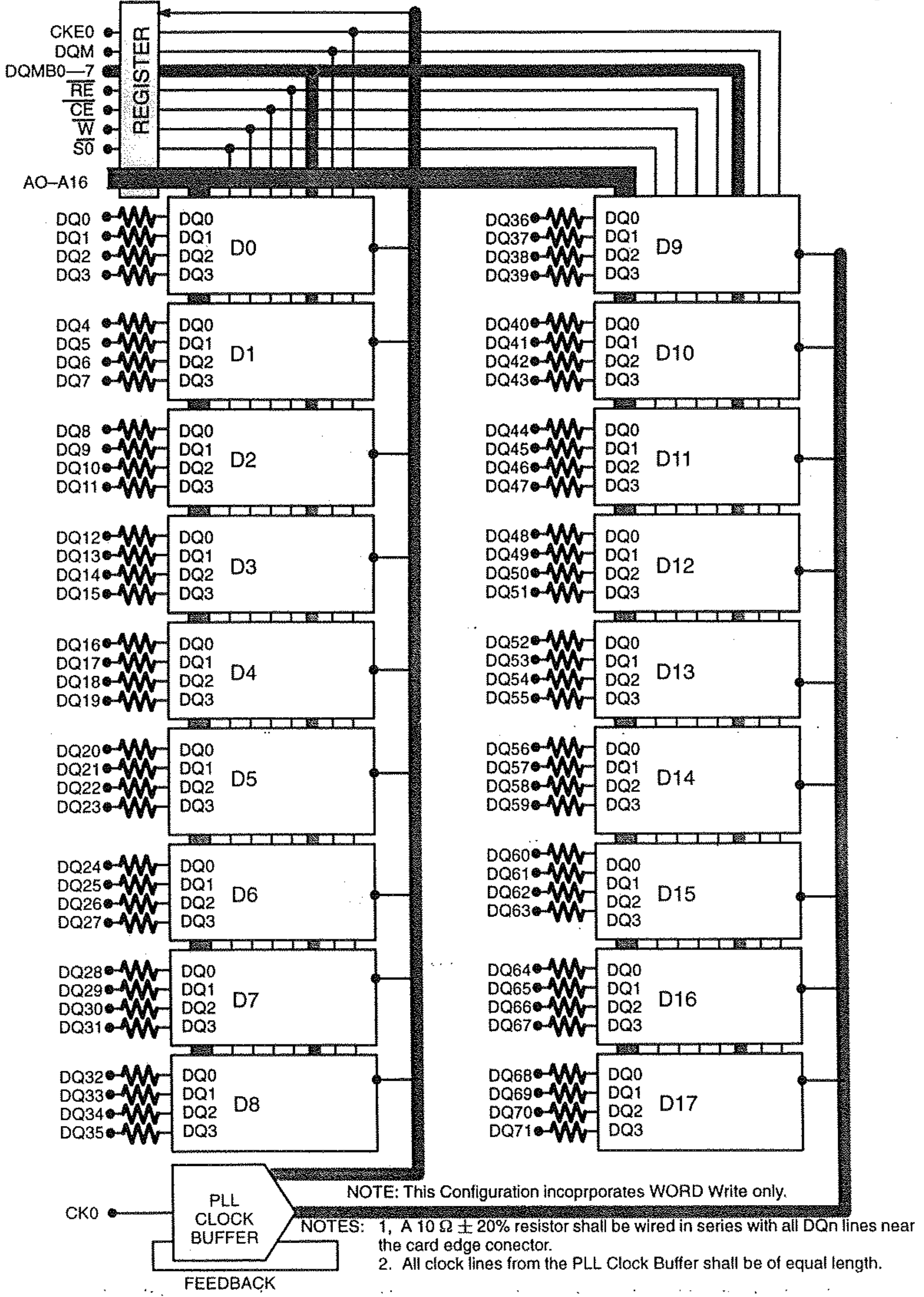


NOTE: This Configuration incoprporates WORD and BYTE Write

Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–G

200 PIN, X64 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs



NOTE: This Configuration incoprporates WORD Write only.

NOTES: 1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–H

200 PIN, X72 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs

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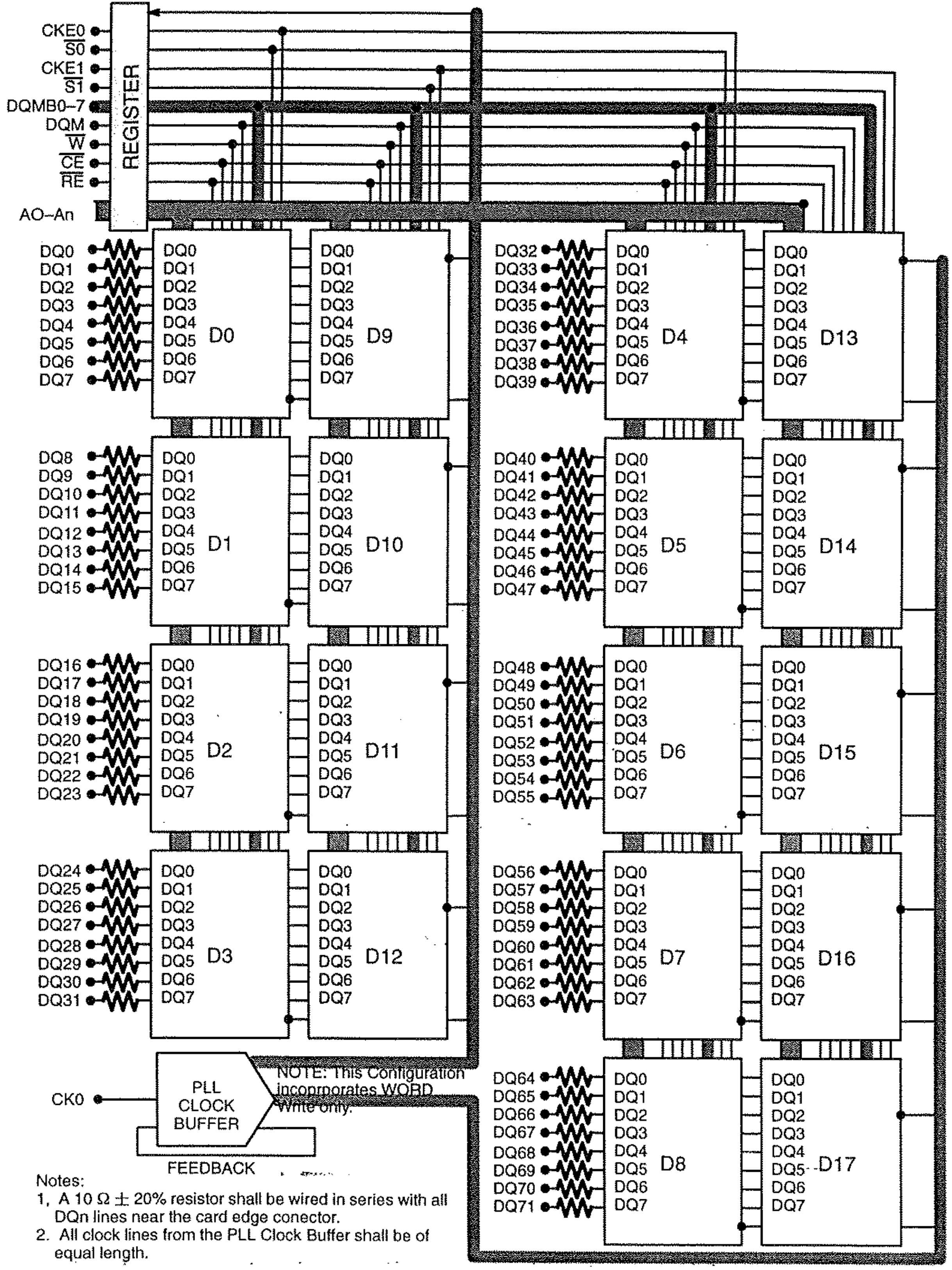
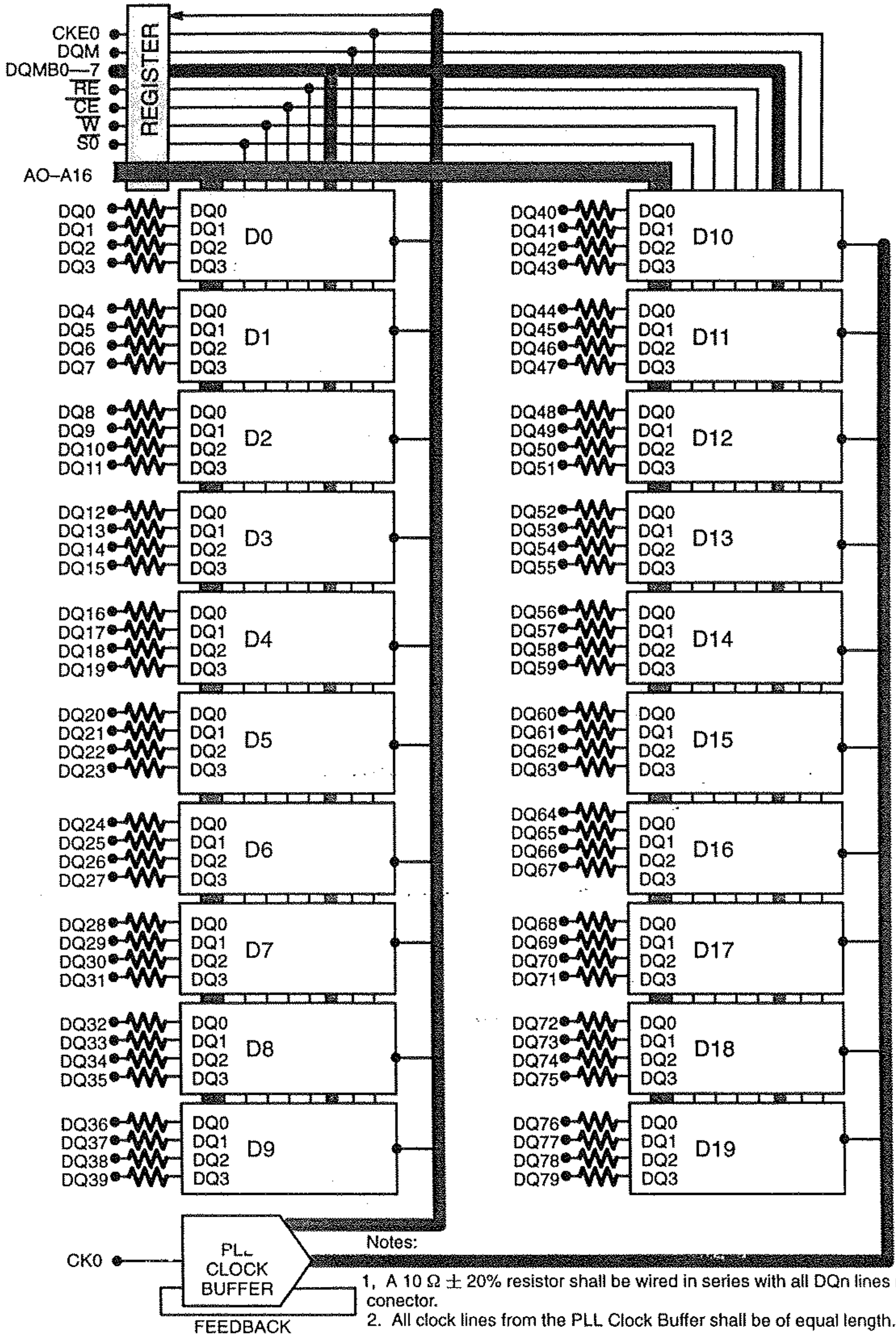


Notes:
1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–I

200 PIN, X72 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs



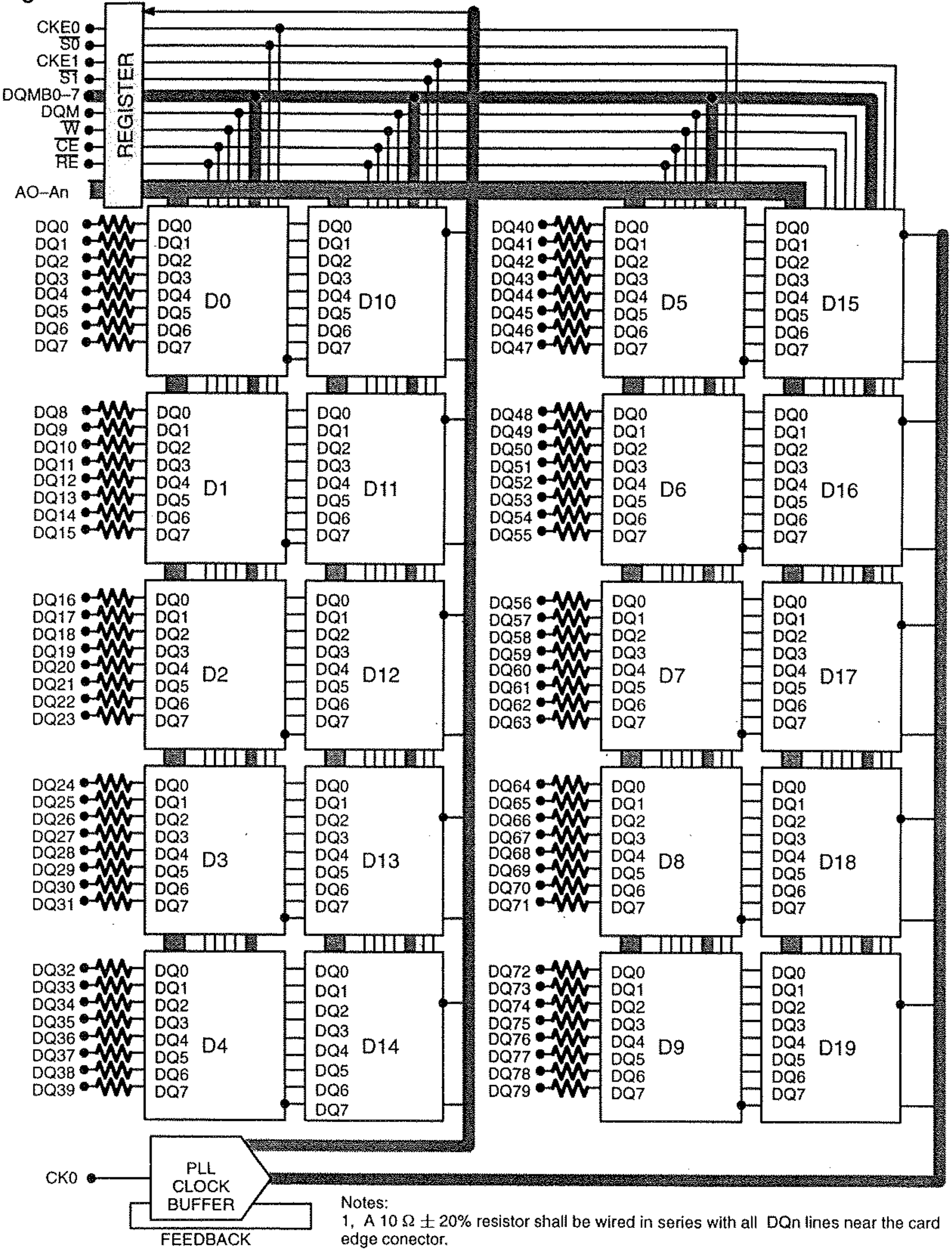
Notes:

1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–J

200 PIN, X80 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs

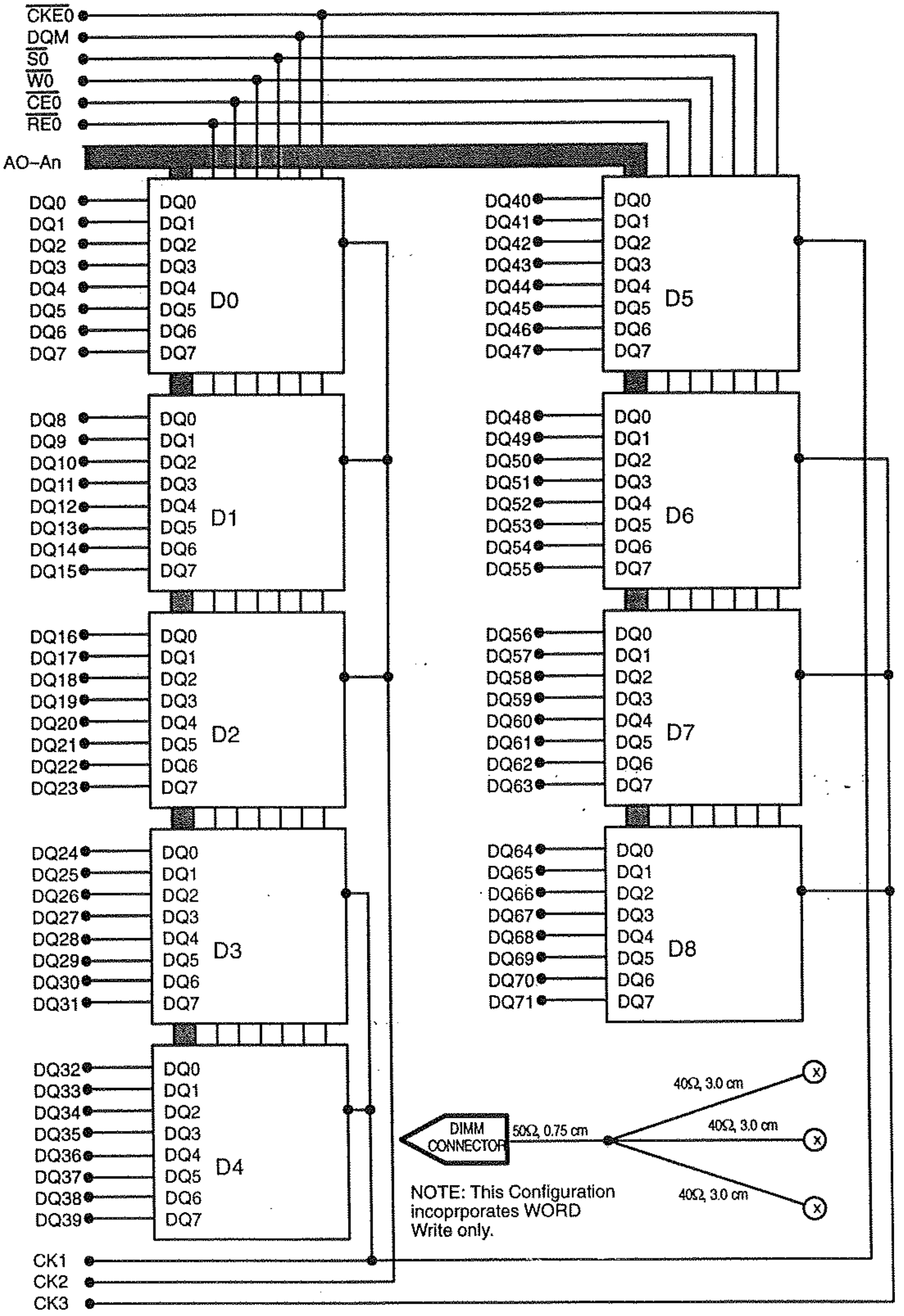
Release 5–7



Notes:
1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–K
200 PIN, X80 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

2 13.

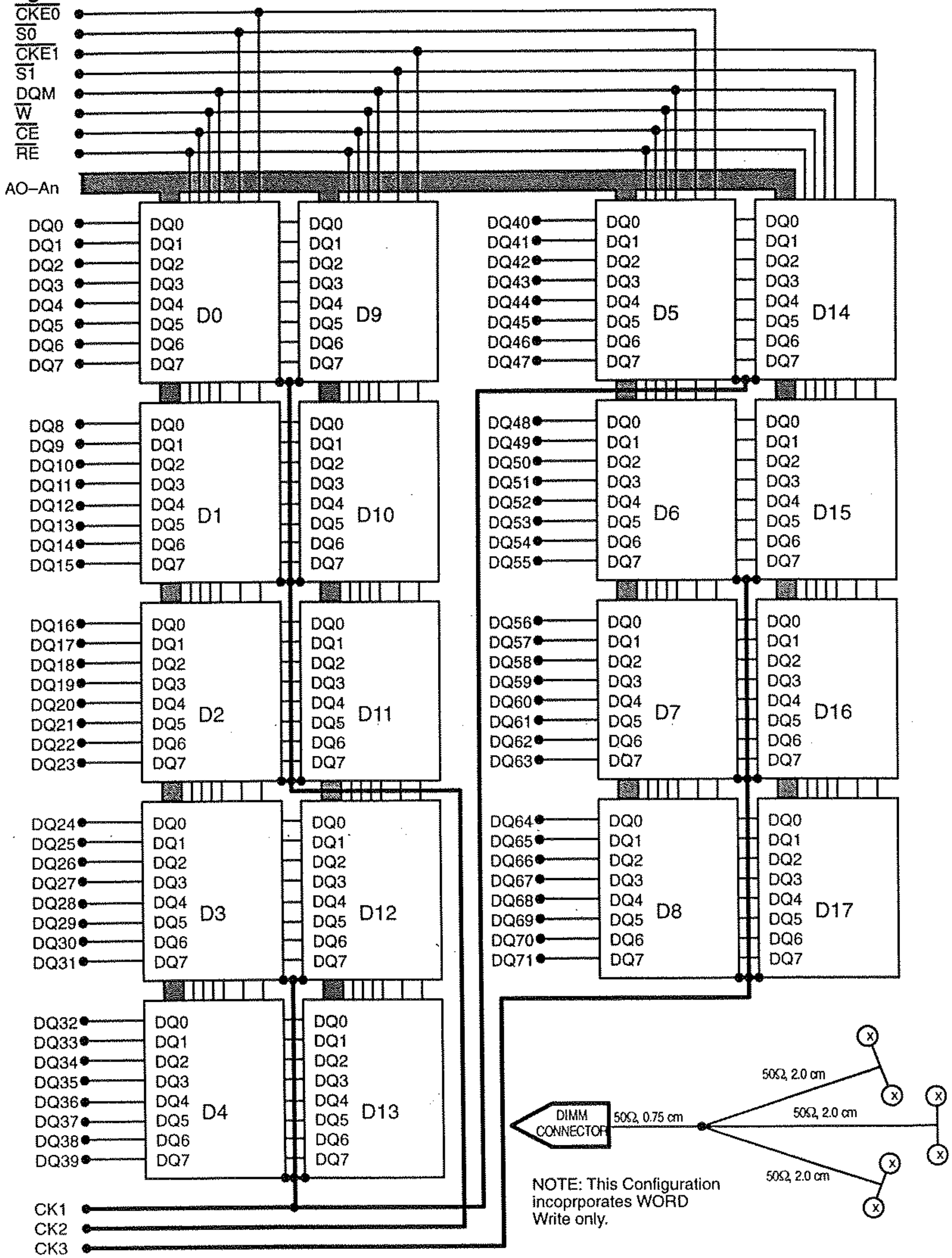


NOTE: This Configuration incoprporates WORD Write only.

Note: All clock trees shall be routed as equal-length "stars" from CK1, CK2, & CK3 inputs as shown in the diagram above.

Figure 4.5.2-L

200 PIN, X72 UNBUFFERED SDRAM DIMM, 1 bank with X8 DRAMs



NOTE: This Configuration incoprporates WORD Write only.

Figure 4.5.2–M

200 PIN, X72 UNBUFFERED SDRAM DIMM, 2 banks with X8 DRAMs

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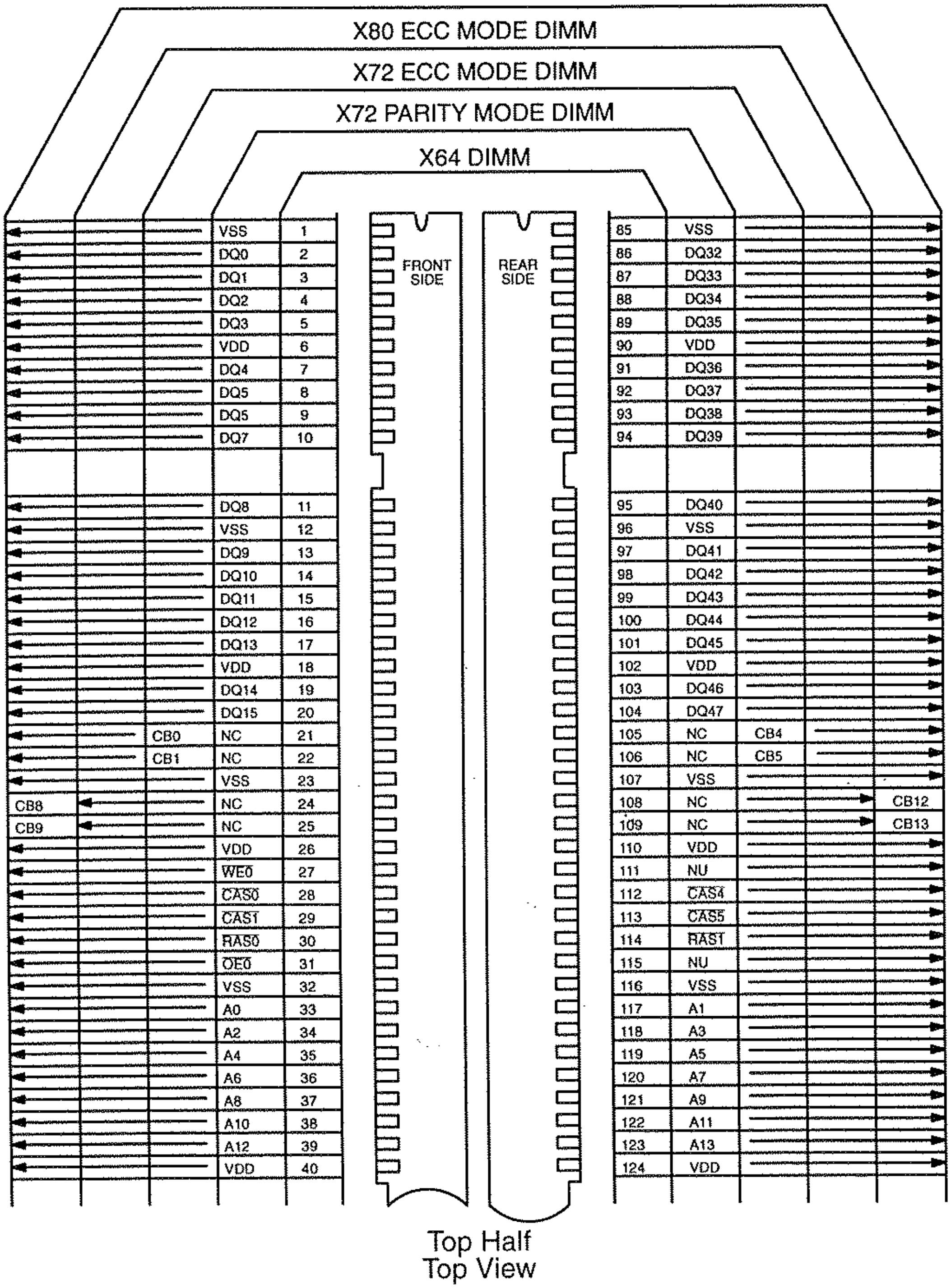
4.5.3 – 168 PIN UNBUFFERED DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES
CONFIGURATION—13 Different Configurations are defined using various combinationa of X1, X4, X8, X16 and X18 memories.
LOGIC FEATURES—The modules contain "SERIAL PRESENCE DETECT" features using EEPROM stored information that profided a variety of encoded information regarding the module such as storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
—Check Bit locations are pre–assigned
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS—Figs. 4.5.3–A, & 4.5.3–B
SPD TABLES—Figs. 4.5.3–C
KEYING METHODOLOGY—Fig. 4.5.3–D
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.3–E through 4.5.3–S

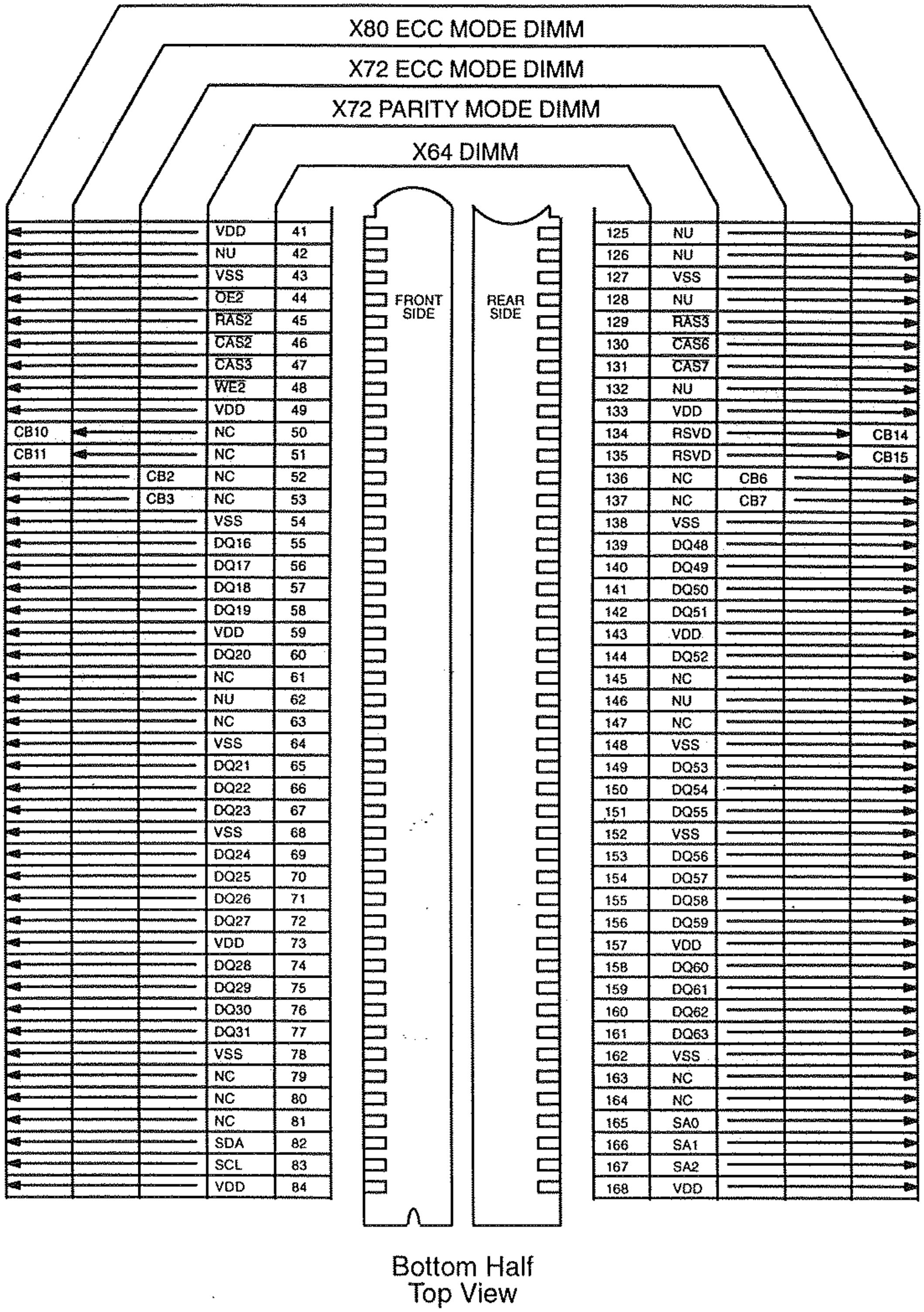
296



X80 ECC MODE DIMM	X72 ECC MODE DIMM	X72 PARITY MODE DIMM	X64 DIMM	Pin	Pin	X64 DIMM	X72 PARITY MODE DIMM	X72 ECC MODE DIMM	X80 ECC MODE DIMM
			VSS	1	85	VSS			
			DQ0	2	86	DQ32			
			DQ1	3	87	DQ33			
			DQ2	4	88	DQ34			
			DQ3	5	89	DQ35			
			VDD	6	90	VDD			
			DQ4	7	91	DQ36			
			DQ5	8	92	DQ37			
			DQ5	9	93	DQ38			
			DQ7	10	94	DQ39			
			DQ8	11	95	DQ40			
			VSS	12	96	VSS			
			DQ9	13	97	DQ41			
			DQ10	14	98	DQ42			
			DQ11	15	99	DQ43			
			DQ12	16	100	DQ44			
			DQ13	17	101	DQ45			
			VDD	18	102	VDD			
			DQ14	19	103	DQ46			
			DQ15	20	104	DQ47			
		CB0	NC	21	105	NC	CB4		
		CB1	NC	22	106	NC	CB5		
			VSS	23	107	VSS			
CB8			NC	24	108	NC			CB12
CB9			NC	25	109	NC			CB13
			VDD	26	110	VDD			
			$\overline{\text{WE0}}$	27	111	NU			
			$\overline{\text{CAS0}}$	28	112	$\overline{\text{CAS4}}$			
			$\overline{\text{CAS1}}$	29	113	$\overline{\text{CAS5}}$			
			$\overline{\text{RAS0}}$	30	114	$\overline{\text{RAS1}}$			
			$\overline{\text{OE0}}$	31	115	NU			
			VSS	32	116	VSS			
			A0	33	117	A1			
			A2	34	118	A3			
			A4	35	119	A5			
			A6	36	120	A7			
			A8	37	121	A9			
			A10	38	122	A11			
			A12	39	123	A13			
			VDD	40	124	VDD			

FIGURE 4.5.3–A
64, 72, or 80 BIT DIMM PINOUT, TOP HALF

.277



		VDD	41
		NU	42
		VSS	43
		OE2	44
		RAS2	45
		CAS2	46
		CAS3	47
		WE2	48
		VDD	49
CB10		NC	50
CB11		NC	51
	CB2	NC	52
	CB3	NC	53
		VSS	54
		DQ16	55
		DQ17	56
		DQ18	57
		DQ19	58
		VDD	59
		DQ20	60
		NC	61
		NU	62
		NC	63
		VSS	64
		DQ21	65
		DQ22	66
		DQ23	67
		VSS	68
		DQ24	69
		DQ25	70
		DQ26	71
		DQ27	72
		VDD	73
		DQ28	74
		DQ29	75
		DQ30	76
		DQ31	77
		VSS	78
		NC	79
		NC	80
		NC	81
		SDA	82
		SCL	83
		VDD	84

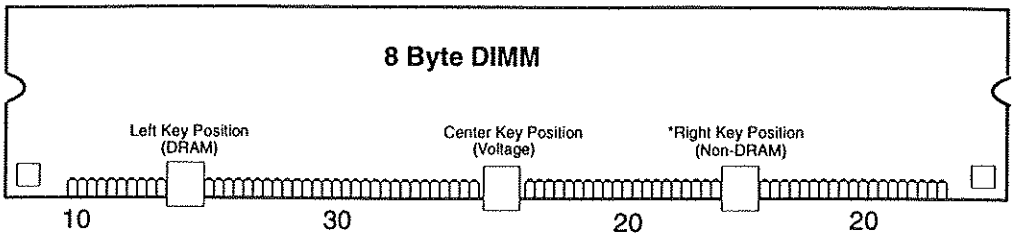
125	NU		
126	NU		
127	VSS		
128	NU		
129	RAS3		
130	CAS6		
131	CAS7		
132	NU		
133	VDD		
134	RSVD		CB14
135	RSVD		CB15
136	NC	CB6	
137	NC	CB7	
138	VSS		
139	DQ48		
140	DQ49		
141	DQ50		
142	DQ51		
143	VDD		
144	DQ52		
145	NC		
146	NU		
147	NC		
148	VSS		
149	DQ53		
150	DQ54		
151	DQ55		
152	VSS		
153	DQ56		
154	DQ57		
155	DQ58		
156	DQ59		
157	VDD		
158	DQ60		
159	DQ61		
160	DQ62		
161	DQ63		
162	VSS		
163	NC		
164	NC		
165	SA0		
166	SA1		
167	SA2		
168	VDD		

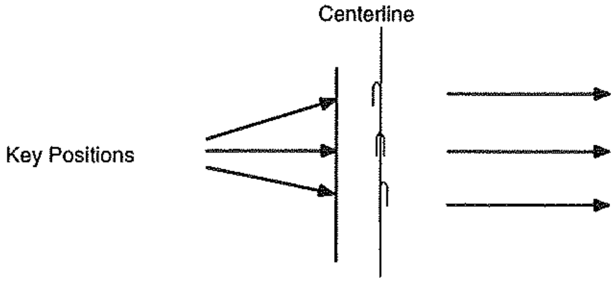
FIGURE 4.5.3–B
64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

2 13

Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins V_{CC} - 16 V_{SS} - 16	35 Power/Gnd Pins V_{CC} - 17 (1 additional pin) V_{SS} - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

FIGURE 4.5.3–C
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM





Left Key	Center Key	*Right Key
RFU	5V	No Key
BUFFERED ASSEMBLY	3.3V	No Key
UNBUFFERED ASSEMBLY	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.

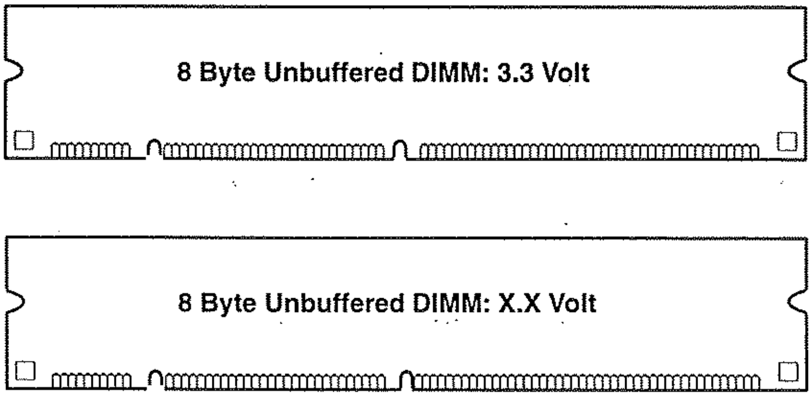


FIGURE 4.5.3–D
168 Pin DRAM DIMM Keying Methodology

31	$\overline{\text{OE}}0$	DU
42	DU	CK0
44	$\overline{\text{OE}}2$	DU
45	$\overline{\text{RAS}}2$	$\overline{\text{S}}2$
46	$\overline{\text{CAS}}2$	DQMB2
47	$\overline{\text{CAS}}3$	DQMB3
48	$\overline{\text{WE}}2$	DU
62	DU	V_{REF} (IF APPLICABLE)
111	DU	$\overline{\text{CAS}}$
112	$\overline{\text{CAS}}4$	DQMB4
113	$\overline{\text{CAS}}5$	DQMB5
114	$\overline{\text{RAS}}1$	$\overline{\text{S}}1$
115	DU	$\overline{\text{RAS}}$
125	DU	CK1
126	DU	A14
128	DU	CKE
129	$\overline{\text{RAS}}3$	$\overline{\text{S}}3$
130	$\overline{\text{CAS}}6$	DQMB6
131	$\overline{\text{CAS}}7$	DQMB7
132	DU	A15
146	DU	V_{REF} (IF APPLICABLE)

Notes:

1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A11 on DRAM DIMM is also BS0 on SDRAM DIMM
3. A12 on DRAM DIMM is also BS1 on SDRAM DIMM (for 4 Bank SDRAMs)

FIGURE 4.5.3–E
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

8 Byte Presence Detect Information

- Serial PD Interface Protocol: IIC (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:

a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		$\overline{\text{RAS}}$ Addr.	$\overline{\text{CAS}}$ Addr.	$\overline{\text{RAS}}$ Addr.	$\overline{\text{CAS}}$ Addr.	$\overline{\text{RAS}}$ Addr.	$\overline{\text{CAS}}$ Addr.
256K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	512K x 8	10	9				
1M x 64/72/80	512K x 8	10	9				
1M x 64/72/80	1M x 4/16	10	10	12	8		
2M x 64/72/80	1M x 4/16	10	10	12	8		
2M x 64/72/80	2M x 8	11	10	12	9		
4M x 64/72/80	2M x 8	11	10	12	9		
4M x 64/72/80	4M x 4/16	11	11	12	10	*13	9
8M x 64/72/80	4M x 4/16	11	11	12	10	*13	9
8M x 64/72/80	8M x 8	12	11	13	10		
16M x 64/72/80	8M x 8	12	11	13	10		
16M x 64/72/80	16M x 4/16	12	12	13	11	*14	10
32M x 64/72/80	16M x 4/16	12	12	13	11	*14	10
32M x 64/72/80	32M x 8	TBD	TBD				
64M x 64/72/80	32M x 8	TBD	TBD				
64M x 64/72/80	64M x 4	TBD	TBD				

(Note: All options possible with DRAM standards are shown)
* This addressing option applies to x16 DRAM configuration

b. Allowable configurations: (Byte 11)

- x64 (Non-parity, Byte controls)
- x72 (Parity, Byte controls)
- x72 (ECC-optimized, Byte controls)
- x80 (ECC-optimized, Byte controls)

c. Functional Attributes:

- Power Supply Voltage/Interface levels (Byte 8)
- $\overline{\text{RAS}}$ access (Byte 9)
- $\overline{\text{CAS}}$ access (Byte 10)
- Refresh rate/type (Byte 12)

Figure 4.5.3–F

168 Pin UNBUFFERED DRAM DIMM SPD ASSIGNMENTS

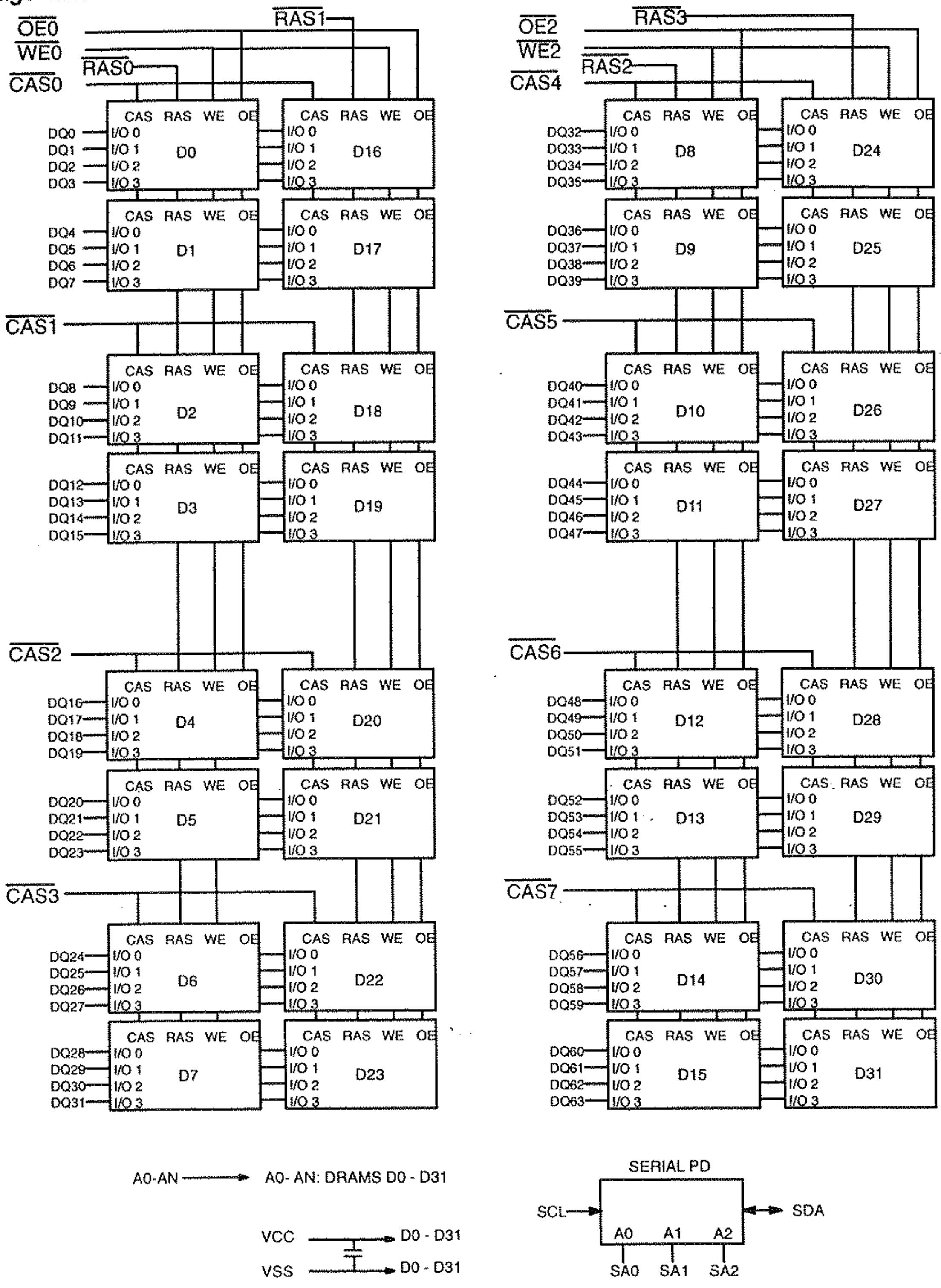


Figure 4.5.3–G
X64 DRAM DIMM, 2 Banks with X4 DRAMs

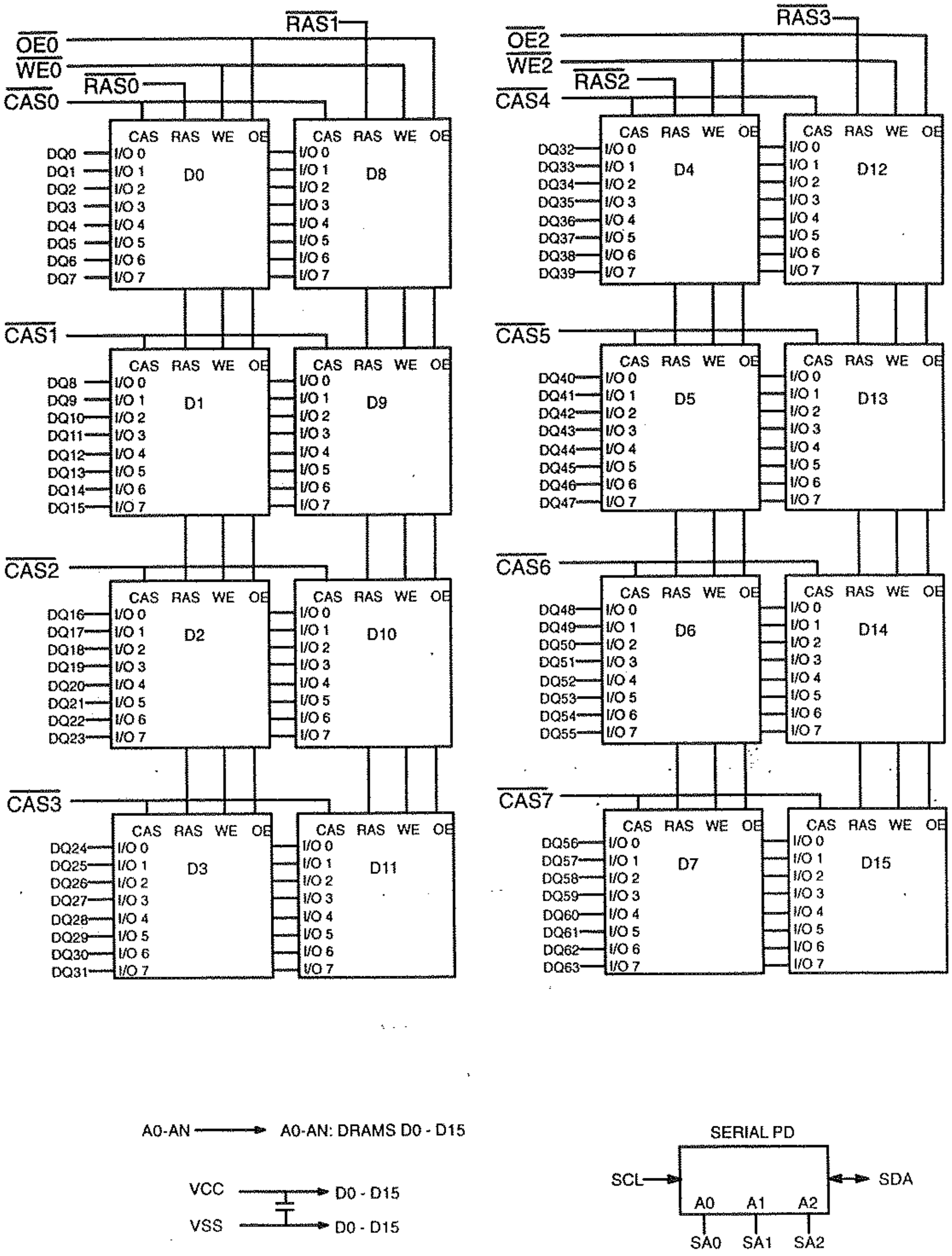


Figure 4.5.3–H
X64 DRAM DIMM, 2 Banks with X8 DRAMs

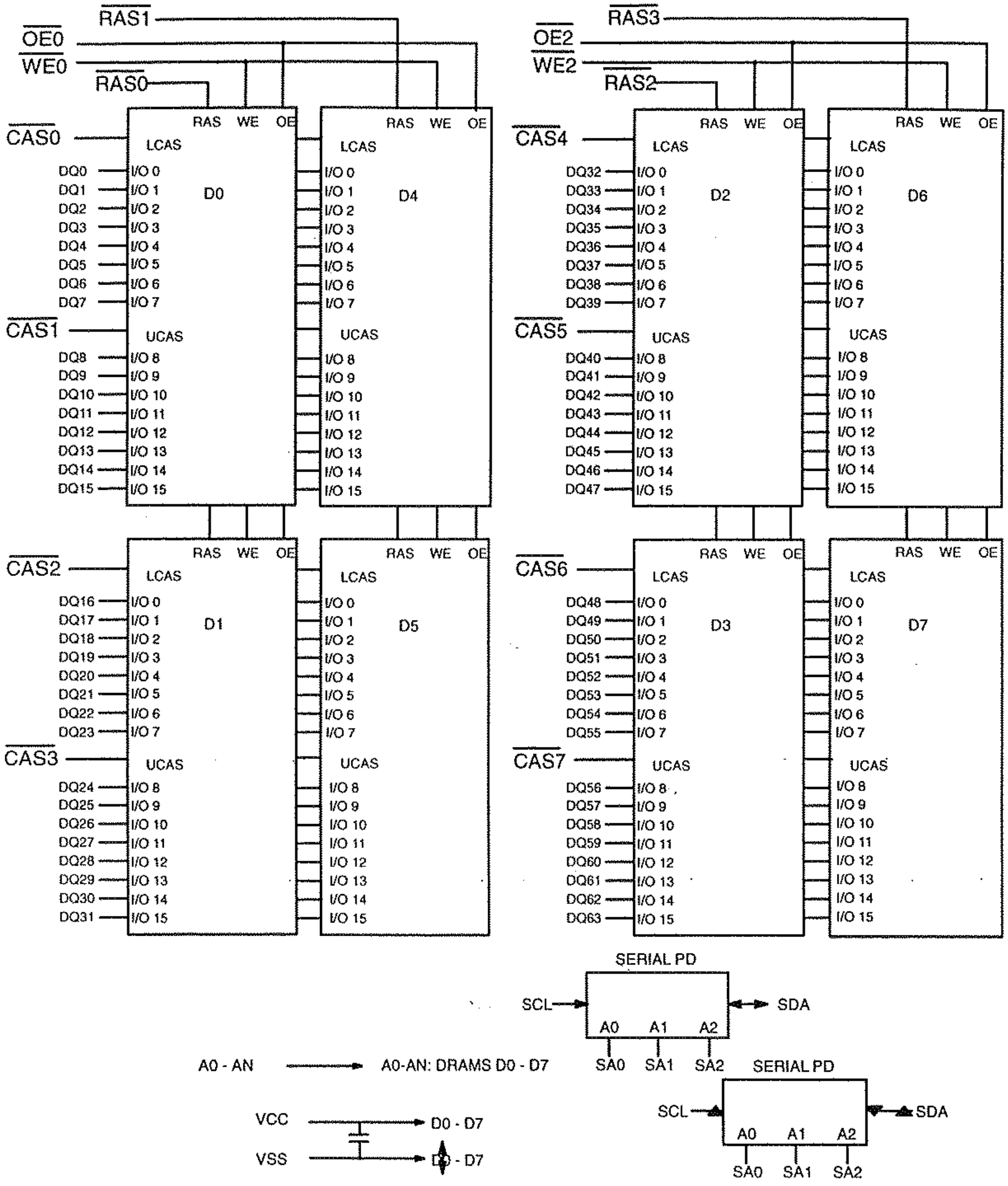


Figure 4.5.3–I
X64 DRAM DIMM, 2 Banks with X16 DRAMs

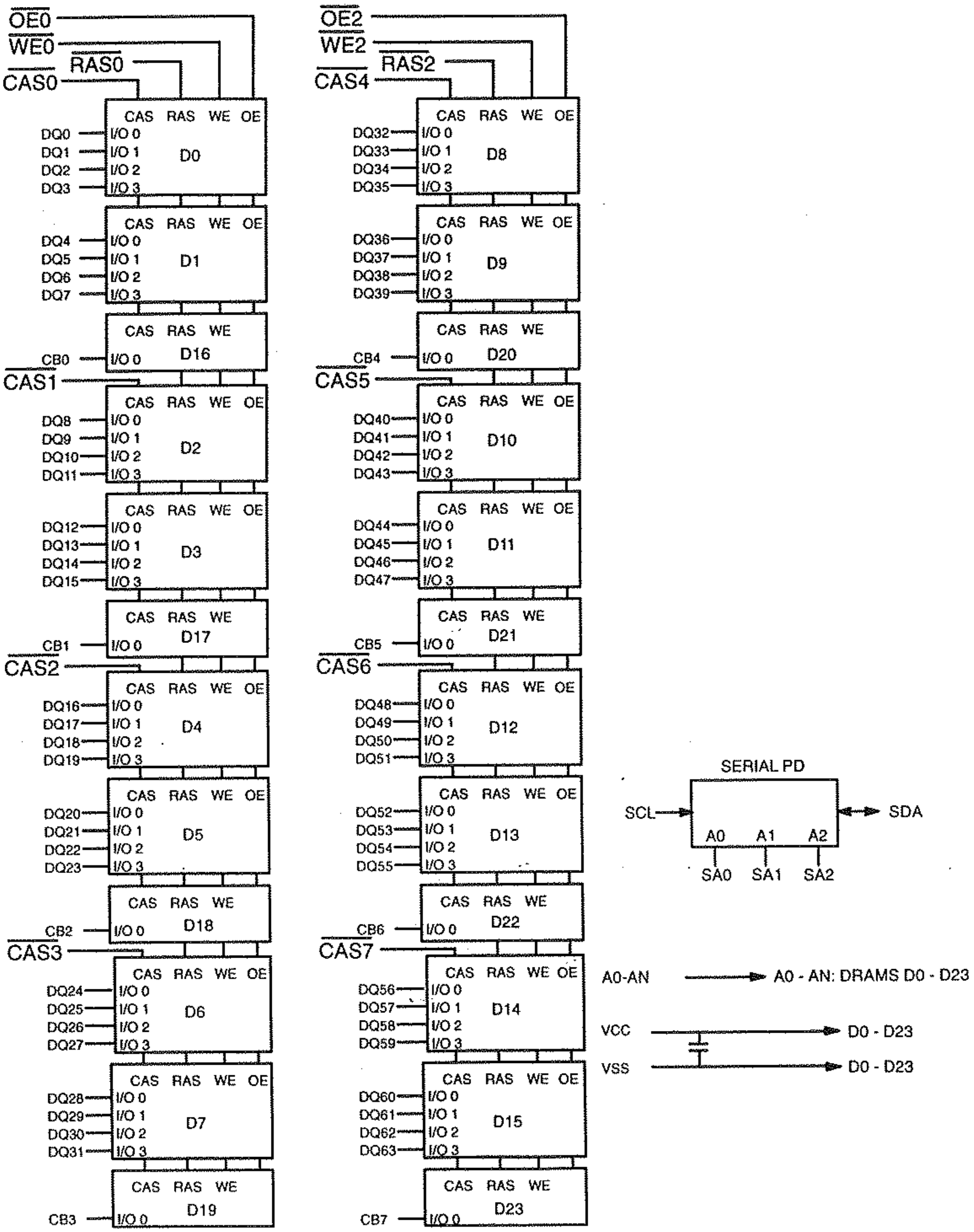


Figure 4.5.3–J
X64 DRAM DIMM, 2 Banks with X4/X1 DRAMs

306

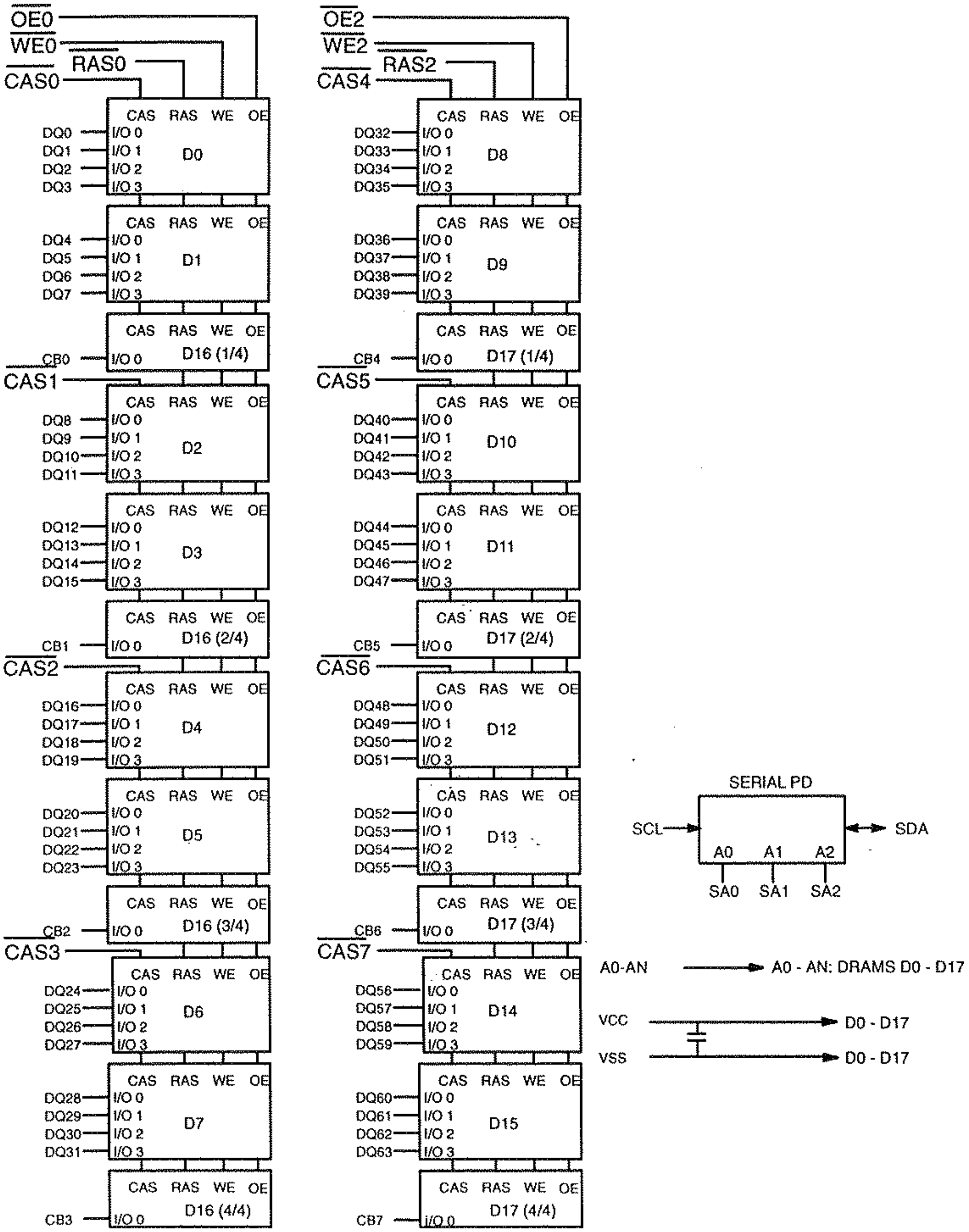


Figure 4.5.3–K
X72 Parity DRAM DIMM, 2 Banks with X4 & X4 W/4 CAS DRAMs

3C1

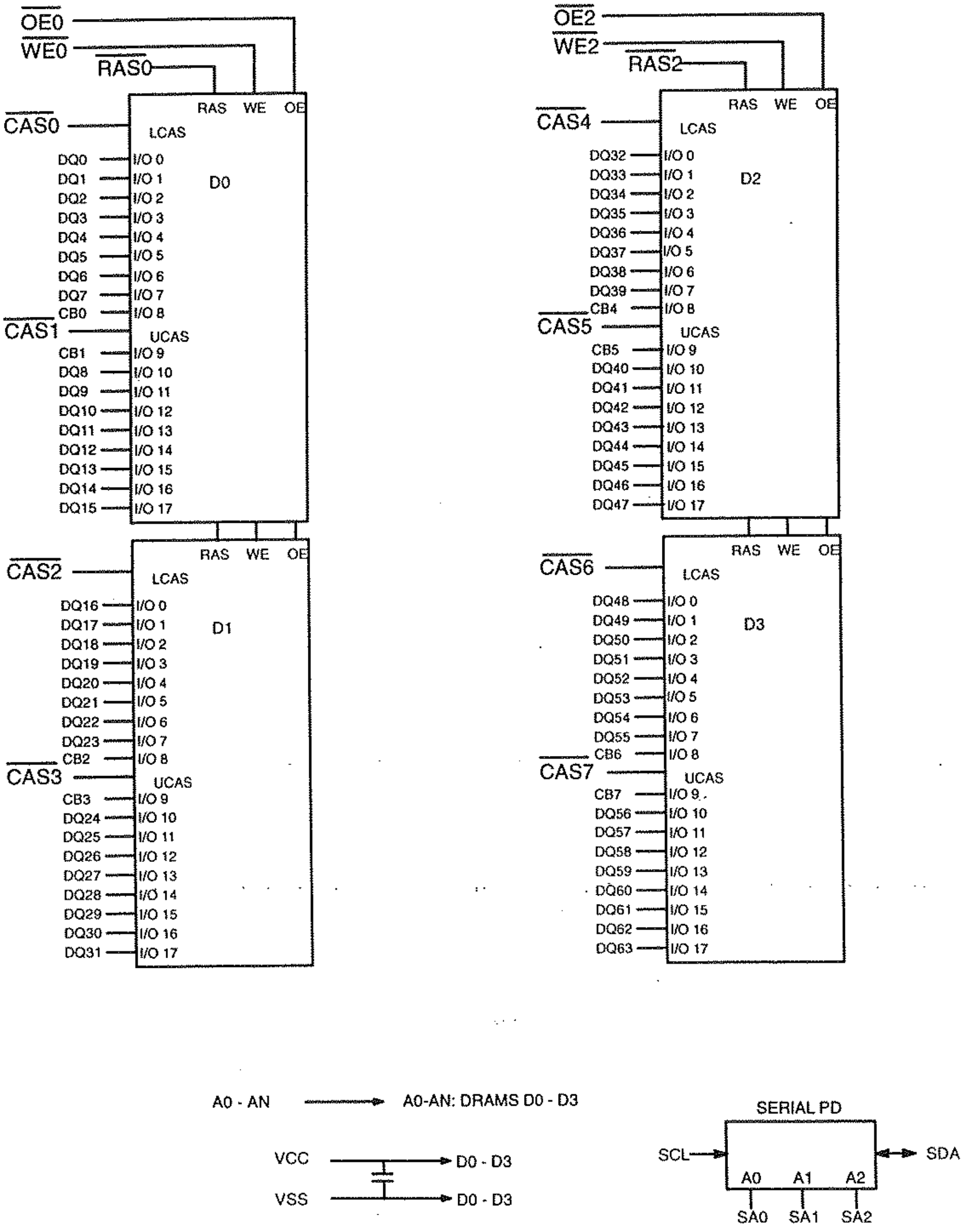


Figure 4.5.3–L
X72 Parity DRAM DIMM, 2 Banks with X16 DRAMs

308

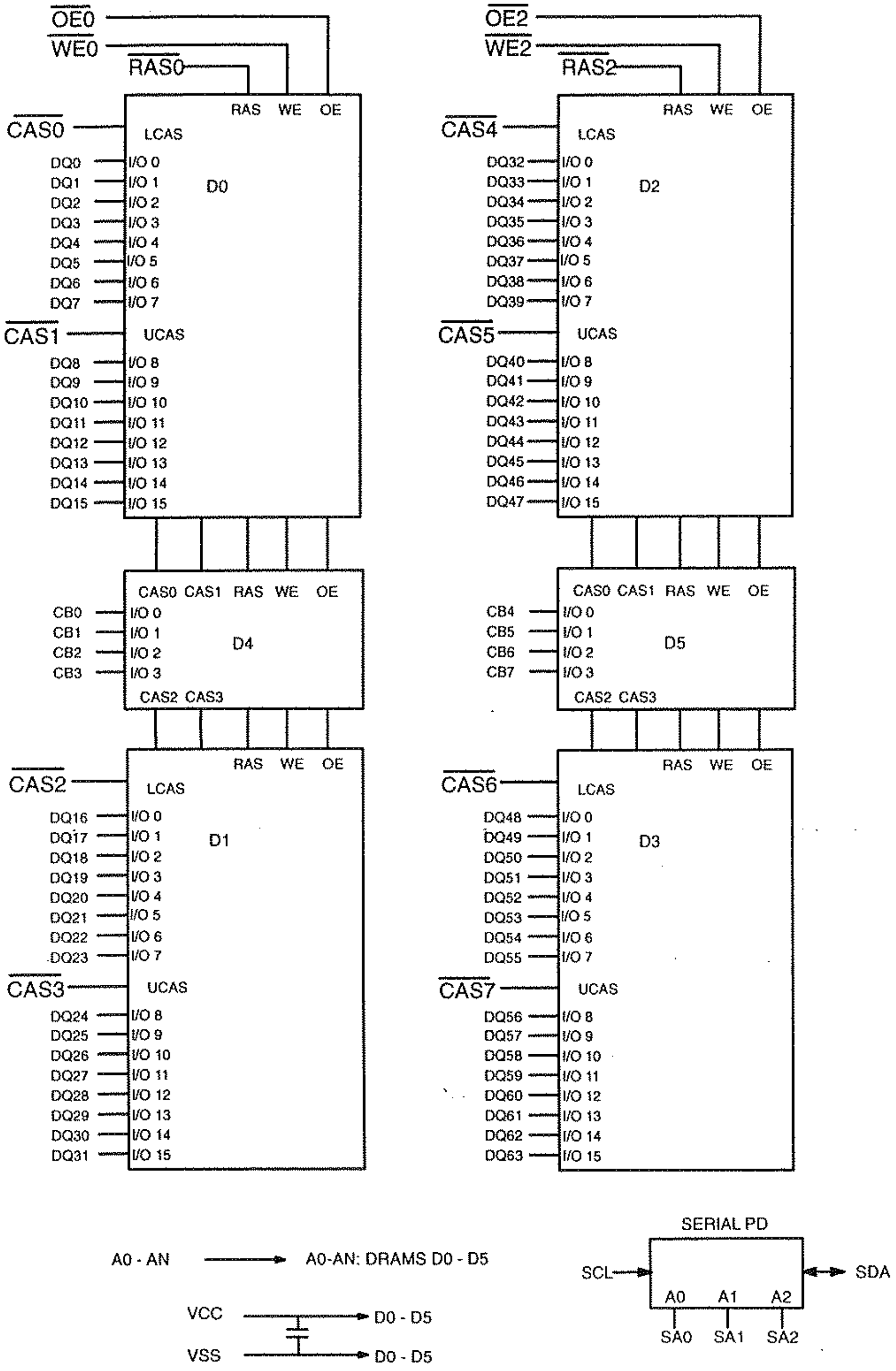


Figure 4.5.3–M
X72 Parity DRAM DIMM, 2 Banks with X16 & X4 W/4 CAS DRAMs

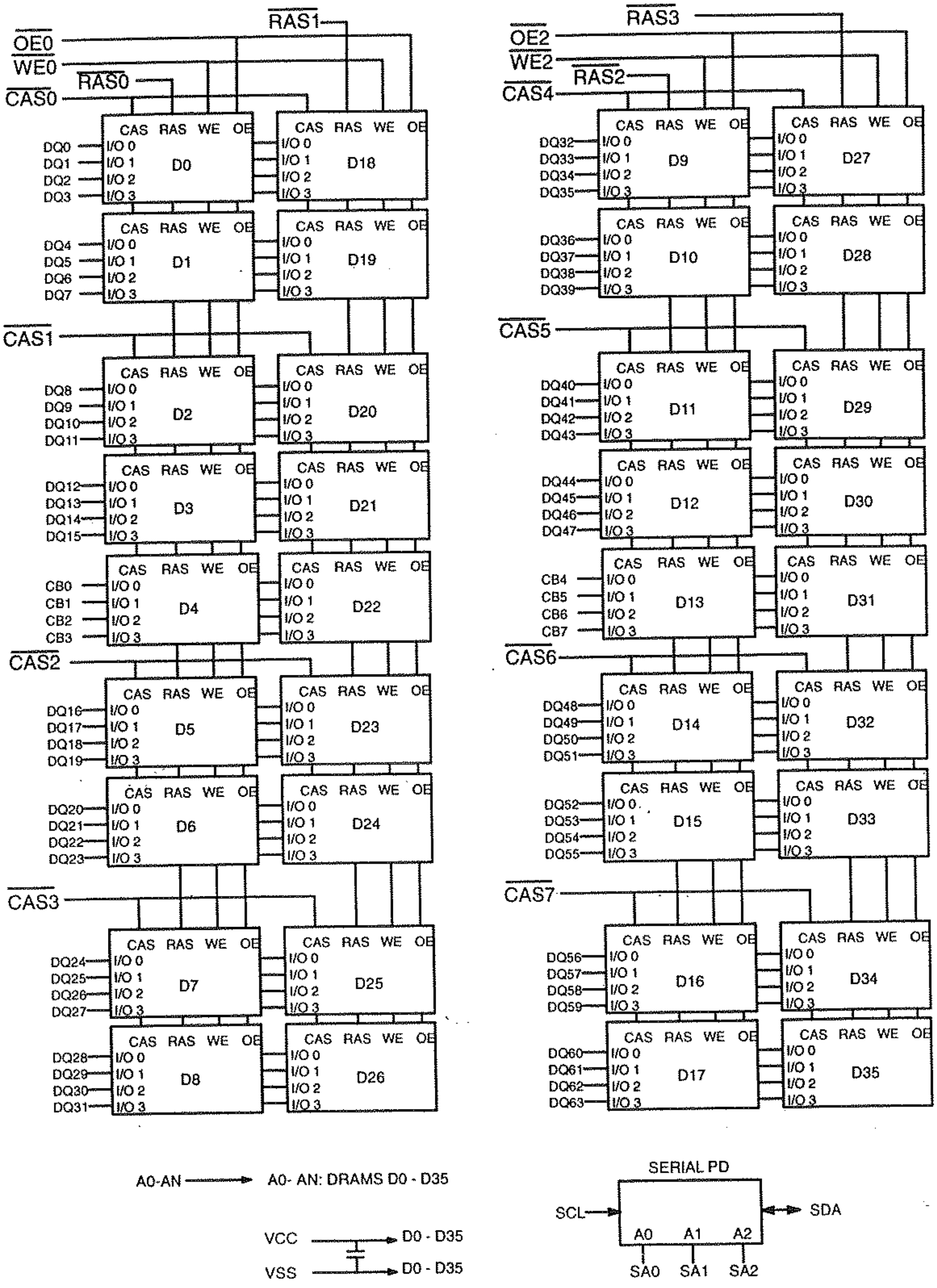


Figure 4.5.3–N
X72 ECC DRAM DIMM, 2 Banks with X4 DRAMs

3ГD

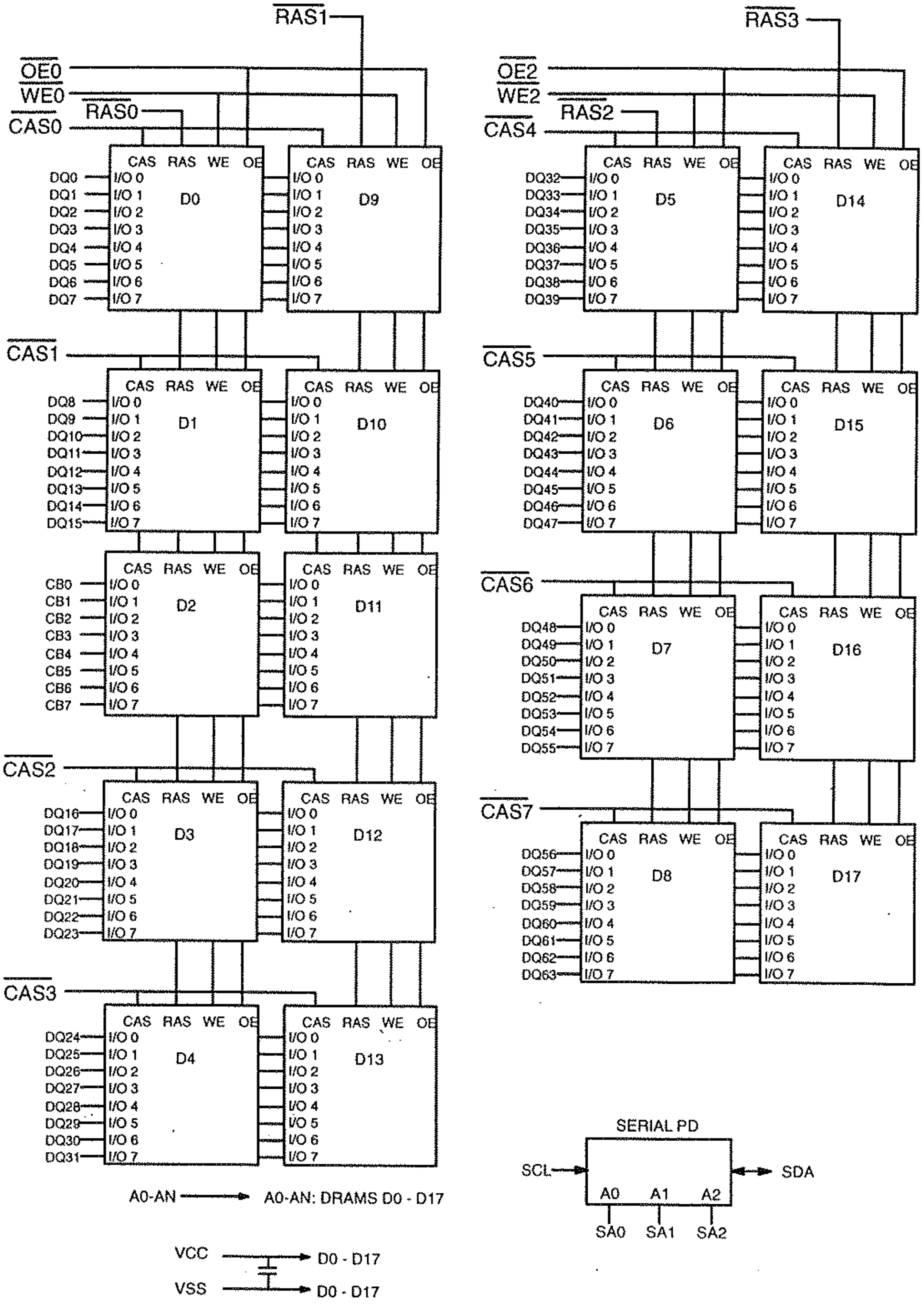


Figure 4.5.3–O
X72 ECC DRAM DIMM, 2 Banks with X8 DRAMs

311

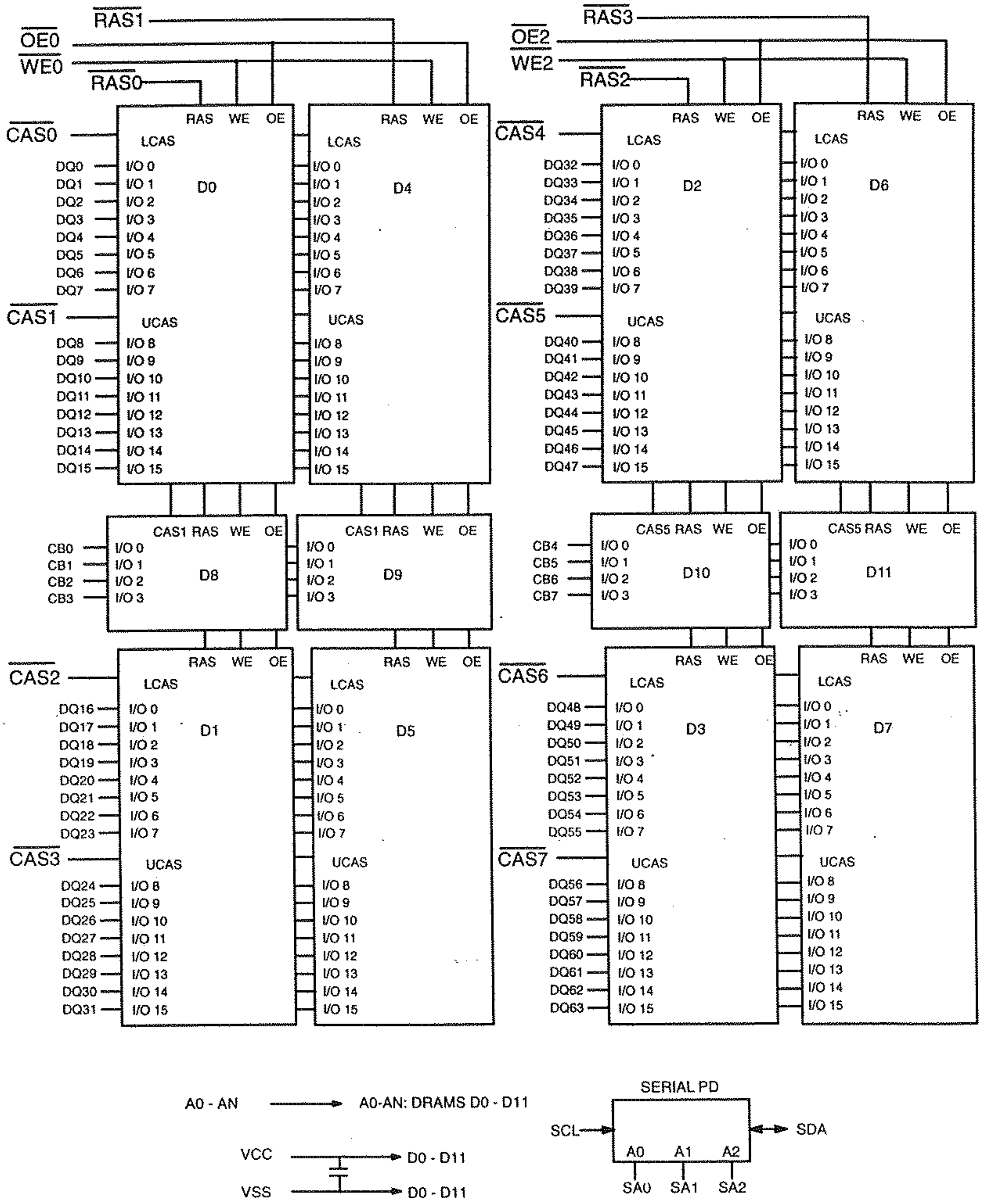


Figure 4.5.3–P
X72 ECC DRAM DIMM, 2 Banks with X16 & X4 DRAMs

315

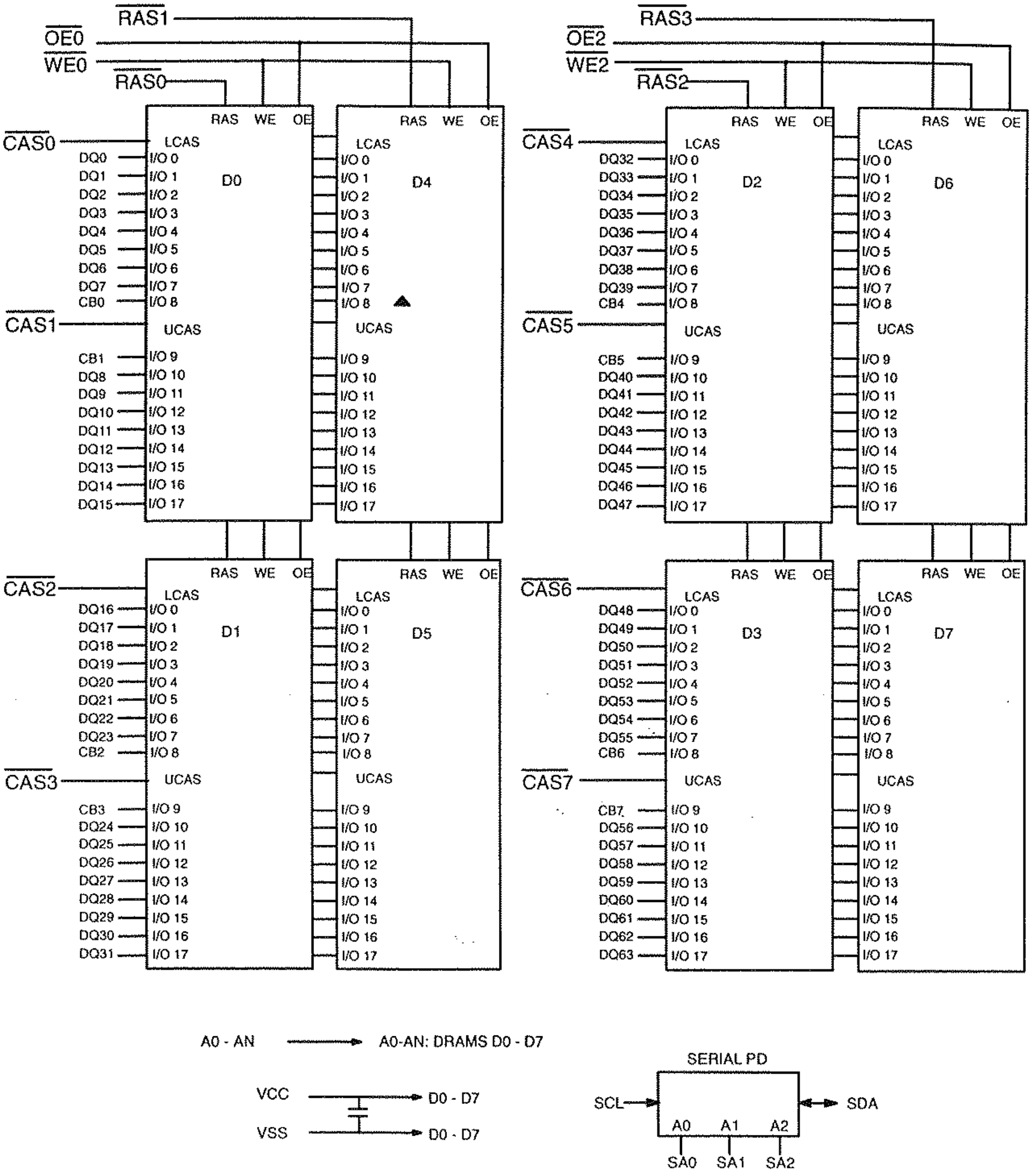


Figure 4.5.3–Q
X72 ECC DRAM DIMM, 2 Banks with X18 DRAMs

313

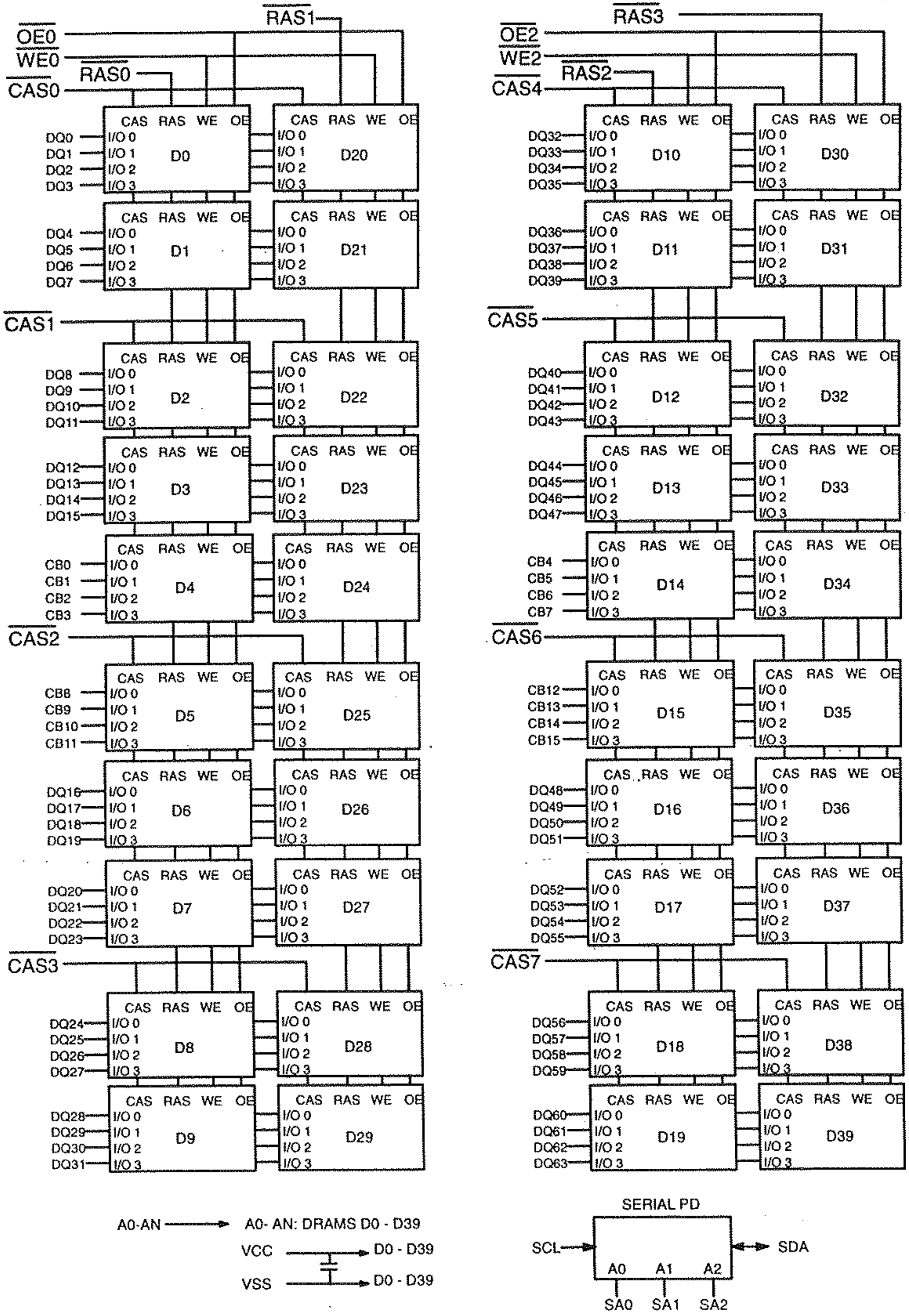


Figure 4.5.3–R
X80 DRAM DIMM, 2 Banks with X4 DRAMs

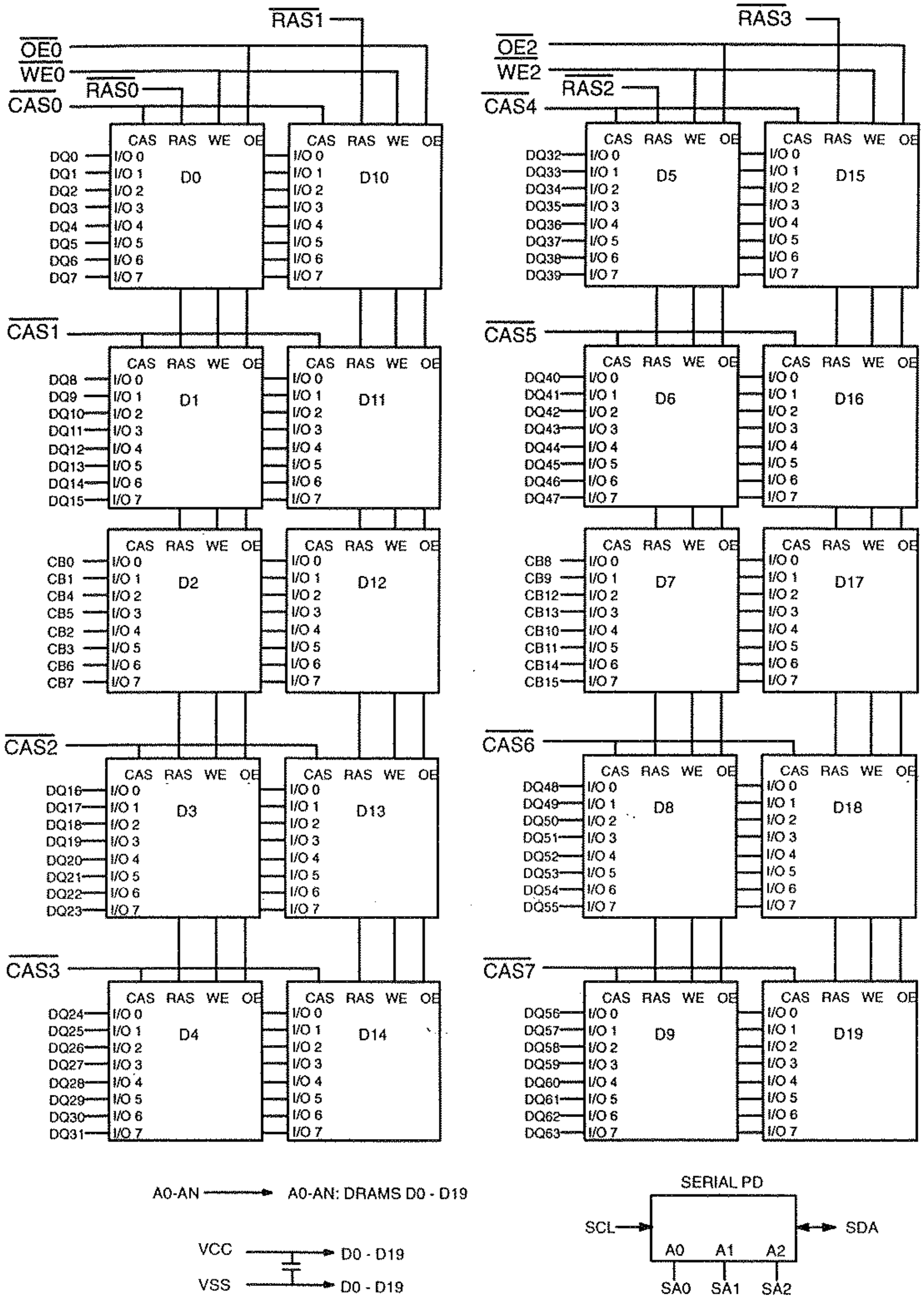


Figure 4.5.3–S

X80 ECC DRAM DIMM, 2 Banks with X8 DRAMs

315

4.5.4 – 168 PIN UNBUFFERED SDRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES
CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memories including 2 bank configurations using X4 devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS—Figs. 4.5.4–A, & 4.5.4–B,
SPD TABLE & INFORMATION—Fig. 4.5.4–C
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM—Fig. 4.5.4–D
KEYING METHODOLOGY—Fig. 4.5.4–E
PINOUT COMPARISON DRAM & SDRAM DIMM—Fig. 4.5.4–F
SDRAM CLOCK LOADING—Fig. 4.5.4–G
SDRAM CLOCK WIRING—Fig. 4.5.4–H
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.4–I through 4.5.4–Y

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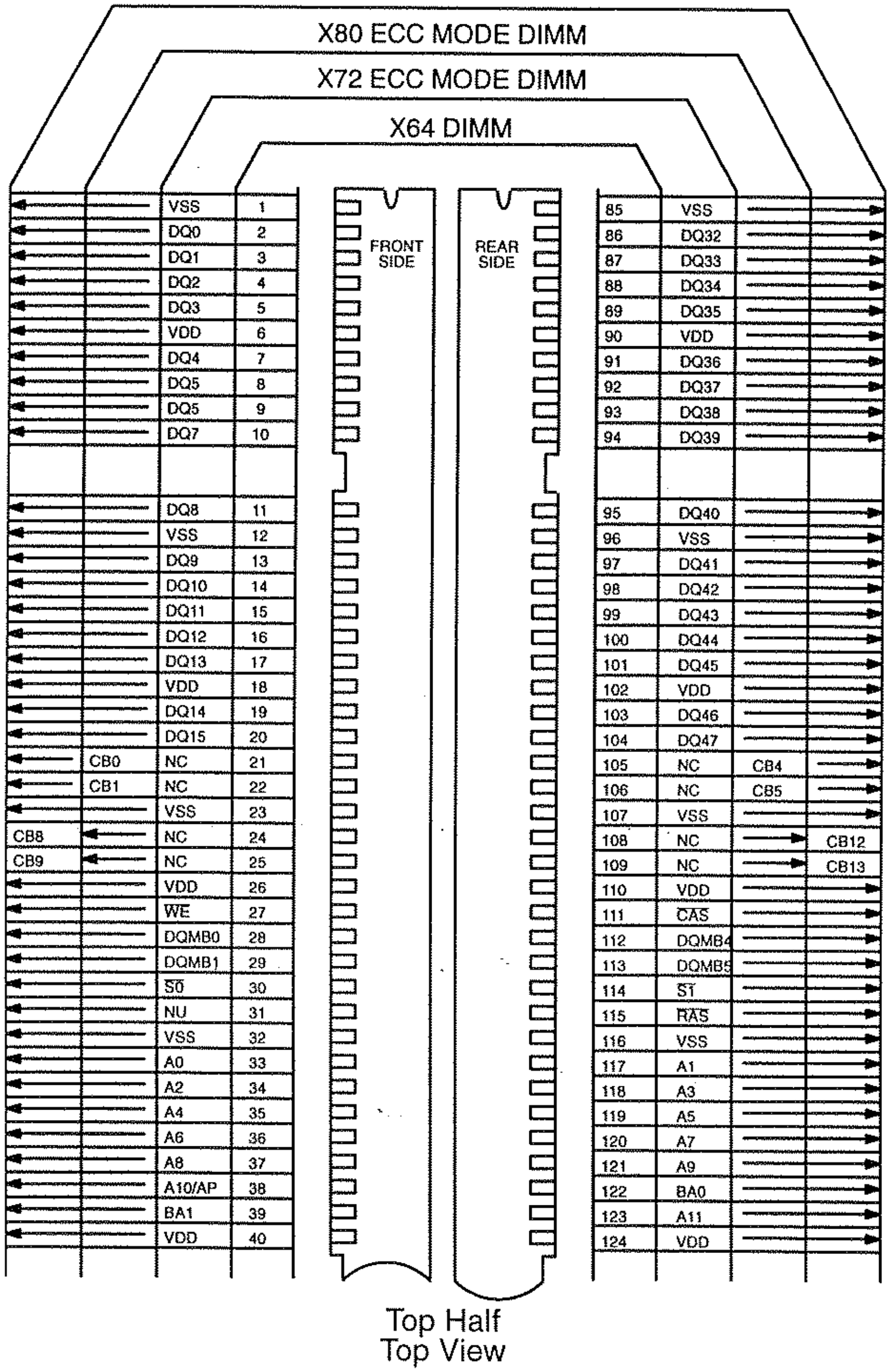

		VSS	1	85	VSS		
		DQ0	2	86	DQ32		
		DQ1	3	87	DQ33		
		DQ2	4	88	DQ34		
		DQ3	5	89	DQ35		
		VDD	6	90	VDD		
		DQ4	7	91	DQ36		
		DQ5	8	92	DQ37		
		DQ5	9	93	DQ38		
		DQ7	10	94	DQ39		
		DQ8	11	95	DQ40		
		VSS	12	96	VSS		
		DQ9	13	97	DQ41		
		DQ10	14	98	DQ42		
		DQ11	15	99	DQ43		
		DQ12	16	100	DQ44		
		DQ13	17	101	DQ45		
		VDD	18	102	VDD		
		DQ14	19	103	DQ46		
		DQ15	20	104	DQ47		
	CB0	NC	21	105	NC	CB4	
	CB1	NC	22	106	NC	CB5	
		VSS	23	107	VSS		
CB8		NC	24	108	NC		CB12
CB9		NC	25	109	NC		CB13
		VDD	26	110	VDD		
		$\overline{WE}$	27	111	$\overline{CAS}$		
		DQMB0	28	112	DQMB4		
		DQMB1	29	113	DQMB5		
		$\overline{S0}$	30	114	$\overline{S1}$		
		NU	31	115	$\overline{RAS}$		
		VSS	32	116	VSS		
		A0	33	117	A1		
		A2	34	118	A3		
		A4	35	119	A5		
		A6	36	120	A7		
		A8	37	121	A9		
		A10/AP	38	122	BA0		
		BA1	39	123	A11		
		VDD	40	124	VDD		

FIGURE 4.5.4–A

168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF

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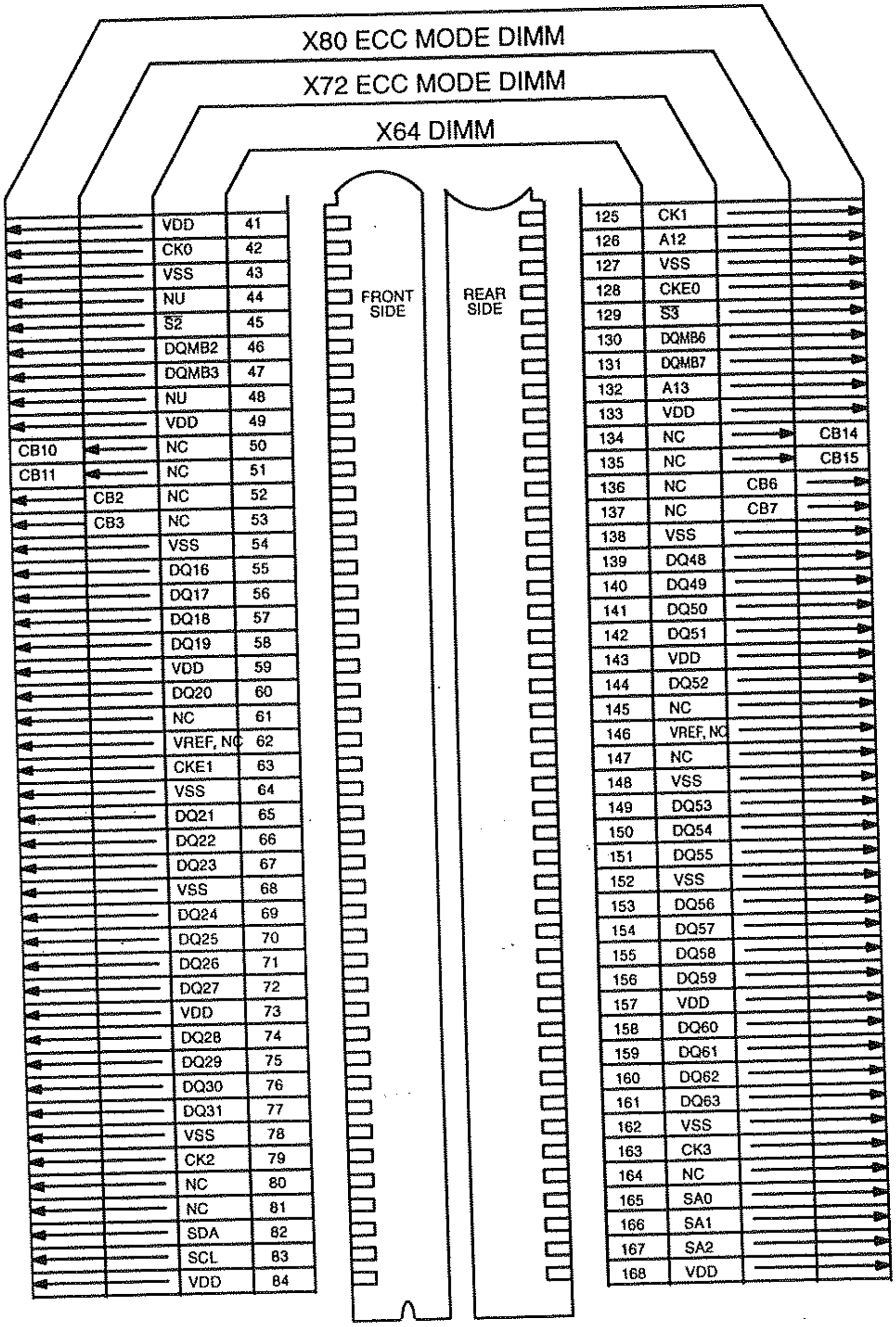


Pin	X64 DIMM	X72 ECC MODE DIMM	X80 ECC MODE DIMM
41	VDD		
42	CK0		
43	VSS		
44	NU		
45	$\overline{S2}$		
46	DQMB2		
47	DQMB3		
48	NU		
49	VDD		
50	NC		CB10
51	NC		CB11
52	NC	CB2	
53	NC	CB3	
54	VSS		
55	DQ16		
56	DQ17		
57	DQ18		
58	DQ19		
59	VDD		
60	DQ20		
61	NC		
62	VREF, NC		
63	CKE1		
64	VSS		
65	DQ21		
66	DQ22		
67	DQ23		
68	VSS		
69	DQ24		
70	DQ25		
71	DQ26		
72	DQ27		
73	VDD		
74	DQ28		
75	DQ29		
76	DQ30		
77	DQ31		
78	VSS		
79	CK2		
80	NC		
81	NC		
82	SDA		
83	SCL		
84	VDD		

Pin	X64 DIMM	X72 ECC MODE DIMM	X80 ECC MODE DIMM
125	CK1		
126	A12		
127	VSS		
128	CKE0		
129	$\overline{S3}$		
130	DQMB6		
131	DQMB7		
132	A13		
133	VDD		
134	NC		CB14
135	NC		CB15
136	NC	CB6	
137	NC	CB7	
138	VSS		
139	DQ48		
140	DQ49		
141	DQ50		
142	DQ51		
143	VDD		
144	DQ52		
145	NC		
146	VREF, NC		
147	NC		
148	VSS		
149	DQ53		
150	DQ54		
151	DQ55		
152	VSS		
153	DQ56		
154	DQ57		
155	DQ58		
156	DQ59		
157	VDD		
158	DQ60		
159	DQ61		
160	DQ62		
161	DQ63		
162	VSS		
163	CK3		
164	NC		
165	SA0		
166	SA1		
167	SA2		
168	VDD		

Bottom Half
Top View

FIGURE 4.5.4-B
168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank accr.	$\overline{\text{RAS}}$ accr.	$\overline{\text{CAS}}$ accr.	# Bank accr.	$\overline{\text{RAS}}$ accr.	$\overline{\text{CAS}}$ accr.	# Bank accr.	$\overline{\text{RAS}}$ accr.	$\overline{\text{CAS}}$ accr.
1M x 64/72/80	1M x 16	1	11	8						
2M x 64/72/80	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72/80	2M x 8	1	11	9						
4M x 64/72/80	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72/80	4M x 4	1	11	10						
4M x 64/72/80	4M x 16	2	12	8	1	13	8			
8M x 64/72/80	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72/80	16M x 4	2	12	10	1	13	10			
16M x 64/72/80	16M x 16	2	13	9						
32M x 64/72/80	16M x 16	2	13	9						
32M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	64M x 4	2	13	11						
(Note: All options possible with SDRAM standards are shown)										

b. Allowable configurations: (Byte 11)
  - x64 (Non-parity, Byte controls)
  - x72 (ECC-optimized, Byte controls)
  - x80 (ECC-optimized, Byte controls)

c. Functional Attributes:
  - Power Supply Voltage/Interface levels (Byte 8)
  - SDRAM cycle time (Byte 9)
  - SDRAM access from Clock (Byte 10)
  - Refresh rate/type (Byte 12)
  - SDRAM module attributes (Byte 13)
  - SDRAM device attributes (Bytes 14 - 20)
  - Primary/Secondary DRAM (Bytes 21 - 22)

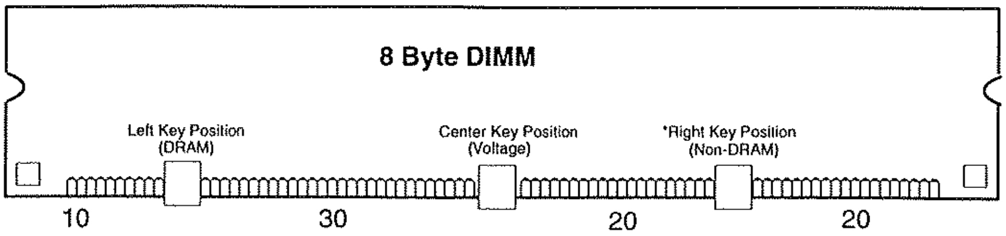
Figure 4.5.4–C
168 Pin UNBUFFERED DRAM DIMM SPD ASSIGNMENTS

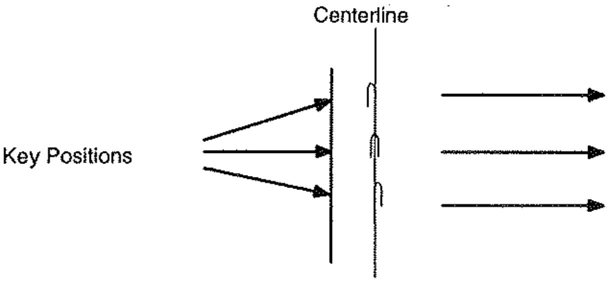
Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins VCC - 16 VSS - 16	35 Power/Gnd Pins VCC - 17 (1 additional pin) VSS - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD. DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

FIGURE 4.5.4–D

Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM

320





Left Key	Center Key	*Right Key
RFU	5V	No Key
BUFFERED ASSEMBLY	3.3V	No Key
UNBUFFERED ASSEMBLY	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.

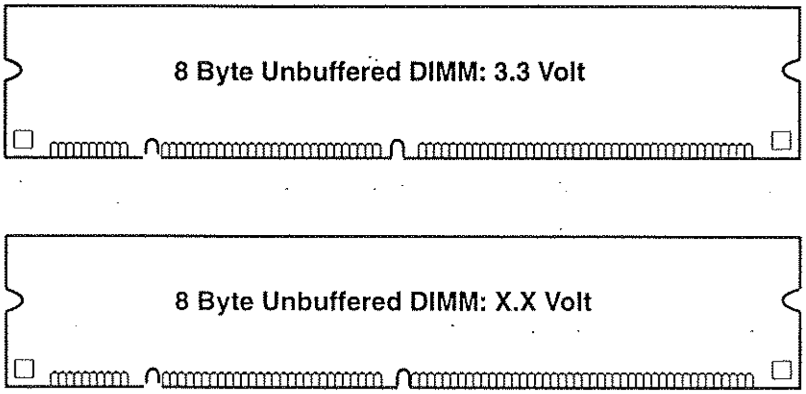


FIGURE 4.5.4–E
168 Pin DRAM DIMM Keying Methodology

Pin number	DRAM DIMM	SDRAM DIMM
39	A12	BA1
42	DU	CK0
44	$\overline{\mathrm{OE}}2$	DU
45	$\overline{\mathrm{RAS}}2$	$\overline{\mathrm{S}}2$
46	$\overline{\mathrm{CAS}}2$	DQMB2
47	$\overline{\mathrm{CAS}}3$	DQMB3
48	$\overline{\mathrm{WE}}2$	DU
62	DU	V_{REF}, NC
63	NC	CKE1
79	NC	CK2
111	DU	$\overline{\mathrm{CAS}}$
112	$\overline{\mathrm{CAS}}4$	DQMB4
113	$\overline{\mathrm{CAS}}5$	DQMB5
114	$\overline{\mathrm{RAS}}1$	$\overline{\mathrm{S}}1$
115	DU	$\overline{\mathrm{RAS}}$
122	A11	BA0
123	A13	A11
125	DU	CK1
126	DU	A12
128	DU	CKE0
129	$\overline{\mathrm{RAS}}3$	$\overline{\mathrm{S}}3$
130	$\overline{\mathrm{CAS}}6$	DQMB6
131	$\overline{\mathrm{CAS}}7$	DQMB7
132	DU	A13
146	DU	V_{REF}, NC
163	NC	CK3

Notes:

1. A10 on DRAM DIMM is also AP on SDRAM DIMM

FIGURE 4.5.4–F
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

X 64 (Non–parity)

SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
x4	1	16	4	4	4	4
x8	1	8	4	4	*	*
x16	1	4	4	*	*	*
x32	1	2	*2	*	*	*
x8	2	16	4	4	4	4
x16	2	8	4	4	*	*
x32	2	4	4	*	*	*

X 72 (ECC)

SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
x4	1	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
x8	1	9	** 4 or 5	** 4 or 5	*	*
x16/x4	1	6	4 (MAX)	4 (MAX)	*	*
x32/x8	1	3	*3	*	*	*
x8	2	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
x16/x4	2	12	4	4	4	
x32/x8	2	6	4 (MAX)	4 (MAX)	*	*

X 80 (ECC)

SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
x4	1	20	5	5	5	5
x8	1	10	5	5	*	*
x16	1	5	5	*	*	*
x32/x8	1	4	4	*	*	*
x8	2	20	5	5	5	5
x16	2	10	5	5	*	*
x32/x8	2	8	4	4	*	*

Notes:

* add padding capacitance per clock wiring detail.

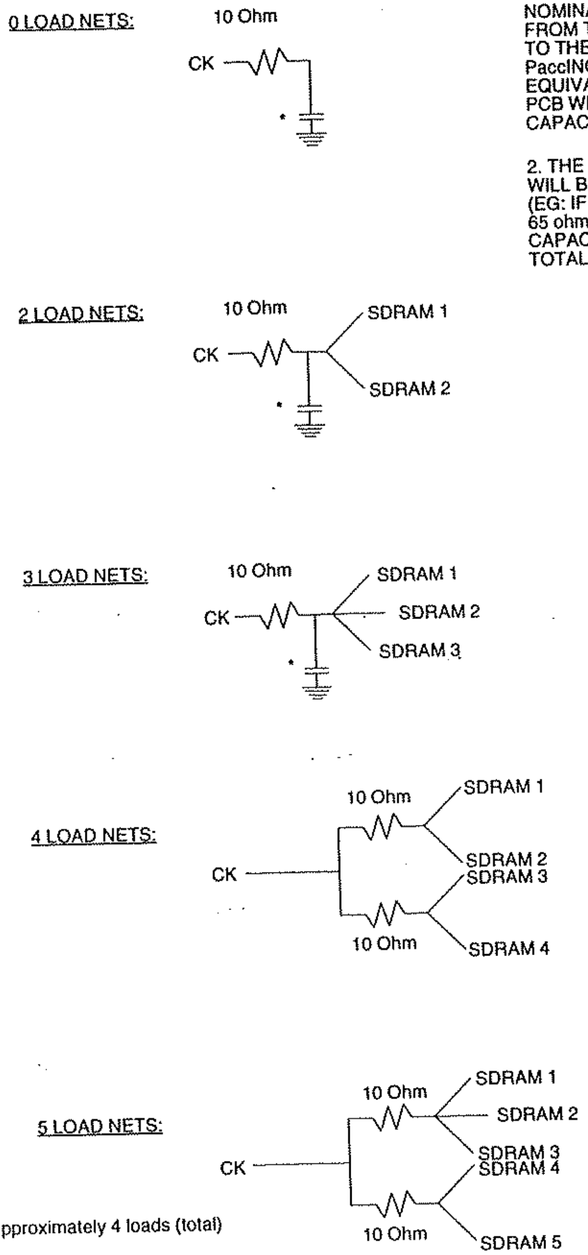
** CK0 + CK2 must total 9 SDRAMs, CK1 + CK3 must total 9 SDRAMs (to allow clock “dotting” at system).

Figure 4.5.4–G
168 Pin UNBUFFERED SDRAM DIMM CLOCK LOADING

TARGET CLOCK (CK) SPECIFICATION:

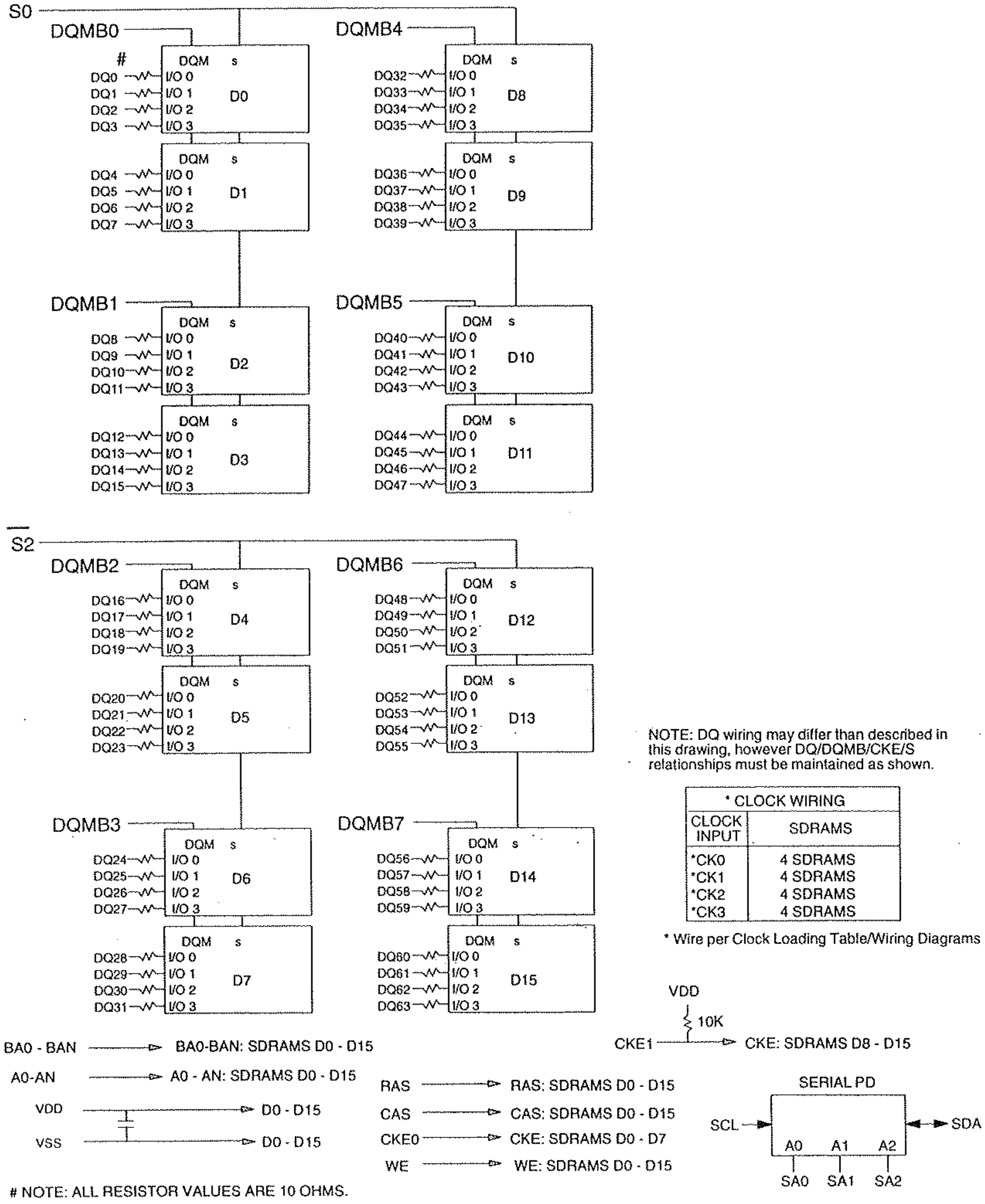
1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .6ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PaccING CAPACITOR). (EG: THIS IS EQUIVALENT TO APPROXIMATELY 3" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2. THE VARIATION OF CK INPUT DELAY WILL BE +/- .1ns FOR ALL FOUR CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/- 3pf IN TOTAL CK INPUT CAPACITANCE).



* add padding capacitance to approximately 4 loads (total)

Figure 4.5.4–H
168 Pin UNBUFFERED DRAM DIMM CLOCK WIRING



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

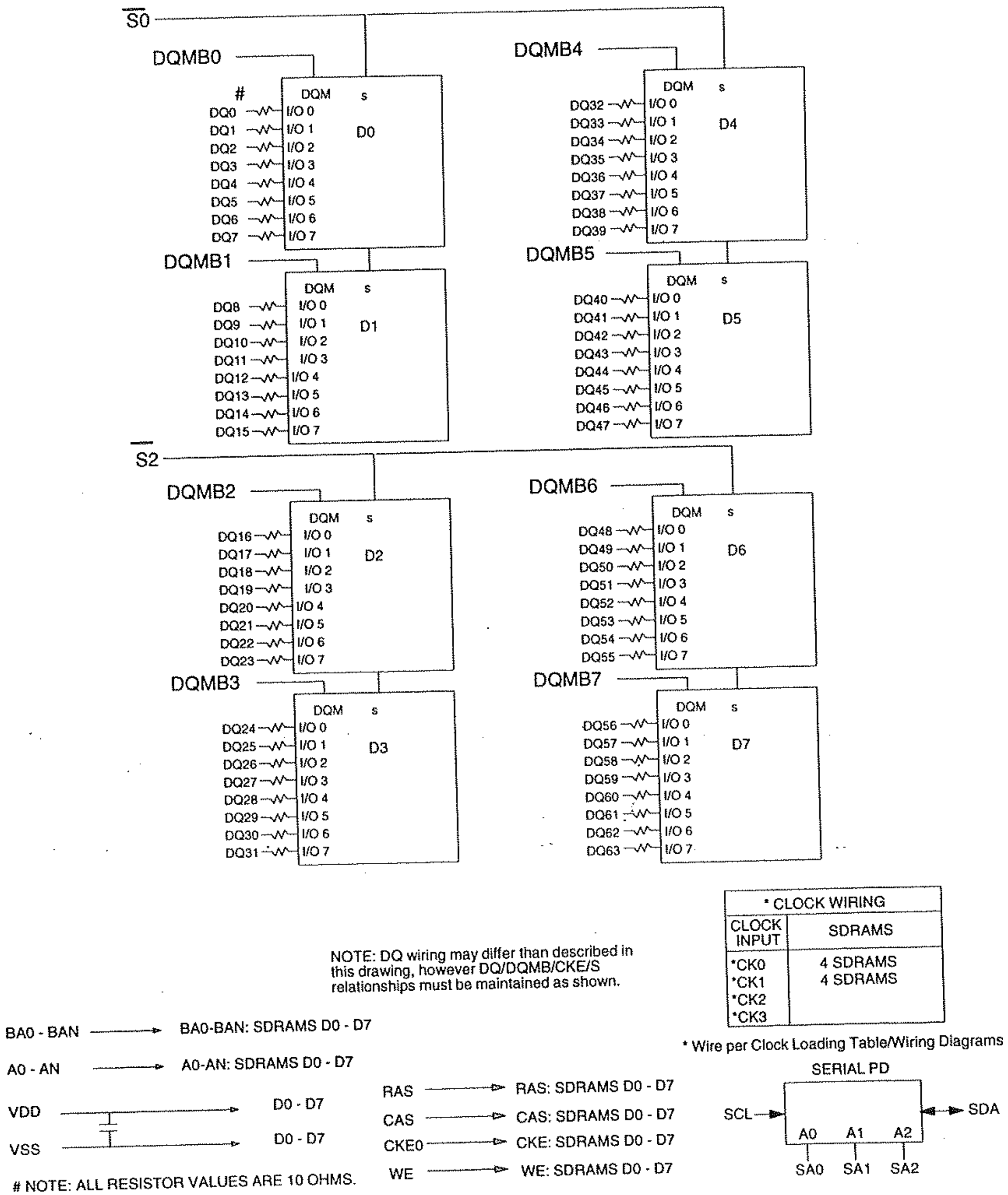
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	4 SDRAMS
*CK3	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–I
X64 SDRAM DIMM, 1 Bank with X4 SDRAMs

325



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

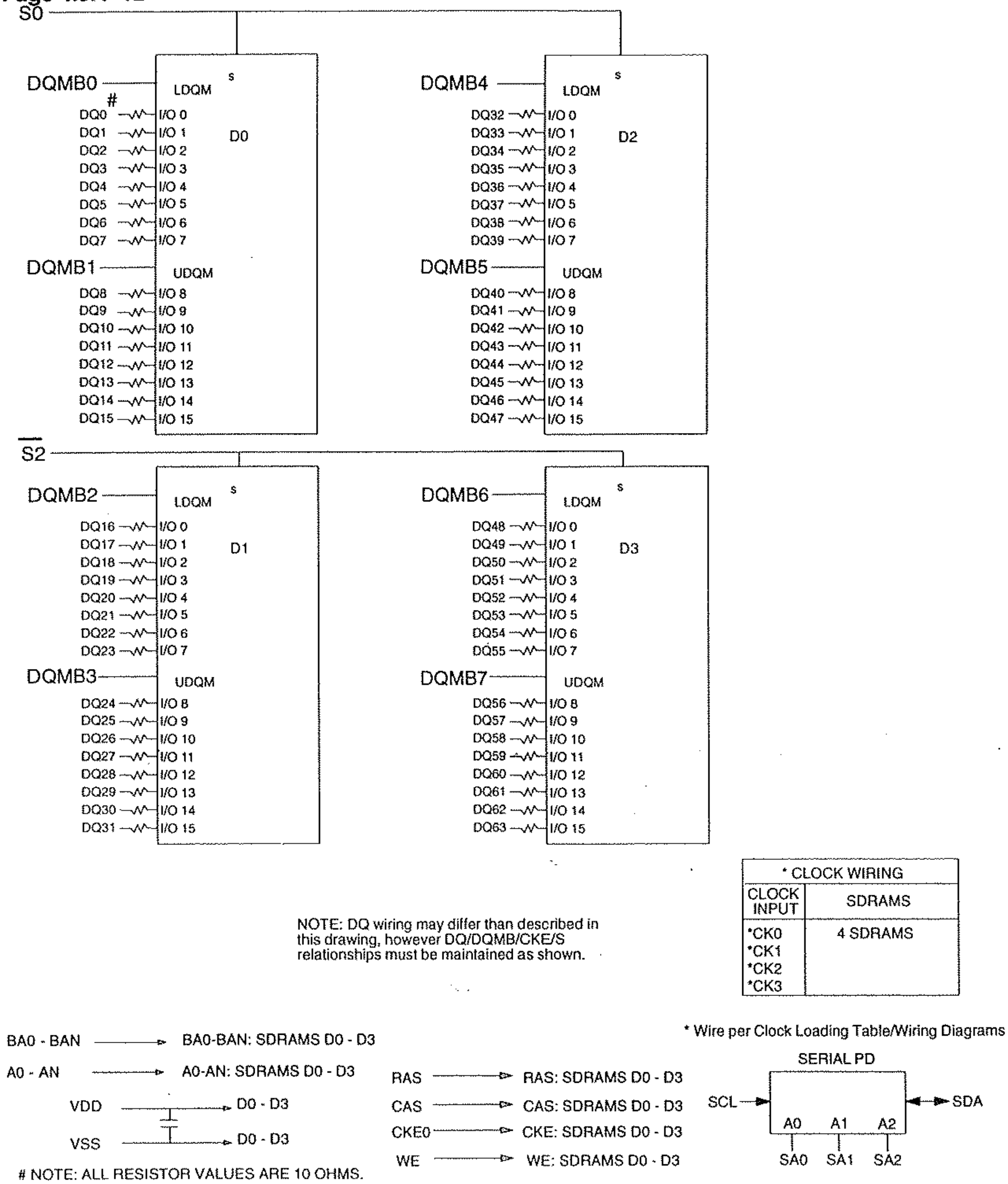
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–J
X64 SDRAM DIMM, 1 Bank with X8 SDRAMs

326



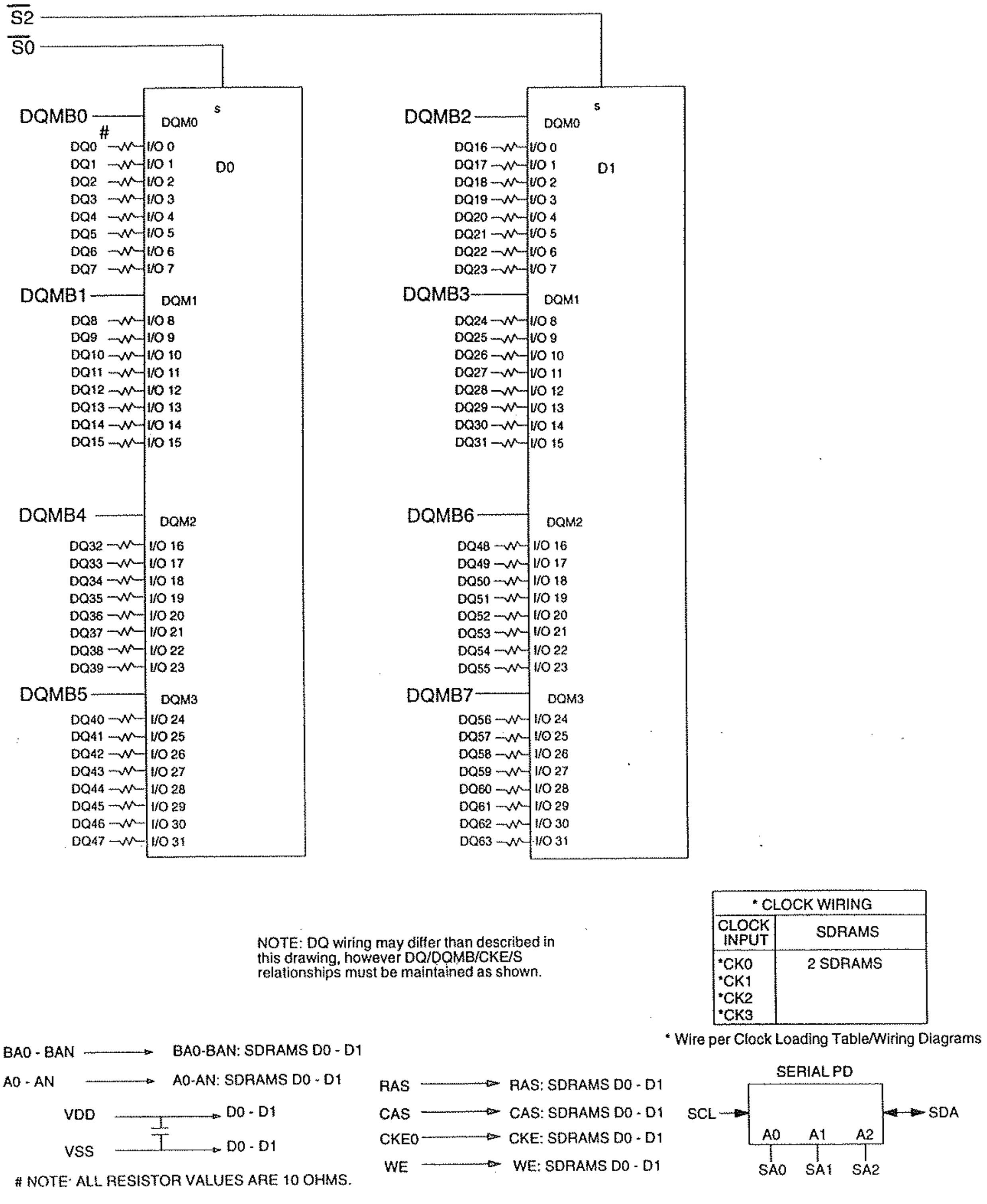
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–K
X64 SDRAM DIMM, 1 Bank with X16 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

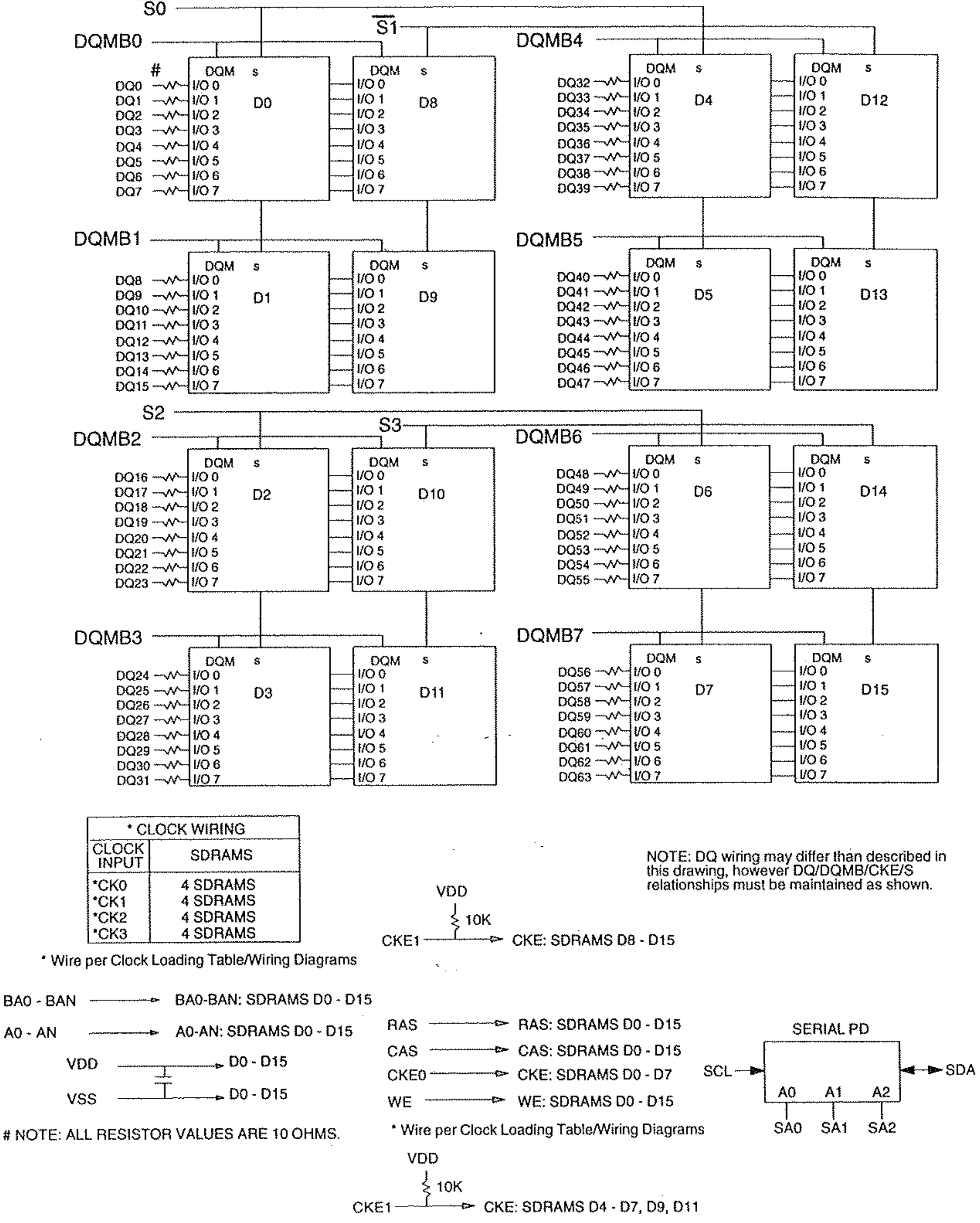
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	2 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–L
X64 SDRAM DIMM, 1 Bank with X32 SDRAMs

355



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	4 SDRAMS
*CK3	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

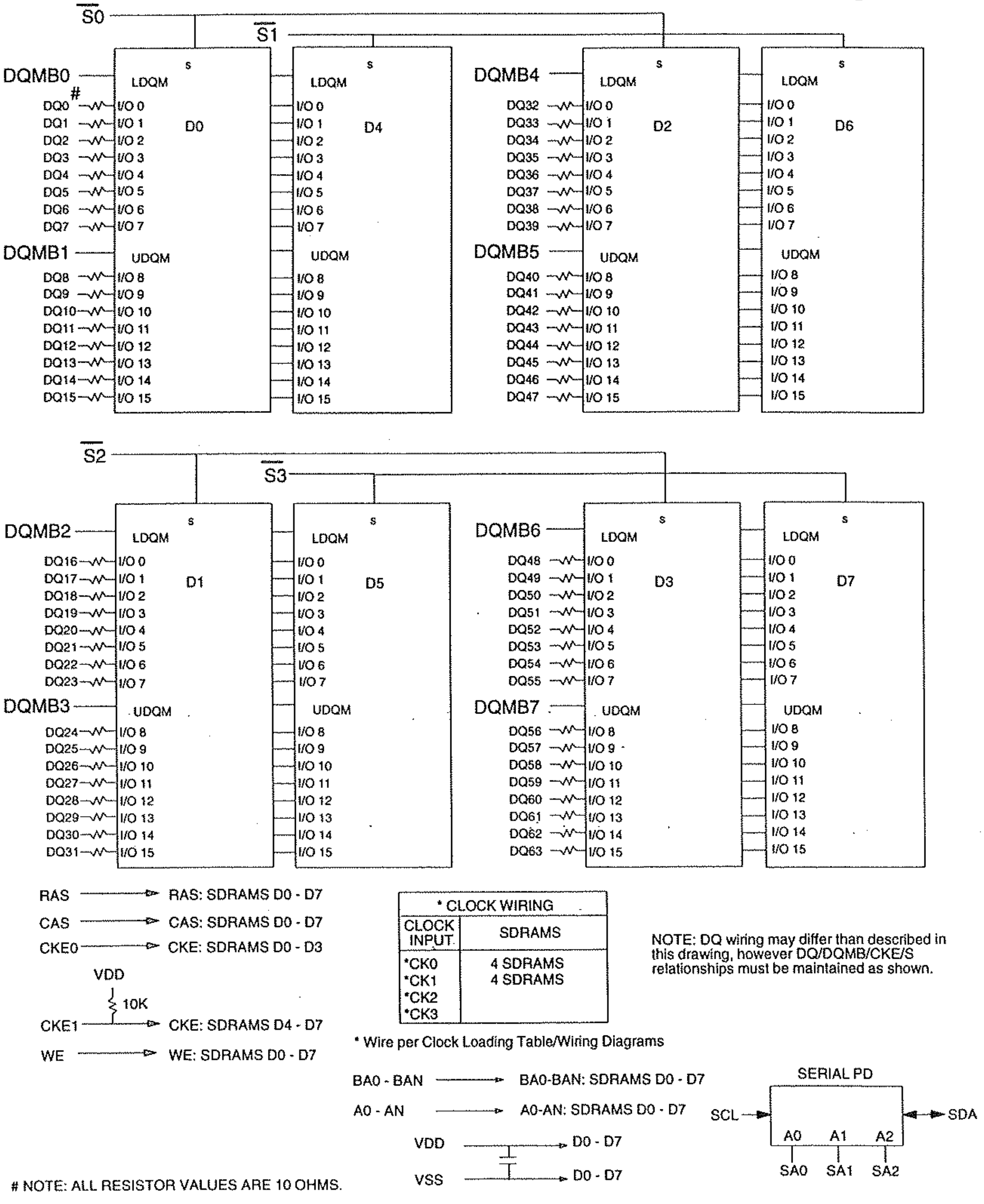
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.4–M
X64 SDRAM DIMM, 2 Banks with X8 SDRAMs

359



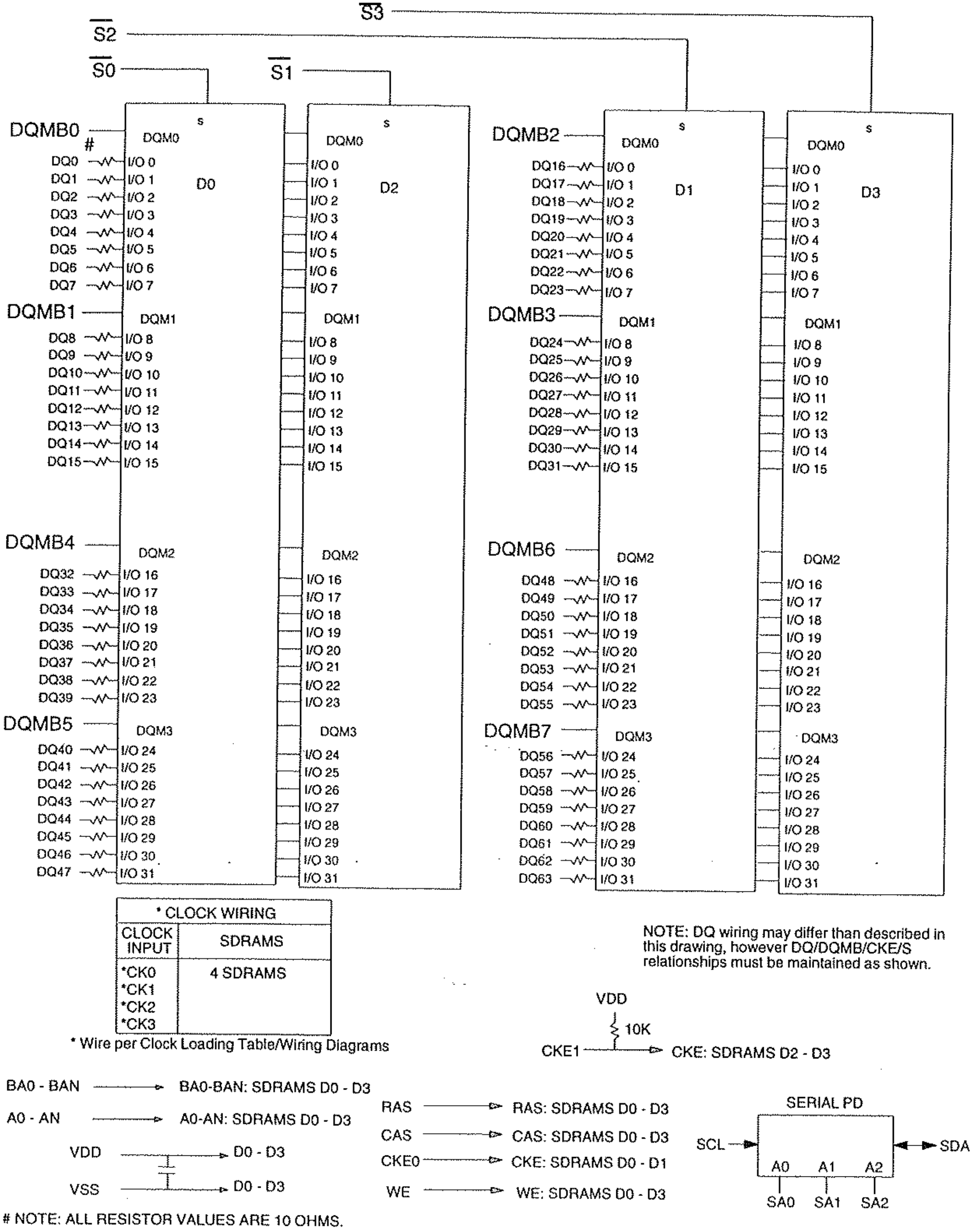
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–N
X64 SDRAM DIMM, 2 Banks with X16 SDRAMs



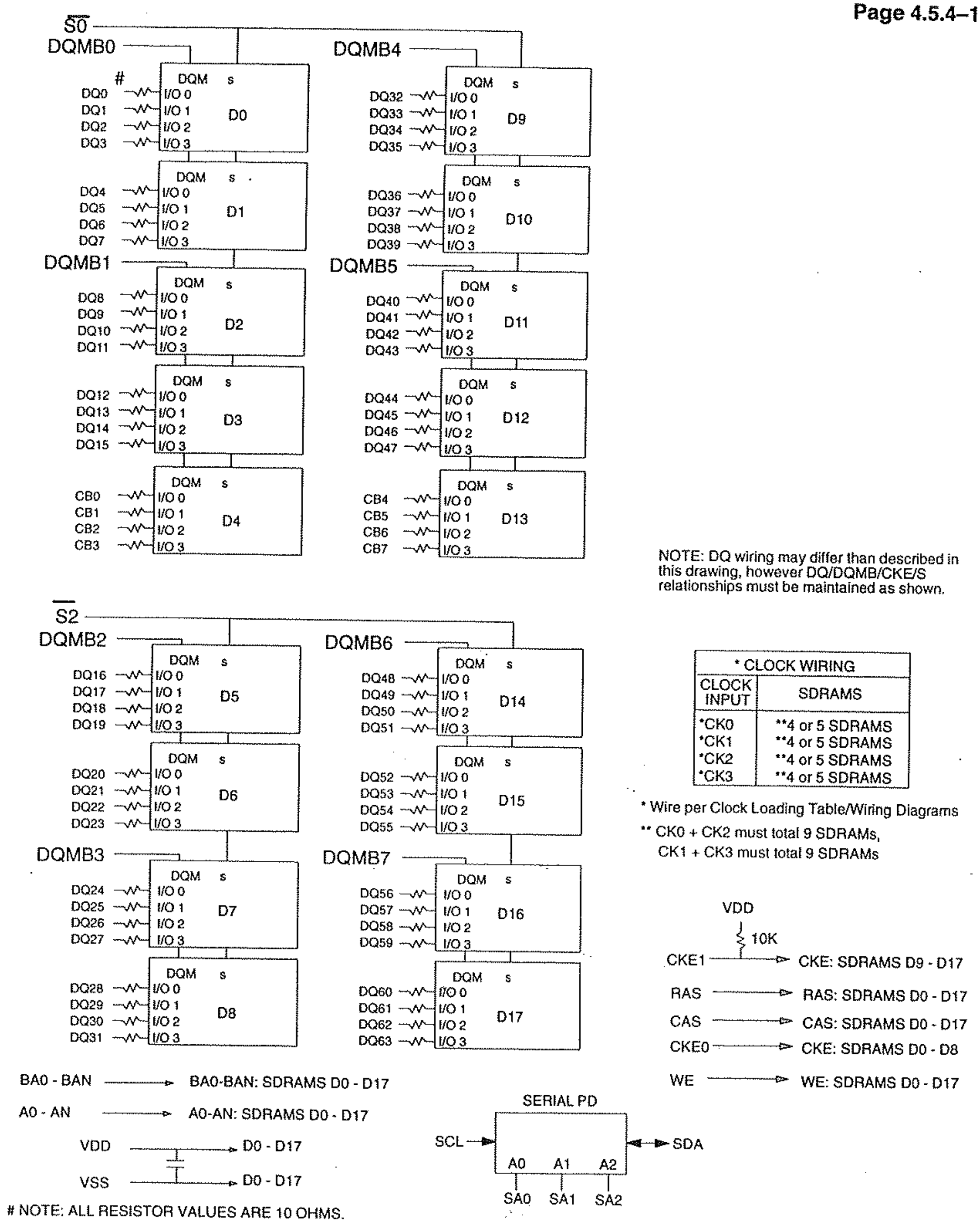
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–O
X64 SDRAM DIMM, 2 Banks with X32 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

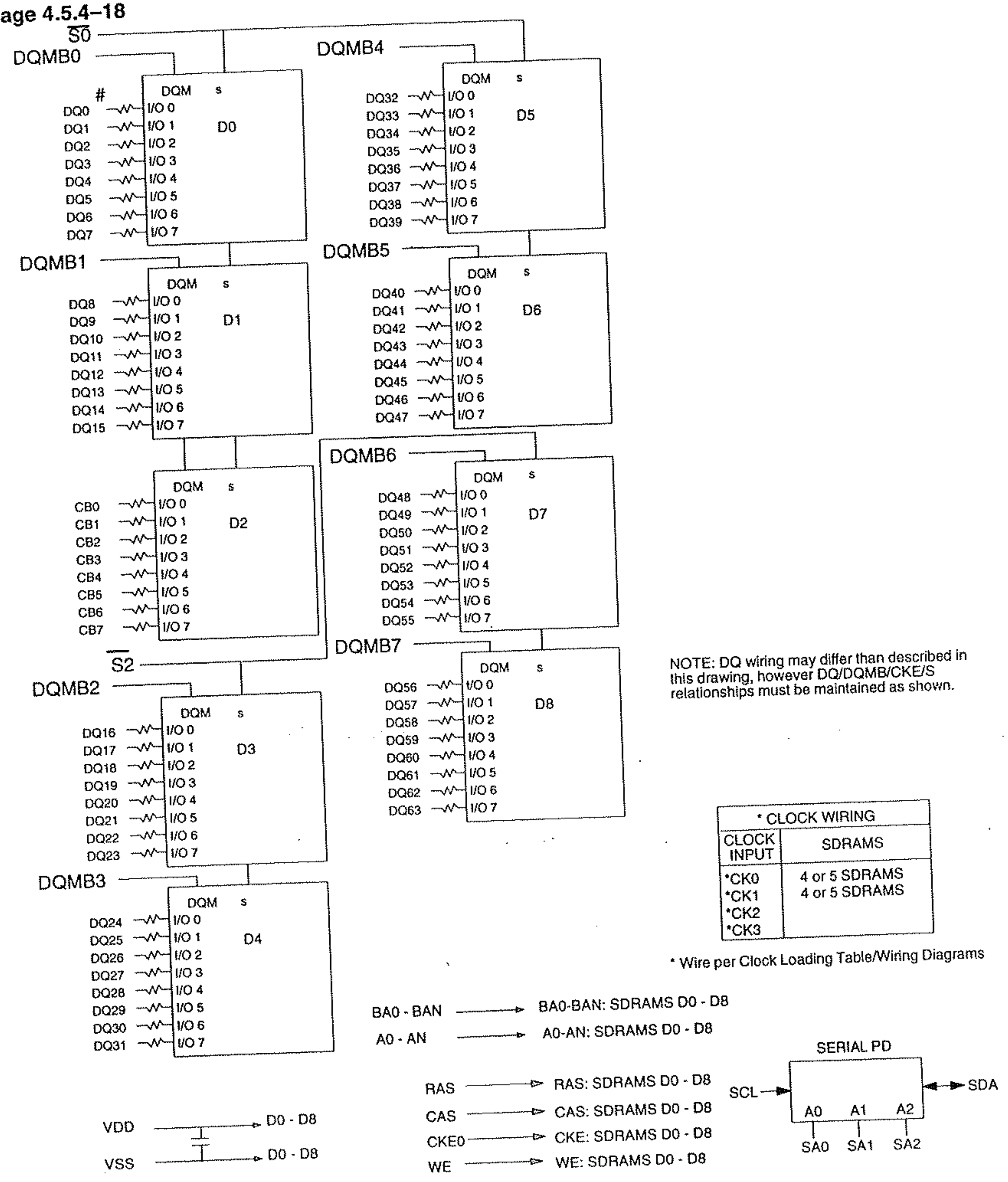
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	**4 or 5 SDRAMS
*CK1	**4 or 5 SDRAMS
*CK2	**4 or 5 SDRAMS
*CK3	**4 or 5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

** CK0 + CK2 must total 9 SDRAMs,
CK1 + CK3 must total 9 SDRAMs

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–P
X72 ECC SDRAM DIMM, 1 Banks with X4 SDRAMs



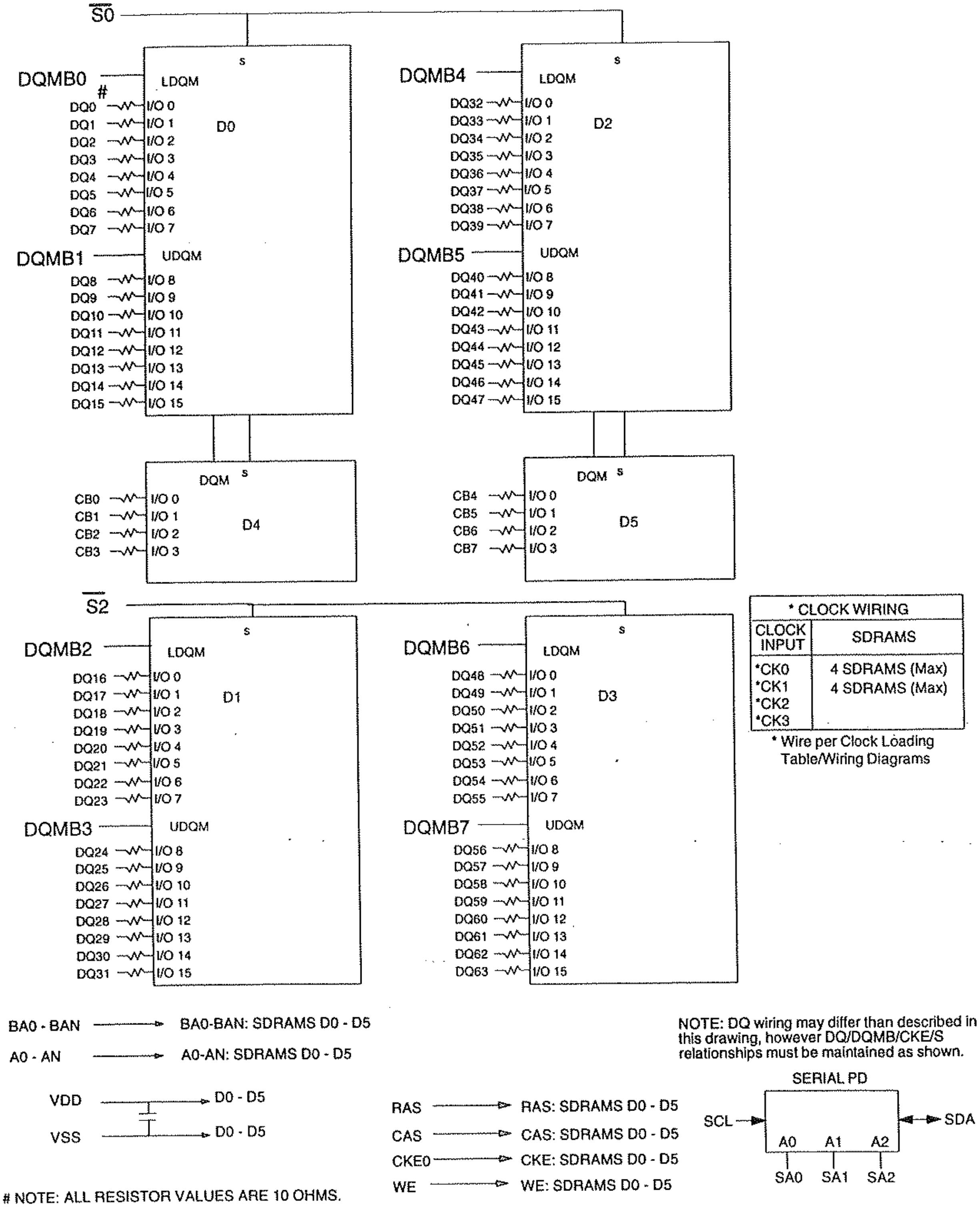
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	4 or 5 SDRAMS 4 or 5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–Q
X72 ECC SDRAM DIMM, 1 Banks with X8 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS (Max)
*CK1	4 SDRAMS (Max)
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–R
X72 ECC SDRAM DIMM, 1 Bank with X16 & X4 SDRAMs

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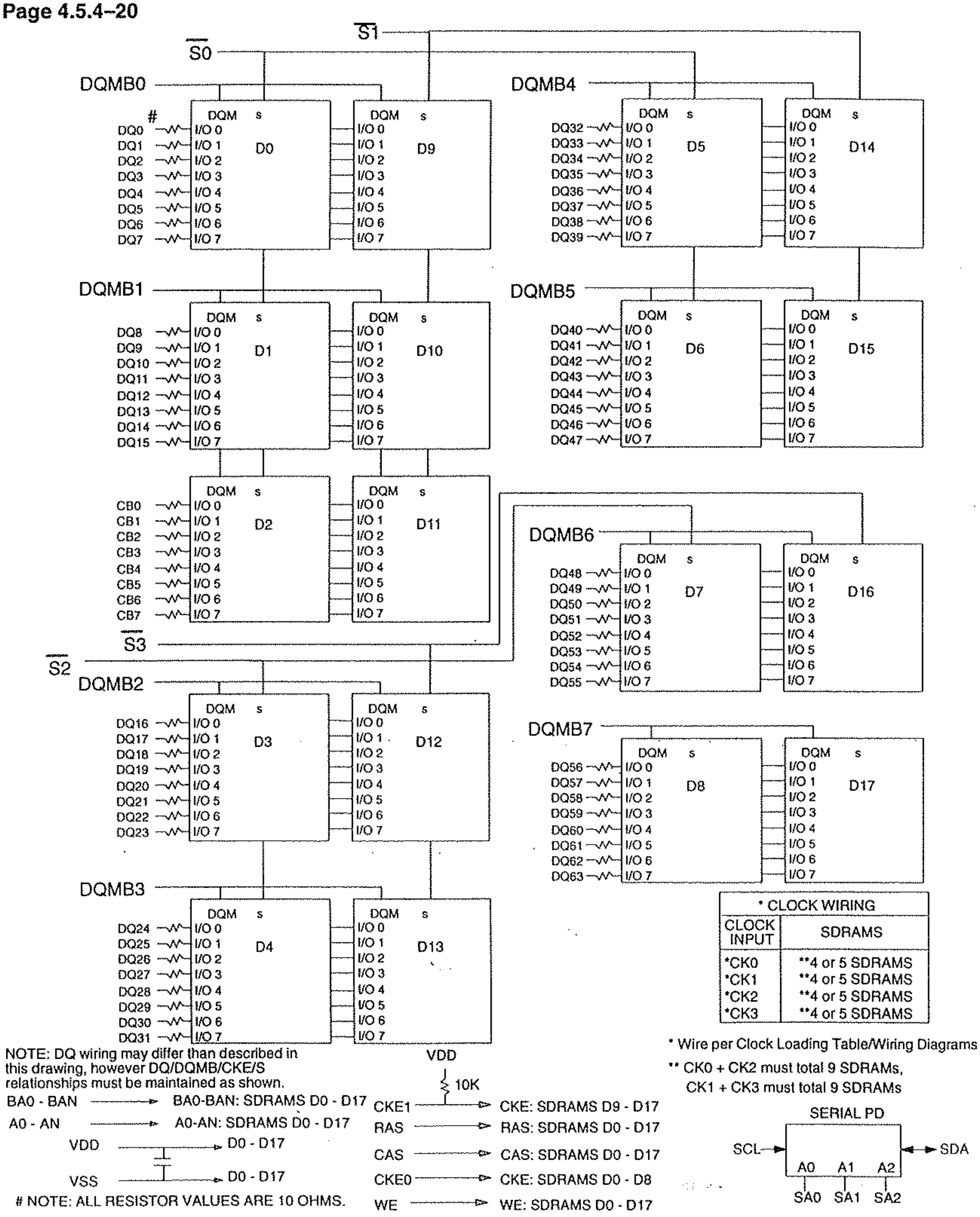


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

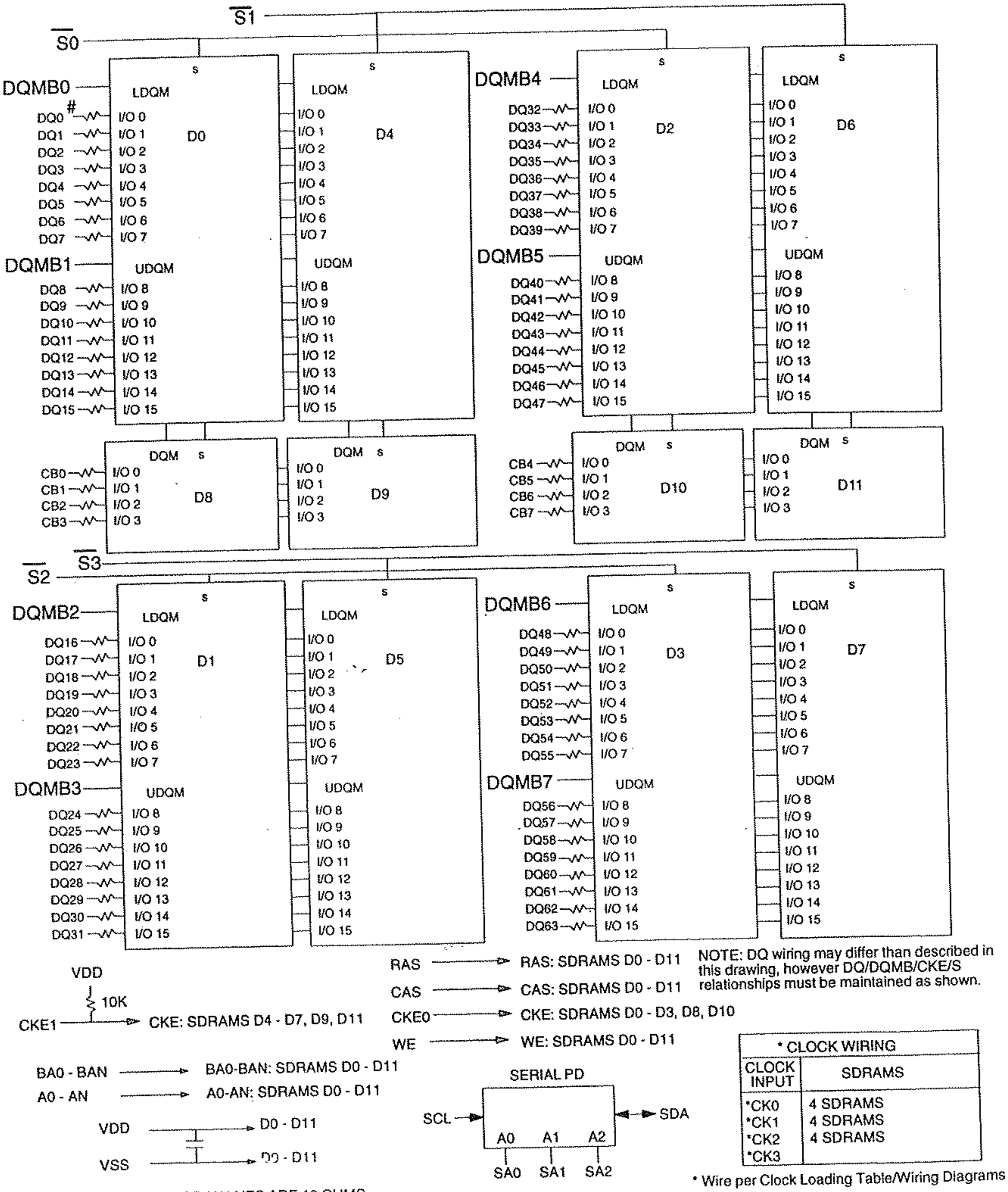
NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	**4 or 5 SDRAMS
*CK1	**4 or 5 SDRAMS
*CK2	**4 or 5 SDRAMS
*CK3	**4 or 5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

** CK0 + CK2 must total 9 SDRAMs, CK1 + CK3 must total 9 SDRAMs

Figure 4.5.4–S
X72 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

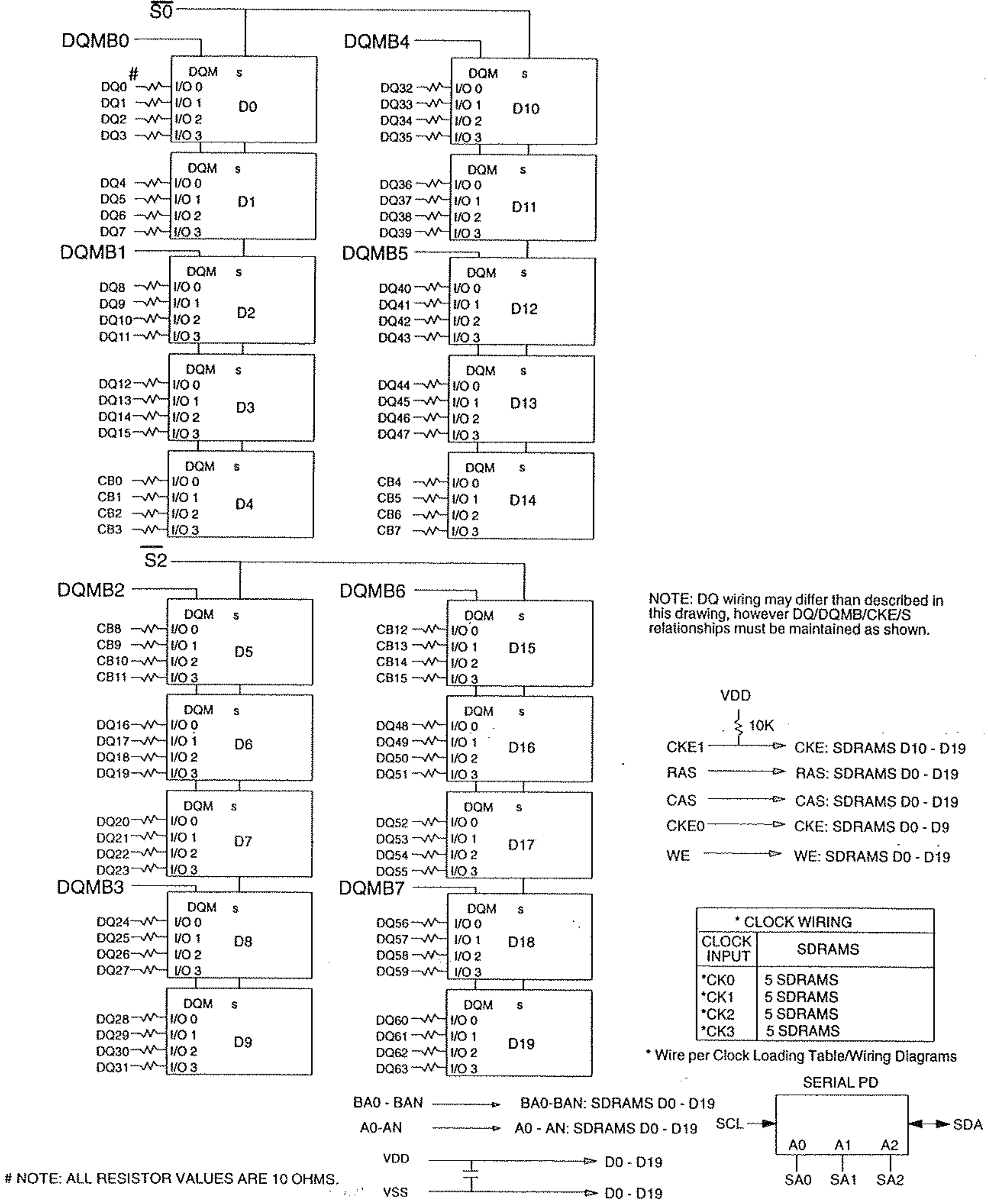
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	4 SDRAMS
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–T
X72 ECC SDRAM DIMM, 2 Banks with X16 & X4 SDRAMs

336



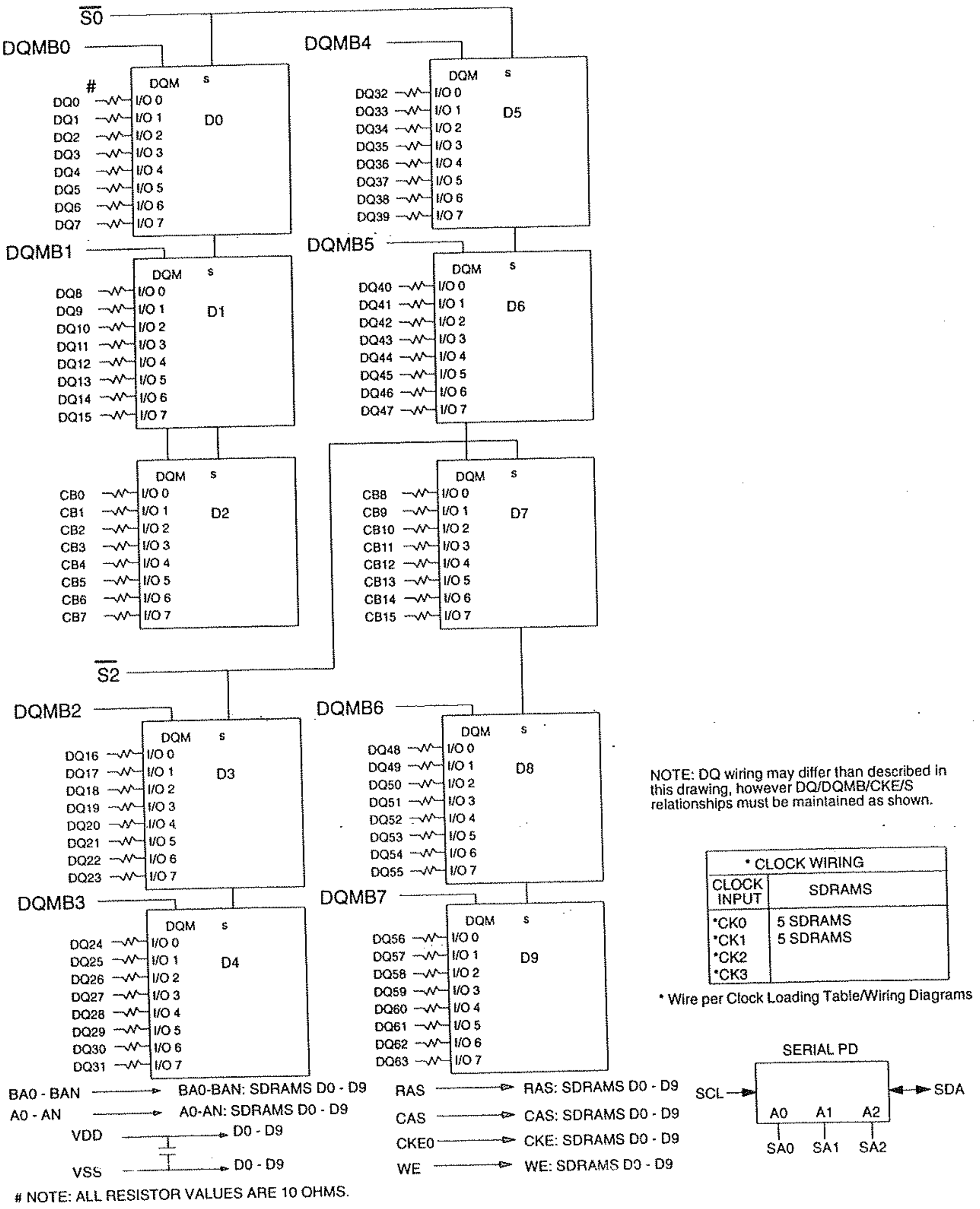
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS
*CK2	5 SDRAMS
*CK3	5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–U
X80 SDRAM DIMM, 1 Bank with X4 SDRAMs



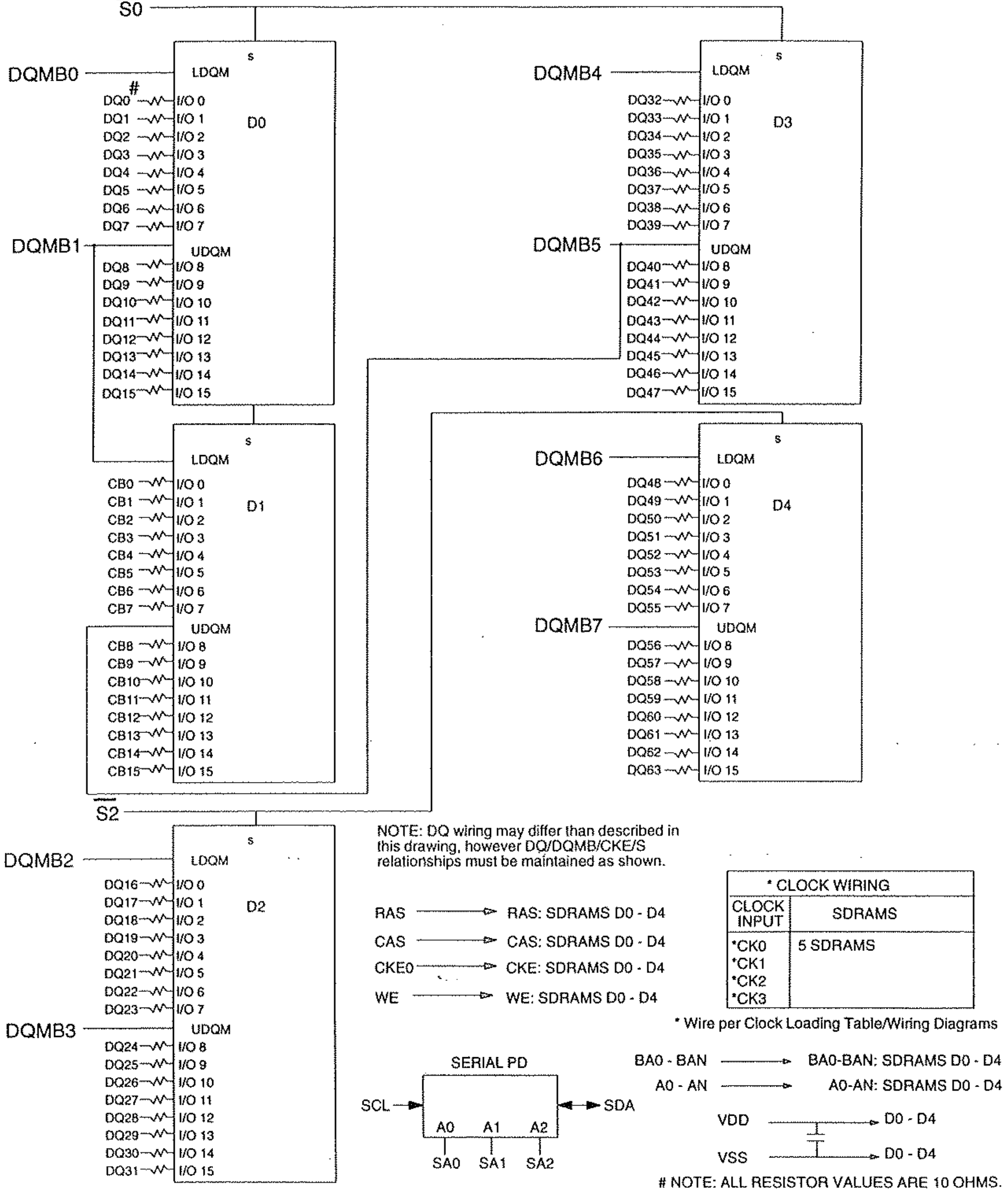
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–V
X80 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs



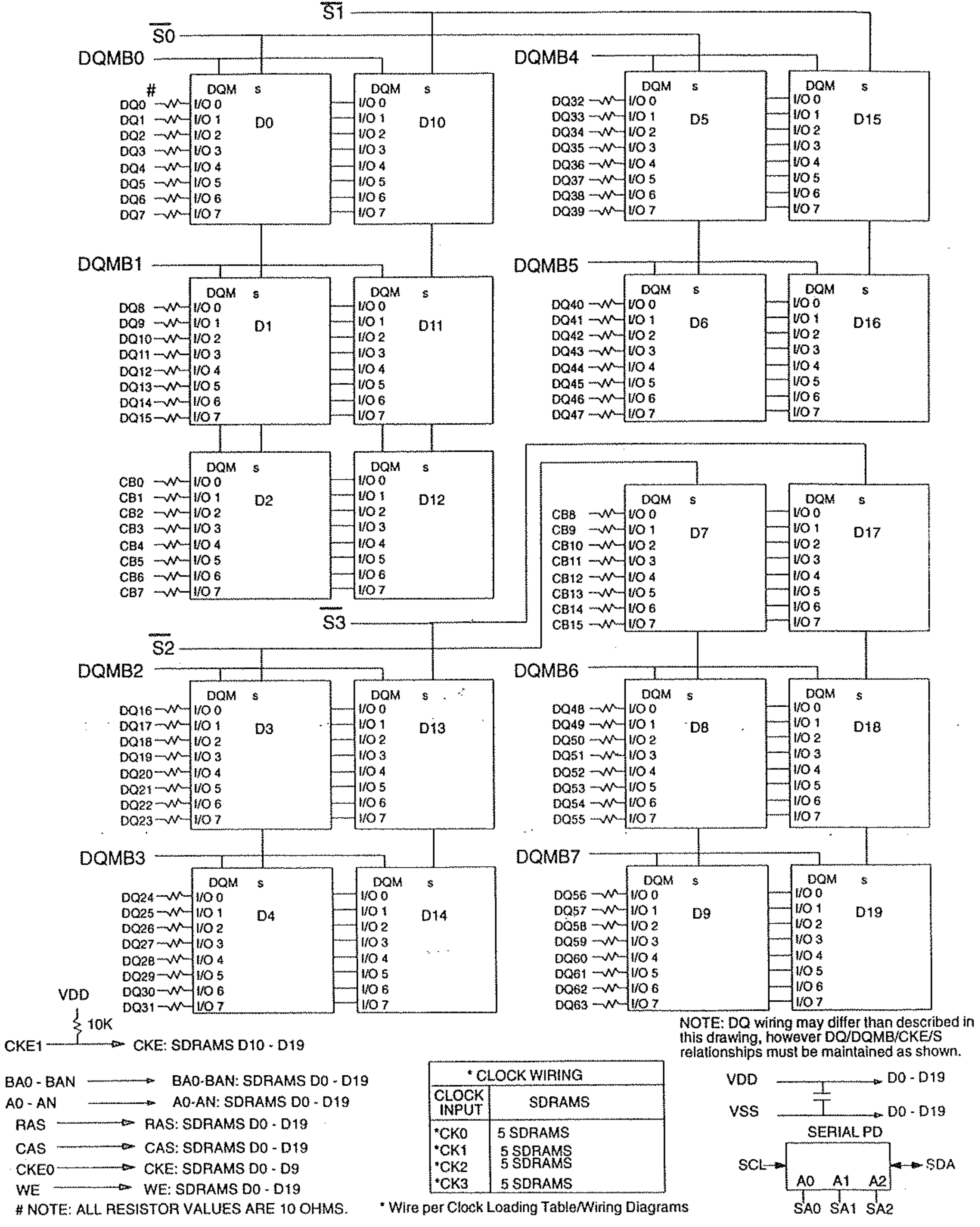
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4-W
X80 ECC SDRAM DIMM, 1 Bank with X16 SDRAMs



* CLOCK WIRING

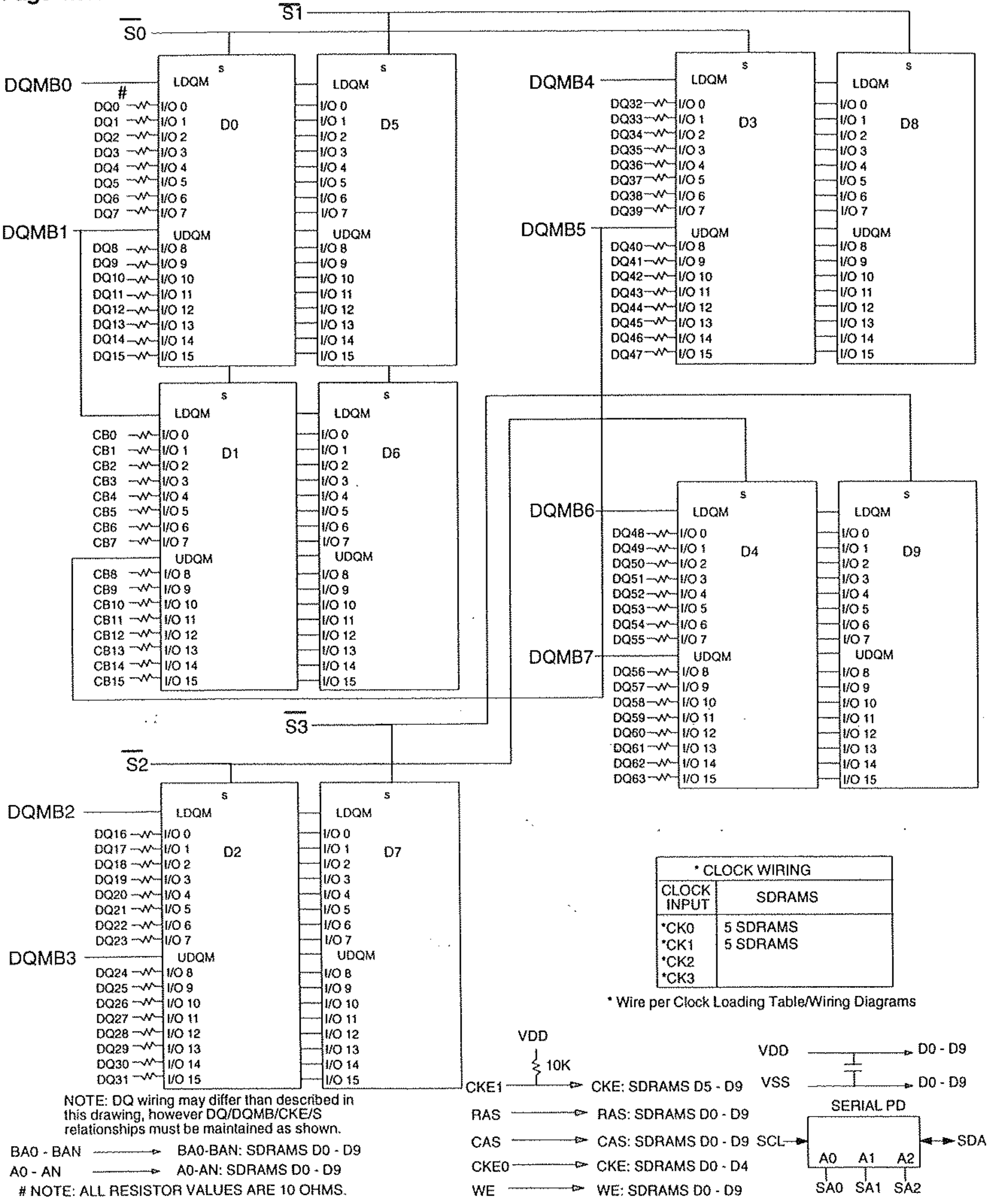
CLOCK INPUT	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS
*CK2	5 SDRAMS
*CK3	5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–X
X80 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–Y
X80 ECC SDRAM DIMM, 2 Banks with X16 SDRAMs

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4.5.5 – 144 PIN DRAM SO–DIMM FAMILY

NOTE: It is recommended that this module be used primarily for main memory applications. At the time this standard was published, the Committee was working on a standard for a Graphics 144 Pin Module to be published in the near future.

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.

DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—64 BIT DRAM without PARITY
—72 BIT DRAM for ECC CODES

CONFIGURATION—10 Different Configurations are defined using various combinationa of X4, X8, and X16 DRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that consist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.5.5–A & 4.5.5–B

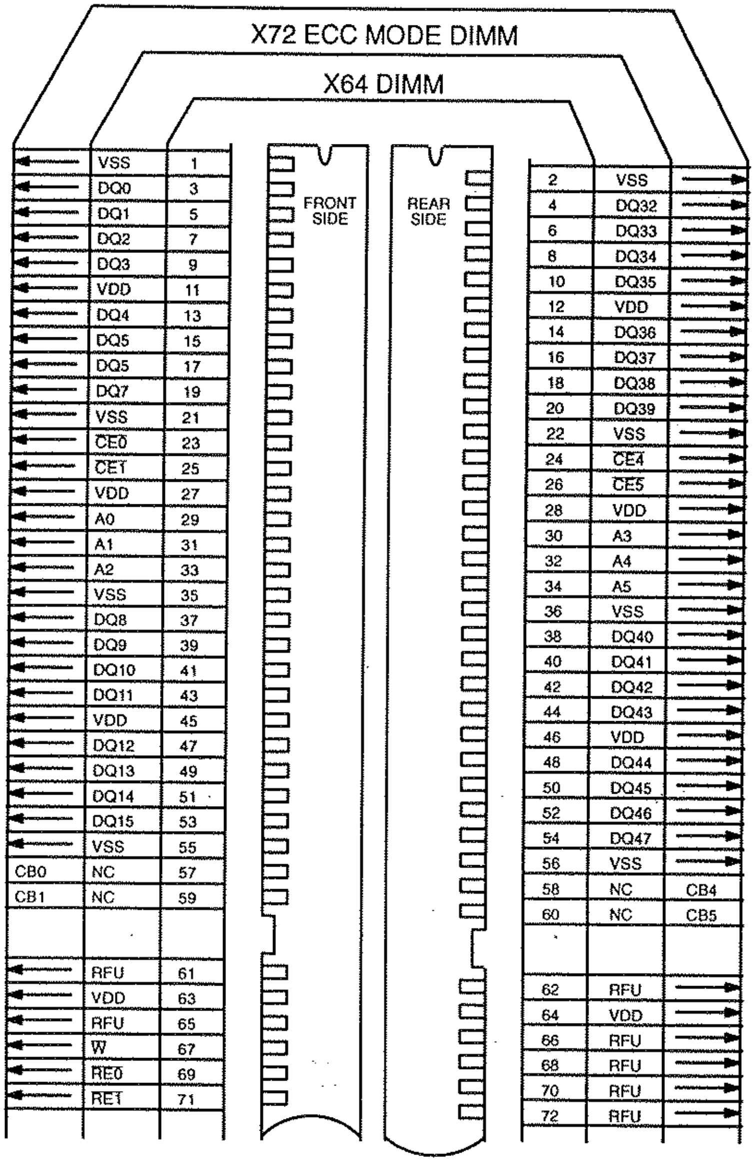
MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.5–C

TECHNOLOGY COMPARISON TABLE — Fig. 4.5.5–D

DRAM SPD INFORMATOION — Fig. 4.5.5–E

X64 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5–F through 4.5.5–J

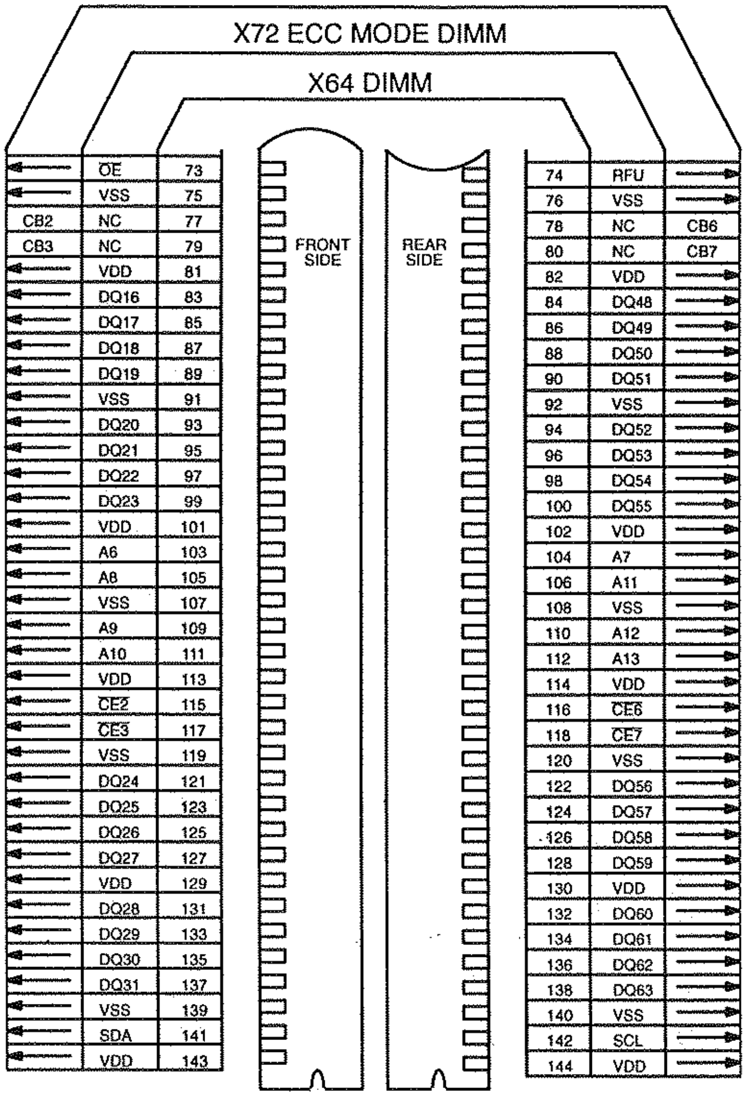
X72 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5–K through 4.5.5–O



←	VSS	1
←	DQ0	3
←	DQ1	5
←	DQ2	7
←	DQ3	9
←	VDD	11
←	DQ4	13
←	DQ5	15
←	DQ5	17
←	DQ7	19
←	VSS	21
←	$\overline{CE0}$	23
←	$\overline{CE1}$	25
←	VDD	27
←	A0	29
←	A1	31
←	A2	33
←	VSS	35
←	DQ8	37
←	DQ9	39
←	DQ10	41
←	DQ11	43
←	VDD	45
←	DQ12	47
←	DQ13	49
←	DQ14	51
←	DQ15	53
←	VSS	55
CB0	NC	57
CB1	NC	59
←	RFU	61
←	VDD	63
←	RFU	65
←	$\overline{W}$	67
←	$\overline{RE0}$	69
←	$\overline{RE1}$	71

2	VSS	→
4	DQ32	→
6	DQ33	→
8	DQ34	→
10	DQ35	→
12	VDD	→
14	DQ36	→
16	DQ37	→
18	DQ38	→
20	DQ39	→
22	VSS	→
24	$\overline{CE4}$	→
26	$\overline{CE5}$	→
28	VDD	→
30	A3	→
32	A4	→
34	A5	→
36	VSS	→
38	DQ40	→
40	DQ41	→
42	DQ42	→
44	DQ43	→
46	VDD	→
48	DQ44	→
50	DQ45	→
52	DQ46	→
54	DQ47	→
56	VSS	→
58	NC	CB4
60	NC	CB5
62	RFU	→
64	VDD	→
66	RFU	→
68	RFU	→
70	RFU	→
72	RFU	→

Figure 4.5.5–A
144 Pin X64 & X72 DRAM SO–DIMM, PIN ASSIGNMENTS
UPPER HALF



←	$\overline{OE}$	73	74	RFU	→
←	VSS	75	76	VSS	→
CB2	NC	77	78	NC	CB6
CB3	NC	79	80	NC	CB7
←	VDD	81	82	VDD	→
←	DQ16	83	84	DQ48	→
←	DQ17	85	86	DQ49	→
←	DQ18	87	88	DQ50	→
←	DQ19	89	90	DQ51	→
←	VSS	91	92	VSS	→
←	DQ20	93	94	DQ52	→
←	DQ21	95	96	DQ53	→
←	DQ22	97	98	DQ54	→
←	DQ23	99	100	DQ55	→
←	VDD	101	102	VDD	→
←	A6	103	104	A7	→
←	A8	105	106	A11	→
←	VSS	107	108	VSS	→
←	A9	109	110	A12	→
←	A10	111	112	A13	→
←	VDD	113	114	VDD	→
←	$\overline{CE2}$	115	116	$\overline{CE6}$	→
←	$\overline{CE3}$	117	118	$\overline{CE7}$	→
←	VSS	119	120	VSS	→
←	DQ24	121	122	DQ56	→
←	DQ25	123	124	DQ57	→
←	DQ26	125	126	DQ58	→
←	DQ27	127	128	DQ59	→
←	VDD	129	130	VDD	→
←	DQ28	131	132	DQ60	→
←	DQ29	133	134	DQ61	→
←	DQ30	135	136	DQ62	→
←	DQ31	137	138	DQ63	→
←	VSS	139	140	VSS	→
←	SDA	141	142	SCL	→
←	VDD	143	144	VDD	→

Figure 4.5.5–B
144 Pin X64 & X72 DRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

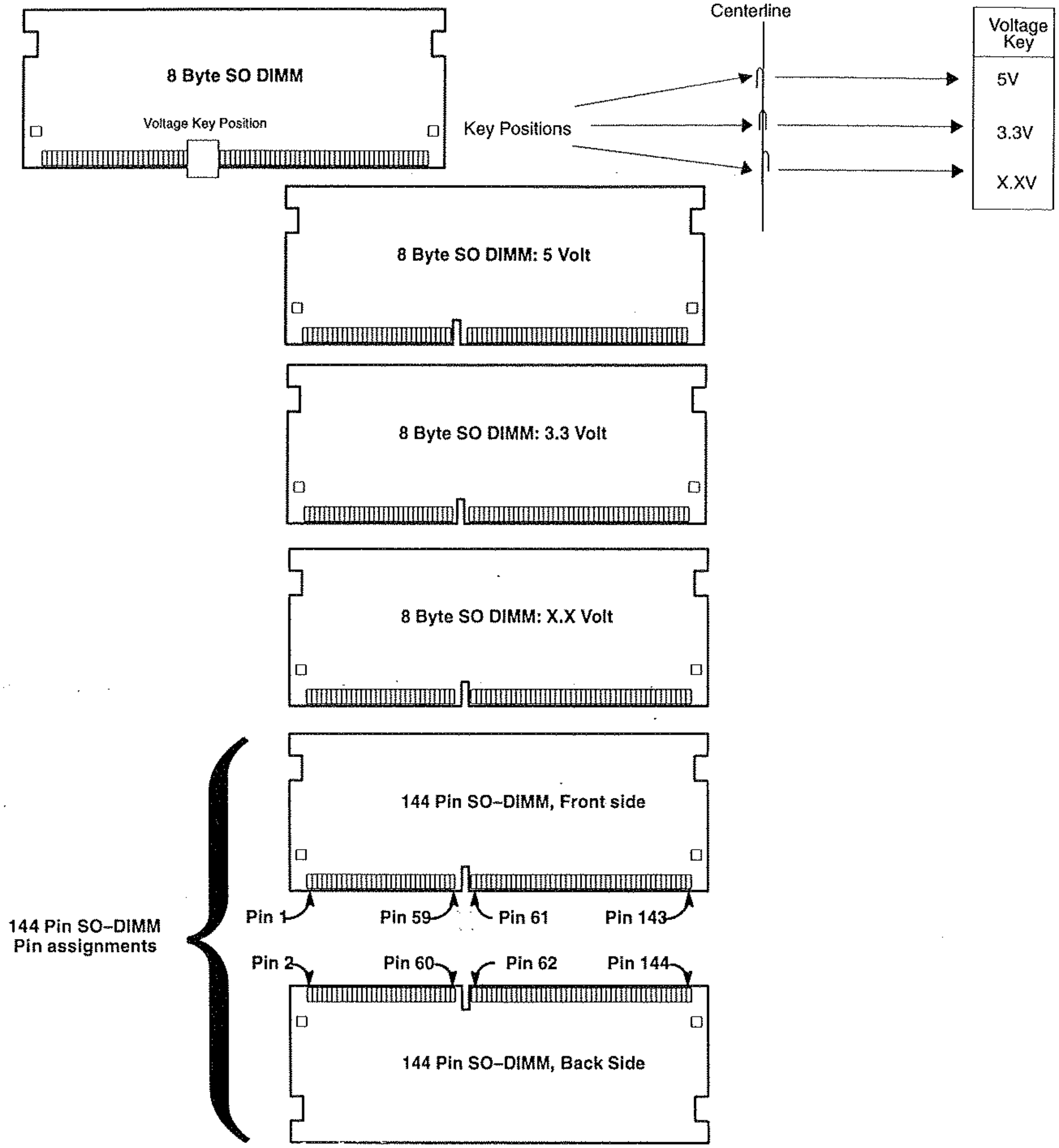


Figure 4.5.5–C
144 Pin SO–DRAM DIMM Keying Methodology

Pin #	DRAM SODIMM	SDRAM SODIMM
23	$\overline{\text{CAS}}0$	DQMB0
25	$\overline{\text{CAS}}1$	DQMB1
61	DU	CK0
65	DU	$\overline{\text{RAS}}$
69	$\overline{\text{RAS}}0$	$\overline{\text{S}}0$
71	$\overline{\text{RAS}}1$	$\overline{\text{S}}1$
73	$\overline{\text{OE}}$	DU
111	A10	A10/AP
115	$\overline{\text{CAS}}2$	DQMB2
117	$\overline{\text{CAS}}3$	DQMB3
24	$\overline{\text{CAS}}4$	DQMB4
26	$\overline{\text{CAS}}5$	DQMB5
62	DU	CKE0
66	DU	$\overline{\text{CAS}}$
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	$\overline{\text{CAS}}6$	DQMB6
118	$\overline{\text{CAS}}7$	DQMB7

Figure 4.5.5–D
Pinout Comparison, 144 Pin DRAM & SDRAM SO–DIMM

8 Byte DRAM SO–DIMM PD Information

- Serial PD Interface Protocol: I^{2}C (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:
  a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.
512K x 64/72	512K x 8	10	9				
1M x 64/72	512K x 8	10	9				
1M x 64/72	1M x 4/16	10	10	12	8		
2M x 64/72	1M x 16	10	10	12	8		
2M x 64/72	2M x 8	11	10	12	9		
4M x 64/72	2M x 8	11	10	12	9		
4M x 64/72	4M x 4/16	11	11	12	10	*13	9
8M x 64/72	4M x 16	11	11	12	10	*13	9
8M x 64/72	8M x 8	12	11	13	10		
16M x 64/72	8M x 8	12	11	13	10		
16M x 64/72	16M x 4/16	12	12	13	11	*14	10
32M x 64/72	16M x 16	12	12	13	11	*14	10
32M x 64/72	32M x 8	13	12	14	11		
64M x 64/72	32M x 8	13	12	14	11		
64M x 64/72	64M x 4	13	13	14	12		

(Note: All options possible with DRAM standards are shown)
* This addressing option applies to x16 DRAM configuration

b. Allowable configurations: (Byte 11)
  - x64 (Non-parity, Byte controls)
  - x72 (ECC-optimized, Byte controls)

c. Functional Attributes:
  - Power Supply Voltage/Interface levels (Byte 8)
  - $\overline{RAS}$ access (Byte 9)
  - $\overline{CAS}$ access (Byte 10)
  - Refresh rate/type (Byte 12)

For Detailed Serial PD Byte data see section 4–?–?, DRAM Serial Presence Detect Definitions.

1. Serial PD interface is standard I^{2}C architecture

2. Pull-up resistors (4.7K typical value) are required on all open drain/open collector bus devices (SCL and SDA).

3. Current sink capability on SCL and SDA source (I_{OL} max) must be at least 3ma to maintain a valid "low level".

4. I^{2}C Bus specification:

Figure 4.5.5–E

144 Pin X64 DRAM SO–DIMM, SPD TABLE AND INFORMATION

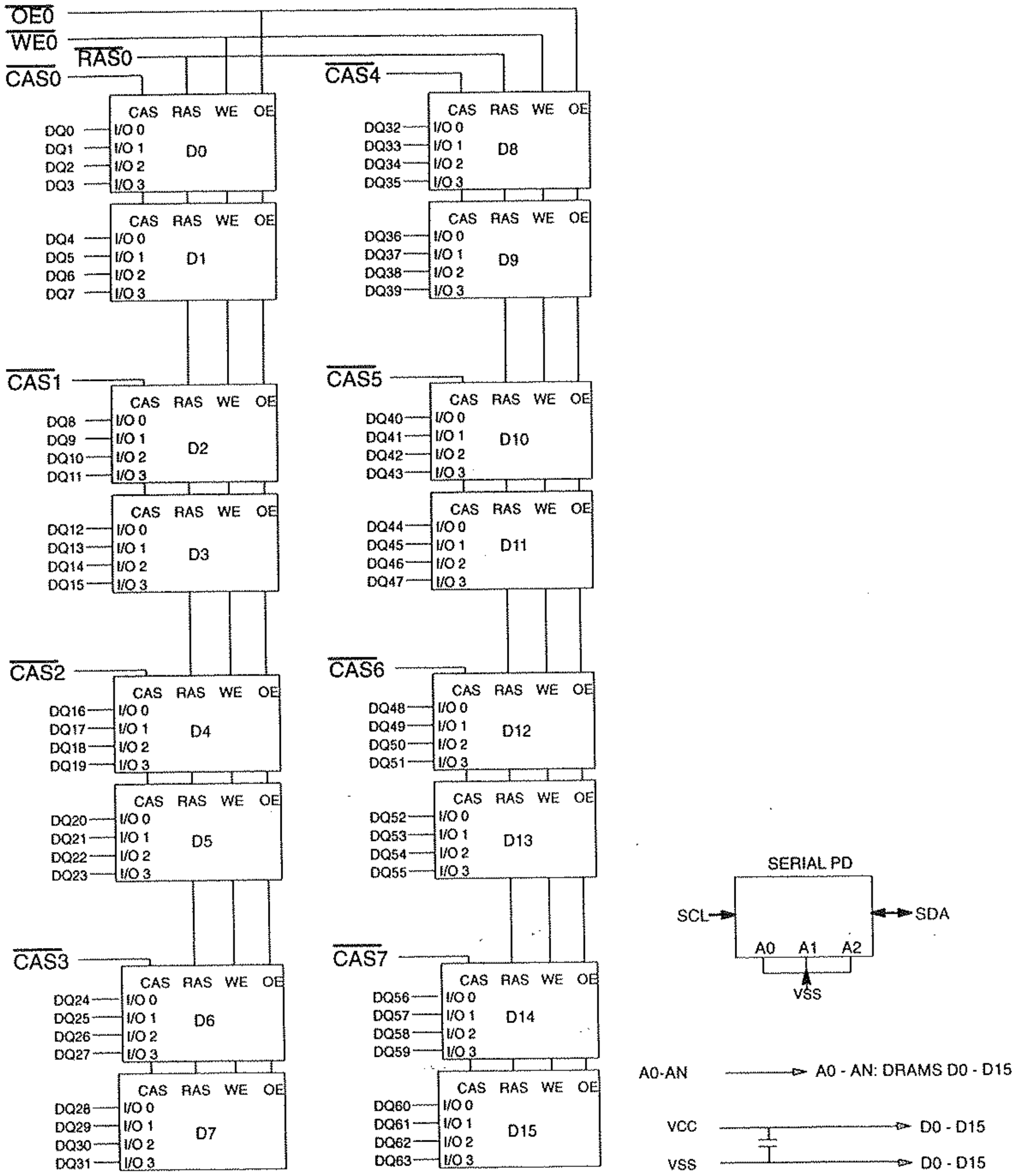


Figure 4.5.5–F

144 Pin X64 DRAM SO–DIMM, 1 Bank with X4 DRAMs

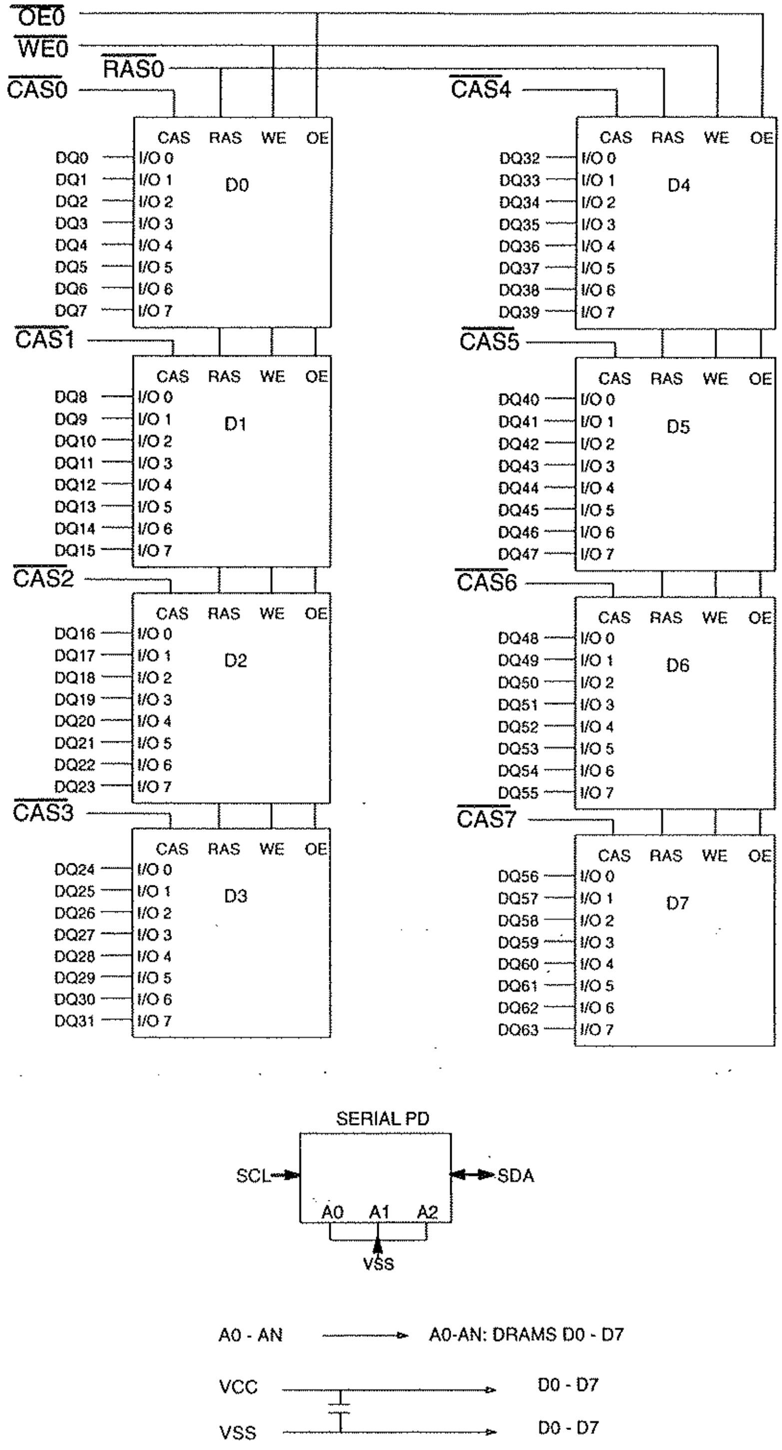


Figure 4.5.5–G
144 Pin X64 DRAM SO–DIMM, 1 Bank with X8 DRAMs

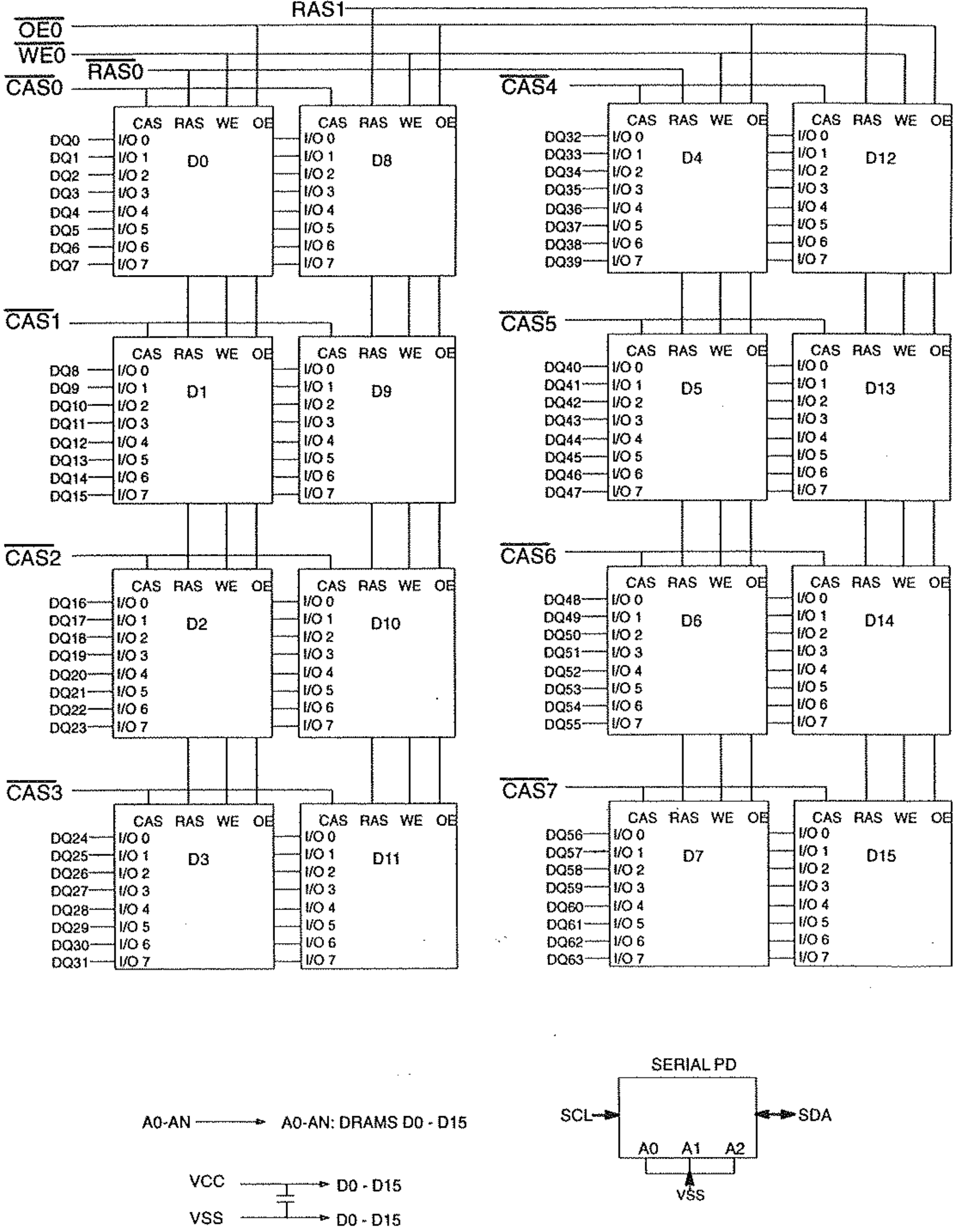


Figure 4.5.5-H
144 Pin X64 DRAM SO-DIMM, 2 Bank with X8 DRAMs

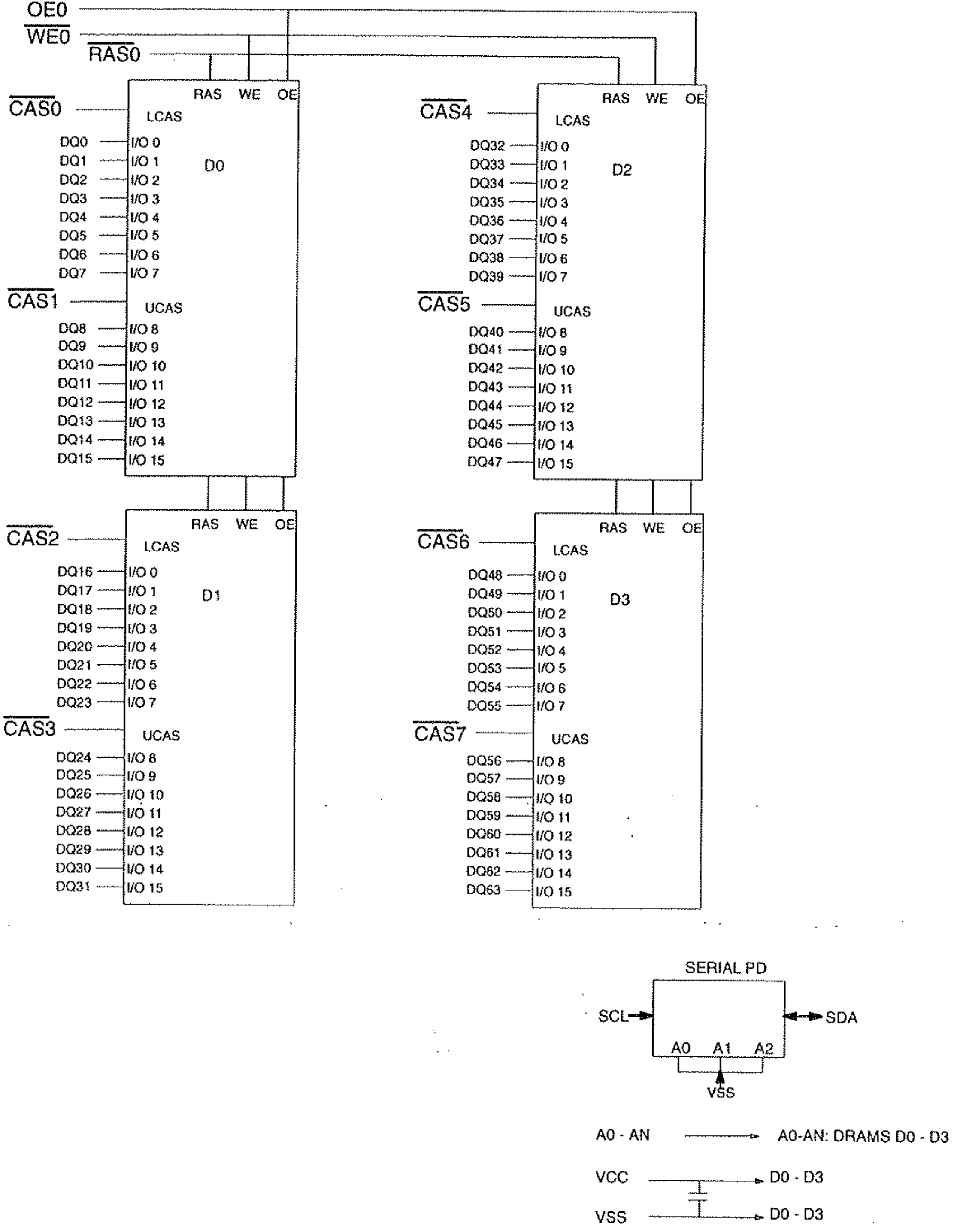


Figure 4.5.5–I
144 Pin X64 DRAM SO–DIMM, 1 Bank with X16 DRAMs

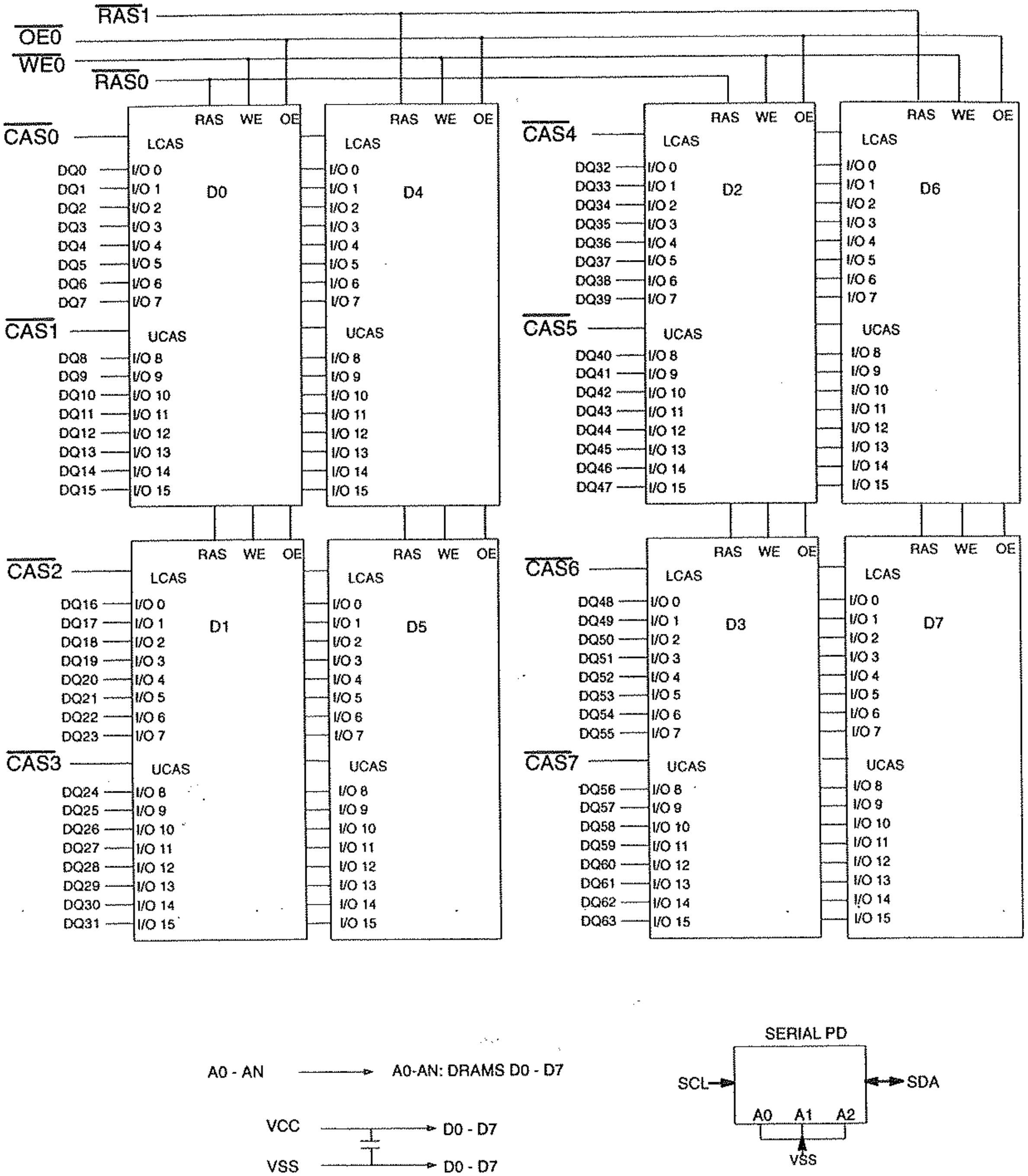


Figure 4.5.5–J
144 Pin X64 DRAM SO–DIMM, 2 Bank with X16 DRAMs

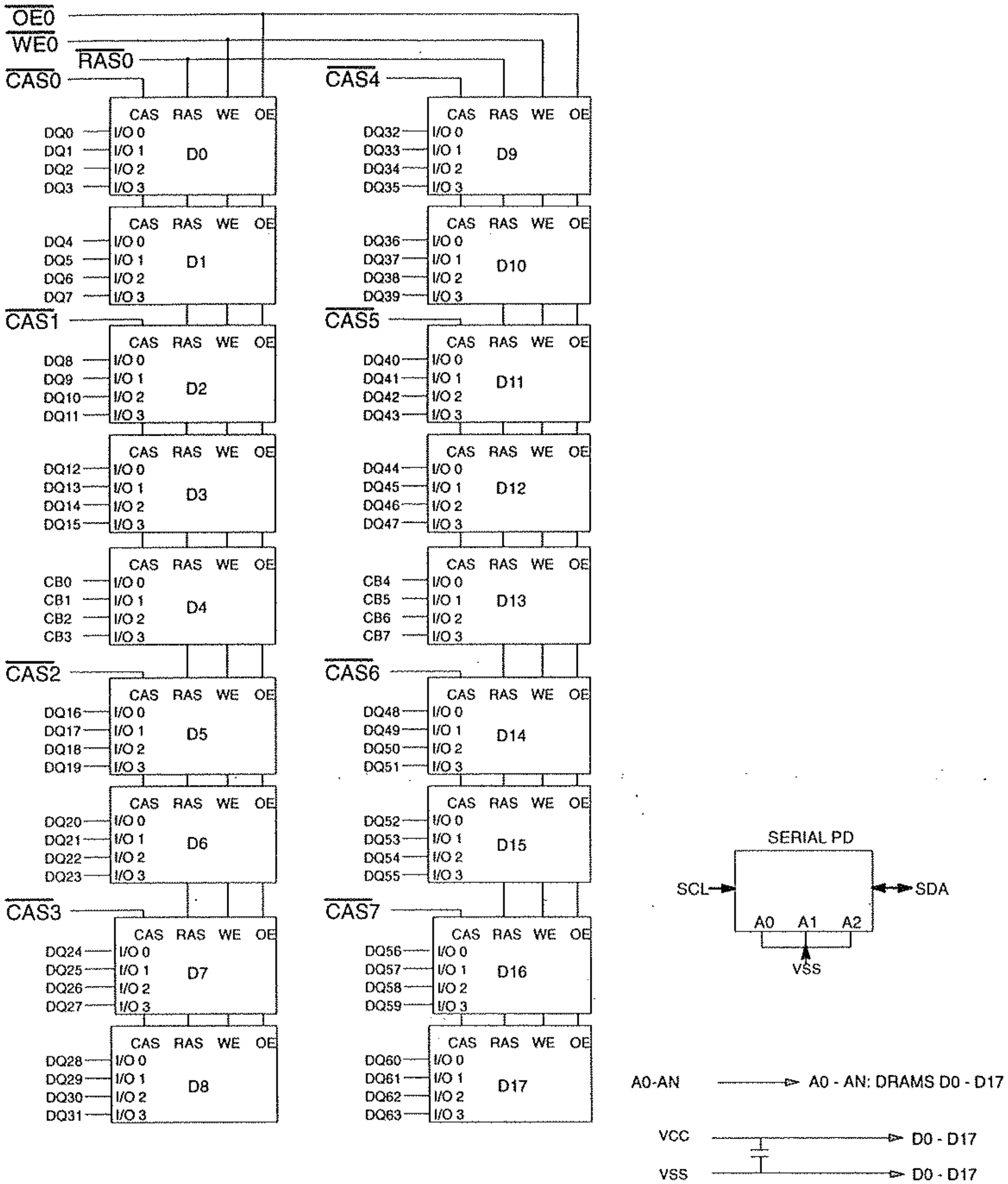


Figure 4.5.5–K
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X4 DRAMs

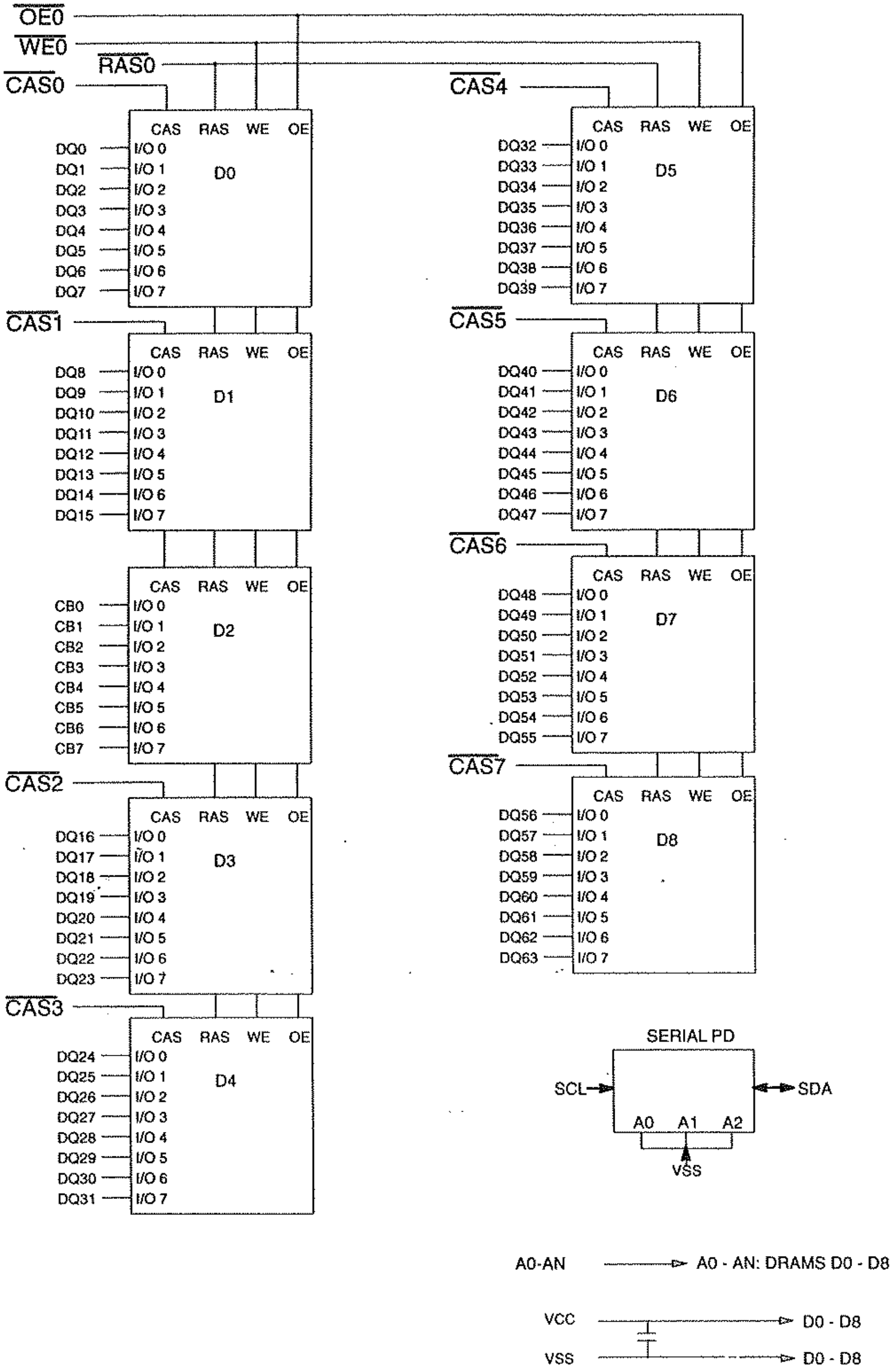


Figure 4.5.5–L
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X8 DRAMs

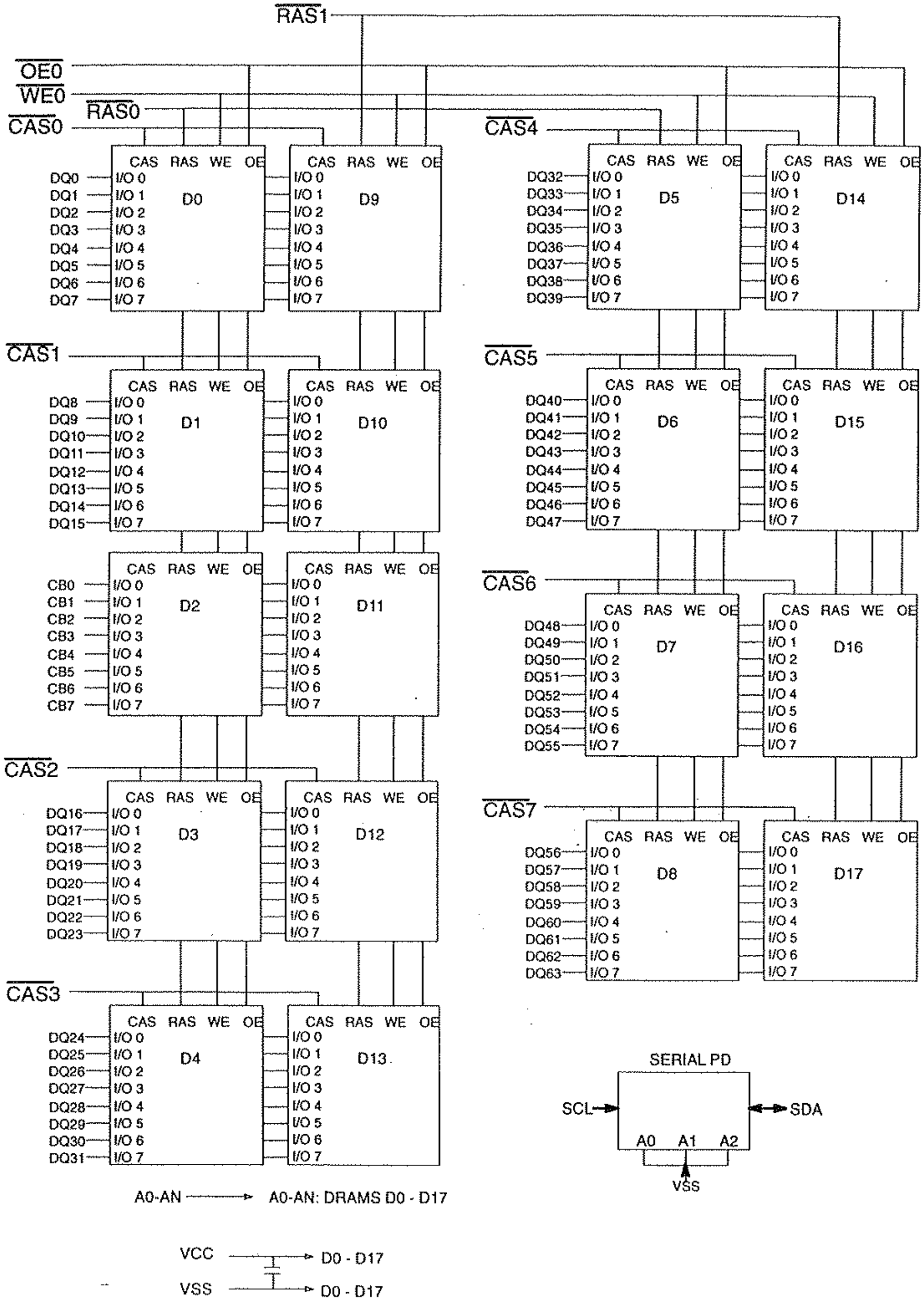


Figure 4.5.5–M
144 Pin X72 ECC DRAM SO–DIMM, 2 Bank with X8 DRAMs

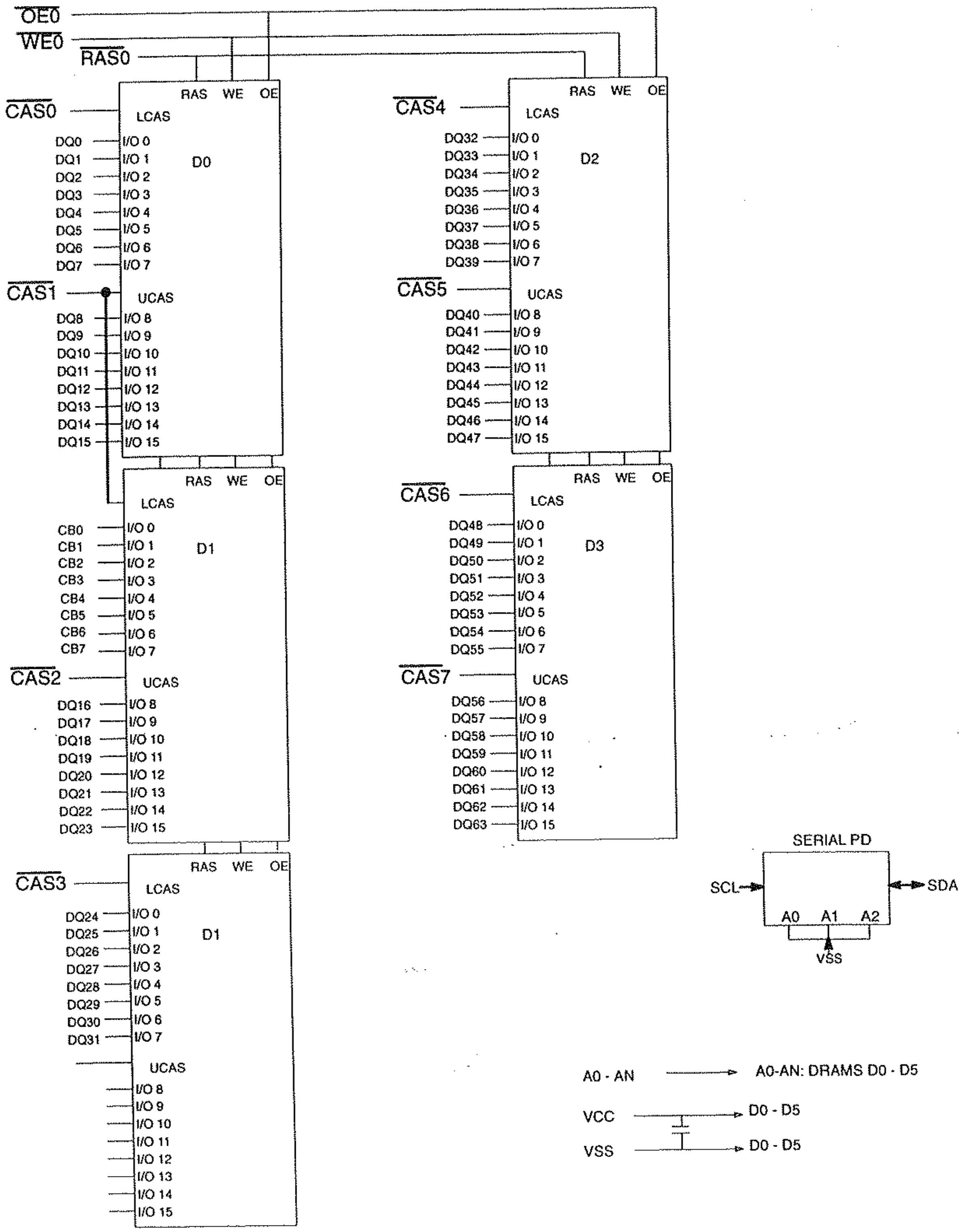


Figure 4.5.5–N
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X16 DRAMs

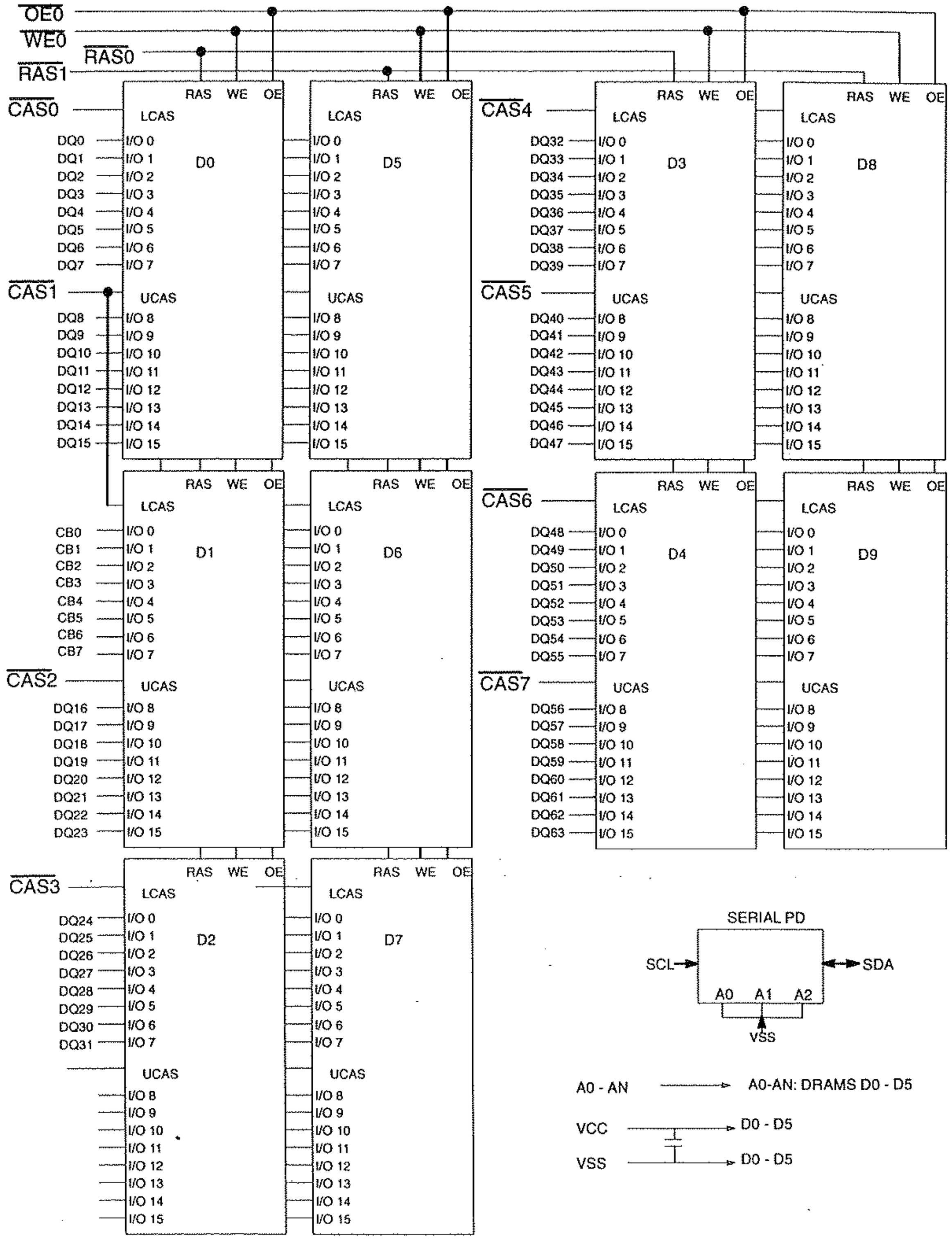
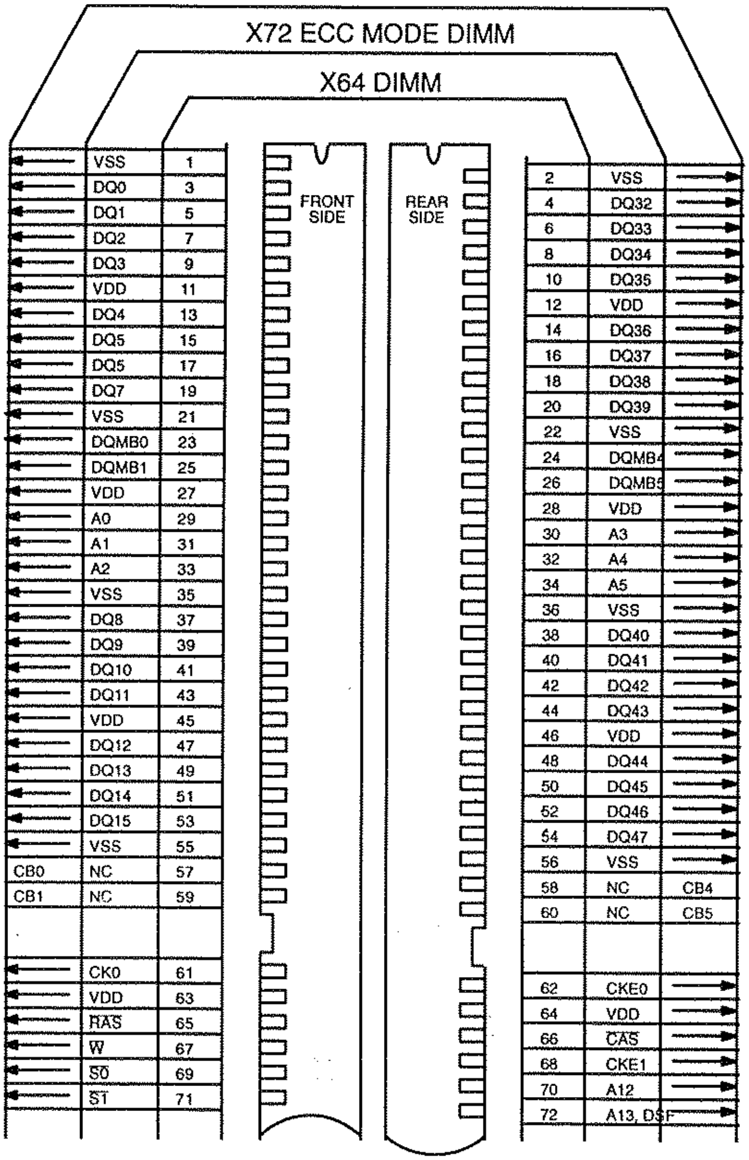


Figure 4.5.5–O
144 Pin X72 ECC DRAM SO–DIMM, 2 Bank with X16 DRAMs

4.5.6 – 144 PIN SDRAM SO–DIMM FAMILY

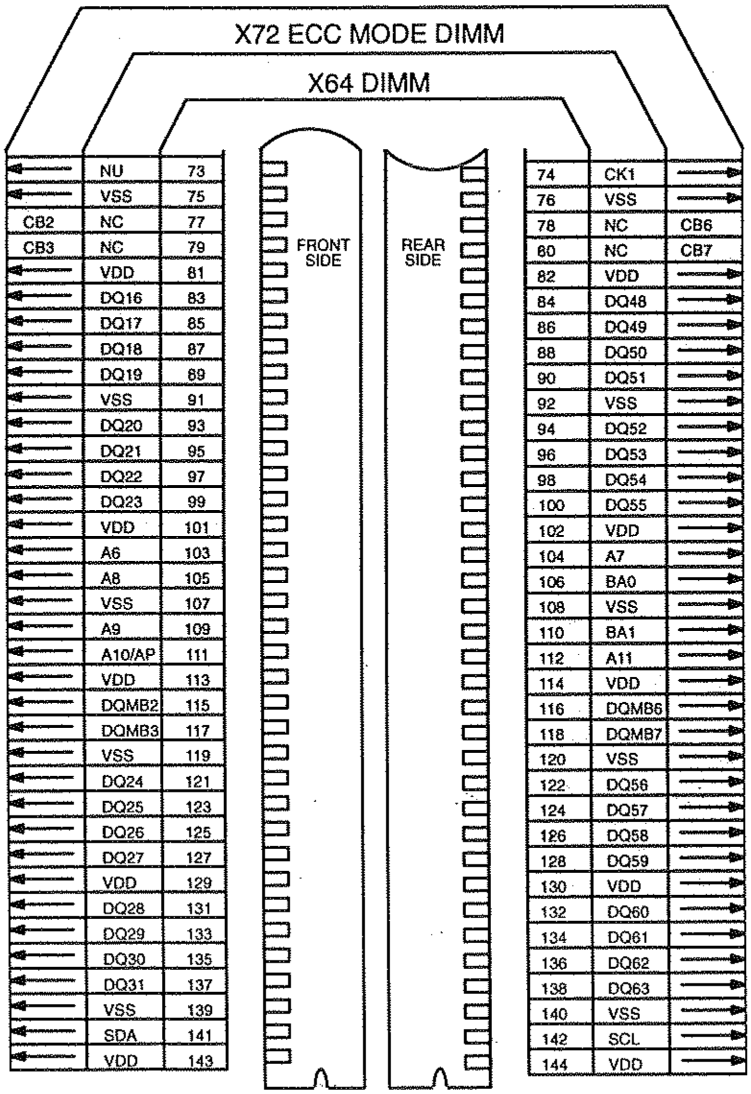
CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.
DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—64 BIT SDRAM without PARITY
—72 BIT SDRAM for ECC CODES
CONFIGURATION—10 Different Configurations are defined using various combinationa of X4, X8, and X16 SDRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.
LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.5.6–A & 4.5.6–B
SDRAM SPD INFORMATOION — Fig. 4.5.6–C
MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.6–D
TECHNOLOGY COMPARISON TABLE — Fig. 4.5.6–E
SDRAM CLOCK LOADING & WIRING—Figs. 4.5.6–F
X64 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6–G through 4.5.6–L
X72 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6–M through 4.5.6–P



←	VSS	1
←	DQ0	3
←	DQ1	5
←	DQ2	7
←	DQ3	9
←	VDD	11
←	DQ4	13
←	DQ5	15
←	DQ5	17
←	DQ7	19
←	VSS	21
←	DQMB0	23
←	DQMB1	25
←	VDD	27
←	A0	29
←	A1	31
←	A2	33
←	VSS	35
←	DQ8	37
←	DQ9	39
←	DQ10	41
←	DQ11	43
←	VDD	45
←	DQ12	47
←	DQ13	49
←	DQ14	51
←	DQ15	53
←	VSS	55
CB0	NC	57
CB1	NC	59
←	CK0	61
←	VDD	63
←	$\overline{\text{RAS}}$	65
←	$\overline{\text{W}}$	67
←	$\overline{\text{S0}}$	69
←	$\overline{\text{S1}}$	71

2	VSS	→
4	DQ32	→
6	DQ33	→
8	DQ34	→
10	DQ35	→
12	VDD	→
14	DQ36	→
16	DQ37	→
18	DQ38	→
20	DQ39	→
22	VSS	→
24	DQMB4	→
26	DQMB5	→
28	VDD	→
30	A3	→
32	A4	→
34	A5	→
36	VSS	→
38	DQ40	→
40	DQ41	→
42	DQ42	→
44	DQ43	→
46	VDD	→
48	DQ44	→
50	DQ45	→
52	DQ46	→
54	DQ47	→
56	VSS	→
58	NC	CB4
60	NC	CB5
62	CKE0	→
64	VDD	→
66	$\overline{\text{CAS}}$	→
68	CKE1	→
70	A12	→
72	A13, DSF	→

Figure 4.5.6–A
144 Pin X64 & X72 SDRAM SO–DIMM, PIN ASSIGNMENTS
UPPER HALF



←	NU	73	74	CK1	→
←	VSS	75	76	VSS	→
CB2	NC	77	78	NC	CB6
CB3	NC	79	80	NC	CB7
←	VDD	81	82	VDD	→
←	DQ16	83	84	DQ48	→
←	DQ17	85	86	DQ49	→
←	DQ18	87	88	DQ50	→
←	DQ19	89	90	DQ51	→
←	VSS	91	92	VSS	→
←	DQ20	93	94	DQ52	→
←	DQ21	95	96	DQ53	→
←	DQ22	97	98	DQ54	→
←	DQ23	99	100	DQ55	→
←	VDD	101	102	VDD	→
←	A6	103	104	A7	→
←	A8	105	106	BA0	→
←	VSS	107	108	VSS	→
←	A9	109	110	BA1	→
←	A10/AP	111	112	A11	→
←	VDD	113	114	VDD	→
←	DQMB2	115	116	DQMB6	→
←	DQMB3	117	118	DQMB7	→
←	VSS	119	120	VSS	→
←	DQ24	121	122	DQ56	→
←	DQ25	123	124	DQ57	→
←	DQ26	125	126	DQ58	→
←	DQ27	127	128	DQ59	→
←	VDD	129	130	VDD	→
←	DQ28	131	132	DQ60	→
←	DQ29	133	134	DQ61	→
←	DQ30	135	136	DQ62	→
←	DQ31	137	138	DQ63	→
←	VSS	139	140	VSS	→
←	SDA	141	142	SCL	→
←	VDD	143	144	VDD	→

Figure 4.5.6–B
144 Pin X64 & X72 SDRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank accr.	$\overline{\text{RAS}}$ accr.	$\overline{\text{CAS}}$ accr.	# Bank accr.	$\overline{\text{RAS}}$ accr.	$\overline{\text{CAS}}$ accr.	# Bank accr.	$\overline{\text{RAS}}$ accr.	$\overline{\text{CAS}}$ accr.
1M x 64/72	1M x 16	1	11	8						
2M x 64/72	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72	2M x 8	1	11	9						
4M x 64/72	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72	16M x 16	2	13	9						
32M x 64/72	16M x 16	2	13	9						
32M x 64/72	32M x 8	2	13	10						
64M x 64/72	32M x 8	2	13	10						
(Note: All options possible with SDRAM standards are shown)										

b. Allowable configurations: (Byte 11)
  - x64 (Non-parity, Byte controls)
  - x72 (ECC-optimized, Byte controls)

c. Functional Attributes:
  - Power Supply Voltage/Interface levels (Byte 8)
  - SDRAM cycle time (Byte 9)
  - SDRAM access from Clock (Byte 10)
  - Refresh rate/type (Byte 12)
  - SDRAM module attributes (Byte 13)
  - SDRAM device attributes (Bytes 14 - 20)
  - Primary/Secondary SDRAM (Bytes 21 - 22)

Figure 4.5.6–C
144 Pin SDRAM SO–DIMM, PD INFORMATION

The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

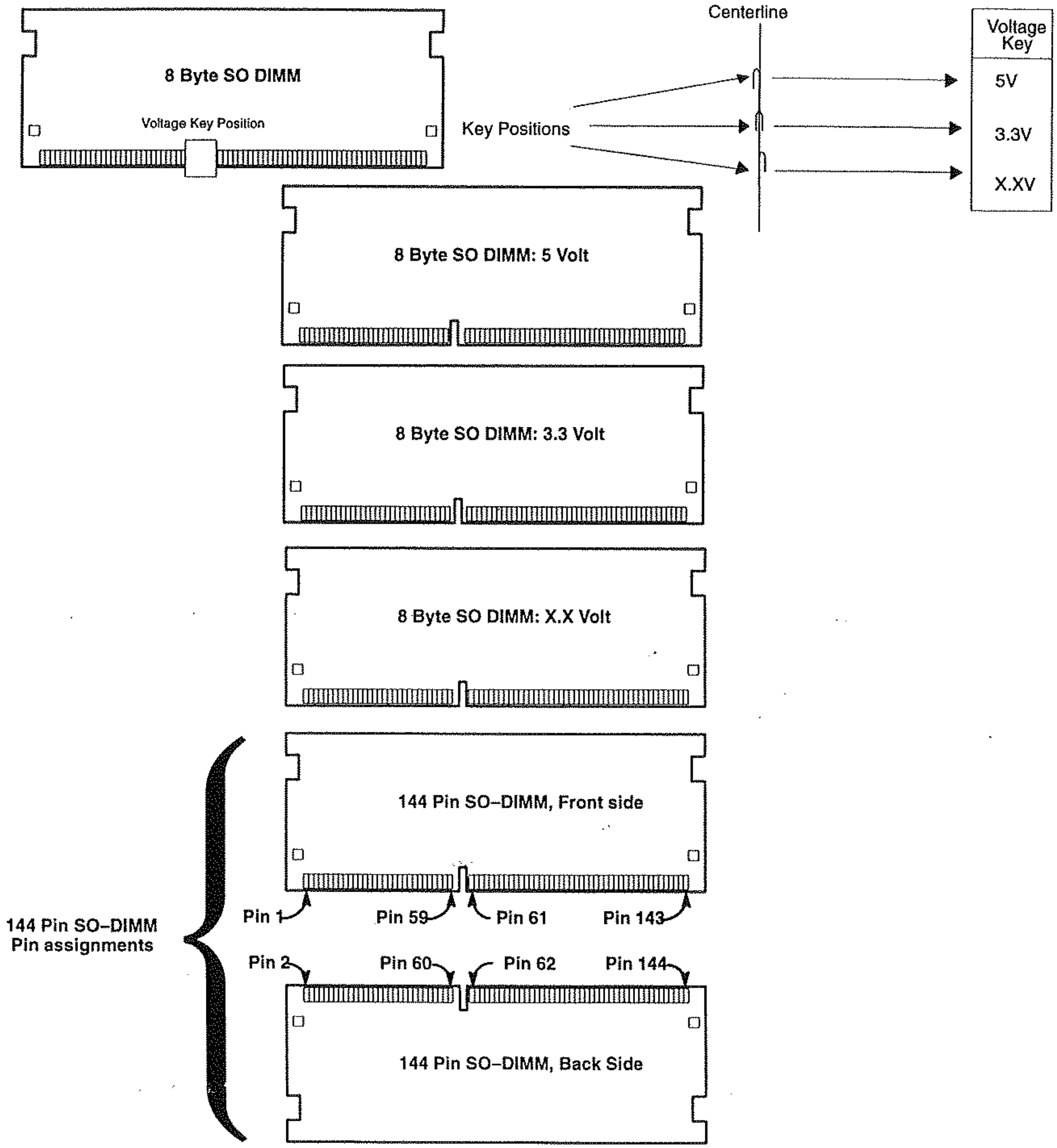


Figure 4.5.6–D
144 Pin SDRAM DIMM Keying Methodology

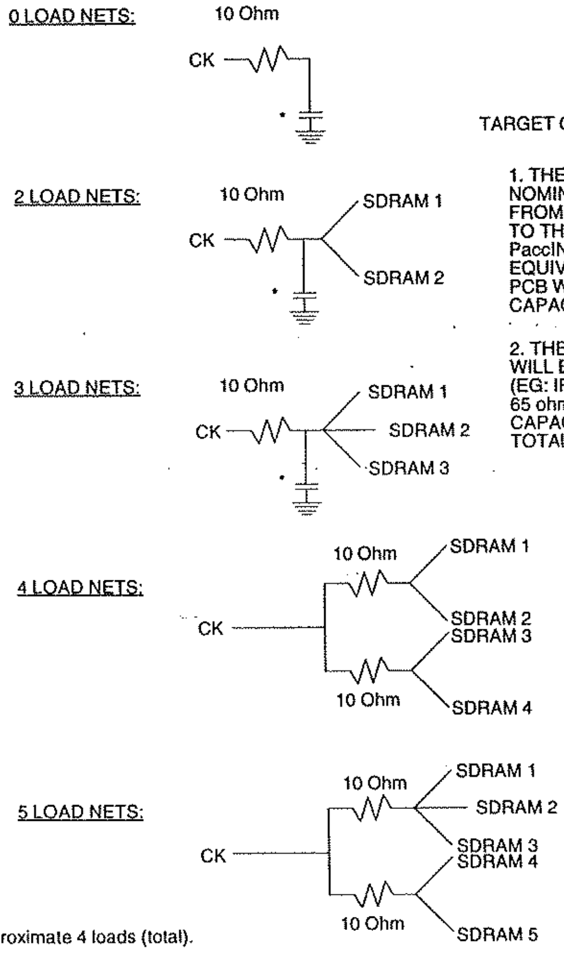
Pin #	DRAM SODIMM	SDRAM SODIMM
23	$\overline{\text{CAS0}}$	DQMB0
25	$\overline{\text{CAS1}}$	DQMB1
61	DU	CK0
65	DU	$\overline{\text{RAS}}$
69	$\overline{\text{RAS0}}$	$\overline{\text{S0}}$
71	$\overline{\text{RAS1}}$	$\overline{\text{S1}}$
73	$\overline{\text{OE}}$	DU
111	A10	A10/AP
115	$\overline{\text{CAS}}$2	DQMB2
117	$\overline{\text{CAS}}$3	DQMB3
24	$\overline{\text{CAS}}$4	DQMB4
26	$\overline{\text{CAS}}$5	DQMB5
62	DU	CKE0
66	DU	$\overline{\text{CAS}}$
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	$\overline{\text{CAS6}}$	DQMB6
118	$\overline{\text{CAS7}}$	DQMB7

FIGURE 4.5.6–E
Pinout Comparison, 144 Pin DRAM & SDRAM SO–DIMM

Configuration	CK0	CK1
x8 (1 bank)	4	4
x16 (1 bank)	4	*
x8 (2 bank)	*1 (PLL)	*
x16 (2 bank)	4	4

Configuration	CK0	CK1
x8 (1 bank)	*4 OR 5	*4 OR 5
x16/x4 (1 bank)	*4 (MAX)	*4 (MAX)
x8 (2 bank)	*1 (PLL)	*
x16/x4 (2 bank)	*1 (PLL)	*

- add padding capacitance per clock wiring diagram.



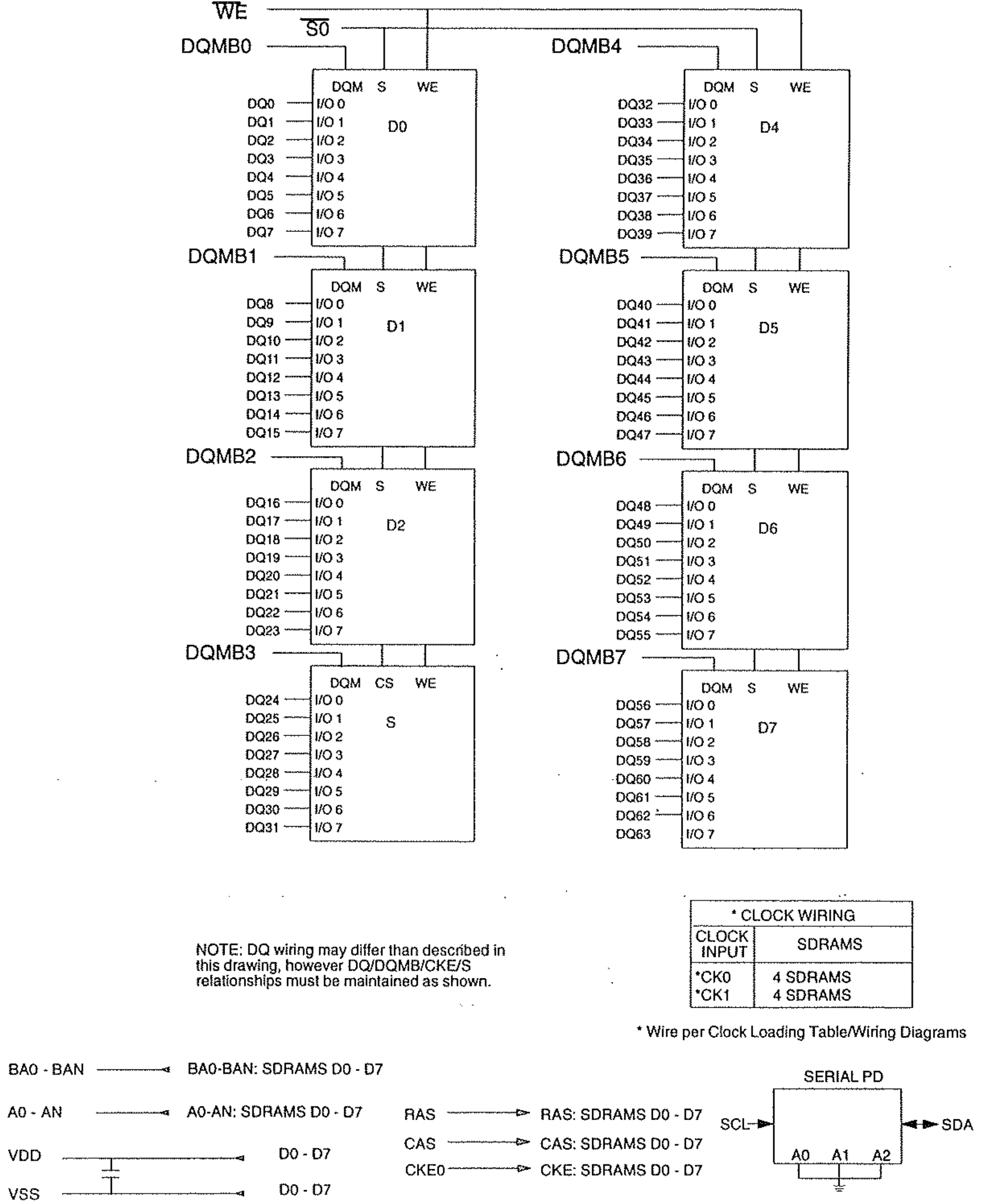
TARGET CLOCK (CK) SPECIFICATION:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .4ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PaccING CAPACITOR). (EG: THIS IS EQUIVALENT TO APPROXIMATELY 2" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2. THE VARIATION OF CK INPUT DELAY WILL BE +/- .1ns FOR BOTH CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/- 3pf IN TOTAL CK INPUT CAPACITANCE).

* add padding capacitance to approximate 4 loads (total).

Figure 4.5.6-F
144 Pin SDRAM SO-DIMM, CLOCK LOADING AND WIRING

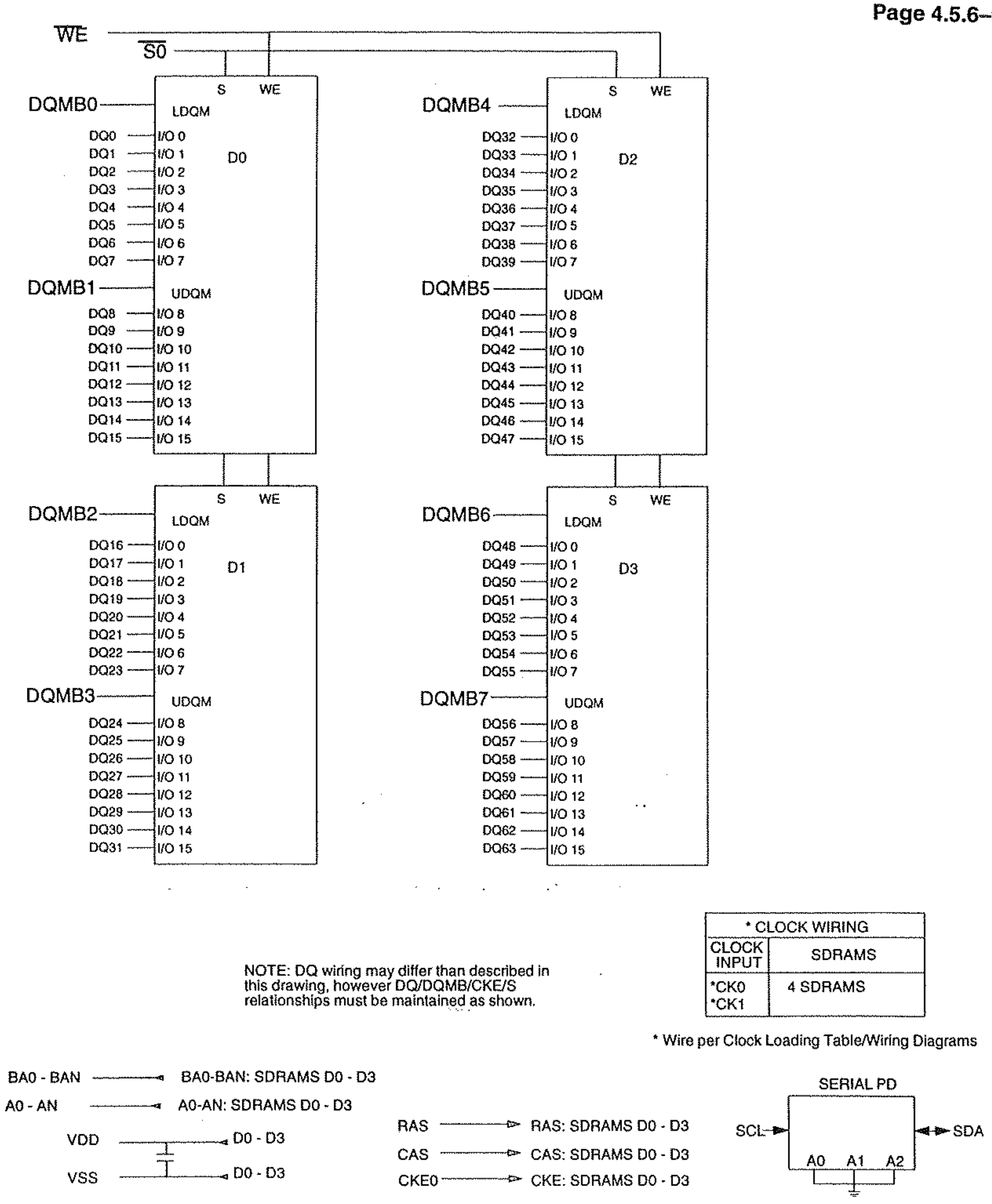


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6–G
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X8 SDRAMs

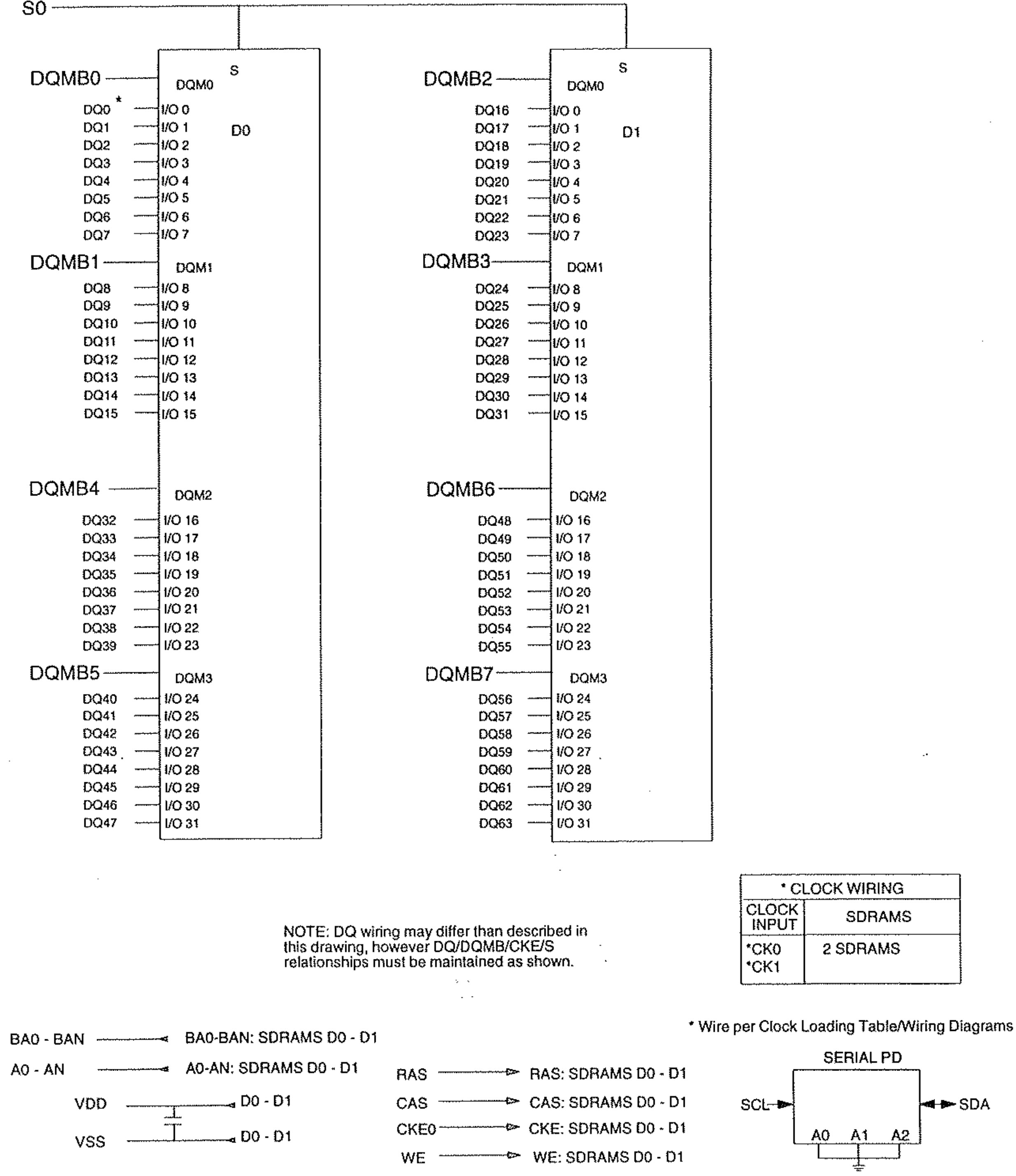


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6–H
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X16 SDRAMs

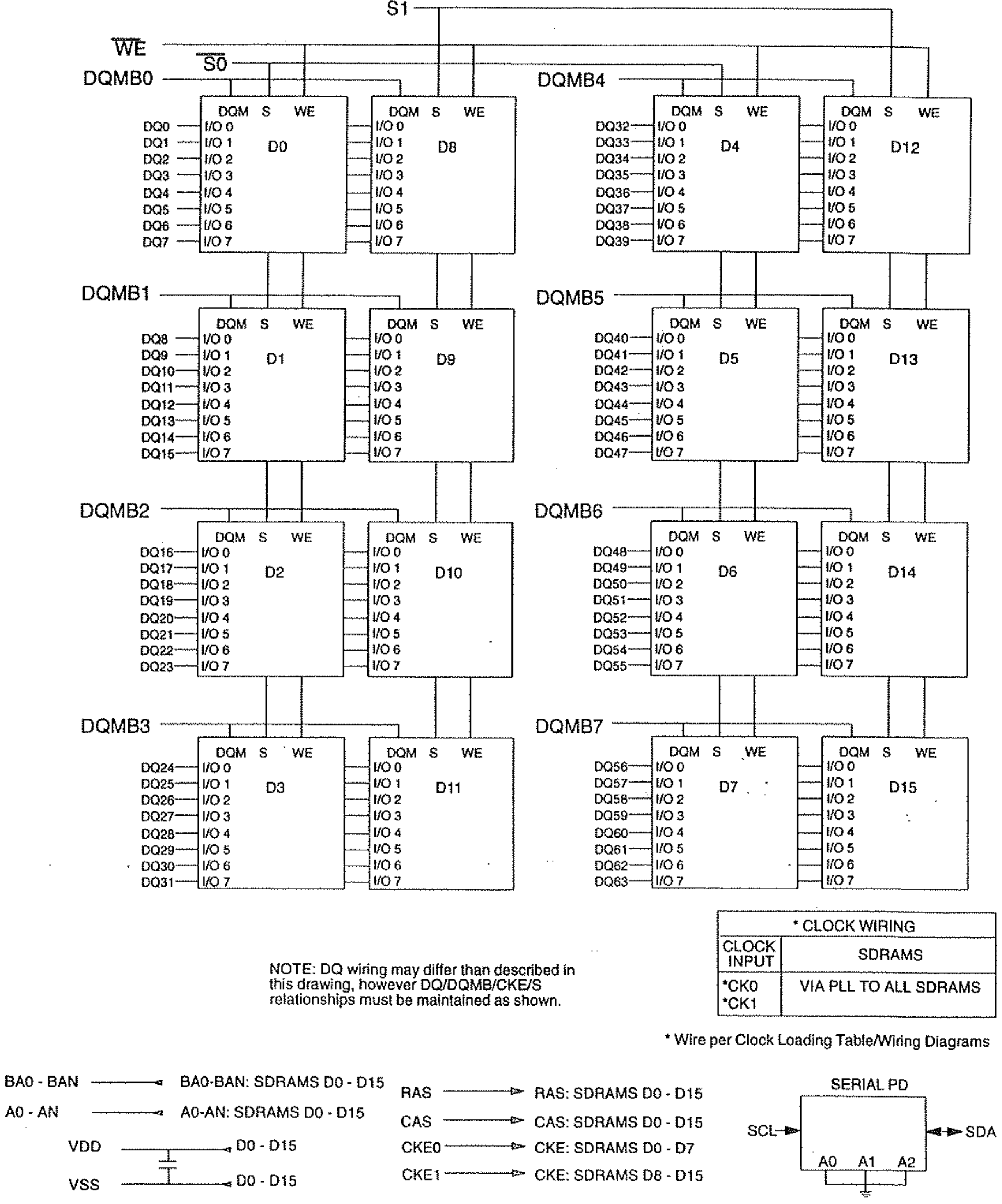


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	2 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6–I
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X32 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	VIA PLL TO ALL SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6–J
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X8 SDRAMs

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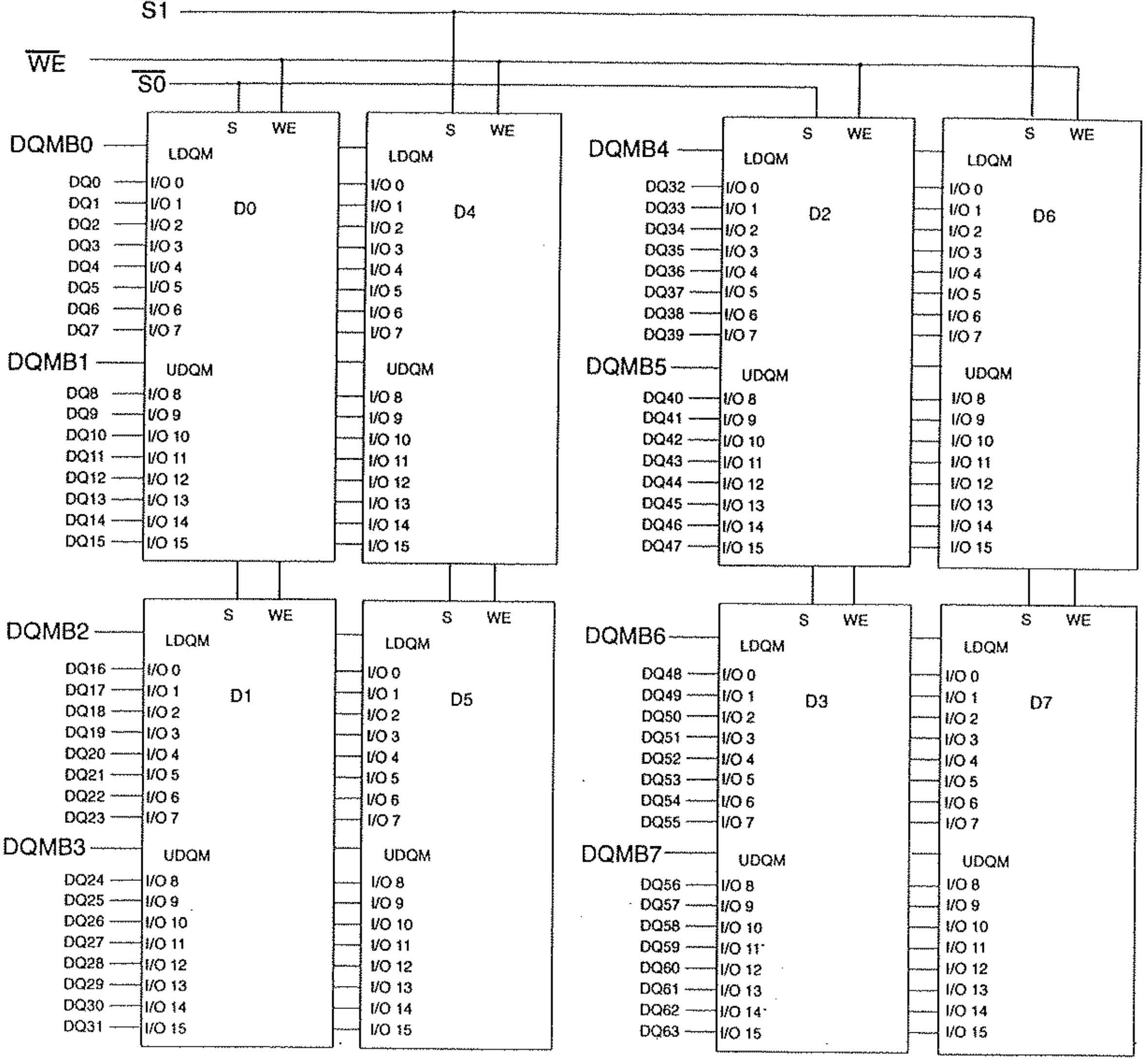


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	4 SDRAMS 4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

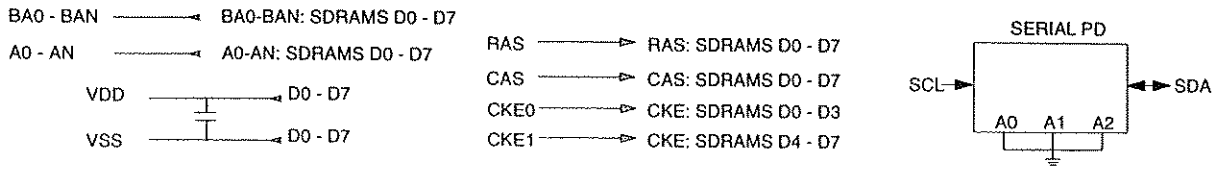
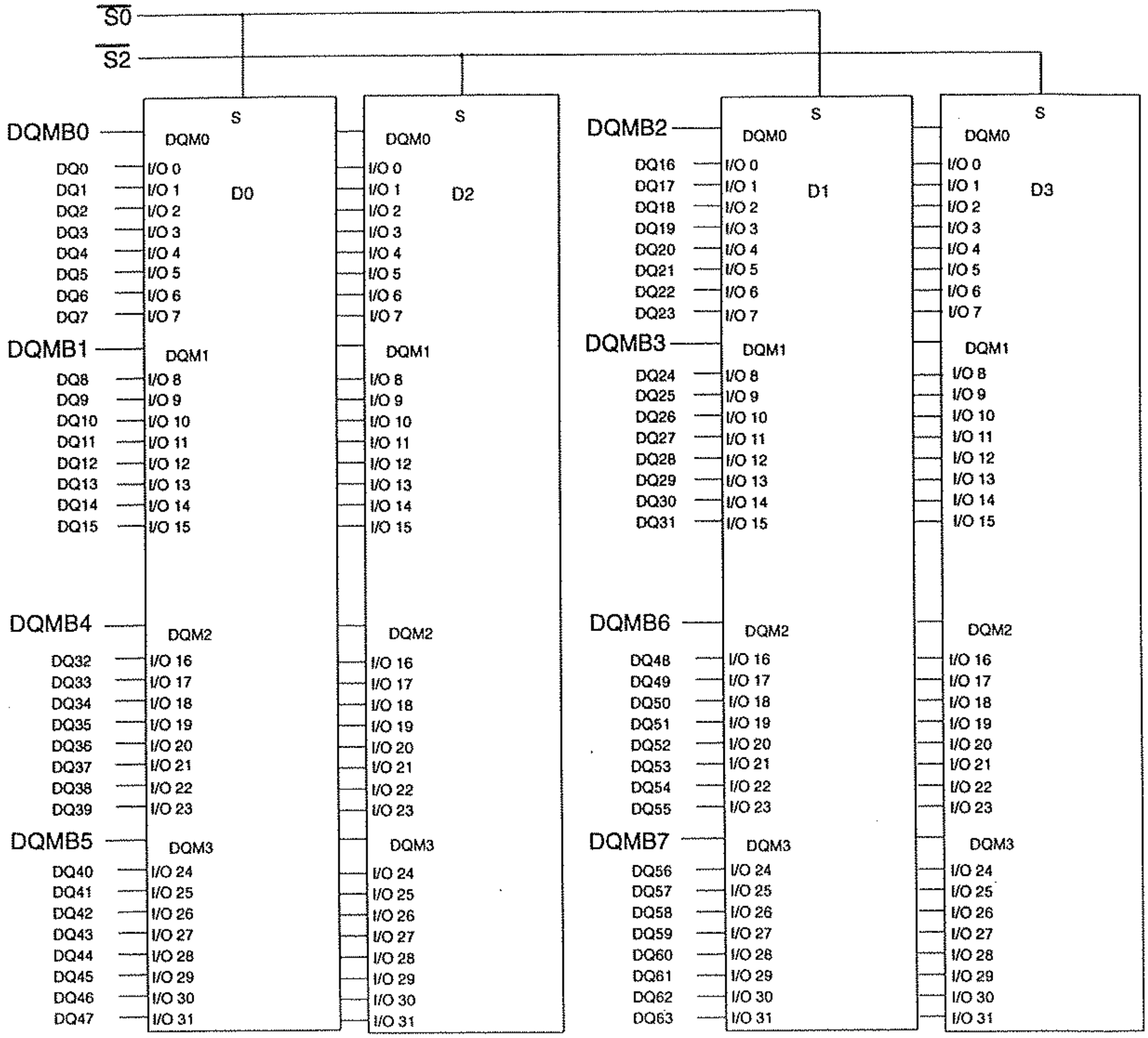


Figure 4.5.6–K
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X16 SDRAMs

369



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

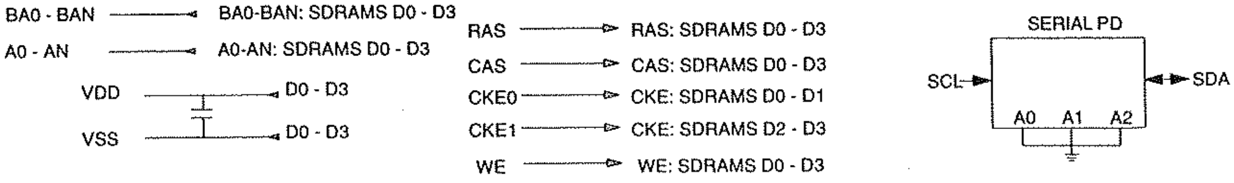
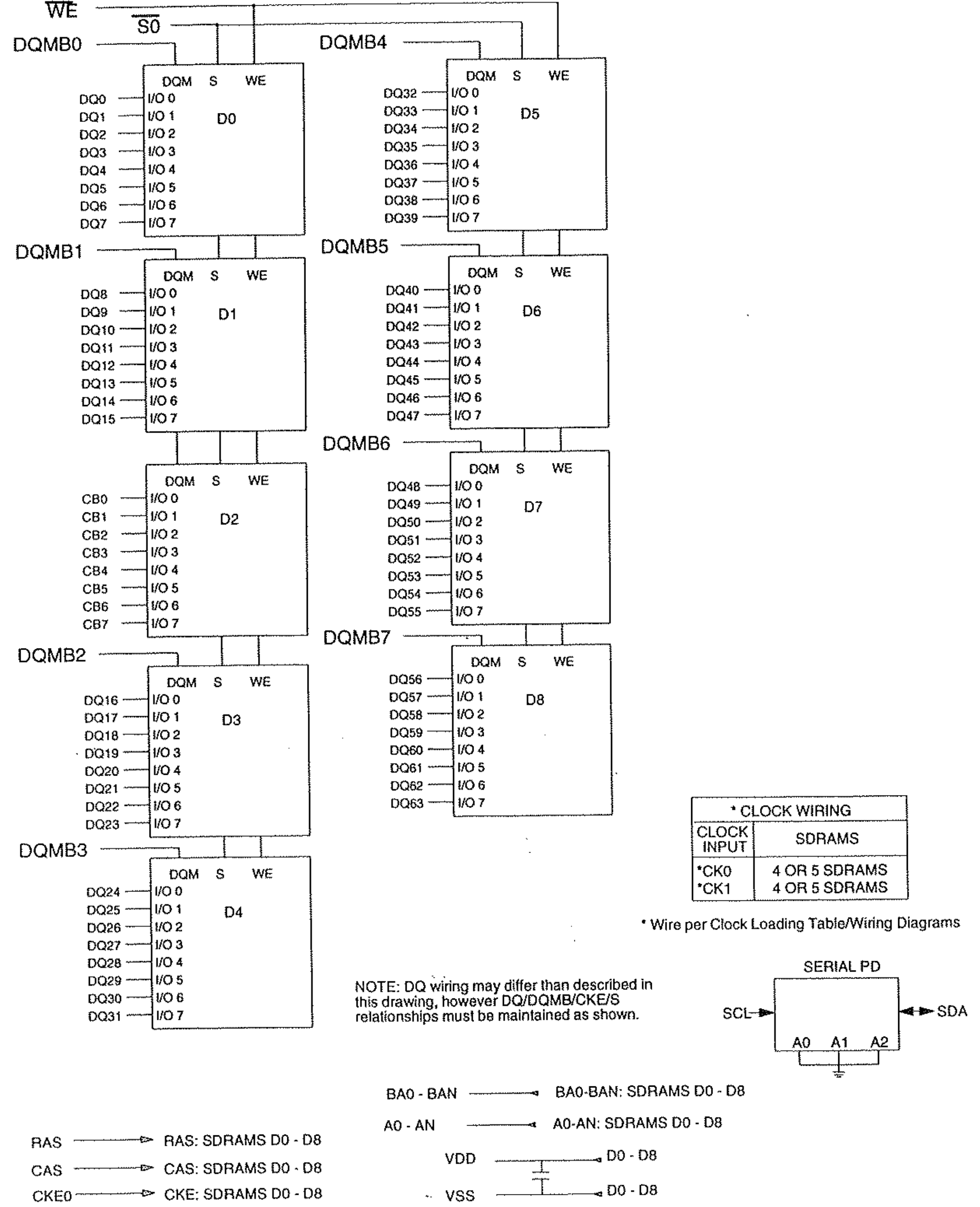


Figure 4.5.6–L
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X32 SDRAMs

370



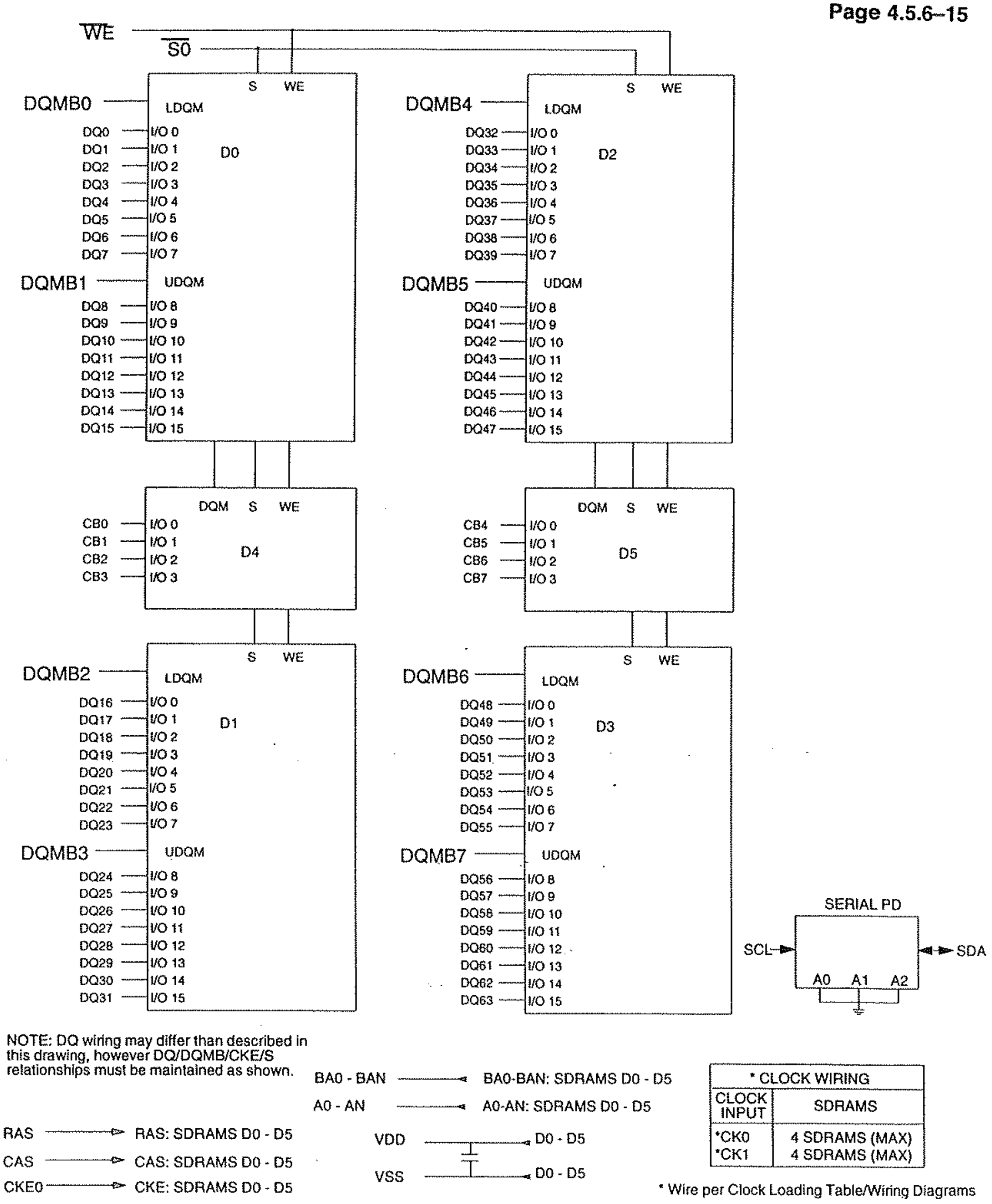
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	4 OR 5 SDRAMS 4 OR 5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

Figure 4.5.6–M
144 Pin X72 ECC SDRAM SO–DIMM, 1 Bank with X8 SDRAMs

3.11



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

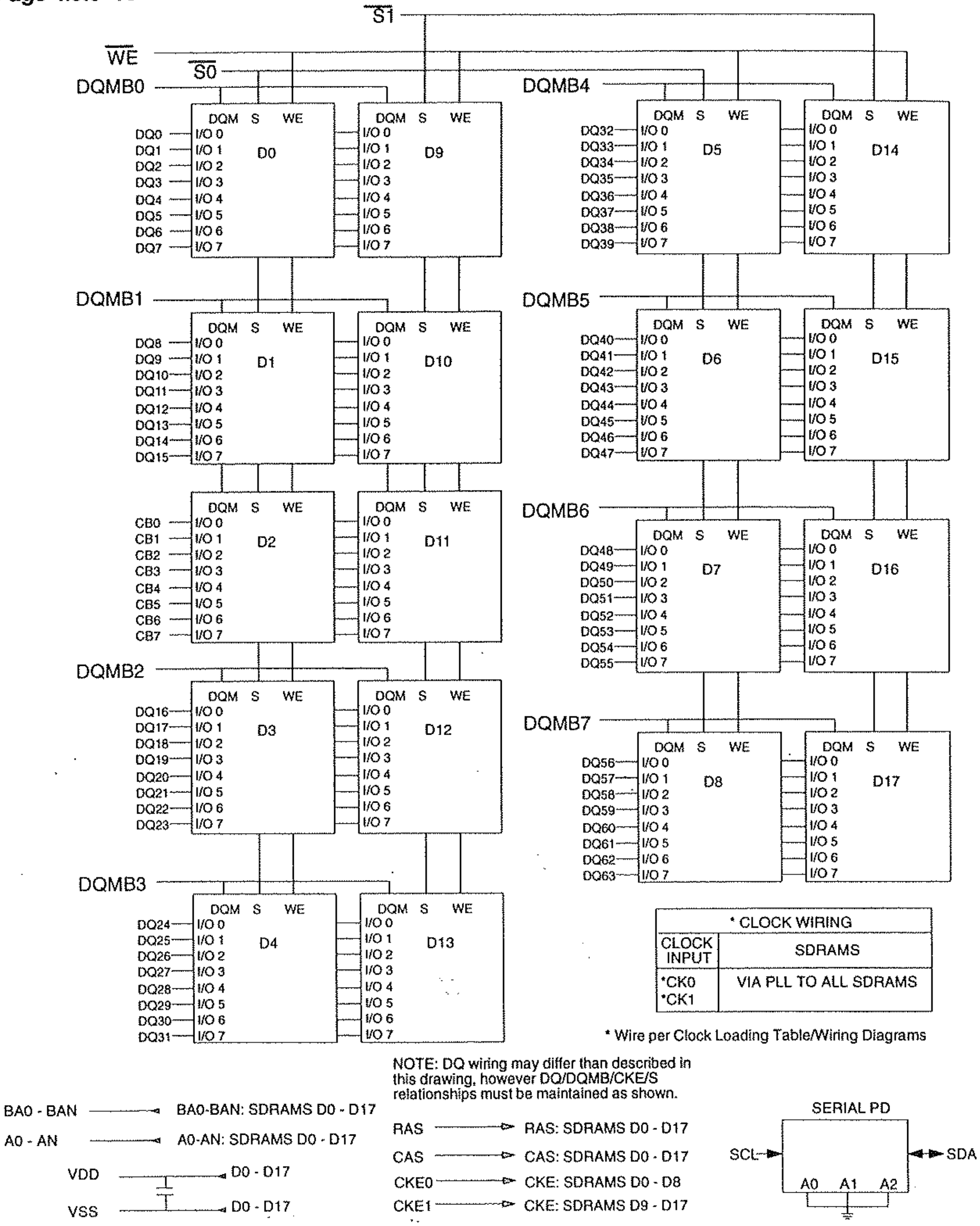
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS (MAX)
*CK1	4 SDRAMS (MAX)

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6-N

144 Pin X72 ECC SDRAM SO-DIMM, 1 Bank with X16 & X4 SDRAMs

312



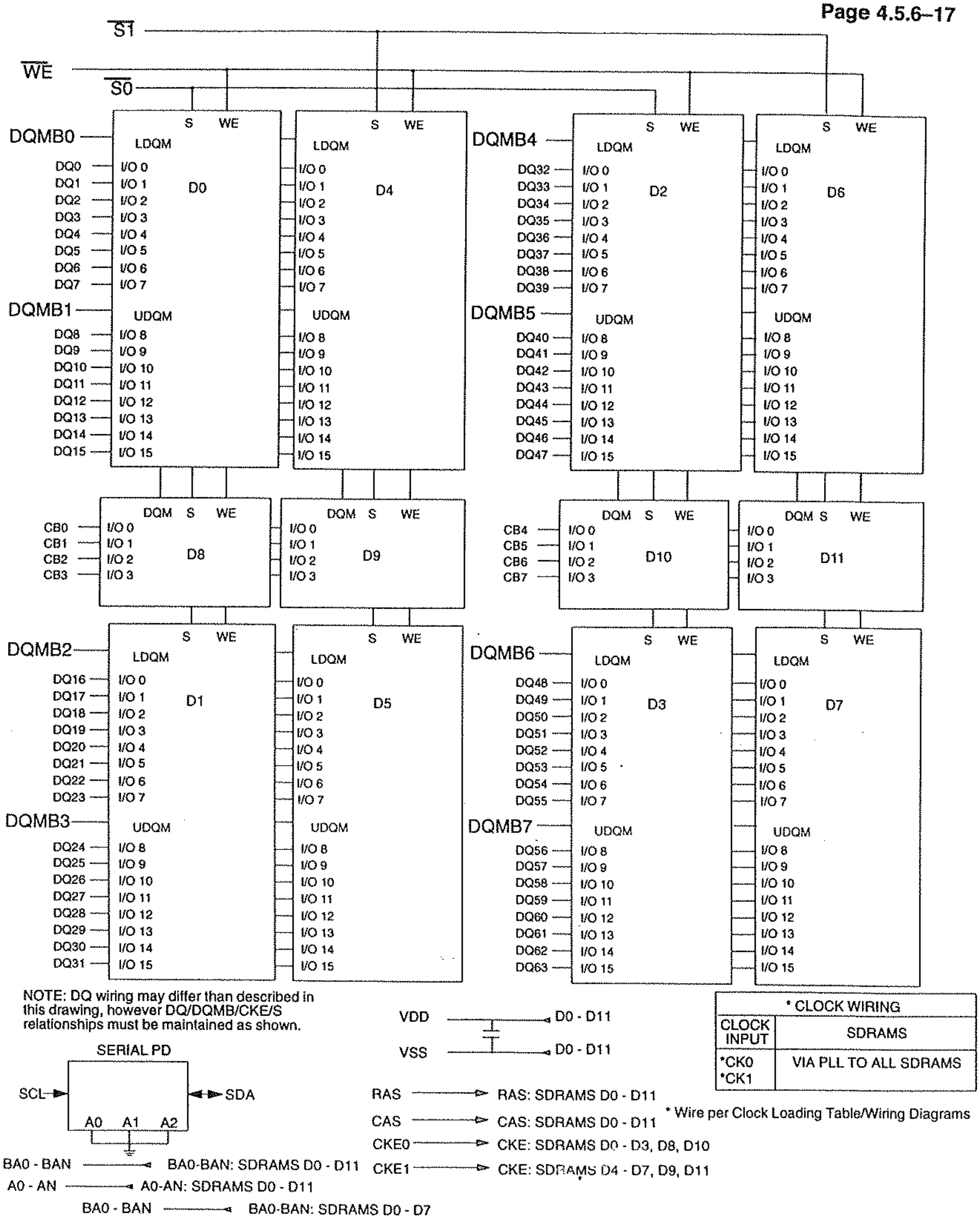
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	VIA PLL TO ALL SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

Figure 4.5.6–O
144 Pin X72 ECC SDRAM SO–DIMM, 2 Bank with X8 SDRAMs

3.13



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	VIA PLL TO ALL SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6–P
144 Pin X72 ECC SDRAM SO–DIMM, 2 Bank with X16 & X4 DRAMs

3 14

4.6 Sixteen Byte Memory Modules

4.6.1 – 278 PIN BUFFERED SDRAM DIMM FAMILY

3.15

4.6.1 – 278 PIN BUFFERED SDRAM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 16 bytes (144 bits).

DATA CONFIGURATIONS—Only one DATA Word configurations is defined in the initial release:
—144 BIT SDRAM with the location of CHECKBITS undefined

CONFIGURATION—2 Different Configurations are defined using X16 SDRAM memories with 1 and 2 banks

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—278 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.6.1–A, 4.6.1–B, & 4.6.1–C
DRAM SPD INFORMATOION — Fig. 4.6.1–D
MODULE KEYING DEFINITION — Fig. 4.6.1–E
MODULE PIN DEFINITIONS — Fig. 4.6.1–F
X144 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.6.1–G and 4.6.1–H

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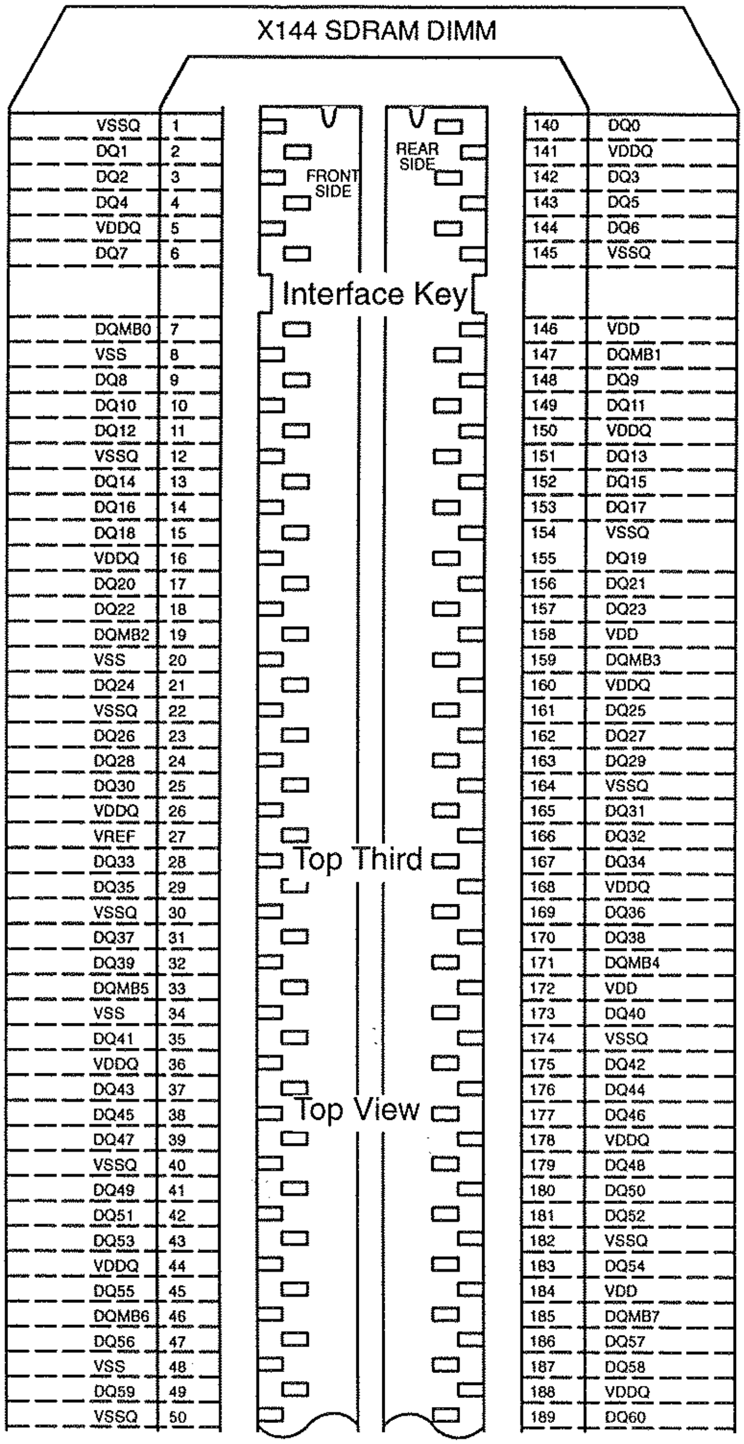
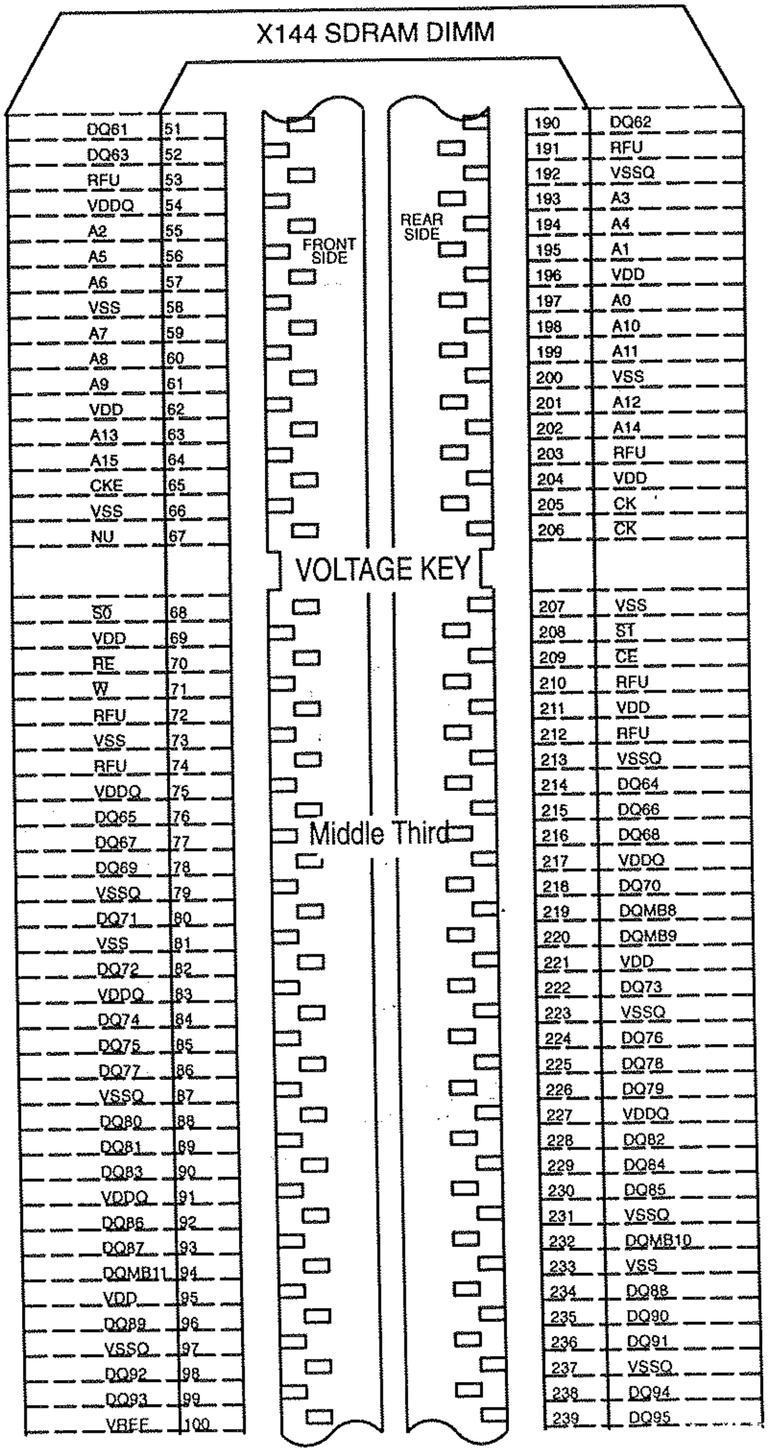


VSSQ	1	140	DQ0
DQ1	2	141	VDDQ
DQ2	3	142	DQ3
DQ4	4	143	DQ5
VDDQ	5	144	DQ6
DQ7	6	145	VSSQ
DQMB0	7	146	VDD
VSS	8	147	DQMB1
DQ8	9	148	DQ9
DQ10	10	149	DQ11
DQ12	11	150	VDDQ
VSSQ	12	151	DQ13
DQ14	13	152	DQ15
DQ16	14	153	DQ17
DQ18	15	154	VSSQ
VDDQ	16	155	DQ19
DQ20	17	156	DQ21
DQ22	18	157	DQ23
DQMB2	19	158	VDD
VSS	20	159	DQMB3
DQ24	21	160	VDDQ
VSSQ	22	161	DQ25
DQ26	23	162	DQ27
DQ28	24	163	DQ29
DQ30	25	164	VSSQ
VDDQ	26	165	DQ31
VREF	27	166	DQ32
DQ33	28	167	DQ34
DQ35	29	168	VDDQ
VSSQ	30	169	DQ36
DQ37	31	170	DQ38
DQ39	32	171	DQMB4
DQMB5	33	172	VDD
VSS	34	173	DQ40
DQ41	35	174	VSSQ
VDDQ	36	175	DQ42
DQ43	37	176	DQ44
DQ45	38	177	DQ46
DQ47	39	178	VDDQ
VSSQ	40	179	DQ48
DQ49	41	180	DQ50
DQ51	42	181	DQ52
DQ53	43	182	VSSQ
VDDQ	44	183	DQ54
DQ55	45	184	VDD
DQMB6	46	185	DQMB7
DQ56	47	186	DQ57
VSS	48	187	DQ58
DQ59	49	188	VDDQ
VSSQ	50	189	DQ60

Figure 4.6.1–A
278 PIN X144 SDRAM DIMM PINOUT (TOP THIRD)

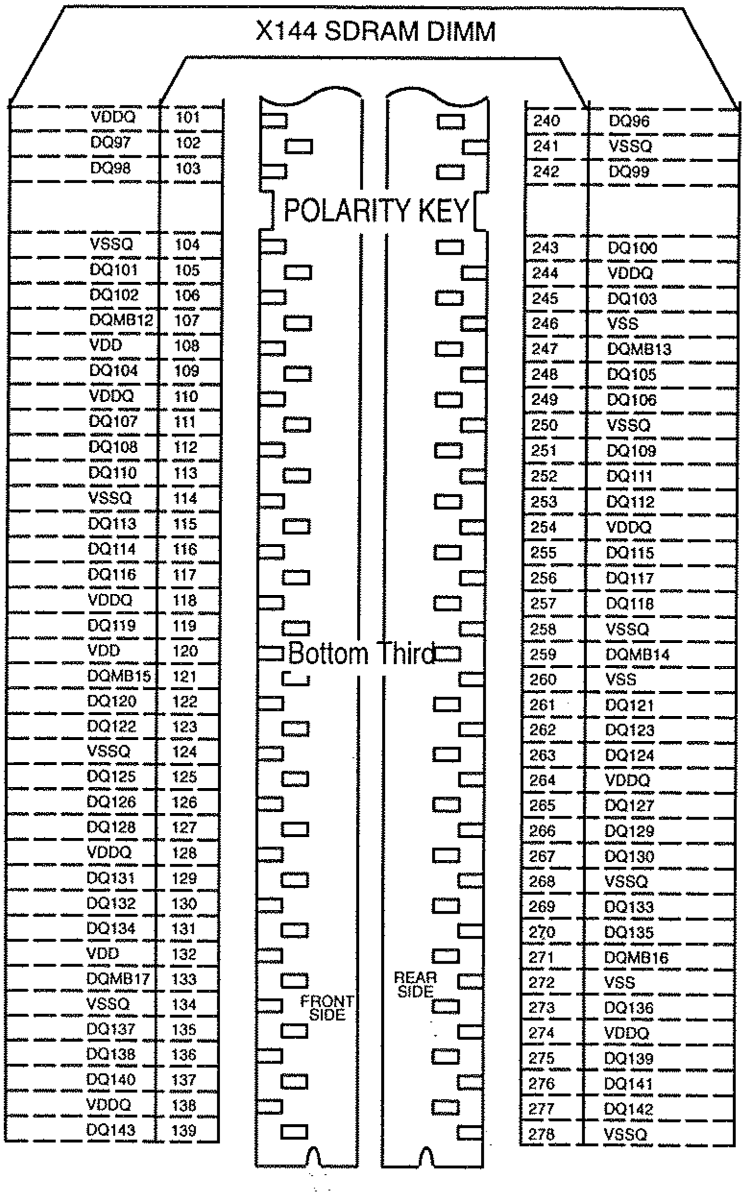
3.11



DQ61	51
DQ63	52
RFU	53
VDDQ	54
A2	55
A5	56
A6	57
VSS	58
A7	59
A8	60
A9	61
VDD	62
A13	63
A15	64
CKE	65
VSS	66
NU	67
$\overline{SO}$	68
VDD	69
$\overline{RE}$	70
$\overline{W}$	71
RFU	72
VSS	73
RFU	74
VDDQ	75
DQ65	76
DQ67	77
DQ69	78
VSSQ	79
DQ71	80
VSS	81
DQ72	82
VDDQ	83
DQ74	84
DQ75	85
DQ77	86
VSSQ	87
DQ80	88
DQ81	89
DQ83	90
VDDQ	91
DQ86	92
DQ87	93
DQMB11	94
VDD	95
DQ89	96
VSSQ	97
DQ92	98
DQ93	99
VREF	100

190	DQ62
191	RFU
192	VSSQ
193	A3
194	A4
195	A1
196	VDD
197	A0
198	A10
199	A11
200	VSS
201	A12
202	A14
203	RFU
204	VDD
205	CK
206	$\overline{CK}$
207	VSS
208	$\overline{ST}$
209	$\overline{CE}$
210	RFU
211	VDD
212	RFU
213	VSSQ
214	DQ64
215	DQ66
216	DQ68
217	VDDQ
218	DQ70
219	DQMB8
220	DQMB9
221	VDD
222	DQ73
223	VSSQ
224	DQ76
225	DQ78
226	DQ79
227	VDDQ
228	DQ82
229	DQ84
230	DQ85
231	VSSQ
232	DQMB10
233	VSS
234	DQ88
235	DQ90
236	DQ91
237	VSSQ
238	DQ94
239	DQ95

Figure 4.6.1–B
278 PIN X144 SDRAM DIMM PINOUT (MIDDLE THIRD)



VDDQ	101	240	DQ96
DQ97	102	241	VSSQ
DQ98	103	242	DQ99
VSSQ	104	243	DQ100
DQ101	105	244	VDDQ
DQ102	106	245	DQ103
DQMB12	107	246	VSS
VDD	108	247	DQMB13
DQ104	109	248	DQ105
VDDQ	110	249	DQ106
DQ107	111	250	VSSQ
DQ108	112	251	DQ109
DQ110	113	252	DQ111
VSSQ	114	253	DQ112
DQ113	115	254	VDDQ
DQ114	116	255	DQ115
DQ116	117	256	DQ117
VDDQ	118	257	DQ118
DQ119	119	258	VSSQ
VDD	120	259	DQMB14
DQMB15	121	260	VSS
DQ120	122	261	DQ121
DQ122	123	262	DQ123
VSSQ	124	263	DQ124
DQ125	125	264	VDDQ
DQ126	126	265	DQ127
DQ128	127	266	DQ129
VDDQ	128	267	DQ130
DQ131	129	268	VSSQ
DQ132	130	269	DQ133
DQ134	131	270	DQ135
VDD	132	271	DQMB16
DQMB17	133	272	VSS
VSSQ	134	273	DQ136
DQ137	135	274	VDDQ
DQ138	136	275	DQ139
DQ140	137	276	DQ141
VDDQ	138	277	DQ142
DQ143	139	278	VSSQ

Figure 4.6.1–C
278 PIN X144 SDRAM DIMM PINOUT (BOTTOM THIRD)

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This page is reserved for the future addition of serial presence detect tables.

Figure 4.6.1–D
278 PIN X144 SDRAM DIMM PD AND CONFIGURATION TABLES

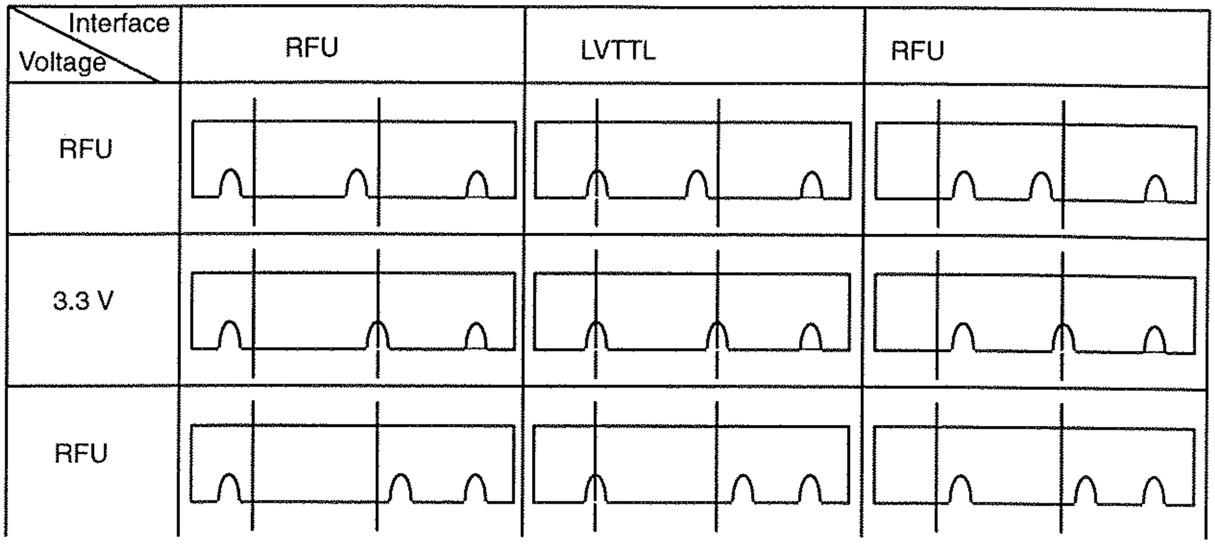


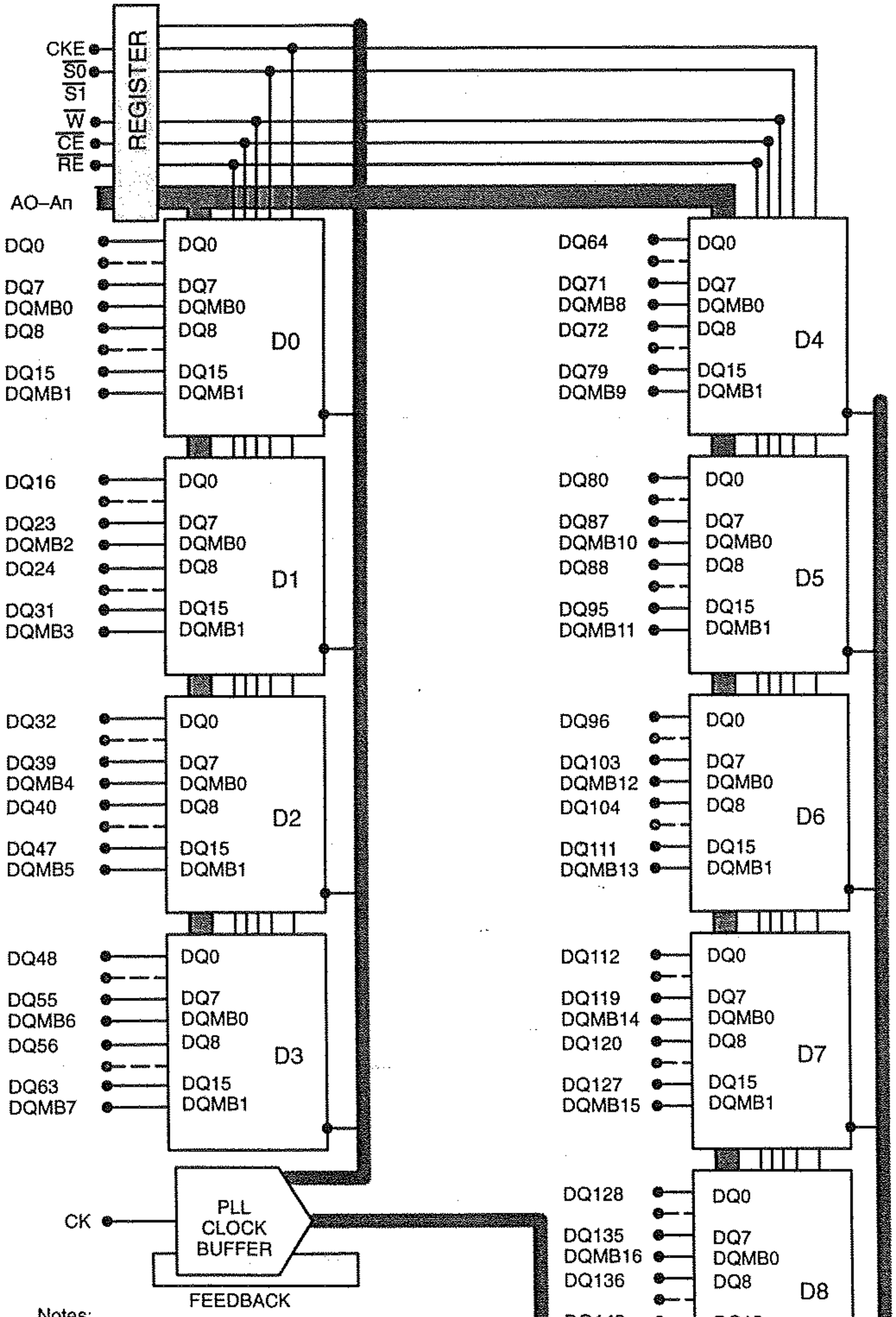
Figure 4.6.1–E
278 PIN 144 BIT SDRAM DIMM MECHANICAL KEY DEFINITION

Pin Name	Number	Function
A0....A15	16	Address Input (multiplexed)
DQ0....DQ143	144	Data Input/Output (common)
CK, $\overline{CK}$	2	Clock Input
CKE	1	Clock Enable Input
$\overline{S0}$, $\overline{S1}$	2	Chip Select Input
$\overline{RE}$	1	Row Enable (RAS) Input
$\overline{CE}$	1	Column Enable (CAS) Input
$\overline{W}$	1	Write Enable Input
DQM	1	Data Mask
DQMB0....DQMB17	18	Byte Data Mask input
VDD	14	Primary Positive Power Supply
VDDQ	27	Posivite Power for Input/Output
VREF	2	Reference Power Supply
VSS	14	Ground
VSSQ	27	Ground for data Input/Output
NU	1	Reserved for board test of PLL
RFU	7	Reserved for Future Use

Notes:

1. NU pin is reserved for board test control of PLL, Make no connection at system level.
2. RFU pins are available for future standardization of serial Presence Detect and VTT.

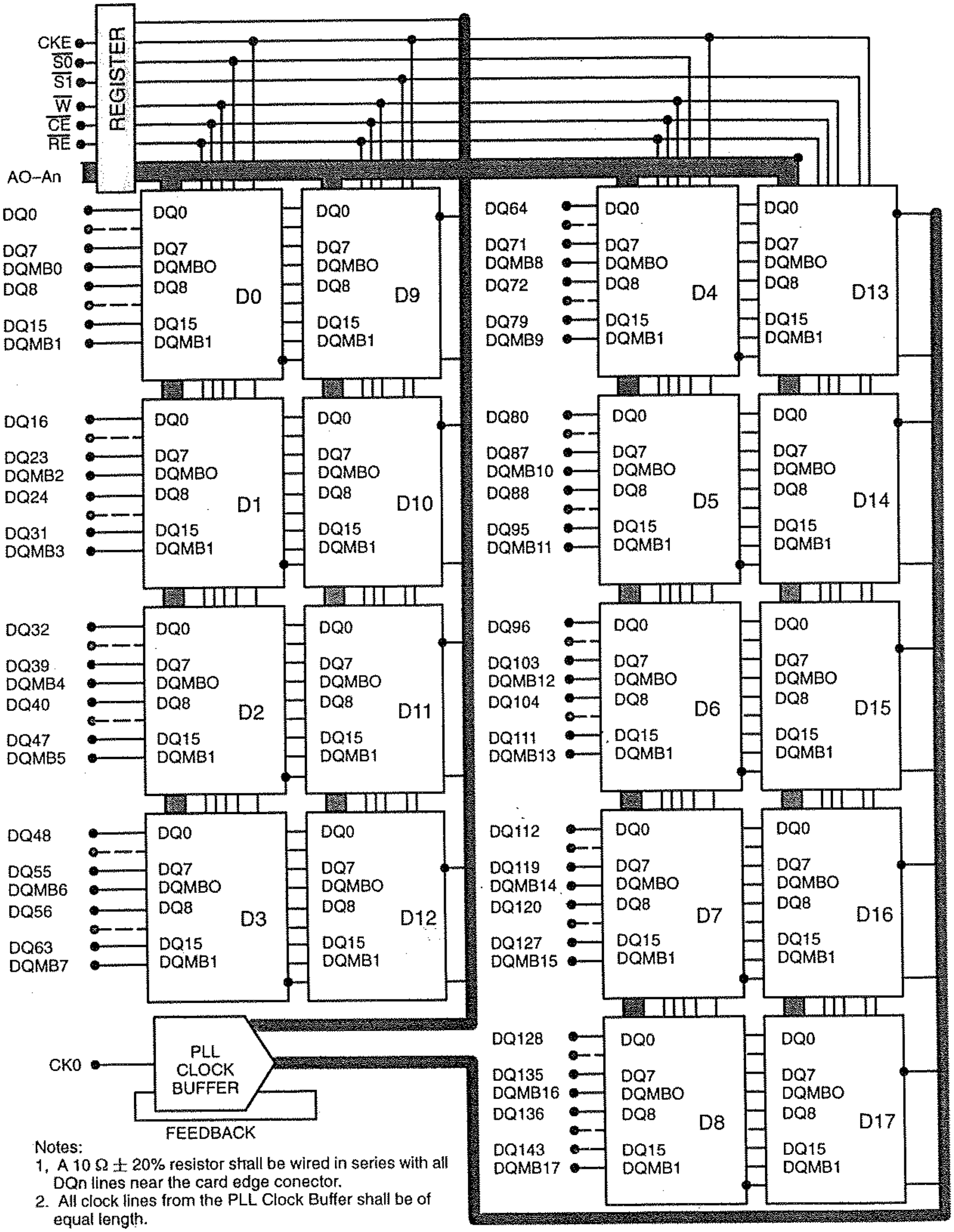
Figure 4.6.1–F
278 PIN 144 BIT SDRAM DIMM PIN DEFINITIONS



Notes:
1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.6.1-G

278 PIN X144 BUFFERED SDRAM DIMM 1 BANK with X16 SDRAM



Notes:
1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.6.1–H

278 PIN X144 BUFFERED SDRAM DIMM 2 BANKS with X16 SDRAM
Release 7