Patent claims

1. A dynamic semiconductor memory device of a random-access type (DRAM/SDRAM) having an initialization circuit which controls the switching-on operation of the semiconductor memory device and of its circuit components and which supplies a supply voltage stable signal (POWERON) once the supply voltage has been stabilized after the switching-on of the semiconductor memory device,
wherein the initialization circuit has an enable circuit (9) that receives the supply voltage stable signal (POWERON) and further command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device, which enable circuit supplies an enable signal (CHIPREADY) after the recognition of a predetermined proper initialization sequence of the command signals (PRE, ARF, MRS) applied to the semiconductor memory device, which enable signal causes the unlatching of a control circuit (13) provided for the proper operation of the semiconductor memory device,
c h a r a c t e r i z e d in that
the command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device in the initialization sequence recognized by the enable circuit (9) comprise the preparation command for word line activation (PRE-CHARGE), and/or the refresh command (AUTOREFRESH), and/or the load configuration register command (MODE-REGISTER-SET).

2. A semiconductor memory device according to Claim 1,
c h a r a c t e r i z e d in that
the enable circuit (9) has at least one bistable multivibrator stage (14, 15, 16) with a set input (S) to which a command signal (PRECHARGE, AUTOREFRESH, MODE-

REGISTER-SET) is applied, a reset input (R) to which the supply voltage stable signal (POWERON) or a signal derived therefrom or a linked signal is applied, and with an output (Q) at which the enable signal (CHIPREADY) (9) is derived.

3. A semiconductor memory device according to Claim 2, characterized in that
the enable circuit (9) has a number of bistable multivibrator stages (14, 15, 16) each associated to a command signal (PRE, ARF, MRS).

4. A semiconductor memory device according to Claim 2 or 3, characterized in that
the output (Q) of at least one of the bistable multivibrator stages (14) is fed to a reset input of a further multivibrator stage (15).

5. A semiconductor memory device according to Claim 3 or 4, characterized in that,
in one of the bistable multivibrator stages (15), the supply voltage stable signal (POWERON) and the signal output from the output (Q) of the further multivibrator stage (14) are fed to the reset input (R) of the multivibrator stage (15) after having been logically combined by a gate (17).

6. A semiconductor memory device according to any one of Claims 3 to 5, characterized in that
the bistable multivibrator stage (14, 15, 16) is formed in each case by an RS multivibrator constructed of at least two NOR or NAND gates (14A, 14B, 15A, 17, 16A, 16B).

7. A semiconductor memory device according to any one of Claims 1 to 6,
c h a r a c t e r i z e d in that
the initialization sequence recognized as a proper initialization sequence by the enable circuit (9) and the initialization sequence triggering of the enable signal (CHIPREADY) is a command sequence conforming to the JEDEC standard.

8. A semiconductor memory device according to any one of Claims 1 to 7,
c h a r a c t e r i z e d in that
the output drivers of the semiconductor memory device remain latched during the switching-on operation until the enable signal (CHIPREADY) generated by the enable circuit (9) is issued.

9. A semiconductor memory device according to any one of Claims 1 to 8,
c h a r a c t e r i z e d in that
the proper initialization sequence, which causes the triggering of an enable signal (CHIPREADY), includes the following chronologically successive command sequences:
(a) first PRE, second ARF, third MRS; or
(b) first PRE, second MRS, third ARF; or
(c) first MRS, second PRE, or third ARF,
wherein the abbreviations denote the following commands:
PRE = the preparation command for word line activation (PRECHARGE),
ARF = the refresh command (AUTOREFRESH), and
MRS = load configuration register command (MODE-REGISTER-SET).

10. A method for initializing a dynamic semiconductor memory

SDRAM) by means of an initialization circuit which controls the switching-on operation of the semiconductor memory device and of its circuit components which initialization circuit supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device,

wherein the initialization circuit supplies an enable signal (CHIP-READY) by means of an enable circuit (9) that receives the supply voltage stable signal (POWERON) and further command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device after identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device, which enable signal causes the unlatching of the control circuit (13) provided for the proper operation of the semiconductor memory device,

c h a r a c t e r i z e d in that

the command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device in the initialization sequence recognized by the enable circuit (9) comprise the preparation command for word line activation (PRECHARGE), and/or the refresh command (AUTOREFRESH), and/or the load configuration register command (MODE-REGISTER-SET).

11. A method according to Claim 10,

c h a r a c t e r i z e d in that

the output drivers of the semiconductor memory device remain latched during the switching-on operation until the enable signal (CHIPREADY) generated by the enable circuit (9) is issued.

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EP Patent Claim No. 99113048.5-2210
Applicant: Infineon Technologies AG
Communication dated September 28, 2005

In response to the above communication, replacement pages 1, 1a, 3, 4 and 9 to 12 have been filed instead of the original pages 1, 3, 4 and 9 to 13 of the application. Also attached is a working copy in which the changes made are underlined.

The feature of the original Claim 2 was included in Claim 1, which, according to the communication, the Office considers to be grantable. Accordingly, the feature of original Claim 12, which corresponds to original Claim 2, was included in subsidiary Claim 11 (10 in the new numbering). The original Claim 14 was deleted.

The description has been adapted accordingly. The relevant prior art is cited on page 1, line 25.

In the communication, reference was made to Claims 15 to 20 in Section 6. However, the application filed contained only Patent Claims 1 to 14. Thus, apart from the set of claims now presented with 11 patent claims, there are no further patent claims in the proceedings.

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